A733 Octa-core Processor

User Manual

Revision 0.92

February 14, 2025

Revision History

Revision	Date	Author	Description
0.90	October 25, 2024	KPA0570	Initial Version
0.91	December 6, 2024	KPA0570	**Chapter 1 Product Description** Update Table 1-1 Ordering Information.
0.92	February 14, 2025	AWA1896	**Chapter 1 Product Description** Remove Ordering Information. For device differences, see *A733_Datasheet.* **Chapter 5 Processors** Update description for bit [18:16] of PLL_CTRL_REG1 register in section 5.1.6.4 **Chapter 11 Memory Controllers** Update CQSSC1 register in section 11.3.8.56 and section 11.3.9.57. **Chapter 15 Video Output** Update D-PHY speed in section 15.5.1. **Chapter 18 Peripherals** 1. Update the following registers: • GPIO_POW_MOD_SEL register in section 18.14.6.1 • GPIO_POW_VAL register in section 18.14.6.2. • SGPIO_POW_MOD_SEL register in section 18.14.7.20 • SGPIO_POW_VAL register in section 18.14.7.21. 2. Update Figure 18-59 RS-485 Transceiver. 3. Update UART_SCH register in section 18.10.9.12.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Contents

Revision History i
Contents ii
Figures v
Tables xiii
About This Document xvii
1 Product Description 1
1.1 Overview 1
1.2 Block Diagram 2
2 Memory Map 4
3 System Boot 13
3.1 Boot ROM (BROM) 13
4 Power, Reset, and Clock Management 19
4.1 Clock Controller Unit (CCU) 19
4.2 Power Reset Clock Management (PRCM) 215
5 Processors 240
5.1 ARM Cortex A76 x2+Cortex A55 x6 Subsystem 240
5.2 RISC-V E902 Subsystem 317
5.3 NPU 322
6 Interprocessor Communication 323
6.1 Message Box (MSGBOX) 323
6.2 Spinlock 334
7 Thermal Sensor 342
7.1 Thermal Sensor Controller (THS) 342
8 Timers 358
8.1 Timer0 358
8.2 Timer1 365
8.3 Watchdog Timer (WDT) 377
9 RTC 384
9.1 RTC 384
10 I/O Memory Management Unit 408

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11 Memory Controllers 409

11.1 SDRAM controller (DRAMC) 409

11.2 Universal Flash Storage Host Controller (UFSHC) 410

11.3 SD/MMC Host Controller (SMHC) 411

11.4 NAND Flash Controller (NDFC) 533

11.5 SPI Flash Controller (SPIF) 534

12 Interrupts 586

12.1 Interrupt Controller 586

12.2 Generic Interrupt Controller (GIC) 593

12.3 Core-Local Interrupt Controller (CLIC) 605

13 DMA 611

13.1 DMA Controller (DMAC) 611

14 Video & Graphics Engine 640

14.1 Video Encoder 640

14.2 Video Decoder 642

14.3 Display Engine (DE) 644

14.4 De-interlacer (DI) 646

14.5 Graphic 2D (G2D) 647

14.6 E-ink 648

15 Video Output 649

15.1 TCON_LCD 649

15.2 TCON_TV 705

15.3 HDMI 738

15.4 eDP1.4 739

15.5 MIPI DSI 796

16 Video Input 841

16.1 CSIC 841

17 Audio 1094

17.1 I2S/PCM 1094

17.2 DMIC 1147

17.3 One Wire Audio (OWA) 1162

18 Peripherals 1194

18.1 GMAC 1194

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.2 SerDes Subsystem 1202
18.3 PCIe3.0 DM 1233
18.4 USB3.1 GEN2 DRD 1338
18.5 USB2.0 DRD 1354
18.6 USB2.0 HOST 1356
18.7 PWM 1358
18.8 SPI 1410
18.9 SPI_DBI 1441
18.10 UART 1492
18.11 Two Wire Interface (TWI) 1530
18.12 General Purpose ADC (GPADC) 1581
18.13 Low Rate ADC (LRADC) 1608
18.14 GPIO 1618
18.15 LEDC 1895
18.16 CIR Receiver (IR_RX) 1916
18.17 CIR Transmitter (IR_TX) 1928
19 Security 1940
19.1 Crypto Engine (CE) 1940

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figures

Figure 1-1 System Block Diagram 2
Figure 3-1 Boot Process in Normal BROM Process 16
Figure 3-2 Boot0 Read Process 17
Figure 3-3 Mandatory Upgrade Process 18
Figure 4-1 CCU Block Diagram 19
Figure 4-2 PLL Distribution 23
Figure 4-3 Bus Clock Tree Diagram 216
Figure 4-4 Module Clock Tree Diagram 217
Figure 5-1 CPUX System Block Diagram 242
Figure 6-1 Message Box Block Diagram 323
Figure 6-2 The Communication Process between CPUX_MSGBOX and CPUS_MSGBOX 325
Figure 6-3 Take and Free Spinlock 335
Figure 6-4 Spinlock State Machine 335
Figure 6-5 CPUX and CPUS Taking/Freeing Spinlock0 Process 337
Figure 7-1 THS Block Diagram 344
Figure 7-2 Thermal Sensor Timing Requirement 344
Figure 7-3 Thermal Sensor Controller Interrupt Source 345
Figure 7-4 THS Initialization 346
Figure 8-1 Timer1 Block Diagram 359
Figure 8-2 Block Diagram for the Timer 366
Figure 8-3 Watchdog Block Diagram 378
Figure 9-1 RTC Block Diagram 386
Figure 9-2 RTC Clock Tree 387
Figure 9-3 RTC Counter 387
Figure 9-4 RTC 1 kHz Counter Step Structure 388
Figure 9-5 RC Calibration Circuit 389
Figure 9-6 RC and DCXO Waveform 389
Figure 9-7 DCXO Scheduled wake-up diagram 390
Figure 11-1 SMHC 0-2 Block Diagram 413
Figure 11-2 SMHC 3 Block Diagram 413
Figure 11-3 Command Token Format 416

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 11-4 Response Token Format....416
Figure 11-5 Data Packet Format for SDR....417
Figure 11-6 Data Packet Format for DDR....418
Figure 11-7 Data Packet Format for DDR in HS400 Mode....419
Figure 11-8 Single-Block and Multi-Block Read Operation....420
Figure 11-9 Single-Block and Multi-Block Write Operation....420
Figure 11-10 IDMAC Descriptor Structure Diagram....421
Figure 11-11 Command Queue Initialization....432
Figure 11-12 SPI_Flash Block Diagram....536
Figure 11-13 Typical Application....538
Figure 11-14 SPI Transfer Mode....540
Figure 11-15 SPI STR Transfer....541
Figure 11-16 SPI DTR Transfer Example, 1-4-4....541
Figure 11-17 SPI DTR Transfer Example, 4-4-4....541
Figure 11-18 SPI DTR Transfer with DQS Input Clock Signal....542
Figure 11-19 SPI CS Select Timing Relation....542
Figure 11-20 SPI 3-Wire Mode....543
Figure 11-21 SPI CMD with Single IO....544
Figure 11-22 SPI Write CMD and DATA with One Wire....544
Figure 11-23 SPI Write CMD and Read DATA with One Wire (No Dummy)....544
Figure 11-24 SPI Write CMD and Read DATA with One Wire (with Dummy)....545
Figure 11-25 SPI Dual Input/Dual Output Mode 1-1-2....545
Figure 11-26 SPI Dual Input/Dual Output Mode (1-2-2)....546
Figure 11-27 SPI Quad Input/Quad Output Mode (1-1-4)....546
Figure 11-28 SPI Quad Input/Quad Output Mode (1-4-4)....547
Figure 11-29 SPI Quad Input/Quad Output Mode (4-4-4)....547
Figure 11-30 SPI Octal Input/Octal Output Mode (1-1-8)....547
Figure 11-31 SPI Octal Input/Octal Output Mode (1-8-8)....548
Figure 11-32 SPI Octal Input/Octal Output Mode (8-8-8)....548
Figure 11-33 Descriptor Structure Diagram....548
Figure 11-34 SPI Programming Flow....553
Figure 11-35 SPI Transfer Phase Flow Diagram....556
Figure 12-1 Interrupt Controller Block Diagram....587
Figure 13-1 DMAC Block Diagram....613

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 13-2 DMA Chained Transfer 617
Figure 13-3 Workflow of the DMAC Handshake Mode....621
Figure 13-4 DMAC Transfer Process....623
Figure 15-1 TCON_LCD Block Diagram 650
Figure 15-2 TCON_LCD Environment Diagram....651
Figure 15-3 HV Interface Vertical Timing....656
Figure 15-4 HV Interface Horizontal Timing....657
Figure 15-5 DC Interface Timing 658
Figure 15-6 Single-channel Transmission Timing 659
Figure 15-7 BT601 Interface Timing 660
Figure 15-8 CPU Interface Timing (left read, right write) 661
Figure 15-9 LVDS Single Link JEDIA Mode Interface Timing....662
Figure 15-10 LVDS Single Link NS Mode Interface Timing....662
Figure 15-11 LVDS Dual Link NS Mode Interface Timing....663
Figure 15-12 FRM Module 664
Figure 15-13 HV Interface Initial Process 664
Figure 15-14 LVDS interface initial sequence 667
Figure 15-15 i8080 Interface Initial Process 671
Figure 15-16 TCON_TV Block Diagram....706
Figure 15-17 TCON_TV Sub-blocks....707
Figure 15-18 TCON_TV Environment Diagram 708
Figure 15-19 Single Pixel Mode 709
Figure 15-20 Dual Pixel Mode....710
Figure 15-21 Quad Pixel Mode 711
Figure 15-22 4-Pixel Mode without Variable Pixel Dring-Picture Width=11 pixels....712
Figure 15-23 RGB Colorbar Pattern 713
Figure 15-24 Grey Pattern 713
Figure 15-25 Dot Pattern 714
Figure 15-26 Grid Pattern 714
Figure 15-27 Line Counting 716
Figure 15-28 Progressive Scanning 718
Figure 15-29 Interlaced Scanning....719
Figure 15-30 eDP Block Diagram 740
Figure 15-31 I2S Sampling Timing....741

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 15-32 Link Training States 742
Figure 15-33 Data Accumulation Delay 744
Figure 15-34 FIFO Accumulation Delay Settings 745
Figure 15-35 Interrupt Detection Logic 745
Figure 15-36 MIPI DSI Block Diagram 798
Figure 15-37 DISPLL Distribution 799
Figure 16-1 CSIC Block Diagram 844
Figure 16-2 8-bit DC Sensor Interface Timing 847
Figure 16-3 8-bit YCbCr4:2:2 with Embedded Syncs (BT.656) 847
Figure 16-4 BT601 v2f mode Timing 848
Figure 16-5 RAW-8 Format 849
Figure 16-6 YUV-8 Format 849
Figure 16-7 UV-Combined Format 849
Figure 17-1 I2S/PCM Interface System Block Diagram 1098
Figure 17-2 I2S Standard Mode Timing 1100
Figure 17-3 Left-Justified Mode Timing 1100
Figure 17-4 Right-Justified Mode Timing 1100
Figure 17-5 PCM Long Frame Mode Timing 1101
Figure 17-6 PCM Short Frame Mode Timing 1101
Figure 17-7 Timing Requirements for Inputs 1102
Figure 17-8 Timing Requirements for Outputs 1102
Figure 17-9 I2S/PCM Operation Flow 1103
Figure 17-10 DMIC Block Diagram 1150
Figure 17-11 DMIC Operation Mode 1151
Figure 17-12 OWA Block Diagram 1166
Figure 17-13 OWA Biphase-Mark Code 1167
Figure 17-14 OWA Sub-Frame Format 1168
Figure 17-15 OWA Frame/Block Format 1169
Figure 17-16 Data-Burst Format 1170
Figure 17-17 Data-burst Preamble 1170
Figure 17-18 Data-burst Preamble words 1170
Figure 17-19 Fields of Burst-information 1171
Figure 17-20 Length of the Burst-Payload Specified by Pd 1171
Figure 17-21 OWA Operation Flow 1172

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 18-1 GMAC Block Diagram 1198
Figure 18-2 GMAC Typical Application 1200
Figure 18-3 SERDES Block Diagram....1206
Figure 18-4 PCIe Block Diagram 1238
Figure 18-5 Outbound ATU 1241
Figure 18-6 Inbound ATU....1242
Figure 18-7 DMA Operation 1243
Figure 18-8 USB3.1 GEN2 DRD Controller Block Diagram 1343
Figure 18-9 USB2.0 DRD Controller Block Diagram....1359
Figure 18-10 USB2.0 Host Controller Block Diagram 1361
Figure 18-11 PWM Block Diagram....1363
Figure 18-12 PWM01 Clock Source Bypass 1364
Figure 18-13 PWM01 Output Logic Module Diagram 1365
Figure 18-14 PWM01 Complementary Pair Output 1366
Figure 18-15 Output Waveform with Dead-time Insertion 1367
Figure 18-16 Group 0-3 PWM Signal Output 1368
Figure 18-17 PWM01 Capture Logic Module Diagram....1369
Figure 18-18 PWM0 Channel Capture Timing 1369
Figure 18-19 SPI Block Diagram....1416
Figure 18-20 Circuit Connection between the Master and Slave 1418
Figure 18-21 SPI Phase 0 Timing Diagram 1419
Figure 18-22 SPI Phase 1 Timing Diagram 1420
Figure 18-23 SPI 3-Wire Mode 1420
Figure 18-24 SPI Dual-Input/Dual-Output Mode 1421
Figure 18-25 SPI Dual I/O Mode 1421
Figure 18-26 SPI Quad-Input/Quad-Output Mode 1422
Figure 18-27 Data Transfer in Query Mode 1424
Figure 18-28 SPI_DBI Block Diagram....1447
Figure 18-29 SPI Application Block Diagram 1449
Figure 18-30 DBI Application Block Diagram....1450
Figure 18-31 DBI 3-Line Display Bus Serial Interface Write Operation Format 1451
Figure 18-32 DBI 3-Line Display Bus Serial Interface 8-bit Read Operation Format....1451
Figure 18-33 DBI 3-Line Display Bus Serial Interface 24-bit Read Operation Format....1452
Figure 18-34 DBI 3-Line Display Bus Serial Interface 32-bit Read Operation Format....1452

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 18-35 DBI 4-Line Display Bus Serial Interface Write Operation Format 1453
Figure 18-36 DBI 4-Line Display Bus Serial Interface 8-bit Read Operation Format....1453
Figure 18-37 DBI 4-Line Display Bus Serial Interface 24-bit Read Operation Format....1454
Figure 18-38 DBI 4-Line Display Bus Serial Interface 32-bit Read Operation Format....1454
Figure 18-39 RGB111 3-Line Interface Transmit Video Format 1455
Figure 18-40 RGB444 3-Line Interface Transmit Video Format 1455
Figure 18-41 RGB565 3-Line Interface Transmit Video Format 1456
Figure 18-42 RGB666 3-Line Interface Transmit Video Format 1456
Figure 18-43 RGB111 4-Line Interface Transmit Video Format 1457
Figure 18-44 RGB444 4-Line Interface Transmit Video Format 1457
Figure 18-45 RGB565 4-Line Interface Transmit Video Format 1458
Figure 18-46 RGB666 4-Line Interface Transmit Video Format 1458
Figure 18-47 RGB444 2 Data Lane Interface Transmit Video Format....1459
Figure 18-48 RGB565 2 Data Lane Interface Transmit Video Format....1460
Figure 18-49 RGB666 2 Data Lane Interface Transmit Video Format 0....1460
Figure 18-50 RGB666 2 Data Lane Interface Transmit Video Format 1 (ilitek) 1461
Figure 18-51 RGB666 2 Data Lane Interface Transmit Video Format 2 (New vision) 1461
Figure 18-52 RGB888 2 Data Lane Interface Transmit Video Format....1461
Figure 18-53 UART Block Diagram....1498
Figure 18-54 UART Controller IO Signals....1500
Figure 18-55RTS/CTS Auto Flow Control 1500
Figure 18-56 RTS/CTS Auto Flow Control Timing....1500
Figure 18-57 IrDA Transceiver 1501
Figure 18-58 Serial IrDA Timing 1501
Figure 18-59 RS-485 Transceiver 1501
Figure 18-60 RS-485 Timing 1502
Figure 18-61 UART Serial Data Format....1502
Figure 18-62 TWI Block Diagram....1536
Figure 18-63 Write Timing in 7-bit Standard Addressing Mode....1538
Figure 18-64 Read Timing in 7-bit Standard Addressing Mode....1538
Figure 18-65 Write Timing in 10-bit Extended Addressing Mode 1539
Figure 18-66 Read Timing in 10-bit Extended Addressing Mode....1539
Figure 18-67 TWI Driver Write Packet Transmission 1540
Figure 18-68 TWI Driver Read Packet Transmission....1541

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 18-69 GPADC Block Diagram 1587
Figure 18-70 GPADC Timing Requirement 1589
Figure 18-71 GPADC Initial Process 1589
Figure 18-72 LRADC Block Diagram 1614
Figure 18-73 LRADC Interrupt 1615
Figure 18-74 GPIO Block Diagram 1624
Figure 18-75 Pull-up, Pull-down, and High-impedance Input Mode 1632
Figure 18-76 IO Buffer Strength Diagram 1633
Figure 18-77 GPIOB Interrupt Diagram 1635
Figure 18-78 LEDC Block Diagram 1902
Figure 18-79 LED Input Data Structure 1903
Figure 18-80 LED Typical Circuit 1903
Figure 18-81 LED Input Data Code 1903
Figure 18-82 LED Data Transfer Mode 1904
Figure 18-83 LEDC Package Output Timing Diagram 1906
Figure 18-84 LEDC 1-frame Output Timing Diagram 1906
Figure 18-85 LEDC Normal Configuration Flow 1909
Figure 18-86 LEDC Timeout Abnormal Processing Flow 1910
Figure 18-87 FIFO Overflow Abnormal Processing Flow 1911
Figure 18-88 CIR Receiver Block Diagram 1923
Figure 18-89 A typical Pulse Train of the NEC 1924
Figure 18-90 Logical 0 and Logical 1 of NEC Protocol 1925
Figure 18-91 ATHR Definition 1925
Figure 18-92 ITHR Definition 1925
Figure 18-93 NTHR Definition 1926
Figure 18-94 CIR Receiver Process 1927
Figure 18-95 IR_TX Block Diagram 1936
Figure 18-96 Definitions of Logical 1 and Logical 0 1937
Figure 18-97 CIR Message Timing Diagram 1938
Figure 18-98 CIR Transmitter Process 1939
Figure 19-1 CE Block Diagram 1949
Figure 19-2 CE XRNG Modify Block Diagram (ce_hash_top) 1950
Figure 19-3 CE Low Power Diagram (ce_top) 1951
Figure 19-4 DES Encryption and Decryption 1952

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 19-5 3DES Encryption and Decryption of a 3-key Operation and a 2-key Operation.....1953
Figure 19-6 ECB Mode Encryption and Decryption 1954
Figure 19-7 CBC Mode Encryption and Decryption 1954
Figure 19-8 CTR Mode Encryption and Decryption 1955
Figure 19-9 CFB Mode Encryption and Decryption 1956
Figure 19-10 OFB Mode Encryption and Decryption.....1957
Figure 19-11 CTS Mode Encryption and Decryption 1958
Figure 19-12 Word Address of Message.....1959
Figure 19-13 Byte Order.....1959
Figure 19-14 Bit Order 1959
Figure 19-15 The Storage Method of 32-bit IV 1960
Figure 19-16 The Storage Method of 64-bit IV 1960
Figure 19-17 Task Chaining of Hash Algorithms and Random Bit Generator Algorithms.....1961
Figure 19-18 Task Chaining of Other Algorithms.....1965
Figure 19-19 Secure Debug Process 1974

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Tables

Table 3-1 BOOT_MODE Setting....14
Table 3-2 GPADC Boot Select Setting....14
Table 3-3 Groups of eFuse_Boot_Select....15
Table 3-4 eFuse Boot Select Setting....15
Table 4-1 PLL Typical Configurations....20
Table 4-2 PLL Specifications....21
Table 4-3 PLL Typical Configuration....22
Table 5-1 Cortex-A55 Power Mode....243
Table 5-2 Cortex-A76 Power Mode....243
Table 5-3 DSU Power Mode....244
Table 7-1 THS Information in the SID....346
Table 9-1 RTC External Signals....386
Table 9-2 RTC Counter Changing Range....388
Table 11-1 SMHC Sub-blocks....413
Table 11-2 SMHC External Signals....414
Table 11-3 SMHC 0-2 DES0 Definition....421
Table 11-4 SMHC 3 DES0 Definition....422
Table 11-5 SMHC0-2 DES1 Definition....422
Table 11-6 SMHC3 DES1 Definition....423
Table 11-7 SMHC0-3 DES2 Definition....423
Table 11-8 SMHC0-3 DES3 Definition....423
Table 11-9 Command and Data Location....424
Table 11-10 Differences of Task Descriptor Between CMDP Mode and CMDQ Mode....433
Table 11-11 SPI_Flash Sub-blocks....536
Table 11-12 SPI_Flash External Signals....537
Table 11-13 SPI_Flash Support List....538
Table 11-14 SPI Flash Modes with Clock Polarity and Phase....540
Table 12-1 Interrupt Sources in CPU Subsystem....595
Table 12-2 Interrupt Sources in RISC-V Subsystem....606
Table 13-1 DMAC Sub-blocks....613
Table 13-2 DMA DRQ Types in CPUX domain....614

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Table 13-3 DMA Address Descriptors....617
Table 15-1 TCON_LCD Sub-blocks....651
Table 15-2 RGB, LVDS, and MIPI DSI External Signals....652
Table 15-3 The Correspondence between LCD and RGB....653
Table 15-4 The Correspondence among LCD, LVDS, and DSI....653
Table 15-5 HV Panel Signals....656
Table 15-6 Analysis of XY Signal....659
Table 15-7 CPU Panel Signals....660
Table 15-8 LVDS Panel Signals....661
Table 15-9 BT.656 Mode Configuration Example....670
Table 15-10 i8080 Interface Configuration Example....672
Table 15-11 HDMI External Signals....708
Table 15-12 MIPI DSI External Signals....798
Table 15-13 DISPLL Specifications....799
Table 15-14 Parameter Configuration....803
Table 16-1 CSIC Sub-blocks....844
Table 16-2 CSIC External Signals....845
Table 16-3 BT.656 Header Code....847
Table 16-4 BT.656 Header Data Bit Definition....848
Table 16-5 CSIC FIFO Distribution....848
Table 16-6 Soft Reset bits for MBUS....855
Table 17-1 I2S/PCM External Signals....1098
Table 17-2 Proper MCLK Values with Different Fsin and Fsout....1102
Table 17-3 DMIC External Signals....1150
Table 17-4 OWA External Signals....1166
Table 17-5 Biphase-Mark Encoder....1167
Table 17-6 Preamble Codes....1168
Table 17-7 Bit Allocation of Data-Burst in IEC 60958 Subframes....1169
Table 17-8 The Relation between Different System Clock and Sample Ratio....1172
Table 18-1 GMAC Sub-blocks....1198
Table 18-2 GMAC External Signals....1199
Table 18-3 SERDES External Signals....1207
Table 18-4 PCIe Sub-blocks....1238
Table 18-5 PCIe External Signals....1240

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Table 18-6 PWM External Signals....1363
Table 18-7 SPI Sub-blocks....1416
Table 18-8 SPI External Signals....1417
Table 18-9 SPI Transmit Format....1419
Table 18-10 SPI Old Sample Mode....1425
Table 18-11 SPI New Sample Mode....1426
Table 18-12 SPI_DBI Sub-blocks....1447
Table 18-13 GPIO multiplexing of SPI1 and DBI....1448
Table 18-14 SPI_DBI External Signals....1449
Table 18-15 2 Data Lane SCLK Frequency....1462
Table 18-16 3 Line SCLK Frequency....1462
Table 18-17 4 Line SCLK Frequency....1462
Table 18-18 UART External Signals....1498
Table 18-19 Errors of Baud Rate in UART Mode....1503
Table 18-20 Errors of Baud Rate in IrDA Mode....1503
Table 18-21 Errors of Baud Rate in RS485 Mode....1503
Table 18-22 Errors of Baud Rate in 19.2M and 26M Clock Source....1504
Table 18-23 TWI Sub-blocks....1536
Table 18-24 TWI Clock Sources....1537
Table 18-25 TWI External Signals....1537
Table 18-26 GPADC External Signals....1588
Table 18-27 GP_SMP_TMS Value Corresponding to Each Sampling Frequency....1591
Table 18-28 Magnification Value Configuration....1592
Table 18-29 LRADC External Signals....1615
Table 18-30 Port B Multiplex Function....1626
Table 18-31 Port C Multiplex Function....1626
Table 18-32 Port D Multiplex Function....1626
Table 18-33 Port E Multiplex Function....1627
Table 18-34 Port F Multiplex Function....1628
Table 18-35 Port G Multiplex Function....1628
Table 18-36 Port H Multiplex Function....1628
Table 18-37 Port J Multiplex Function....1629
Table 18-38 Port K Multiplex Function....1629
Table 18-39 Port L Multiplex Function....1630

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Table 18-40 Port M Multiplex Function 1630
Table 18-41 Port Function.....1632
Table 18-42 LEDC Sub-blocks 1902
Table 18-43 LEDC External Signals 1903
Table 18-44 LED Data Input Time 1903
Table 18-45 IR_RX External Signals 1924
Table 18-46 IR_TX External Signals 1937

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

About This Document

Purpose and Target Readers

This document details the features, logical structures, functional description, programming guidelines, and related registers of each module about the SoC. A basic knowledge of digital circuits, logical circuits, SoCs, and so on is necessary to use this manual. Particular attention should be paid to the cautions and notes within the body of the text.

Related Documentation

For a complete listing of related documentation and development-support tools for the device, contact the Allwinner FAE or access the Allwinner Customer Service Platform by visiting https://open.allwinnertech.com/.

Revision Number Definition

Revision 0.90-0.9x

This document is released based on the design completion products yet to be mass-produced. Therefore, the information in this document may be modified by reason of mass-produced verification.

All statements, information and recommendations in this document do not constitute any express or implied representation or warranty (including, but not limited to, the warranties of fitness for a particular purpose, merchantability, non-infringement, and accuracy and completeness of the document). Allwinner shall not be liable for any person's use of such information or/and this document.

If you have any questions about the document, please contact us to confirm and obtain the latest version.

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
CAUTION	A caution means that damage to equipment is possible.
NOTE	Provides additional information to emphasize or supplement important points of the main text.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

Notation of Symbols and Numbers

The expressions of the data capacity, the frequency, and the data rate are described as follows.

Type	Symbol	Value
Data capacity	K	1024
	M	1,048,576
	G	1,073,741,824
Frequency, data rate	k	1000
	M	1,000,000
	G	1,000,000,000

The expressions of addresses and data are described as follows.

Number	Example	Description
0x	0x0200,0x79	Address or data in hexadecimal
0b	0b010,0b00 000 111	Data or sequence in binary (register description is excluded.)
X	00X,XX1	In data expression, X indicates 0 or 1.For example, 00X indicates 000 or 001, XX1 indicates 001,011,101 or 111.

Register Attributes

The register attributes that may be found in this document are defined as follows.

Abbr. & Symbol	Description
R	Read Only
R/W	Read/Write
R/WAC	Read/Write-Automatic-Clear, clear the bit automatically when the operation of complete. Writing 0 has no effect.
R/WC	Read/Write-Clear
R/W0C	Read/Write 0 to Clear. Writing 1 has no effect
R/W1C	Read/Write 1 to Clear. Writing 0 has no effect
R/W1S	Read/Write 1 to Set. Writing 0 has no effect
W	Write Only

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Abbr. & Symbol	Description
/	If the default value in the row of a bit or multiple bits is / , this bit is unused.
UDF	If the default value of a bit or multiple bits is UDF , this default value is undefined.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

1 Product Description

1.1 Overview

The A733 family features high-performance platform processors targeted for mid-to-high-end tablets and interactive display applications. It can also be applied in tablet PCs and ARM PCs.

It integrates dual-core ARM Cortex™-A76+hexa-core ARM Cortex™-A55, BXM-4-64 MC1, 3 Tops NPU, LPDDR4/LPDDR4x/LPDDR5 to ensure rapid response and smooth operation for daily applications like online video, web browsing, 3D games, and so on.

It supports rich peripheral interfaces including high-speed interfaces such as PCIe3.0 DM, USB3.1 GEN2 DRD, GMAC, video input interfaces such as MIPI CSI and Parallel CSI, and video output interfaces such as HDMI, RGB, LVDS, MIPI-DSI, eDP1.4b/DP1.4, and E-ink, greatly facilitating product expansion.

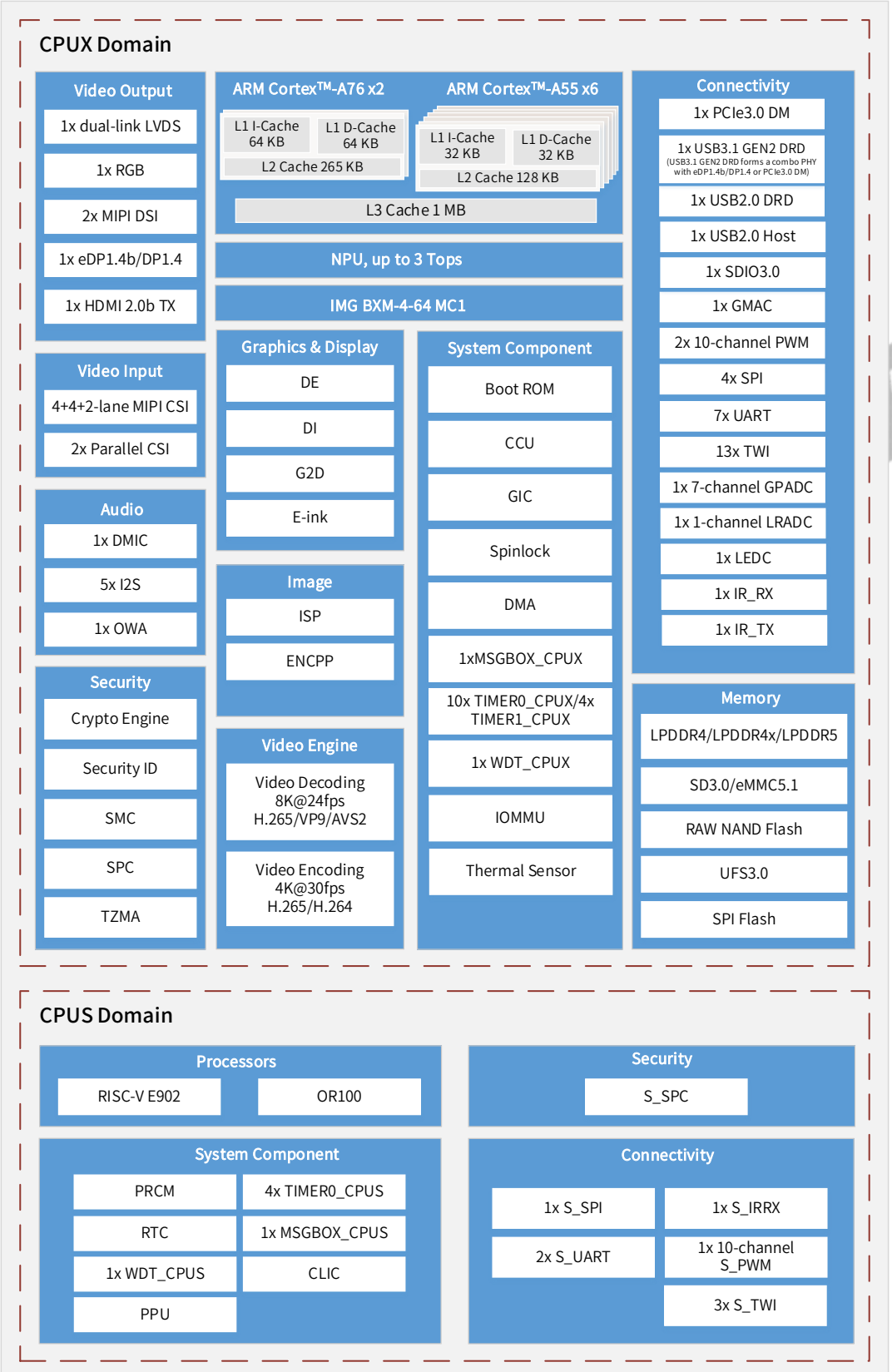
It supports independent/synchronous output on dual display, H.265/VP9/AVS2 video decoding up to 8K@24fps, H.265/H.264 video encoding up to 4K@30fps, and ISP Allwinner SmartColor5.0 display enhancement technology to provide excellent video experience for users. Besides, the digital audio interfaces like I2S, DMIC, and OWA enable this chip family to meet the requirements of mainstream audio recognition solutions.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

1.2 Block Diagram

The following figure shows the system block diagram.

Figure 1-1 System Block Diagram



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

NOTE

Some modules shown in this block diagram are not offered on all devices, please refer to *A733_Datasheet*.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

2 Memory Map

The following table shows the memory mapping viewed from ARM A76+A55.

NOTE

The memory locations not shown in the following tables are either reserved or unused.

Module	Address	Size (Bytes)
BROM & SRAM		
FIXS_BROM	0x00000000---0x00010FFF	68K
HS_BROM	0x00011000---0x00016FFF	24K
NS_BROM	0x00017000---0x00021FFF	44K
SRAM_A2	0x00040000---0x00073FFF	16K+192K (The 16K is only used by CPUS.)
SH_SRAM		
SHARED_SRAM	0x00074000---0x000F3FFF	512K (It can be used after NPU mapping. NPU cannot power off.)
GPU_SYS		
GPU0	0x01800000---0x0188FFFF	576K
VE_SYS		
VE_DEC	0x01C0E000---0x01C0FFFF	8K
VE_ENC	0x01C10000---0x01C10FFF	4K
SYSTEM_APP0		
GPIO	0x02000000---0x02001FFF	8K
CCU	0x02002000---0x02005FFF	16K
NSI	0x02020000---0x0202FFFF	64K
WDT0	0x02050000---0x02050FFF	4K
TIMER1	0x02052000---0x02052FFF	4K
SPC	0x02054000---0x02054FFF	4K
INT_CTRL	0x02055000---0x02056FFF	8K
APB2JTAG	0x02057000---0x02057FFF	4K
PERIPH_APP0		
UART0	0x02500000---0x02500FFF	4K

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

UART1	0x02501000---0x02501FFF	4K
UART2	0x02502000---0x02502FFF	4K
UART3	0x02503000---0x02503FFF	4K
UART4	0x02504000---0x02504FFF	4K
UART5	0x02505000---0x02505FFF	4K
UART6	0x02506000---0x02506FFF	4K
PERIPH_APP1		
TWI0	0x02510000---0x02510FFF	4K
TWI1	0x02511000---0x02511FFF	4K
TWI2	0x02512000---0x02512FFF	4K
TWI3	0x02513000---0x02513FFF	4K
TWI4	0x02514000---0x02514FFF	4K
TWI5	0x02515000---0x02515FFF	4K
TWI6	0x02516000---0x02516FFF	4K
TWI7	0x02517000---0x02517FFF	4K
TWI8	0x02518000---0x02518FFF	4K
TWI9	0x02519000---0x02519FFF	4K
TWI10	0x0251A000---0x0251AFFF	4K
TWI11	0x0251B000---0x0251BFFF	4K
TWI12	0x0251C000---0x0251CFFF	4K
PERIPH_APP2		
LEDC	0x02520000---0x02520FFF	4K
GPADC0	0x02521000---0x02521FFF	4K
THS	0x02522000---0x02522FFF	4K
LRADC	0x02524000---0x02524FFF	4K
IR_TX	0x02525000---0x02525FFF	4K
IR_RX	0x02526000---0x02526FFF	4K
PWM0	0x02527000---0x02527FFF	4K
PWM1	0x02528000---0x02528FFF	4K
PERIPH_APP3		
DMIC	0x02531000---0x02531FFF	4K
I2S0	0x02532000---0x02532FFF	4K
I2S1	0x02533000---0x02533FFF	4K
I2S2	0x02534000---0x02534FFF	4K

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

I2S3	0x02535000---0x02535FFF	4K
I2S4	0x02536000---0x02536FFF	4K
OWA	0x02537000---0x02537FFF	4K
PERIPH_AHB SLAVE		
SPI1	0x02541000---0x02541FFF	4K
SPI2	0x02542000---0x02542FFF	4K
SPI3	0x02543000---0x02543FFF	4K
SYSTEM_ AHB SLAVE		
SYSCTRL	0x03000000---0x03000FFF	4K
CPUX_MSGBOX	0x03004000---0x03004FFF	4K
SPINLOCK	0x03005000---0x03005FFF	4K
SID	0x03006000---0x03006FFF	4K
TIMER0	0x03009000---0x03009FFF	4K
GIC	0x03400000---0x0358FFFF	25*64K
IOMMU0	0x03900000---0x0390FFFF	64K
IOMMU1	0x03910000---0x0391FFFF	64K
NPU_SYS		
NPU	0x03600000---0x03600FFF	4K
STORE_SYS		
SPI0	0x02540000---0x02540FFF	4K
NAND	0x04011000---0x04011FFF	4K
SMHC0	0x04020000---0x04020FFF	4K
SMHC1	0x04021000---0x04021FFF	4K
SMHC2	0x04022000---0x04022FFF	4K
SMHC3	0x04023000---0x04023FFF	4K
DMAC1	0x04024000---0x04025FFF	8K
MSI_LITE1	0x04026000---0x04026FFF	4K
UFS	0x04520000---0x0452FFFF	64K
SPI_FLASH	0x047F0000---0x047F0FFF	4K
HIGH-SPEED INTERFACE		
USB0	0x04100000---0x041FFFFF	1M
USB1	0x04200000---0x042FFFFF	1M
MSI_LITE2	0x04400000---0x04400FFF	4K
PCIE0	0x06400000---0x064FFFFF	5M

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

USB3P1_DRD	0x06A00000---0x06BFFFFF	2M
SERDES_SYS	0x06C00000---0x06C7FFFF	512K
COMBPHY0	0x06C80000---0x06C9FFFF	64K
COMBPHY1	0x06CA0000---0x06CBFFFF	64K
MSI_LITE0_SYS		
GMAC0	0x04508000---0x0450FFFF	64K
MSI_LITE0	0x04600000---0x04600FFF	4K
DMAC0	0x04601000---0x04602FFF	8K
CE_NS	0x04603000---0x046037FF	2K
CE_S	0x04603800---0x04603FFF	2K
CE_KEY_SRAM	0x04604400---0x04604FFF	3K (only accessed by CE)
SECURE_DEBUG_CFG	0x04605000---0x046053FF	1K (used for security debug registers)
MEMC		
MEMC0	0x0A000000---0x0B0FFFFF	17M
SMC0	0x0A000000---0x0A00FFFF	64K
SMC1	0x0A010000---0x0A01FFFF	64K
DRAMC Common	0x0A020000---0x0A02FFFF	64K
CPU AXI2HIF0	0x0A030000---0x0A03FFFF	64K
CPU AXI2HIF1	0x0A040000---0x0A04FFFF	64K
DRAM Controller0	0x0A100000---0x0A4FFFFF	4M
DRAM Controller1	0x0A500000---0x0A8FFFFF	4M
DRAM PHY	0x0A900000---0x0B04FFFF	8M
DE_SYS		
DE0	0x05000000---0x053FFFFF	4M
DI	0x05400000---0x0543FFFF	256K
G2D	0x05440000---0x0547FFFF	256K
EINK	0x05480000---0x05480FFF	4K
VIDEO_OUT0_SYS		
DISPLAY0_TOP	0x05500000---0x05500FFF	4K
TCON_LCD0	0x05501000---0x05501FFF	4K
TCON_LCD1	0x05502000---0x05502FFF	4K
DSC	0x05504000---0x05504FFF	4K
DSI0	0x05506000---0x05507FFF	8K

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

DSI1	0x05508000---0x05509FFF	8K
VIDEO_OUT1_SYS		
DISPLAY1_TOP	0x05510000---0x05510FFF	4K
HDMI	0x05520000---0x0561FFFF	1M
TCON_TV0	0x05730000---0x05730FFF	4K
TCON_TV1	0x05731000---0x05731FFF	4K
eDP0	0x05740000---0x0577FFFF	256K
VIDEO_IN_SYS		
CSI	0x05800000---0x058FFFFF	1M
ISP	0x05900000---0x05CFFFFF	4M
SYSCPUS_APBS0		
S_SPC	0x07002000---0x07002FFF	4K
S_TZMA	0x07003000---0x07003FFF	4K
S_PRCM	0x07010000---0x0701FFFF	64K
S_WDG	0x07021000---0x07021FFF	4K
S_TWD	0x07022000---0x07022FFF	4K
S_PWM	0x07023000---0x07023FFF	4K
S_INTC	0x07024000---0x07024FFF	4K
S_GPIO	0x07025000---0x07026FFF	8K
CPUS_E902_CFG	0x07032000---0x07032FFF	4K
E902_LCNT	0x07033000---0x07033FFF	4K
S_IR_RX	0x07040000---0x07041FFF	8K
CPUIDLE	0x07050000---0x0705FFFF	64K
PPU	0x07060000---0x07078FFF	100K
SYSCPUS_APBS1		
S_UART0	0x07080000---0x07080FFF	4K
S_UART1	0x07081000---0x07081FFF	4K
S_TWI0	0x07083000---0x07083FFF	4K
S_TWI1	0x07084000---0x07084FFF	4K
S_TWI2	0x07085000---0x07085FFF	4K
SYSCPUS_AHBS		
RTC	0x07090000---0x07090FFF	4K
S_TIMER	0x07091000---0x07091FFF	4K
S_SPI	0x07092000---0x07092FFF	4K

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

S_MBOX	0x07094000---0x07094FFF	4K
CPUX Related		
CPU_SUBSYS_CTRL	0x08000000---0x0800FFFF	64K
TIMESTAMP_STA	0x08010000---0x08010FFF	4K
TIMESTAMP_CTRL	0x08020000---0x08020FFF	4K
CPU_PLL_CFG	0x08870000---0x0887FFFF	64K
SPI_FLASH		
SPI_FLASH_XIP	0x0E000000---0x0FFFFFFF	32M (SPI_FLASH should be configured as XIP mode to access the space.)
PCIE		
PCIE_SLAVE	0x20000000---0x27FFFFFF 0x440000000---0x53FFFFFFF	4G
DRAM Space		
DRAM SPACE	0x40000000---0x43FFFFFFF	16G (Note: E902 only access the address space ranging from 0x4000 0000---0x7FFF FFFF)

The following table shows the memory mapping viewed from RISC-V E902.

Module	Address	Size (Bytes)	Description
SHARED_SRAM	0x00074000---0x000F3FFF	512K	It can be used after NPU mapping. NPU cannot power off.
L4_TOP_CONN	0x00080000---0x06FFFFFF	1G-192K-512K	CPUX subsystem peripherals
CPUS_CFG	0x07000000---0x0709FFFF		CPUS subsystem peripherals
Other modules	0x08000000---0x3FEFFFFF		Same with CPUX memory mapping
SRAM SPACE	0x40000000---0x40033FFF	208K	0x00_0000~0x0003_3FFFi mapped to DDR to access sramA2
DRAM SPACE	0x40034000---0x7FFFFFFF	1G-208K	
DRAM SPACE	0x80000000---0xBFFFFFFF	1G	The default configuration is E902_ddr_remap=3 b0000, the E902 address 0x8000 0000---0xBFFF FFFF is not mapped.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

DRAM SPACE	0xC0000000---0xFFFFFFFF	1G	Configure e902_remap=4 h1. Then, the E902 address 0x8000 0000---0xBFFF FFFF is mapped to DDR address 0xC000 0000---0xFFFF FFFF.
DRAM SPACE	0x100000000---0x13FFFFFFF	1G	Configure e902_remap=4 h2. Then, the E902 address 0x8000 0000---0xBFFF FFFF is mapped to DDR address 0x10000 0000---0x13FFF FFFF.
DRAM SPACE	0x140000000---0x17FFFFFFF	1G	Configure e902_remap=4 h3. Then, the E902 address 0x8000 0000---0xBFFF FFFF is mapped to DDR address 0x14000 0000---0x17FFF FFFF.
DRAM SPACE	0x180000000---0x1BFFFFFFF	1G	Configure e902_remap=4 h4. Then, the E902 address 0x8000 0000---0xBFFF FFF is mapped to DDR address 0x18000 0000---0x1BFFF FFFF.
DRAM SPACE	0x1C0000000---0x1FFFFFFFF	1G	Configure e902_remap=4 h5. Then, the E902 address 0x8000 0000---0xBFFF FFFF is mapped to DDR address 0x1C000 0000---0x1FFFF FFFF.
DRAM SPACE	0x200000000---0x23FFFFFFF	1G	Configure e902_remap=4 h6. Then, the E902 address 0x8000 0000---0xBFFF FFFF is mapped to DDR address 0x20000 0000---0x23FFF FFFF.
DRAM SPACE	0x240000000---0x27FFFFFFF	1G	Configure e902_remap=4 h7. Then, the E902 address 0x8000 0000---0xBFFF FFFF is mapped to DDR address 0x24000 0000---0x27FFF FFFF.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

DRAM SPACE	0x280000000---0x2BFFFFFFF	1G	Configure e902_remap=4 h8. Then, the E902 address 0x8000 0000---0xBFFF FFFF is mapped to DDR address 0x28000 0000---0x2BFFF FFFF.
DRAM SPACE	0x2C0000000---0x2FFFFFFFF	1G	Configure e902_remap=4 h9. Then, the E902 address 0x8000 0000---0xBFFF FFFF is mapped to DDR address 0x2C000 0000---0x2FFFF FFFF.
DRAM SPACE	0x300000000---0x33FFFFFFF	1G	Configure e902_remap=4 hA. Then, the E902 address 0x8000 0000---0xBFFF FFFF is mapped to DDR address 0x30000 0000---0x33FFF FFFF.
DRAM SPACE	0x340000000---0x37FFFFFFF	1G	Configure e902_remap=4 Hb. Then, the E902 address 0x8000 0000---0xBFFF FFFF is mapped to DDR address 0x34000 0000---0x37FFF FFFF.
DRAM SPACE	0x380000000---0x3BFFFFFFF	1G	Configure e902_remap=4 Hc. Then, the E902 address 0x8000 0000---0xBFFF FFFF is mapped to DDR address 0x38000 0000---0x3BFFF FFFF.
DRAM SPACE	0x3C0000000---0x3FFFFFFFF	1G	Configure e902_remap=4 Hd. Then, the E902 address 0x8000 0000---0xBFFF FFFF is mapped to DDR address 0x3C000 0000---0x3FFFF FFFF.
DRAM SPACE	0x400000000---0x43FFFFFFF	1G	Configure e902_remap=4 hE. Then, the E902 address 0x8000 0000---0xBFFF FFFF is mapped to DDR address 0x40000 0000---0x43FFF FFFF.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

3 System Boot

3.1 Boot ROM (BROM)

3.1.1 Overview

The BROM system is actually split up into two parts: FEL and Media Boot. The task of FEL is to write the external data to the local NVM, and the task of the Media Boot is to load from NVM to obtain and run an effective and legitimate BOOT0.

The BROM system includes the following features:

- Supports the core0 of A55 CPU boot process
- Supports Mandatory Upgrade Process through USB or SD card
- Supports GPADC to select the kind of boot media to boot
- Supports eFuse to select the kind of boot media to boot
- Supports Normal Boot and Secure Boot
- Supports loading only certified firmware in Secure Boot
- Ensures that the Secure Boot is in a trusted environment
- Supports cryptographic algorithms
  - ECDSA-256/384/521
  - RSA-2048/3072/4096
  - SHA-256/SHA-512

3.1.2 Security Settings

If the SoC has implemented the ARM TrustZone technology, the SoC will enable the ARM TrustZone technology when the Secure Enable Bit is enabled. The minimal security functionality, an ARM TrustZone technology based system, must be implemented for its Trusted Boot.

So the BROM is divided into Normal BROM and BROM Monitor. The BROM Monitor protects against the potential threat of attackers modifying the areas of codes or data in programmable memory.

3.1.3 Boot Medium Select

The BROM system supports the following boot media:

- SD Card
- eMMC
- RAW NAND Flash

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- UFS
- SPI NOR Flash (Quad Mode and Single Mode)
- SPI NAND Flash

There are two ways to select the boot medium: GPADC Select and eFuse Select. The BROM will read the state of BOOT_MODE first, and then select the boot medium to boot according to the state of BOOT_MODE. The BOOT_MODE is the BROM_Config in the eFuse mapping.

The following table shows the BOOT_MODE setting:

Table 3-1 BOOT_MODE Setting

BOOT_MODE[0]	Boot Select type
0	GPADC boot select
1	eFuse boot select

3.1.3.1 GPADC Boot Select

If the state of the BOOT_MODE is 0, select the GPADC Boot.

If BROM fails to boot from the selected medium, it will try other media with the following priority:

EMMC_USR -> EMMC_BOOT -> SLC_NAND -> MLC_NAND -> SPI_NOR -> SPI_NAND -> UFS

And the medium selected by GPADC will be skipped.

For example, when BROM fails to boot from SPI NOR, it will try other media with the following priority:

SPI NOR (selected by GPADC) -> EMMC_USR -> EMMC_BOOT -> SLC_NAND -> MLC_NAND -> SPI_NAND -> UFS

The following table shows GPADC Boot Select setting.

Table 3-2 GPADC Boot Select Setting

KEY_VALUE	Boot Select type
0x00~0xb6	SMHC0->MLC NAND->SLC NAND->try
0xb7~0x22b	SMHC0->SLC NAND->MLC NAND->try
0x22c~0x3af	SMHC0->EMMC_USER->EMMC_BOOT->try
0x3b0~0x57b	SMHC0->EMMC_BOOT->EMMC_USER->try
0x57c~0x73c	SMHC0->SPI0 NOR->try
0x73d~0x8cc	SMHC0->SPI0 NAND->try
0xe7d~0xfff	SMHC0->UFS->try

NOTE

When trying SPI NOR, BROM try quad mode first, then single mode.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.1.3.2 eFuse Boot Select

If the state of the BOOT_MODE is 1, select the eFuse Boot.

The eFuse_Boot_Select_Cfg is divided into 3 groups and each group is 4-bit. The following table shows the groups of eFuse_Boot_Select.

Table 3-3 Groups of eFuse_Boot_Select

eFuse_Boot_Select_Cfg [11:0]	Description
eFuse_Boot_Select[3:0]	eFuse_Boot_Select_1
eFuse_Boot_Select[7:4]	eFuse_Boot_Select_2
eFuse_Boot_Select[11:8]	eFuse_Boot_Select_3

These three groups take effect with the following priority:

eFuse_Boot_Select_1 -> eFuse_Boot_Select_2 -> eFuse_Boot_Select_3

For example, eFuse_Boot_Select_2 will not take effect unless eFuse_Boot_Select_1 is set as 0b1111(skip), eFuse_Boot_Select_3 will not take effect unless eFuse_Boot_Select_2 is set as 0b1111(skip), etc. If all three groups are set to 0b1111, no other groups can be used for boot select, BROM assume try is selected.

In the Try mode, the BROM follows the order below to select the boot medium:

SMHC0 -> SMHC2 -> RAW NAND Flash ->SPI NOR -> SPI NAND Flash -> UFS

The following table shows the boot medium priority for the different values of eFuse_Boot_Select_n, where n = [3:1].

Table 3-4 eFuse Boot Select Setting

eFuse_Boot_Select_n	Boot media
0000	Try (except SPI in PI)
0001	SMHC0->SLC NAND -> MLC NAND
0010	SMHC0->EMMC_USER -> EMMC_BOOT
0011	SMHC0->SPI0 NOR
0100	SMHC0->SPI0 NAND
0101	SMHC0->MLC NAND -> SLC NAND
0110	SMHC0->MMC_BOOT -> EMMC_USER
0111	SMHC0->UFS
1111	Skip (when n=1,2) -- Boot media is decided by eFuse_Boot_Select_(n+1) Try (when n=3)

3.1.4 Boot Process Description

3.1.4.1 Normal BROM Process

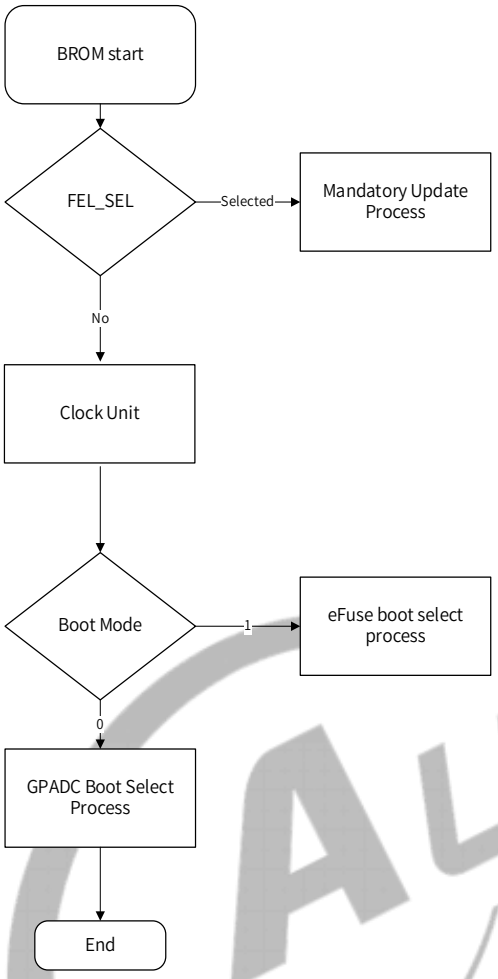
In Normal BROM Mode, the system boot starts from Core0 of A55 CPU, and then the BROM will read the state of the FEL pin. If the FEL Pin signal is detected to pulled to high level, then the

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

system will jump to the Fast Boot process; otherwise, it will jump to the mandatory upgrade process.

The following figure shows the boot process in Normal BROM Mode.

Figure 3-1 Boot Process in Normal BROM Process

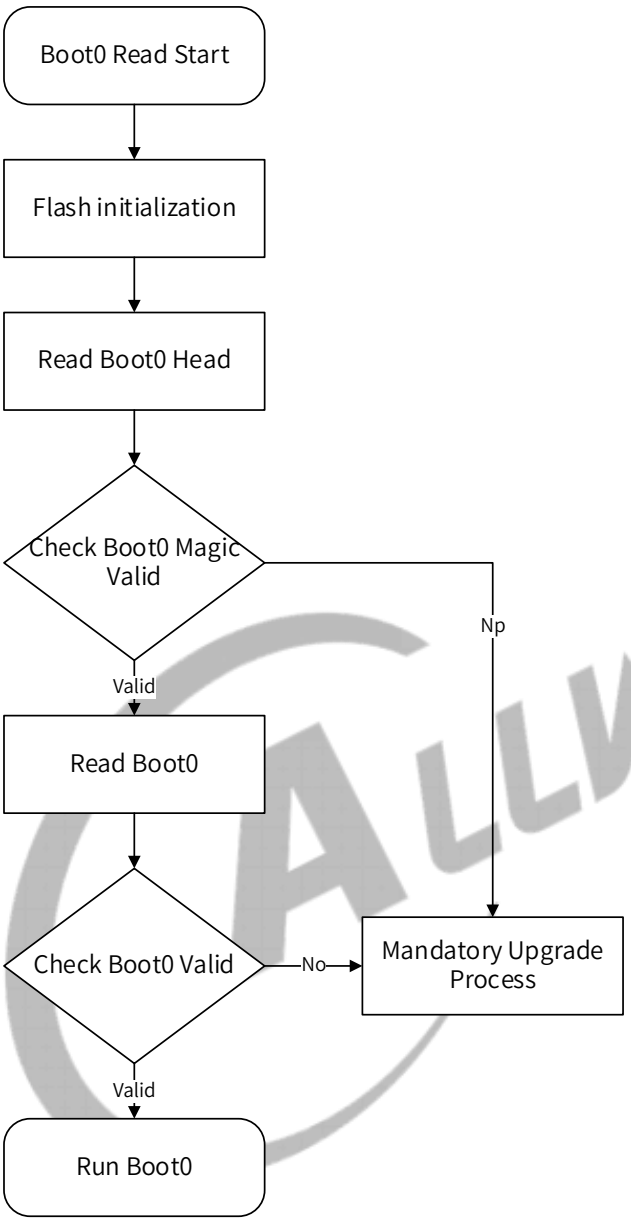


Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

The GPADC boot select process and the efuse boot select process will read the boot0, and check the validity of boot0.

The following figure shows the boot0 read process.

Figure 3-2 Boot0 Read Process

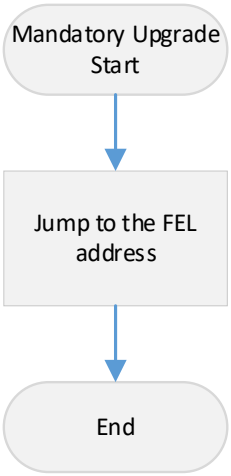


Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.1.4.2 Mandatory Upgrade Process

If the FEL pin is detected to pull low, the system will jump to the mandatory upgrade process. The following figure shows the mandatory upgrade process.

Figure 3-3 Mandatory Upgrade Process



ALLWINNER

4 Power, Reset, and Clock Management

4.1 Clock Controller Unit (CCU)

4.1.1 Overview

The clock controller unit (CCU) controls the PLL configurations and most of the clock generation, division, distribution, synchronization, and gating in CPUX domain. The input signals of the CCU include the external clock for the reference frequency (26MHz). The outputs from the CCU are mostly clocks to other blocks in the system.

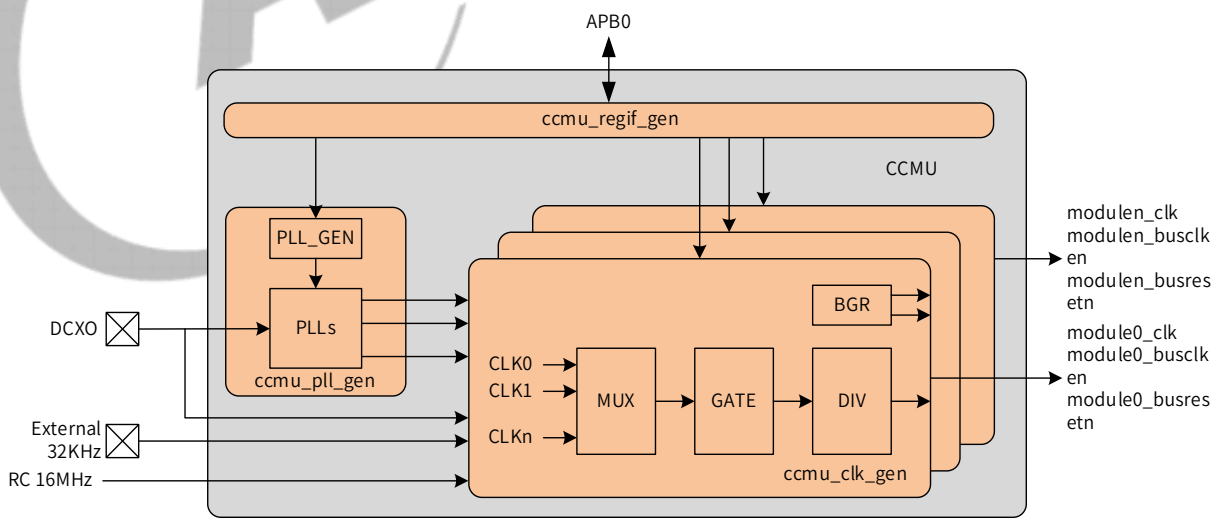
The CCU includes the following features:

- Bus source and divisions
- Clock output control
- Configurable module clock
- Bus clock gating
- Bus software reset

4.1.2 Block Diagram

The following figure shows the functional block diagram of the CCU.

Figure 4-1 CCU Block Diagram

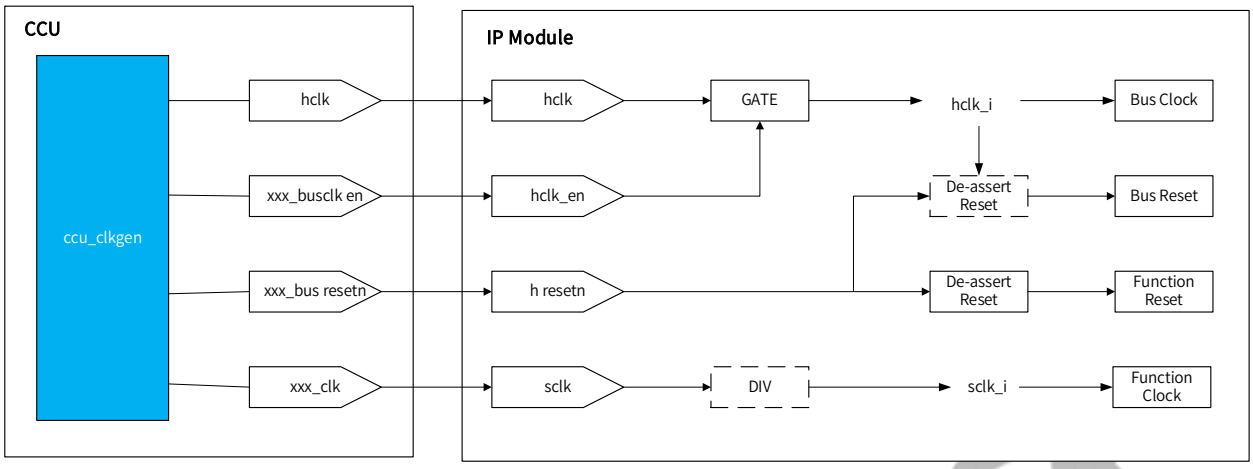


Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.3 Functional Description

4.1.3.1 Typical Application

Table 4-1 PLL Typical Configurations



CCU outputs the clock and reset of buses and modules.

Before using the bus clock of modules, the clock gating of modules should be enabled in advance. for some subsystems, CCU offers modules with the exclusive bus clock that has been added with gating. Therefore, to use the exclusive bus clock, enabling the clock gating is necessary.

Each module reset is released by input reset signals. To prevent some modules from not performing synchronous release, release module reset, and then enable the output gating of modules.

4.1.3.2 PLL Specifications

The A733 has 21 PLLs, which are distributed in CCU, CPU, and VIDEOOUT. The specifications of each PLL are shown in the following table.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Table 4-2 PLL Specifications

Subsystem	PLL	Fvco	Pre-divider	Typical VCO frequency	Post-divider	Spread Spectrum	Linear FM	Jitter Requirements Pk-Pk	Lock time	Reference clock
CPU	CPU_BACK_PLL	1.26G~2.52G	1/2	<2.0G	P0: 1~8	Yes	No	50ps	0.1ms	26MHz
	CPU_L_PLL	480M~2.26G	1~8	<2.0G	M0: 1~4 M1: 1~16	Yes	Yes		1.5ms	26MHz
	CPU_B_PLL	480M~2.26G	1~8	<2.0G	M0: 1~4 M1: 1~16	Yes	Yes		1.5ms	26MHz
	CPU_DSU_PLL	480M~2.26G	1~8	<2.0G	M0: 1~4 M1: 1~16	Yes	Yes		1.5ms	26MHz
CCMU	PLL_REF	1.9G~2.8G	1/2	2.496G	P0: 1~128	No	No		0.1ms	26MHz
	PLL_DDR	1.26G~2.52G	1/2	1.8G	P0: 1~8	Yes	No	40ps+freqperiod*2.5% (200M~667M) 140ps+freqperiod*2.5% (667M~1066M)	0.1ms	24MHz
	PPL_PERI0	1.26G~2.52G	1/2	2.4G	P0: 1~8 P1: 1~8 P2: 1~8	Yes	No	200ps	0.1ms	24MHz
	PLL_PERI1	1.26G~2.52G	1/2	2.4G/2.496G	P0: 1~8 P1: 1~8 P2: 1~8	Yes	No	200ps	0.1ms	24MHz
	PLL_GPU0	1.26G~2.52G	1/2	1.8G	P0: 1~8	Yes	No	50ps	0.1ms	24MHz
	PLL_VIDEO0	1.26G~2.52G	1/2	2.376G	P0: 1~8 P1: 1~8	Yes	No	70ps @ 1GHz	0.1ms	24MHz
	PLL_VIDEO1	1.26G~2.52G	1/2	2.376G	P0: 1~8 P1: 1~8	Yes	No		0.1ms	24MHz
	PLL_VIDEO2	1.26G~2.52G	1/2	2.376G	P0: 1~8 P1: 1~8	Yes	No		0.1ms	24MHz
	PLL_VE0	1.26G~2.52G	1/2	1.872G	P0: 1~8	Yes	No	200ps	0.1ms	24MHz
	PLL_VE1	1.26G~2.52G	1/2	1.872G	P0: 1~8	Yes	No	200ps	0.1ms	24MHz
	PLL_AUDIO0	1.26G~2.52G	1/2		P0: 1~128	Yes	No	200ps (time accuracy<50 ppm)	0.1ms	24MHz
	PLL_AUDIO1	1.8G~3.1G	1/2	3.072G/ 2.359296G	P0: 1~8 P1: 1~8	Yes	No	200ps (time accuracy <50ppm)	0.1ms	24MHz 24MHz
	PLL_NPU	1.26G~2.52G	1/2	1.8G	P0: 1~8	Yes	No	50ps	0.1ms	24MHz
	PLL_DE	1.26G~2.52G	1/2	2.088G	P0: 1~8 P1: 1~8	Yes	No	200ps	0.1ms	24MHz
VIDEO_OUT0	PLL_DIS0	1.26G~2.52G	1/2	1.611G/ 1.782G	M0: 1~8 M1: 1~8 M2: 1~8 M3: 1~8	Yes	Yes	70ps @ 1GHz	0.1ms	26MHz
	PLL_DIS1	1.26G~2.52G	1/2	1.611G/ 1.782G	M0: 1~8 M1: 1~8 M2: 1~8 M3: 1~8	Yes	Yes	70ps @ 1GHz	0.1ms	26MHz
VIDEO_OUT1	PLL_HDMI	1.26G~2.52G	1/2	2.376G	P0: 1~128	No	No	88.33ps	0.1ms	26MHz

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.3.3 PLL Configuration

The typical configurations of each PLL are shown in the following table.

Table 4-3 PLL Typical Configuration

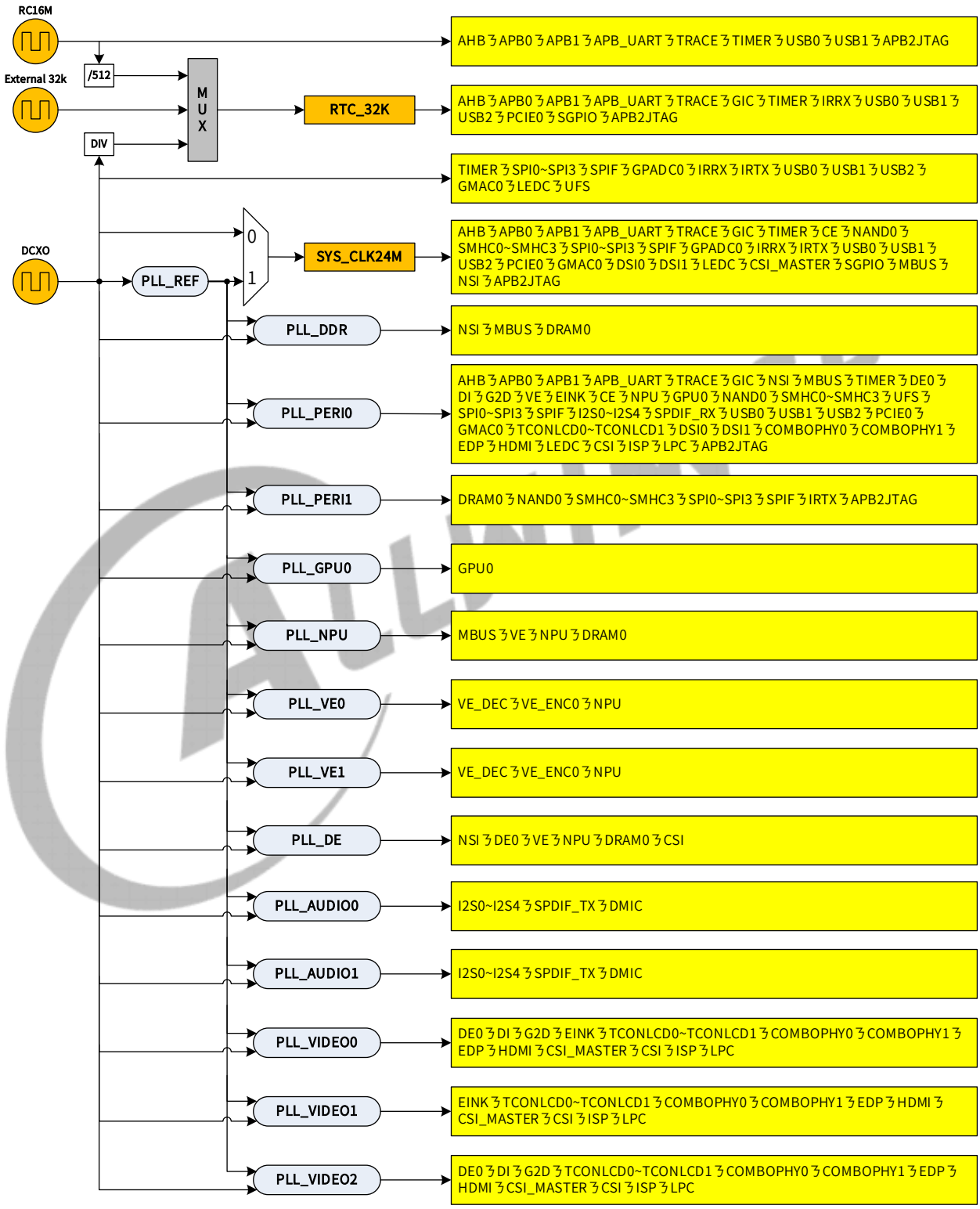
PLL	DCXO/MHz	REF_SEL	N(INT)	N(FRAC)	VCO/MHz	OUT/MHz	Remark
REF_PLL	26	/	96		2496	24	
PERI0_PLL	24	0	100		2400	2x：1200 3x：800 5x：480	
PERI1_PLL	24	0	104		2496	2x：1248 3x：832 5x：499.2	
DDR_PLL	24	0	75		1800	900	
NPU_PLL/ GPU_PLL	24	0	70		1680	840	
DE_PLL	24	0	87		2088	4x：1044 3x：696	
VIDEO0~1_PLL	24	0	99		2376	4x：1188 3x：792	
VIDEO2_PLL	24	0	88		2112	3x：704	
VE0_PLL	24	0	91		2184	546	
VE1_PLL	24	0	87		2088	696	
AUDIO0_PLL	24	0	67	0x179A7	1625.7024	90.3168	22.5792*4
AUDIO1_PLL	24	/	128		3072	1536/614.4	24.576

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.3.4 PLL Distribution

The following figure shows the PLL distribution for buses and modules.

Figure 4-2 PLL Distribution



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.3.5 PLL Spreading/Fractional Division

The fractional division is to add a fractional value to the divider N of a PLL to achieve a more precise frequency configuration. By applying fractional division, the multiplication factor N of the PLL can be expressed as N.x, where N represents the added fractional value.

The PLL spreading is to add a triangular wave to the N value of a PLL to let the final output frequency exhibit a triangular wave variation. Spreading parameters consist of spread amplitude and spread spectrum period. The spread amplitude refers to the range of variation in the output frequency; while the spread spectrum period is the duration of one cycle of the triangular wave modulation, whose reciprocal is spread spectrum frequency.

PLL spreading/fractional division is configured through PLLx_PAT0_CTRL_REG and PLLx_PAT1_CTRL_REG; therefore, the generic/linear PLL spreading/fractional division procedures are the same. All the parameters in the two types of registers are divided into static parameters and control parameters.

Static parameters are used to adjust the order and phase interpolation of the fractional division loop and don't support dynamic switching. To alter parameters, disable PLL spreading/fractional division, configure static parameters, and then enable PLL spreading/fractional division. The parameters are shown as below.

- SPR_FREQ_MODE: SDM mode switching.
- PLL_PI_EN: It is used to decide whether to enable phase interpolation (PI) mode.
- PLL_PI_CFG: PI circuit current control.
- SMOOTH_EN: It is used to enable frequency modulation smooth.
- DITHER_EN: It is used to enable dither. When dither is enabled, a pseudo-random sequence will be added to the frequency modulation curve.

Control parameters are used to control frequency modulation curve and support dynamic switching. It should be reminded that if the SMOOTH_EN is set, control parameters only can be switched in the condition that SDM_BUSY is set to 0. The control parameters are shown as below.

- WAVE_STEP: Spreading step. The formula is shown as below.

  $$WAVE_STEP = 2^{17}*(x2-x1)*2/(Fclk/FREQ)$$

  x2 is the upper limit; x2 is the lower limit; Fclk is the PLL reference clock frequency; FREQ is the spreading slope. PLL multiplication factors range from N.x1 to N.x2.

- WAVE_BOT: Spreading starting point. The formula is shown as below.

  for upward frequency spreading, $SDM_BOT = x1*2^{17}$

  for downward frequency spreading, $SDM_BOT = x2*2^{17}$

- FREQ: Spreading slope. To dynamically switch this parameter, switch WAVE_STEP at the same time.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- SDM_DIRECTION: Spreading direction, including upward frequency spreading and downward frequency spreading. During upward frequency spreading, the curve starts from x1 and then adjusts to x2 before reversing; during downward frequency spreading, the curve starts from x2 and then adjusts to x1 before reversing. To dynamically switch this parameter, switch WAVE_BOT at the same time.
- FRAC_EN: Fractional division enable.
- FRAC_IN: Fractional division frequency point. The formula is shown as below.

FRAC_IN = x*2^17

The master switch of PLL spreading/fractional division is SIG_DELT_PAT_EN. It should be enabled before PLL spreading/fractional division usage.

PLL spreading/fractional division configuration is shown as below.

SIG_DELT_PAT_EN	FRAC_EN	WAVE_STEP	FRAN_IN	MODE
1	0	Not equal to 0	/	PLL spreading
1	0	Equal to 0	/	fractional division
1	1	/	Arbitrary	fractional division

4.1.3.6 Linear PLL Frequency Modulation

The linear PLL frequency modulation mode is designed to address the re-locking issue encountered when switching N values in integer frequency duplication. In this mode, the N value can be directly configured, and the PLL will smoothly converge the N value to the target frequency point based on the configured frequency slope.

When configuring linear frequency modulation, static parameters in the fractional divider need to be set, while the control parameters are automatically managed by the linear frequency modulation.

4.1.4 Programming Guidelines

4.1.4.1 Generic PLL Frequency Modulation

All the PLLs in the CCMU subsystem are generic PLLs.

Some PLLs are configured to source from DCXO or REFPLL. The frequency of DCXO is same to that of REFPLL, which can be 24M/19.2M/26M. The actual DCXO frequency can be obtained by reading the XO_CTRL0_REG (bit[15:14]). The REFPLL frequency is fixed to 24M.

The jitter performance of DCXO is better than that of REFPLL. for the PLLs that have no requirements on output clock performance, REFPLL is recommended as parameters can be uniformly configured. for the PLLs that have requirements on output clock performance, DCXO is recommended; the parameters can be configured based on the frequency switching, and decimal frequency division can be used in the case that the final frequency cannot be obtained by integer frequency multiplier.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

PLL Enable

There are two configuration methods. The one is used in the startup phase, during which there is a period of instable clock output once when PLL is enabled. The other is not recommended to be used in the startup phase as there exists glitches when PLL_OUTPUT_GATE is enabled; after PLLs become stable, output clock.

Method 1:

Step 1 Set PLL_LDO_EN in the PLL_DDR_CTRL_REG as 1.

Step 2 Set PLL_OUTPUT_GATE in the PLL_DDR_CTRL_REG as 1.

Step 3 Set the values of N, M1, M0, P in the PLL_DDR_CTRL_REG.

Step 4 Set PLL_EN in the PLL_DDR_CTRL_REG as 1.

Step 5 Set LOCK_ENABLE in the PLL_DDR_CTRL_REG as 1.

Step 6 Wait the LOCK status in the PLL_DDR_CTRL_REG to be 1, and perform the adjustment for three times.

Step 7 After 20 us latency, the PLL_DDR can be used.

Method 2:

Step 1 Set PLL_LDO_EN in the PLL_DDR_CTRL_REG as 1.

Step 2 Set the values of N, M1, M0, P in the PLL_DDR_CTRL_REG.

Step 3 Set PLL_EN in the PLL_DDR_CTRL_REG as 1.

Step 4 Set LOCK_ENABLE in the PLL_DDR_CTRL_REG as 1.

Step 5 Wait the LOCK status in the PLL_DDR_CTRL_REG to be 1, and perform the adjustment for three times.

Step 6 Wait 20 us latency.

Step 7 Set the PLL_OUTPUT_GATE in the PLL_DDR_CTRL_REG as 1. Then, PLLs can be used.

NOTE

When more than one channel output exists in PLLs, write 1 to PLL_OUTPUT_GATE for each output clock to be used.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

PLL Disable

Follow the steps below to disable PLLs. Before this, ensure that the PLL clock has been switched to other clock source or closed.

Step 1 Set PLL_OUTPUT_GATE in the PLL_DDR_CTRL_REG as 0.

Step 2 Set LOCK_ENABLE in the PLL_DDR_CTRL_REG as 0.

Step 3 Set PLL_EN in the PLL_DDR_CTRL_REG as 0.

Step 4 Set PLL_LDO_EN in the PLL_DDR_CTRL_REG as 0.

NOTE

It is not suggested to enable or disable the PLLs during usage, as the PLL enable/disable will lead to the disturbance among PLLs, which will cause system instability. When the clock is not required, it is recommended to set the PLL_OUTPUT_GATE bit in the PLLx_CTRL_REG as 0.

PLL Spreading

Step 1 Enable PLLs.

Step 2 Configure the static parameters as below

- SPR_FREQ_MODE is recommended to be 3.
- PLL_PI_EN is recommended to be 1.
- PLL_PI_CFG is recommended to use the default value.
- SMOOTH_EN is recommended to be 0.
- DITHER is recommended to be 0.

Step 3 Configure WAVE_STEP, WAVE_BOT, FREQ, SDM_DIRECTION, FRAC_IN and FRAC_EN in conformity with PLL spreading/fractional divider formulas.

Step 4 Configure SIG_DELT_PAT_EN and other parameters to enable PLL spreading/fractional dividers.

Step 5 To adjust static parameters, configure SIG_DELT_PAT_EN as 0. After SDM_BUSY is 0, go back to step 1.

Step 6 To adjust control parameters when PLL spreading/fractional dividers are enabled, configure WAVE_STEP, WAVE_BOT, FREQ, SDM_DIRECTION, and FRAC_IN.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 7 To disable PLL spreading, set SIG_DELT_PAT_EN as 0. To enable PLL spreading next time, judge SDM_BUSY as 0 first.

PLL Frequency Modulation

Follow the steps below to perform PLL frequency modulation.

Step 1 Ensure the PLL is enabled. If not, enable the PLL by referring to the section PLL Enable.

Step 2 Set PLL_OUTPUT_GATE in the PLLx_CTRL_REG as 0

Step 3 Configure N, M1, M0, and P factors in the PLLx_CTRL_REG.

Step 4 Write 0 to LOCK_ENABLE in the PLLx_CTRL_REG, and then write 1.

Step 5 Wait the LOCK in the PLLx_CTRL_REG to be 1. Judge the state for three times.

Step 6 Wait 20 us latency.

Step 7 Set the PLL_OUTPUT_GATE in the PLLx_CTRL_REG as 1.

4.1.4.2 PLL Lock Status Judgement

As the output signal is unstable in the PLL initial startup phase or when the N value of FM alters, frequency fluctuation may occur when lock status is enabled for the first time. Therefore, it is recommended to read the lock status after 3 us. If the lock status is found to be well enabled after reading for three times, it proves to be stable.

4.1.4.3 Bus Clock Configuration

The bus clock supports dynamic switching, but the switching process needs to obey the following two rules.

- To switch from a lower frequency to a higher frequency: configure the frequency division factor first, and then switch the clock source.
- To switch from a higher frequency to a lower frequency: switch the clock source first, and then set the frequency division factor.

The bus frequencies are as follows.

- **AHB:** The typical frequency is 200 MHz. The maximum frequency is no more than 200 MHz.
- **APB0:** The typical frequency is 100 MHz. The maximum frequency is no more than 100 MHz.
- **APB1:** The typical frequency is 100 MHz. The maximum frequency is no more than 100 MHz.
- **APB_UART:** The frequency is configured based on UART request, which is no more than 160 MHz.
- **NSI:** The typical frequency is 700 MHz. The maximum frequency is no more than 700 MHz.
- **MBUS:** The typical frequency is 600 MHz. The maximum frequency is no more than 600 MHz.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Of which, the suggested NSI clock source configuration is shown as below.

When NSI_CLK runs at 700MHz, select DEPLL3X as the clock source, whose frequency is 696MHz by default. Therefore, it is not recommended to modify the DEPLL3X frequency.

As DEPLL3X/DEPLL4X will be the clock source of DE0_CLK. If DE module runs at 4KHz, the needed clock frequency is 696 MHz; then, DEPLL3X is selected as the clock source. If DE module runs at 2KHz, DEPLL3X is not recommended to be the clock source; other clock sources should be considered.

NOTE

for NSI/MBUS clock configuration, write 1 to NSI_CLK_REG (bit[27]) and MBUS_CLK_REG (bit[27]) to update the NSI_DIV1and MBUS_DIV1, then the readback result will be the updated parameters. If not, the readback result will be the initial state.

4.1.4.4 Module Clock Configuration

Generic Configuration

for the bus gating reset register of a module, the reset bit is de-asserted first, and then the gating clock is passed to avoid potential problems caused by the asynchronous release of the reset signal.

for all module clocks, configure the clock sources and frequency division factors first, and then write 1 to the gating clock. for the configuration order of the clock source and frequency division factor, follow the rules below:

- To switch from a lower frequency to a higher frequency: set the frequency division factor first, and then configure the clock source.
- To switch from a higher frequency to a lower frequency: configure the clock source first, and then set the frequency division factor.

GPU Clock Configuration

GPU working clock differs from generic working clock. for the generic working clock, clock frequency division is realized by counting, and FACTOR_M indicates division coefficient; for the GPU working clock, FACTOR_M indicates the designated cycles of masks every 16 cycles, through which the clock frequency division is realized. There are two points should be noted.

- The GPU_CLK frequency computing formula is GPU_CLK=CLK_SRC*((16-M)/16).
- The effective clock cycle of GPU_CLK is consistent with clock frequency.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.4.5 Update Clock Configuration

The configured clock parameters of NSI/MBUS/GPU0/DRAM0 should be additionally updated. The following precautions are shown as below.

Write 1 to NSI/MBUS/GPU0/DRAM0_UPD bit in the NSI/MBUS/GPU0/DRAM0_CLK_REG to update the configured parameters of NSI/MBUS/GPU0/DRAM0_SEL, NSI/MBUS/GPU0/DRAM0_DIV1, NSI/MBUS/GPU0/DRAM0_CLK_GATING; then, the readback result will be the updated parameters. If not, the readback result will be the original state.

4.1.4.6 Auto Clock Gating

Some buses and PLLs support auto clock gating. The detailed configuration methods are shown as below.

Bus Auto Gating Configuration

Step 1 Set AHB_MAT_CLK_GATING_REG (bit[31]) as 0 to disable auto clock gating, and then AHB BUSMATRIX clock will be always enabled; set AHB_MAT_CLK_GATING_REG (bit[31]) as 1 to enable auto gating, then the clock will be auto disabled in case of no bus operation.

Step 2 Set AHB_MAT_CLK_GATING_REG (bit[29]) as 0 to disable auto gating, and then SD BUSMATRIX clock will be always enabled; set AHB_MAT_CLK_GATING_REG (bit[29]) as 1 to enable auto gating, then the clock will be auto disabled in case of no bus operation.

PLL Auto Gating Configuration

The following takes DDRPLL as an example to explicate the auto clock gating of PLLs.

Step 1 Set DDRPLL_GATE_EN_REG (bit[16])as 1 and then set DDRPLL_GATE_EN_REG (bit[0])as 1 to disable auto gating.

Step 2 Set DDRPLL_GATE_EN_REG (bit[16]) as 1 and then set DDRPLL_GATE_EN_REG (bit[0])as 0 to enable auto gating.

Step 3 Read DDRPLL_GATE_STAT_REG(bit[16]) to acknowledge the current DDRPLL Clock Gate Status.

4.1.5 Register List

Module Name	Base Address
CCU	0x02002000

Register Name	Offset	Description
PLL_DDR_CTRL_REG	0x0020	PLL_DDR Control Register
PLL_DDR_LOCK_CTRL_REG	0x0024	PLL_DDR Lock Control Register
PLL_DDR_PAT0_CTRL_REG	0x0028	PLL_DDR Pattern0 Control Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
PLL_DDR_PAT1_CTRL_REG	0x002C	PLL_DDR Pattern1 Control Register
PLL_DDR_BIAS_REG	0x0030	PLL_DDR Bias Register
PLL_PERI0_CTRL_REG	0x00A0	PLL_PERI0 Control Register
PLL_PERI0_LOCK_CTRL_REG	0x00A4	PLL_PERI0 Lock Control Register
PLL_PERI0_PAT0_CTRL_REG	0x00A8	PLL_PERI0 Pattern0 Control Register
PLL_PERI0_PAT1_CTRL_REG	0x00AC	PLL_PERI0 Pattern1 Control Register
PLL_PERI0_BIAS_REG	0x00B0	PLL_PERI0 Bias Register
PLL_PERI1_CTRL_REG	0x00C0	PLL_PERI1 Control Register
PLL_PERI1_LOCK_CTRL_REG	0x00C4	PLL_PERI1 Lock Control Register
PLL_PERI1_PAT0_CTRL_REG	0x00C8	PLL_PERI1 Pattern0 Control Register
PLL_PERI1_PAT1_CTRL_REG	0x00CC	PLL_PERI1 Pattern1 Control Register
PLL_PERI1_BIAS_REG	0x00D0	PLL_PERI1 Bias Register
PLL_GPU0_CTRL_REG	0x00E0	PLL_GPU0 Control Register
PLL_GPU0_LOCK_CTRL_REG	0x00E4	PLL_GPU0 Lock Control Register
PLL_GPU0_PAT0_CTRL_REG	0x00E8	PLL_GPU0 Pattern0 Control Register
PLL_GPU0_PAT1_CTRL_REG	0x00EC	PLL_GPU0 Pattern1 Control Register
PLL_GPU0_BIAS_REG	0x00F0	PLL_GPU0 Bias Register
PLL_VIDEO0_CTRL_REG	0x0120	PLL_VIDEO0 Control Register
PLL_VIDEO0_LOCK_CTRL_REG	0x0124	PLL_VIDEO0 Lock Control Register
PLL_VIDEO0_PAT0_CTRL_REG	0x0128	PLL_VIDEO0 Pattern0 Control Register
PLL_VIDEO0_PAT1_CTRL_REG	0x012C	PLL_VIDEO0 Pattern1 Control Register
PLL_VIDEO0_BIAS_REG	0x0130	PLL_VIDEO0 Bias Register
PLL_VIDEO1_CTRL_REG	0x0140	PLL_VIDEO1 Control Register
PLL_VIDEO1_LOCK_CTRL_REG	0x0144	PLL_VIDEO1 Lock Control Register
PLL_VIDEO1_PAT0_CTRL_REG	0x0148	PLL_VIDEO1 Pattern0 Control Register
PLL_VIDEO1_PAT1_CTRL_REG	0x014C	PLL_VIDEO1 Pattern1 Control Register
PLL_VIDEO1_BIAS_REG	0x0150	PLL_VIDEO1 Bias Register
PLL_VIDEO2_CTRL_REG	0x0160	PLL_VIDEO2 Control Register
PLL_VIDEO2_LOCK_CTRL_REG	0x0164	PLL_VIDEO2 Lock Control Register
PLL_VIDEO2_PAT0_CTRL_REG	0x0168	PLL_VIDEO2 Pattern0 Control Register
PLL_VIDEO2_PAT1_CTRL_REG	0x016C	PLL_VIDEO2 Pattern1 Control Register
PLL_VIDEO2_BIAS_REG	0x0170	PLL_VIDEO2 Bias Register
PLL_VE0_CTRL_REG	0x0220	PLL_VE0 Control Register
PLL_VE0_LOCK_CTRL_REG	0x0224	PLL_VE0 Lock Control Register
PLL_VE0_PAT0_CTRL_REG	0x0228	PLL_VE0 Pattern0 Control Register
PLL_VE0_PAT1_CTRL_REG	0x022C	PLL_VE0 Pattern1 Control Register
PLL_VE0_BIAS_REG	0x0230	PLL_VE0 Bias Register
PLL_VE1_CTRL_REG	0x0240	PLL_VE1 Control Register
PLL_VE1_LOCK_CTRL_REG	0x0244	PLL_VE1 Lock Control Register
PLL_VE1_PAT0_CTRL_REG	0x0248	PLL_VE1 Pattern0 Control Register
PLL_VE1_PAT1_CTRL_REG	0x024C	PLL_VE1 Pattern1 Control Register
PLL_VE1_BIAS_REG	0x0250	PLL_VE1 Bias Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
PLL_AUDIO0_CTRL_REG	0x0260	PLL_AUDIO0 Control Register
PLL_AUDIO0_LOCK_CTRL_REG	0x0264	PLL_AUDIO0 Lock Control Register
PLL_AUDIO0_PAT0_CTRL_REG	0x0268	PLL_AUDIO0 Pattern0 Control Register
PLL_AUDIO0_PAT1_CTRL_REG	0x026C	PLL_AUDIO0 Pattern1 Control Register
PLL_AUDIO0_BIAS_REG	0x0270	PLL_AUDIO0 Bias Register
PLL_AUDIO1_CTRL_REG	0x0280	PLL_AUDIO1 Control Register
PLL_AUDIO1_LOCK_CTRL_REG	0x0284	PLL_AUDIO1 Lock Control Register
PLL_AUDIO1_PAT0_CTRL_REG	0x0288	PLL_AUDIO1 Pattern0 Control Register
PLL_AUDIO1_PAT1_CTRL_REG	0x028C	PLL_AUDIO1 Pattern1 Control Register
PLL_AUDIO1_BIAS_REG	0x0290	PLL_AUDIO1 Bias Register
PLL_NPU_CTRL_REG	0x02A0	PLL_NPU Control Register
PLL_NPU_LOCK_CTRL_REG	0x02A4	PLL_NPU Lock Control Register
PLL_NPU_PAT0_CTRL_REG	0x02A8	PLL_NPU Pattern0 Control Register
PLL_NPU_PAT1_CTRL_REG	0x02AC	PLL_NPU Pattern1 Control Register
PLL_NPU_BIAS_REG	0x02B0	PLL_NPU Bias Register
PLL_DE_CTRL_REG	0x02E0	PLL_DE Control Register
PLL_DE_LOCK_CTRL_REG	0x02E4	PLL_DE Lock Control Register
PLL_DE_PAT0_CTRL_REG	0x02E8	PLL_DE Pattern0 Control Register
PLL_DE_PAT1_CTRL_REG	0x02EC	PLL_DE Pattern1 Control Register
PLL_DE_BIAS_REG	0x02F0	PLL_DE Bias Register
AHB_CLK_REG	0x0500	AHB Clock Register
APB0_CLK_REG	0x0510	APB0 Clock Register
APB1_CLK_REG	0x0518	APB1 Clock Register
APB_UART_CLK_REG	0x0538	APB_UART Clock Register
TRACE_CLK_REG	0x0540	TRACE Clock Register
GIC_CLK_REG	0x0560	GIC Clock Register
CPU_PERI_CLK_REG	0x0568	CPU_PERI Clock Register
ITS0_BGR_REG	0x0574	ITS0 Bus Gating Reset Register
NSI_CLK_REG	0x0580	NSI Clock Register
NSI_BGR_REG	0x0584	NSI Bus Gating Reset Register
MBUS_CLK_REG	0x0588	MBUS Clock Register
IOMMU0_BGR_REG	0x058C	IOMMU0 Bus Gating Reset Register
MSI_LITE0_BGR_REG	0x0594	MSI_LITE0 Bus Gating Reset Register
MSI_LITE1_BGR_REG	0x059C	MSI_LITE1 Bus Gating Reset Register
MSI_LITE2_BGR_REG	0x05A4	MSI_LITE2 Bus Gating Reset Register
IOMMU1_BGR_REG	0x05B4	IOMMU1 Bus Gating Reset Register
AHB_MAT_CLK_GATING_REG	0x05C0	AHB Master Clock Gating Register
MBUS_MAT_CLK_GATING_REG	0x05E0	MBUS Master Clock Gating Register
MBUS_GATE_EN_REG	0x05E4	MBUS Gate Enable Register
DMA0_BGR_REG	0x0704	DMA0 Bus Gating Reset Register
DMA1_BGR_REG	0x070C	DMA1 Bus Gating Reset Register
SPINLOCK_BGR_REG	0x0724	SPINLOCK Bus Gating Reset Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
MSGBOX0_BGR_REG	0x0744	MSGBOX0 Bus Gating Reset Register
PWM0_BGR_REG	0x0784	PWM0 Bus Gating Reset Register
PWM1_BGR_REG	0x078C	PWM1 Bus Gating Reset Register
DBGSYS_BGR_REG	0x07A4	DBGSYS Bus Gating Reset Register
SYSDAP_BGR_REG	0x07AC	SYSDAP Bus Gating Reset Register
TIMER0_CLK0_CLK_REG	0x0800	TIMER0_CLK0 Clock Register
TIMER0_CLK1_CLK_REG	0x0804	TIMER0_CLK1 Clock Register
TIMER0_CLK2_CLK_REG	0x0808	TIMER0_CLK2 Clock Register
TIMER0_CLK3_CLK_REG	0x080C	TIMER0_CLK3 Clock Register
TIMER0_CLK4_CLK_REG	0x0810	TIMER0_CLK4 Clock Register
TIMER0_CLK5_CLK_REG	0x0814	TIMER0_CLK5 Clock Register
TIMER0_CLK6_CLK_REG	0x0818	TIMER0_CLK6 Clock Register
TIMER0_CLK7_CLK_REG	0x081C	TIMER0_CLK7 Clock Register
TIMER0_CLK8_CLK_REG	0x0820	TIMER0_CLK8 Clock Register
TIMER0_CLK9_CLK_REG	0x0824	TIMER0_CLK9 Clock Register
TIMER0_BGR_REG	0x0850	TIMER0 Bus Gating Reset Register
DE0_CLK_REG	0x0A00	DE0 Clock Register
DE0_BGR_REG	0x0A04	DE0 Bus Gating Reset Register
DI_CLK_REG	0x0A20	DI Clock Register
DI_BGR_REG	0x0A24	DI Bus Gating Reset Register
G2D_CLK_REG	0x0A40	G2D Clock Register
G2D_BGR_REG	0x0A44	G2D Bus Gating Reset Register
EINK_CLK_REG	0x0A60	EINK Clock Register
EINK_PANEL_CLK_REG	0x0A64	EINK PANEL Clock Register
EINK_BGR_REG	0x0A6C	EINK Bus Gating Reset Register
DE_SYS_BGR_REG	0x0A74	DE_SYS Bus Gating Reset Register
VE_ENC0_CLK_REG	0x0A80	VE_ENC0 Clock Register
VE_DEC_CLK_REG	0x0A88	VE_DEC Clock Register
VE_BGR_REG	0x0A8C	VE Bus Gating Reset Register
CE_CLK_REG	0x0AC0	CE Clock Register
CE_BGR_REG	0x0AC4	CE Bus Gating Reset Register
NPU_CLK_REG	0x0B00	NPU Clock Register
NPU_BGR_REG	0x0B04	NPU Bus Gating Reset Register
GPU0_CLK_REG	0x0B20	GPU0 Clock Register
GPU0_GATING_REG	0x0B24	GPU0 Gating Reset Configuration Register
DRAM0_CLK_REG	0x0C00	DRAM0 Clock Register
DRAM0_BGR_REG	0x0C0C	DRAM0 Bus Gating Reset Register
NAND0_CLK0_CLK_REG	0x0C80	NAND0 CLK0 Clock Register
NAND0_CLK1_CLK_REG	0x0C84	NAND0 CLK1 Clock Register
NAND0_BGR_REG	0x0C8C	NAND0 Bus Gating Reset Register
SMHC0_CLK_REG	0x0D00	SMHC0 Clock Register
SMHC0_BGR_REG	0x0D0C	SMHC0 Bus Gating Reset Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
SMHC1_CLK_REG	0x0D10	SMHC1 Clock Register
SMHC1_BGR_REG	0x0D1C	SMHC1 Bus Gating Reset Register
SMHC2_CLK_REG	0x0D20	SMHC2 Clock Register
SMHC2_BGR_REG	0x0D2C	SMHC2 Bus Gating Reset Register
SMHC3_CLK_REG	0x0D30	SMHC3 Clock Register
SMHC3_BGR_REG	0x0D3C	SMHC3 Bus Gating Reset Register
UFS_AXI_CLK_REG	0x0D80	UFS_AXI Clock Register
UFS_CFG_CLK_REG	0x0D84	UFS_CFG Clock Register
UFS_BGR_REG	0x0D8C	UFS Bus Gating Reset Register
UFS_REF_CLK_EN_REG	0x0D90	UFS Reference Clock Enable Register
UART0_BGR_REG	0x0E00	UART0 Bus Gating Reset Register
UART1_BGR_REG	0x0E04	UART1 Bus Gating Reset Register
UART2_BGR_REG	0x0E08	UART2 Bus Gating Reset Register
UART3_BGR_REG	0x0E0C	UART3 Bus Gating Reset Register
UART4_BGR_REG	0x0E10	UART4 Bus Gating Reset Register
UART5_BGR_REG	0x0E14	UART5 Bus Gating Reset Register
UART6_BGR_REG	0x0E18	UART6 Bus Gating Reset Register
TWI0_BGR_REG	0x0E80	TWI0 Bus Gating Reset Register
TWI1_BGR_REG	0x0E84	TWI1 Bus Gating Reset Register
TWI2_BGR_REG	0x0E88	TWI2 Bus Gating Reset Register
TWI3_BGR_REG	0x0E8C	TWI3 Bus Gating Reset Register
TWI4_BGR_REG	0x0E90	TWI4 Bus Gating Reset Register
TWI5_BGR_REG	0x0E94	TWI5 Bus Gating Reset Register
TWI6_BGR_REG	0x0E98	TWI6 Bus Gating Reset Register
TWI7_BGR_REG	0x0E9C	TWI7 Bus Gating Reset Register
TWI8_BGR_REG	0x0EA0	TWI8 Bus Gating Reset Register
TWI9_BGR_REG	0x0EA4	TWI9 Bus Gating Reset Register
TWI10_BGR_REG	0x0EA8	TWI10 Bus Gating Reset Register
TWI11_BGR_REG	0x0EAC	TWI11 Bus Gating Reset Register
TWI12_BGR_REG	0x0EB0	TWI12 Bus Gating Reset Register
SPI0_CLK_REG	0x0F00	SPI0 Clock Register
SPI0_BGR_REG	0x0F04	SPI0 Bus Gating Reset Register
SPI1_CLK_REG	0x0F08	SPI1 Clock Register
SPI1_BGR_REG	0x0F0C	SPI1 Bus Gating Reset Register
SPI2_CLK_REG	0x0F10	SPI2 Clock Register
SPI2_BGR_REG	0x0F14	SPI2 Bus Gating Reset Register
SPIF_CLK_REG	0x0F18	SPIF Clock Register
SPIF_BGR_REG	0x0F1C	SPIF Bus Gating Reset Register
SPI3_CLK_REG	0x0F20	SPI3 Clock Register
SPI3_BGR_REG	0x0F24	SPI3 Bus Gating Reset Register
GPADC0_24M_CLK_REG	0x0FC0	GPADC0_24M Clock Register
GPADC0_BGR_REG	0x0FC4	GPADC0 Bus Gating Reset Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
THS0_BGR_REG	0x0FE4	THS0 Bus Gating Reset Register
IRRX_CLK_REG	0x1000	IRRX Clock Register
IRRX_BGR_REG	0x1004	IRRX Bus Gating Reset Register
IRTX_CLK_REG	0x1008	IRTX Clock Register
IRTX_BGR_REG	0x100C	IRTX Bus Gating Reset Register
LRADC_BGR_REG	0x1024	LRADC Bus Gating Reset Register
I2SPCM0_CLK_REG	0x1200	I2SPCM0 Clock Register
I2SPCM0_BGR_REG	0x120C	I2SPCM0 Bus Gating Reset Register
I2SPCM1_CLK_REG	0x1210	I2SPCM1 Clock Register
I2SPCM1_BGR_REG	0x121C	I2SPCM1 Bus Gating Reset Register
I2SPCM2_CLK_REG	0x1220	I2SPCM2 Clock Register
I2SPCM2_ASRC_CLK_REG	0x1224	I2SPCM2_ASRC Clock Register
I2SPCM2_BGR_REG	0x122C	I2SPCM2 Bus Gating Reset Register
I2SPCM3_CLK_REG	0x1230	I2SPCM3 Clock Register
I2SPCM3_BGR_REG	0x123C	I2SPCM3 Bus Gating Reset Register
I2SPCM4_CLK_REG	0x1240	I2SPCM4 Clock Register
I2SPCM4_BGR_REG	0x124C	I2SPCM4 Bus Gating Reset Register
OWA_TX_CLK_REG	0x1280	OWA TX Clock Register
OWA_RX_CLK_REG	0x1284	OWA RX Clock Register
OWA_BGR_REG	0x128C	OWA Bus Gating Reset Register
DMIC_CLK_REG	0x12C0	DMIC Clock Register
DMIC_BGR_REG	0x12CC	DMIC Bus Gating Reset Register
USB0_CLK_REG	0x1300	USB0 Clock Register
USB0_BGR_REG	0x1304	USB0 Bus Gating Reset Register
USB1_CLK_REG	0x1308	USB1 Clock Register
USB1_BGR_REG	0x130C	USB1 Bus Gating Reset Register
USB0_USB1_REF_CLK_REG	0x1340	USB0_USB1_REF Clock Register
USB2_U2_REF_CLK_REG	0x1348	USB2_U2_REF Clock Register
USB2_SUSPEND_CLK_REG	0x1350	USB2_SUSPEND Clock Register
USB2_MF_CLK_REG	0x1354	USB2_MF Clock Register
USB2_BGR_REG	0x135C	USB2 Bus Gating Reset Register
USB2_U3_UTMI_CLK_REG	0x1360	USB2_U3_UTMI Clock Register
USB2_U2_PIPE_CLK_REG	0x1364	USB2_U2_PIPE Clock Register
PCIE0_AUX_CLK_REG	0x1380	PCIE0_AUX Clock Register
PCIE0_AXI_SLV_CLK_REG	0x1384	PCIE0_AXI_SLV Clock Register
PCIE0_BGR_REG	0x138C	PCIE0 Bus Gating Reset Register
SERDES_PHY_CFG_CLK_REG	0x13C0	SERDES_PHY_CFG Clock Register
SERDES_BGR_REG	0x13C4	SERDES Bus Gating Reset Register
GMAC_PTP_CLK_REG	0x1400	GMAC_PTP Clock Register
GMAC0_PHY_CLK_REG	0x1410	GMAC0_PHY Clock Register
GMAC0_BGR_REG	0x141C	GMAC0 Bus Gating Reset Register
VO0_TCONLCD0_CLK_REG	0x1500	VO0_TCONLCD0 Clock Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
VO0_TCONLCD0_BGR_REG	0x1504	VO0_TCONLCD0 Bus Gating Reset Register
VO0_TCONLCD1_CLK_REG	0x1508	VO0_TCONLCD1 Clock Register
VO0_TCONLCD1_BGR_REG	0x150C	VO0_TCONLCD1 Bus Gating Reset Register
LVDS0_BGR_REG	0x1544	LVDS0 Bus Gating Reset Register
LVDS1_BGR_REG	0x154C	LVDS1 Bus Gating Reset Register
DSI0_CLK_REG	0x1580	DSI0 Clock Register
DSI0_BGR_REG	0x1584	DSI0 Bus Gating Reset Register
DSI1_CLK_REG	0x1588	DSI1 Clock Register
DSI1_BGR_REG	0x158C	DSI1 Bus Gating Reset Register
COMBPHY0_CLK_REG	0x15C0	COMBPHY0 Clock Register
COMBPHY1_CLK_REG	0x15C4	COMBPHY1 Clock Register
TCONTV0_BGR_REG	0x1604	TCONTV0 Bus Gating Reset Register
TCONTV1_BGR_REG	0x160C	TCONTV1 Bus Gating Reset Register
EDP_TV_CLK_REG	0x1640	EDP_TV Clock Register
EDP_BGR_REG	0x164C	EDP Bus Gating Reset Register
HDMI_CEC_CLK_REG	0x1680	HDMI CEC Clock Register
HDMI_TV_CLK_REG	0x1684	HDMI_TV Clock Register
HDMI_BGR_REG	0x168C	HDMI Bus Gating Reset Register
HDMI_SFR_CLK_REG	0x1690	HDMI SFR Clock Register
HDCP_ESM_CLK_REG	0x1694	HDCP ESM Clock Register
DPSS_TOP0_BGR_REG	0x16C4	DPSS_TOP0 Bus Gating Reset Register
DPSS_TOP1_BGR_REG	0x16CC	DPSS_TOP1 Bus Gating Reset Register
VIDEO_OUT0_BGR_REG	0x16E4	VIDEO_OUT0 Bus Gating Reset Register
VIDEO_OUT1_BGR_REG	0x16EC	VIDEO_OUT1 Bus Gating Reset Register
LEDC_CLK_REG	0x1700	LEDC Clock Register
LEDC_BGR_REG	0x1704	LEDC Bus Gating Reset Register
DSC_BGR_REG	0x1744	DSC Bus Gating Reset Register
CSI_MASTER0_CLK_REG	0x1800	CSI Master0 Clock Register
CSI_MASTER1_CLK_REG	0x1804	CSI Master1 Clock Register
CSI_MASTER2_CLK_REG	0x1808	CSI Master2 Clock Register
CSI_CLK_REG	0x1840	CSI Clock Register
CSI_BGR_REG	0x1844	CSI Bus Gating Reset Register
ISP_CLK_REG	0x1860	ISP Clock Register
VIDEO_IN_BGR_REG	0x1884	VIDEO_IN Bus Gating Reset Register
DDRPLL_GATE_EN_REG	0x1904	DDRPLL Gate Enable Register
PERI0PLL_GATE_EN_REG	0x1908	PERI0PLL Gate Enable Register
PERI1PLL_GATE_EN_REG	0x190C	PERI1PLL Gate Enable Register
VIDEOPLL_GATE_EN_REG	0x1910	VIDEOPLL Gate Enable Register
GPUPLL_GATE_EN_REG	0x1914	GPUPLL Gate Enable Register
VEPLL_GATE_EN_REG	0x1918	VEPLL Gate Enable Register
AUDIOPLL_GATE_EN_REG	0x191C	AUDIOPLL Gate Enable Register
NPUPLL_GATE_EN_REG	0x1920	NPUPLL Gate Enable Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
DEPLL_GATE_EN_REG	0x1928	DEPLL Gate Enable Register
DDRPLL_GATE_STAT_REG	0x1984	DDRPLL Gate Status Register
PERI0PLL_GATE_STAT_REG	0x1988	PERI0PLL Gate Status Register
PERI1PLL_GATE_STAT_REG	0x198C	PERI1PLL Gate Status Register
VIDEOPLL_GATE_STAT_REG	0x1990	VIDEOPLL Gate Status Register
GPUPLL_GATE_STAT_REG	0x1994	GPUPLL Gate Status Register
VEPLL_GATE_STAT_REG	0x1998	VEPLL Gate Status Register
AUDIOPLL_GATE_STAT_REG	0x199C	AUDIOPLL Gate Status Register
NPUPLL_GATE_STAT_REG	0x19A0	NPUPLL Gate Status Register
DEPLL_GATE_STAT_REG	0x19A8	DEPLL Gate Status Register
CLK24M_GATE_EN_REG	0x1A00	CLK24M Gate Enable Register
CM_VI_CFG_REG	0x1B00	CM VI Enable Configuration Register
CM_DESYS_CFG_REG	0x1B04	CM DESYS Enable Configuration Register
CM_VE_DEC_CFG_REG	0x1B10	CM VE_DEC Enable Configuration Register
CM_VE_ENC_CFG_REG	0x1B14	CM VE_ENC Enable Configuration Register
CM_NPU_CFG_REG	0x1B1C	CM NPU Enable Configuration Register
CM_PCIE0_CFG_REG	0x1B28	CM PCIE0 Enable Configuration Register
CM_USB2_CFG_REG	0x1B30	CM USB2 Enable Configuration Register
CM_VO_CFG_REG	0x1B34	CM VO Enable Configuration Register
CM_VO1_CFG_REG	0x1B38	CM VO1 Enable Configuration Register
APB2JTAG_CLK_REG	0x1C00	APB2JTAG Clock Register
APB2JTAG_BGR_REG	0x1C04	APB2JTAG Bus Gating Reset Register
CCMU_SEC_SWITCH_REG	0x1F00	CCMU Security Switch Register
SYSDAP_REQ_CTRL_REG	0x1F10	SYSDAP REQ Control Register
PLL_CFG0_REG	0x1F20	PLL Configuration0 Register
PLL_CFG1_REG	0x1F24	PLL Configuration1 Register
PLL_CFG2_REG	0x1F28	PLL Configuration2 Register
CCMU_FAN_GATE_REG	0x1F30	CCMU FANOUT CLOCK GATE Register
CLK27M_FAN_REG	0x1F34	CLK27M FANOUT Register
CLK_FAN_REG	0x1F38	PCLK FANOUT Register
CCMU_FAN_REG	0x1F3C	CCMU FANOUT Register

4.1.6 Register Description

4.1.6.1 0x0020 PLL_DDR Control Register (Default Value: 0x4030_4700)

Offset: 0x0020			Register Name: PLL_DDR_CTRL_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0020			Register Name: PLL_DDR_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN. PLL Enable. 0: Disable. 1: Enable. The DDRPLL= InputFreq*N/M1/P0. Note: When DCXO is 26MHz, REFPLL is 432MHz by default.
30	R/W	0x1	PLL_LDO_EN. LDO enable. 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x0	PLL_OUTPUT_GATE PLL Output Gating Enable. 0: Disable 1: Enable
26:23	/	/	/
22:20	R/W	0x3	PLL_OUTPUT_DIV. PLL Output Div P0. P0=PLL_OUTPUT_DIV + 1 PLL_OUTPUT_DIV is from 0 to 7.
19:16	/	/	/
15:8	R/W	0x47	PLL_N PLL N N= PLL_N +1 PLL_N is from 0 to 254 PLL_N should be no less than 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0020			Register Name: PLL_DDR_CTRL_REG
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV. PLL Input Div M1. M1=PLL_INPUT_DIV + 1 PLL_INPUT_DIV is from 0 to 1.
0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.2 0x0024 PLL_DDR Lock Control Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: PLL_DDR_LOCK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W1C	0x0	PLL_DDR_UNLOCK_STAT PLL_DDR Unlock Status. set 1 to the bit will clear it. 1: Pending 0: No effect
3:1	/	/	/
0	R/W	0x0	PLL_DDR_UNLOCK_IRQEN PLL_DDR Unlock Interrupt Enable 1: Enable 0: Disable

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.3 0x0028 PLL_DDR Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: PLL_DDR_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0028			Register Name: PLL_DDR_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: pulse swallow 01: Triangular (1bit) 10: Triangular (2bit) 11: Triangular (3bit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_DIRECTION. SDM direction. 0: UP 1: DOWN
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.4 0x002C PLL_DDR Pattern1 Control Register (Default Value: 0x3000_0000)

Offset: 0x002C			Register Name: PLL_DDR_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_PI_EN Fraction PI Enable. 0: Disable 1: Enable
30:28	R/W	0x3	PLL_PI_CFG Phase Interpolator bias current control 000:8uA 001: 16uA 010: 24uA 011: 32uA 100: 40uA 101: 48uA 110: 56uA 111: 64uA

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x002C			Register Name: PLL_DDR_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
27	R/W	0x0	PLL_SDM_EN. PLL SDM Enable. 0: Disable 1: Enable
26	R	0x0	SDM_BUSY. SDM Busy Status. 0: Not Busy 1: Busy Note: When Smooth is enable, need to check SDM_BUSY before update SDM parameters. Cannot update parameters if sdm is busy.
25	R/W	0x0	SMOOTH_EN. SDM Smooth Enable. 0: Disable 1: Enable
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.5 0x0030 PLL_DDR Bias Register (Default Value: 0x0015_0000)

Offset: 0x0030			Register Name: PLL_DDR_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x15	PLL_CP. PLL bias control.
15:0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.6 0x00A0 PLL_PERI0 Control Register (Default Value: 0x4012_6310)

Offset: 0x00A0	Register Name: PLL_PERI0_CTRL_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN. PLL Enable. 0: Disable. 1: Enable. PERI0PLL2X = 24MHz*N/M1/P0. PERI0_800M = 24MHz*N/M1/P1. PERI0_480M = 24MHz*N/M1/P2. PERI0_600M = PERI0PLL2X/2. PERI0_400M = PERI0PLL2X/3. PERI0_300M = PERI0_600M/2. PERI0_200M = PERI0_400M/2. PERI0_160M = PERI0_480M/3. PERI0_150M = PERI0_300M/2. When DCXO is 26MHz, PERI0PLL2X is 1.2 GHz by default. PERI0_800M default is 800MHz. PERI0_480M default is 480MHz. The output frequency of PERI0PLL2X should be fixed to 1.2GHz. The configuration parameter should be modified based on the reference frequency.
30	R/W	0x1	PLL_LDO_EN LDO enable 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x0	PLL_OUTPUT0_GATE PLL Output0 Gating Enable. 0: Disable 1: Enable
26	R/W	0x0	PLL_OUTPUT1_GATE PLL Output1 Gating Enable. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

25	R/W	0x0	PLL_OUTPUT2_GATE PLL Output2 Gating Enable. 0: Disable 1: Enable
24:23	/	/	/
22:20	R/W	0x1	PLL_OUTPUT0_DIV. PLL Output Div P0. P0=PLL_OUTPUT0_DIV + 1 PLL_OUTPUT0_DIV is from 0 to 7.
19	/	/	/
18:16	R/W	0x2	PLL_OUTPUT1_DIV. PLL Output Div P1. P1=PLL_OUTPUT1_DIV + 1 PLL_OUTPUT1_DIV is from 0 to 7.
15:8	R/W	0x63	PLL_N PLL N. N= PLL_N +1 PLL_N is from 0 to 254. PLL_N should be no less than 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	R/W	0x4	PLL_OUTPUT2_DIV. PLL Output Div P2. P2=PLL_OUTPUT2_DIV + 1 PLL_OUTPUT2_DIV is from 0 to 7.
1	R/W	0x0	PLL_INPUT_DIV. PLL Input Div M1. M1=PLL_INPUT_DIV + 1 PLL_INPUT_DIV is from 0 to 1.
0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.7 0x00A4 PLL_PERI0 Lock Control Register (Default Value: 0x0000_0000)

Offset: 0x00A4	Register Name: PLL_PERI0_LOCK_CTRL_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W1C	0x0	PLL_PERI0_UNLOCK_STAT PLL_PERI0 Unlock Status. set 1 to the bit will clear it. 1: Pending 0:No effect
3:1	/	/	/
0	R/W	0x0	PLL_PERI0_UNLOCK_IRQEN PLL_PERI0 Unlock Interrupt Enable 1: Enable 0: Disable

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.8 0x00A8 PLL_PERI0 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: PLL_PERI0_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: pulse swallow 01: Triangular (1bit) 10: Triangular (2bit) 11: Triangular (3bit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_DIRECTION. SDM direction. 0: UP 1: DOWN
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.9 0x00AC PLL_PERI0 Pattern1 Control Register (Default Value: 0x3000_0000)

Offset: 0x00AC			Register Name: PLL_PERI0_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_PI_EN Fraction PI Enable. 0: Disable 1: Enable
30:28	R/W	0x3	PLL_PI_CFG Phase Interpolator bias current control 000: 8uA 001: 16uA 010: 24uA 011: 32uA 100: 40uA 101: 48uA 110: 56uA 111: 64uA
27	R/W	0x0	PLL_SDM_EN PLL SDM Enable. 0: Disable 1: Enable
26	R	0x0	SDM_BUSY. SDM Busy Status. 0: Not Busy 1: Busy Note: When Smooth is enable, need to check SDM_BUSY before update SDM parameters. Cannot update parameters if sdm is busy.
25	R/W	0x0	SMOOTH_EN. SDM Smooth Enable. 0: Disable 1: Enable
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.10 0x00B0 PLL_PERI0 Bias Register (Default Value: 0x0015_0000)

Offset: 0x00B0			Register Name: PLL_PERI0_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x15	PLL_CP. PLL bias control .
15:0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.11 0x00C0 PLL_PERI1 Control Register (Default Value: 0x4012_6310)

Offset: 0x00C0			Register Name: PLL_PERI1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN. PLL Enable. 0: Disable. 1: Enable. PERI1PLL2X = 24MHz*N/M1/P0. PERI1_800M = 24MHz*N/M1/P1. PERI1_480M = 24MHz*N/M1/P2. PERI1_600M = PERI1PLL2X/2. PERI1_400M = PERI1PLL2X/3. PERI1_300M = PERI1_600M/2. PERI1_200M = PERI1_400M/2. PERI1_160M = PERI1_480M/3. PERI1_150M = PERI1_300M/2. When DCXO is 26MHz, PERI1PLL2X is 1.2GHz by default. PERI1_800M default is 800MHz.PERI1_480M default is 480MHz. The output frequency of PERI0PLL2X should be fixed to 1.2GHz. The configuration parameter should be modified based on the reference frequency.
30	R/W	0x1	PLL_LDO_EN. LDO enable. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00C0			Register Name: PLL_PERI1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x0	PLL_OUTPUT0_GATE PLL Output0 Gating Enable. 0: Disable 1: Enable
26	R/W	0x0	PLL_OUTPUT1_GATE PLL Output1 Gating Enable. 0: Disable 1: Enable
25	R/W	0x0	PLL_OUTPUT2_GATE PLL Output2 Gating Enable. 0: Disable 1: Enable
24:23	/	/	/
22:20	R/W	0x1	PLL_OUTPUT0_DIV. PLL Output Div P0. P0=PLL_OUTPUT0_DIV + 1 PLL_OUTPUT0_DIV is from 0 to 7.
19	/	/	/
18:16	R/W	0x2	PLL_OUTPUT1_DIV. PLL Output Div P1. P1=PLL_OUTPUT1_DIV + 1 PLL_OUTPUT1_DIV is from 0 to 7.
15:8	R/W	0x63	PLL_N PLL N. N= PLL_N +1 PLL_N is from 0 to 254. PLL_N should be no less than 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00C0			Register Name: PLL_PERI1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	R/W	0x4	PLL_OUTPUT2_DIV. PLL Output Div P2. P2=PLL_OUTPUT2_DIV + 1 PLL_OUTPUT2_DIV is from 0 to 7.
1	R/W	0x0	PLL_INPUT_DIV. PLL Input Div M1. M1=PLL_INPUT_DIV + 1 PLL_INPUT_DIV is from 0 to 1.
0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.12 0x00C4 PLL_PERI1 Lock Control Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: PLL_PERI1_LOCK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W1C	0x0	PLL_PERI1_UNLOCK_STAT PLL_PERI1 Unlock Status. set 1 to the bit will clear it. 1: Pending 0:No effect
3:1	/	/	/
0	R/W	0x0	PLL_PERI1_UNLOCK_IRQEN PLL_PERI1 Unlock Interrupt Enable 1: Enable 0: Disable

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.13 0x00C8 PLL_PERI1 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: PLL_PERI1_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00C8			Register Name: PLL_PERI1_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: pulse swallow 01: Triangular (1bit) 10: Triangular (2bit) 11: Triangular (3bit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_DIRECTION. SDM direction. 0: UP 1: DOWN
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.14 0x00CC PLL_PERI1 Pattern1 Control Register (Default Value: 0x3000_0000)

Offset: 0x00CC			Register Name: PLL_PERI1_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_PI_EN Fraction PI Enable. 0: Disable 1: Enable
30:28	R/W	0x3	PLL_PI_CFG Phase Interpolator bias current control 000: 8uA 001: 16uA 010: 24uA 011: 32uA 100: 40uA 101: 48uA 110: 56uA 111: 64uA

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00CC			Register Name: PLL_PERI1_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
27	R/W	0x0	PLL_SDM_EN PLL SDM Enable. 0: Disable 1: Enable
26	R	0x0	SDM_BUSY. SDM Busy Status. 0: Not Busy 1: Busy Note: When Smooth is enable, need to check SDM_BUSY before update SDM parameters. Cannot update parameters if sdm is busy.
25	R/W	0x0	SMOOTH_EN. SDM Smooth Enable. 0: Disable 1: Enable
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.15 0x00D0 PLL_PERI1 Bias Register (Default Value: 0x0015_0000)

Offset: 0x00D0			Register Name: PLL_PERI1_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x15	PLL_CP PLL bias control
15:0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.16 0x00E0 PLL_GPU0 Control Register (Default Value: 0x4010_4500)

Offset: 0x00E0	Register Name: PLL_GPU0_CTRL_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN. PLL Enable. 0: Disable. 1: Enable. The GPU0PLL = InputFreq*N/M1/P0. Note: When DCXO is 26MHz, GPU0PLL is 840MHz by default.
30	R/W	0x1	PLL_LDO_EN. LDO enable. 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x0	PLL_OUTPUT_GATE PLL Output Gating Enable. 0: Disable 1: Enable
26:23	/	/	/
22:20	R/W	0x1	PLL_OUTPUT_DIV. PLL Output Div P0. P0=PLL_OUTPUT_DIV + 1 PLL_OUTPUT_DIV is from 0 to 7.
19:16	/	/	/
15:8	R/W	0x45	PLL_N PLL Factor N. N= PLL_N +1 PLL_N is from 0 to 254. PLL_N should be no less than 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV. PLL Input Div M1. M1=PLL_INPUT_DIV + 1 PLL_INPUT_DIV is from 0 to 1.
0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.17 0x00E4 PLL_GPU0 Lock Control Register (Default Value: 0x0000_0000)

Offset: 0x00E4			Register Name: PLL_GPU0_LOCK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W1C	0x0	PLL_GPU0_UNLOCK_STAT PLL_GPU0 Unlock Status. set 1 to the bit will clear it. 1: Pending 0: No effect
3:1	/	/	/
0	R/W	0x0	PLL_GPU0_UNLOCK_IRQEN PLL_GPU0 Unlock Interrupt Enable 1: Enable 0: Disable

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.18 0x00E8 PLL_GPU0 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x00E8			Register Name: PLL_GPU0_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: pulse swallow 01: Triangular (1bit) 10: Triangular (2bit) 11: Triangular (3bit)

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00E8			Register Name: PLL_GPU0_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_DIRECTION. SDM direction. 0: UP 1: DOWN
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.19 0x00EC PLL_GPU0 Pattern1 Control Register (Default Value: 0x3000_0000)

Offset: 0x00EC			Register Name: PLL_GPU0_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_PI_EN Fraction PI Enable. 0: Disable 1: Enable
30:28	R/W	0x3	PLL_PI_CFG Phase Interpolator bias current control 000: 8uA 001: 16uA 010: 24uA 011: 32uA 100: 40uA 101: 48uA 110: 56uA 111: 64uA
27	R/W	0x0	PLL_SDM_EN PLL SDM Enable. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00EC			Register Name: PLL_GPU0_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
26	R	0x0	SDM_BUSY. SDM Busy Status. 0: Not Busy 1: Busy Note: When Smooth is enable, need to check SDM_BUSY before update SDM parameters. Cannot update parameters if sdm is busy.
25	R/W	0x0	SMOOTH_EN. SDM Smooth Enable. 0: Disable 1: Enable
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.20 0x00F0 PLL_GPU0 Bias Register (Default Value: 0x000B_0000)

Offset: 0x00F0			Register Name: PLL_GPU0_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0xB	PLL_CP PLL bias control
15:0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.21 0x0120 PLL_VIDEO0 Control Register (Default Value: 0x4012_6200)

Offset: 0x0120			Register Name: PLL_VIDEO0_CTRL_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0120			Register Name: PLL_VIDEO0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable. 0: Disable. 1: Enable. for application, VIDEO0PLL4X = InputFreq *N/M1/P0. VIDEO0PLL3X = InputFreq *N/M1/P1. Note: When DCXO is 26MHz, VIDEO0PLL4X is 1188MHz by default, and VIDEO0PLL3X is 792MHz by default.
30	R/W	0x1	PLL_LDO_EN. LDO enable. 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x0	PLL_OUTPUT0_GATE PLL Output0 Gating Enable. 0: Disable 1: Enable
26	R/W	0x0	PLL_OUTPUT1_GATE PLL Output1 Gating Enable. 0: Disable 1: Enable
25:23	/	/	/
22:20	R/W	0x1	PLL_OUTPUT0_DIV. PLL Output Div P0. P0=PLL_OUTPUT0_DIV + 1 PLL_OUTPUT0_DIV is from 0 to 7.
19	/	/	/
18:16	R/W	0x2	PLL_OUTPUT1_DIV. PLL Output Div P1. P1=PLL_OUTPUT1_DIV + 1 PLL_OUTPUT1_DIV is from 0 to 7.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0120			Register Name: PLL_VIDEO0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
15:8	R/W	0x62	PLL_N PLL N. N= PLL_N +1 PLL_N is from 0 to 254. PLL_N should be no less than 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV. PLL Input Div M1. M1=PLL_INPUT_DIV + 1 PLL_INPUT_DIV is from 0 to 1.
0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.22 0x0124 PLL_VIDEO0 Lock Control Register (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: PLL_VIDEO0_LOCK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W1C	0x0	PLL_VIDEO0_UNLOCK_STAT PLL_VIDEO0 Unlock Status. set 1 to the bit will clear it. 1: Pending 0: No effect
3:1	/	/	/
0	R/W	0x0	PLL_VIDEO0_UNLOCK_IRQEN PLL_VIDEO0 Unlock Interrupt Enable 1: Enable 0: Disable

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.23 0x0128 PLL_VIDEO0 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: PLL_VIDEO0_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: pulse swallow 01: Triangular (1bit) 10: Triangular (2bit) 11: Triangular (3bit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_DIRECTION. SDM direction. 0: UP 1: DOWN
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.24 0x012C PLL_VIDEO0 Pattern1 Control Register (Default Value: 0x3000_0000)

Offset: 0x012C			Register Name: PLL_VIDEO0_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_PI_EN Fraction PI Enable. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x012C			Register Name: PLL_VIDEO0_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
30:28	R/W	0x3	PLL_PI_CFG Phase Interpolator bias current control 000:8uA 001: 16uA 010: 24uA 011: 32uA 100: 40uA 101: 48uA 110: 56uA 111: 64uA
27	R/W	0x0	PLL_SDM_EN PLL SDM Enable. 0: Disable 1: Enable
26	R	0x0	SDM_BUSY. SDM Busy Status. 0: Not Busy 1: Busy Note: When Smooth is enable, need to check SDM_BUSY before update SDM parameters. Cannot update parameters if sdm is busy.
25	R/W	0x0	SMOOTH_EN. SDM Smooth Enable. 0: Disable 1: Enable
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.25 0x0130 PLL_VIDEO0 Bias Register (Default Value: 0x0015_0000)

Offset: 0x0130			Register Name: PLL_VIDEO0_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0130			Register Name: PLL_VIDEO0_BIAS_REG
Bit	Read/Write	Default/Hex	Description
20:16	R/W	0x15	PLL_CP PLL bias control
15:0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.26 0x0140 PLL_VIDEO1 Control Register (Default Value: 0x4012_6200)

Offset: 0x0140			Register Name: PLL_VIDEO1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN. PLL Enable. 0: Disable. 1: Enable. for application, VIDEO1PLL4X = InputFreq *N/M1/P0. VIDEO1PLL3X = InputFreq *N/M1/P1. Note: When DCXO is 26MHz, VIDEO1PLL4X is 1188 MHz by default, and VIDEO1PLL3X is 792 MHz by default.
30	R/W	0x1	PLL_LDO_EN. LDO enable. 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x0	PLL_OUTPUT0_GATE PLL Output0 Gating Enable. 0: Disable 1: Enable
26	R/W	0x0	PLL_OUTPUT1_GATE PLL Output1 Gating Enable. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0140			Register Name: PLL_VIDEO1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
25:23	/	/	/
22:20	R/W	0x1	PLL_OUTPUT0_DIV. PLL Output Div P0. P0=PLL_OUTPUT0_DIV + 1 PLL_OUTPUT0_DIV is from 0 to 7.
19	/	/	/
18:16	R/W	0x2	PLL_OUTPUT1_DIV. PLL Output Div P1. P1=PLL_OUTPUT1_DIV + 1 PLL_OUTPUT1_DIV is from 0 to 7.
15:8	R/W	0x62	PLL_N PLL N. N= PLL_N +1 PLL_N is from 0 to 254. PLL_N should be no less than 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV. PLL Input Div M1. M1=PLL_INPUT_DIV + 1 PLL_INPUT_DIV is from 0 to 1.
0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.27 0x0144 PLL_VIDEO1 Lock Control Register (Default Value: 0x0000_0000)

Offset: 0x0144			Register Name: PLL_VIDEO1_LOCK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0144			Register Name: PLL_VIDEO1_LOCK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
4	R/W1C	0x0	PLL_VIDEO1_UNLOCK_STAT PLL_VIDEO1 Unlock Status. set 1 to the bit will clear it. 1: Pending 0:No effect
3:1	/	/	/
0	R/W	0x0	PLL_VIDEO1_UNLOCK_IRQEN PLL_VIDEO1 Unlock Interrupt Enable 1: Enable 0: Disable

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.28 0x0148 PLL_VIDEO1 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: PLL_VIDEO1_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: pulse swallow 01: Triangular (1bit) 10: Triangular (2bit) 11: Triangular (3bit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_DIRECTION. SDM direction. 0: UP 1: DOWN
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.29 0x014C PLL_VIDEO1 Pattern1 Control Register (Default Value: 0x3000_0000)

Offset: 0x014C			Register Name: PLL_VIDEO1_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_PI_EN Fraction PI Enable. 0: Disable 1: Enable
30:28	R/W	0x3	PLL_PI_CFG Phase Interpolator bias current control 000: 8uA 001: 16uA 010: 24uA 011: 32uA 100: 40uA 101: 48uA 110: 56uA 111: 64uA
27	R/W	0x0	PLL_SDM_EN PLL SDM Enable. 0: Disable 1: Enable
26	R	0x0	SDM_BUSY. SDM Busy Status. 0: Not Busy 1: Busy Note: When Smooth is enable, need to check SDM_BUSY before update SDM parameters. Cannot update parameters if sdm is busy.
25	R/W	0x0	SMOOTH_EN. SDM Smooth Enable. 0: Disable 1: Enable
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.30 0x0150 PLL_VIDEO1 Bias Register (Default Value: 0x0015_0000)

Offset: 0x0150			Register Name: PLL_VIDEO1_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x15	PLL_CP. PLL bias control .
15:0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.31 0x0160 PLL_VIDEO2 Control Register (Default Value: 0x4012_6200)

Offset: 0x0160			Register Name: PLL_VIDEO2_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN. PLL Enable. 0: Disable. 1: Enable. for application, VIDEO2PLL4X = InputFreq *N/M1/P0. VIDEO2PLL3X = InputFreq *N/M1/P1. Note: When DCXO is 26MHz, VIDEO2PLL4X is 1188 MHz by default, and VIDEO2PLL3X is 792 MHz by default.
30	R/W	0x1	PLL_LDO_EN. LDO enable. 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0160			Register Name: PLL_VIDEO2_CTRL_REG
Bit	Read/Write	Default/Hex	Description
27	R/W	0x0	PLL_OUTPUT0_GATE PLL Output0 Gating Enable. 0: Disable 1: Enable
26	R/W	0x0	PLL_OUTPUT1_GATE PLL Output1 Gating Enable. 0: Disable 1: Enable
25:23	/	/	/
22:20	R/W	0x1	PLL_OUTPUT0_DIV. PLL Output Div P0. P0=PLL_OUTPUT0_DIV + 1 PLL_OUTPUT0_DIV is from 0 to 7.
19	/	/	/
18:16	R/W	0x2	PLL_OUTPUT1_DIV. PLL Output Div P1. P1=PLL_OUTPUT1_DIV + 1 PLL_OUTPUT1_DIV is from 0 to 7.
15:8	R/W	0x62	PLL_N PLL N. N= PLL_N +1 PLL_N is from 0 to 254. PLL_N should be no less than 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV. PLL Input Div M1. M1=PLL_INPUT_DIV + 1 PLL_INPUT_DIV is from 0 to 1.
0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.32 0x0164 PLL_VIDEO2 Lock Control Register (Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: PLL_VIDEO2_LOCK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W1C	0x0	PLL_VIDEO2_UNLOCK_STAT PLL_VIDEO2 Unlock Status. set 1 to the bit will clear it. 1: Pending 0:No effect
3:1	/	/	/
0	R/W	0x0	PLL_VIDEO2_UNLOCK_IRQEN PLL_VIDEO2 Unlock Interrupt Enable 1: Enable 0: Disable

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.33 0x0168 PLL_VIDEO2 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0168			Register Name: PLL_VIDEO2_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: pulse swallow 01: Triangular (1bit) 10: Triangular (2bit) 11: Triangular (3bit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_DIRECTION. SDM direction. 0: UP 1: DOWN
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0168			Register Name: PLL_VIDEO2_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.34 0x016C PLL_VIDEO2 Pattern1 Control Register (Default Value: 0x3000_0000)

Offset: 0x016C			Register Name: PLL_VIDEO2_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_PI_EN Fraction PI Enable. 0: Disable 1: Enable
30:28	R/W	0x3	PLL_PI_CFG Phase Interpolator bias current control 000: 8uA 001: 16uA 010: 24uA 011: 32uA 100: 40uA 101: 48uA 110: 56uA 111: 64uA
27	R/W	0x0	PLL_SDM_EN PLL SDM Enable. 0: Disable 1: Enable
26	R	0x0	SDM_BUSY. SDM Busy Status. 0: Not Busy 1: Busy Note: When Smooth is enable, need to check SDM_BUSY before update SDM parameters. Cannot update parameters if sdm is busy.
25	R/W	0x0	SMOOTH_EN. SDM Smooth Enable. 0: Disable 1: Enable
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x016C			Register Name: PLL_VIDEO2_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.35 0x0170 PLL_VIDEO2 Bias Register (Default Value: 0x0015_0000)

Offset: 0x0170			Register Name: PLL_VIDEO2_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x15	PLL_CP. PLL bias control .
15:0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.36 0x0220 PLL_VE0 Control Register (Default Value: 0x4030_5A00)

Offset: 0x0220			Register Name: PLL_VE0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN. PLL Enable. 0: Disable. 1: Enable. The VE0PLL = InputFreq*N/M1/P0. Note: When DCXO is 26MHz, VE0PLL is 546 MHz by default.
30	R/W	0x1	PLL_LDO_EN. LDO enable. 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0220			Register Name: PLL_VE0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
28	R	0x0	LOCK PLL Lock Info. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x0	PLL_OUTPUT_GATE PLL Output Gating Enable. 0: Disable 1: Enable
26:23	/	/	/
22:20	R/W	0x3	PLL_OUTPUT_DIV. PLL Output Div P0. P0=PLL_OUTPUT_DIV + 1 PLL_OUTPUT_DIV is from 0 to 7.
19:16	/	/	/
15:8	R/W	0x5A	PLL_N PLL N. N= PLL_N +1 PLL_N is from 0 to 254. PLL_N should be no less than 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV. PLL Input Div M1. M1=PLL_INPUT_DIV + 1 PLL_INPUT_DIV is from 0 to 1.
0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.37 0x0224 PLL_VE0 Lock Control Register (Default Value: 0x0000_0000)

Offset: 0x0224	Register Name: PLL_VE0_LOCK_CTRL_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W1C	0x0	PLL_VE0_UNLOCK_STAT PLL_VE0 Unlock Status. set 1 to the bit will clear it. 1: Pending 0:No effect
3:1	/	/	/
0	R/W	0x0	PLL_VE0_UNLOCK_IRQEN PLL_VE0 Unlock Interrupt Enable 1: Enable 0: Disable

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.38 0x0228 PLL_VE0 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0228			Register Name: PLL_VE0_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: pulse swallow 01: Triangular (1bit) 10: Triangular (2bit) 11: Triangular (3bit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_DIRECTION. SDM direction. 0: UP 1: DOWN
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.39 0x022C PLL_VE0 Pattern1 Control Register (Default Value: 0x3000_0000)

Offset: 0x022C			Register Name: PLL_VE0_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_PI_EN Fraction PI Enable. 0: Disable 1: Enable
30:28	R/W	0x3	PLL_PI_CFG Phase Interpolator bias current control 000: 8uA 001: 16uA 010: 24uA 011: 32uA 100: 40uA 101: 48uA 110: 56uA 111: 64uA
27	R/W	0x0	PLL_SDM_EN PLL SDM Enable. 0: Disable 1: Enable
26	R	0x0	SDM_BUSY. SDM Busy Status. 0: Not Busy 1: Busy Note: When Smooth is enable, need to check SDM_BUSY before update SDM parameters. Cannot update parameters if sdm is busy.
25	R/W	0x0	SMOOTH_EN. SDM Smooth Enable. 0: Disable 1: Enable
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.40 0x0230 PLL_VE0 Bias Register (Default Value: 0x000B_0000)

Offset: 0x0230			Register Name: PLL_VE0_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0xB	PLL_CP. PLL bias control.
15:0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.41 0x0240 PLL_VE1 Control Register (Default Value: 0x4020_5600)

Offset: 0x0240			Register Name: PLL_VE1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN. PLL Enable. 0: Disable. 1: Enable. The VE1PLL = InputFreq*N/M1/P0. Note: When DCXO is 26MHz, VE1PLL is 696 MHz by default.
30	R/W	0x1	PLL_LDO_EN. LDO enable. 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x0	PLL_OUTPUT_GATE PLL Output Gating Enable. 0: Disable 1: Enable
26:23	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0240			Register Name: PLL_VE1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
22:20	R/W	0x2	PLL_OUTPUT_DIV. PLL Output Div P0. P0=PLL_OUTPUT_DIV + 1 PLL_OUTPUT_DIV is from 0 to 7.
19:16	/	/	/
15:8	R/W	0x56	PLL_N PLL N. N= PLL_N +1 PLL_N is from 0 to 254. PLL_N should be no less than 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV. PLL Input Div M1. M1=PLL_INPUT_DIV + 1 PLL_INPUT_DIV is from 0 to 1.
0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.42 0x0244 PLL_VE1 Lock Control Register (Default Value: 0x0000_0000)

Offset: 0x0244			Register Name: PLL_VE1_LOCK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W1C	0x0	PLL_VE1_UNLOCK_STAT PLL_VE1 Unlock Status. set 1 to the bit will clear it. 1: Pending 0: No effect
3:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0244			Register Name: PLL_VE1_LOCK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	PLL_VE1_UNLOCK_IRQEN PLL_VE1 Unlock Interrupt Enable 1: Enable 0: Disable

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.43 0x0248 PLL_VE1 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0248			Register Name: PLL_VE1_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: pulse swallow 01: Triangular (1bit) 10: Triangular (2bit) 11: Triangular (3bit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_DIRECTION. SDM direction. 0: UP 1: DOWN
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5 KHz 01: 32 KHz 10: 32.5 KHz 11: 33 KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.44 0x024C PLL_VE1 Pattern1 Control Register (Default Value: 0x3000_0000)

Offset: 0x024C			Register Name: PLL_VE1_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x024C			Register Name: PLL_VE1_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_PI_EN Fraction PI Enable. 0: Disable 1: Enable
30:28	R/W	0x3	PLL_PI_CFG Phase Interpolator bias current control 000:8uA 001: 16uA 010: 24uA 011: 32uA 100: 40uA 101: 48uA 110: 56uA 111: 64uA
27	R/W	0x0	PLL_SDM_EN PLL SDM Enable. 0: Disable 1: Enable
26	R	0x0	SDM_BUSY. SDM Busy Status. 0: Not Busy 1: Busy Note: When Smooth is enable, need to check SDM_BUSY before update SDM parameters. Cannot update parameters if sdm is busy.
25	R/W	0x0	SMOOTH_EN. SDM Smooth Enable. 0: Disable 1: Enable
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.45 0x0250 PLL_VE1 Bias Register (Default Value: 0x000B_0000)

Offset: 0x0250			Register Name: PLL_VE1_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0xB	PLL_CP PLL bias control
15:0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.46 0x0260 PLL_AUDIO0 Control Register (Default Value: 0x4014_5500)

Offset: 0x0260			Register Name: PLL_AUDIO0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN. PLL Enable. 0: Disable 1: Enable AUDIO0PLL4X = 24MHz*N/M1/P0. When DCXO is 26MHz, AUDIO0PLL4X defaults to be 24.5714*4 MHz.
30	R/W	0x1	PLL_LDO_EN. LDO enable. 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.) This bit will take effect only when the bit29 in this register is set to 1.
27	R/W	0x0	PLL_OUTPUT_GATE PLL Output Gating Enable. 0: Disable 1: Enable
26:23	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0260			Register Name: PLL_AUDIO0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
22:16	R/W	0x14	PLL_OUTPUT_DIV. PLL Output Div P0. P0=PLL_OUTPUT_DIV + 1 PLL_OUTPUT_DIV is from 0 to 127.
15:8	R/W	0x55	PLL_N PLL N. N= PLL_N +1 PLL_N is from 0 to 254. PLL_N should be no less than 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV. PLL Input Div M1. M1=PLL_INPUT_DIV + 1 PLL_INPUT_DIV is from 0 to 1.
0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.47 0x0264 PLL_AUDIO0 Lock Control Register (Default Value: 0x0000_0000)

Offset: 0x0264			Register Name: PLL_AUDIO0_LOCK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W1C	0x0	PLL_AUDIO0_UNLOCK_STAT PLL_AUDIO0 Unlock Status. set 1 to the bit will clear it. 1: Pending 0: No effect
3:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0264			Register Name: PLL_AUDIO0_LOCK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	PLL_AUDIO0_UNLOCK_IRQEN PLL_AUDIO0 Unlock Interrupt Enable 1: Enable 0: Disable

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.48 0x0268 PLL_AUDIO0 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0268			Register Name: PLL_AUDIO0_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: pulse swallow 01: Triangular (1bit) 10: Triangular (2bit) 11: Triangular (3bit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_DIRECTION. SDM direction. 0: UP 1: DOWN
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.49 0x026C PLL_AUDIO0 Pattern1 Control Register (Default Value: 0x3000_0000)

Offset: 0x026C			Register Name: PLL_AUDIO0_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x026C			Register Name: PLL_AUDIO0_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_PI_EN Fraction PI Enable. 0: Disable 1: Enable
30:28	R/W	0x3	PLL_PI_CFG Phase Interpolator bias current control 000: 8uA 001: 16uA 010: 24uA 011: 32uA 100: 40uA 101: 48uA 110: 56uA 111: 64uA
27	R/W	0x0	PLL_SDM_EN PLL SDM Enable. 0: Disable 1: Enable
26	R	0x0	SDM_BUSY. SDM Busy Status. 0: Not Busy 1: Busy Note: When Smooth is enable, need to check SDM_BUSY before update SDM parameters. Cannot update parameters if sdm is busy.
25	R/W	0x0	SMOOTH_EN. SDM Smooth Enable. 0: Disable 1: Enable
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.50 0x0270 PLL_AUDIO0 Bias Register (Default Value: 0x0015_0000)

Offset: 0x0270			Register Name: PLL_AUDIO0_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x15	PLL_CP. PLL bias control.
15:0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.51 0x0280 PLL_AUDIO1 Control Register (Default Value: 0x4014_7F00)

Offset: 0x0280			Register Name: PLL_AUDIO1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN. PLL Enable. 0: Disable 1: Enable AUDIO1PLL_DIV2 = 24MHz*N/M1/P0 AUDIO1PLL_DIV5 = 24MHz*N/M1/P1 Note: When DCXO is 26MHz, AUDIO1PLL_DIV2 is 1536 MHz by default, and AUDIO1PLL_DIV5 is 614.4 MHz (24.576Mhz*25) by default.
30	R/W	0x1	PLL_LDO_EN. LDO enable. 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.) This bit will take effect only when the bit29 in this register is set to 1.
27	R/W	0x0	PLL_OUTPUT_GATE. PLL Output Gating Enable. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0280			Register Name: PLL_AUDIO1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
26:23	/	/	/
22:20	R/W	0x1	PLL_P0 PLL Output Div P0. P0=PLL_P0 + 1 PLL_P0 is from 0 to 7.
19	/	/	/
18:16	R/W	0x4	PLL_P1. PLL Output Div P1. P1=PLL_P1 + 1 PLL_P1 is from 0 to 7.
15:8	R/W	0x7F	PLL_N PLL N. N= PLL_N +1 PLL_N is from 0 to 254. PLL_N should be no less than 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV. PLL Input Div M1. M1=PLL_INPUT_DIV + 1 PLL_INPUT_DIV is from 0 to 1.
0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.52 0x0284 PLL_AUDIO1 Lock Control Register (Default Value: 0x0000_0000)

Offset: 0x0284			Register Name: PLL_AUDIO1_LOCK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0284			Register Name: PLL_AUDIO1_LOCK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
4	R/W1C	0x0	PLL_AUDIO1_UNLOCK_STAT PLL_AUDIO1 Unlock Status. set 1 to the bit will clear it. 1: Pending 0:No effect
3:1	/	/	/
0	R/W	0x0	PLL_AUDIO1_UNLOCK_IRQEN PLL_AUDIO1 Unlock Interrupt Enable 1: Enable 0: Disable

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.53 0x0288 PLL_AUDIO1 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0288			Register Name: PLL_AUDIO1_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: pulse swallow 01: Triangular (1bit) 10: Triangular (2bit) 11: Triangular (3bit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_DIRECTION. SDM direction. 0: UP 1: DOWN
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5 KHz 01: 32 KHz 10: 32.5 KHz 11: 33 KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.54 0x028C PLL_AUDIO1 Pattern1 Control Register (Default Value: 0x3000_0000)

Offset: 0x028C			Register Name: PLL_AUDIO1_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_PI_EN Fraction PI Enable. 0: Disable 1: Enable
30:28	R/W	0x3	PLL_PI_CFG Phase Interpolator bias current control 000: 8uA 001: 16uA 010: 24uA 011: 32uA 100: 40uA 101: 48uA 110: 56uA 111: 64uA
27	R/W	0x0	PLL_SDM_EN PLL SDM Enable. 0: Disable 1: Enable
26	R	0x0	SDM_BUSY. SDM Busy Status. 0: Not Busy 1: Busy Note: When Smooth is enable, need to check SDM_BUSY before update SDM parameters. Cannot update parameters if sdm is busy.
25	R/W	0x0	SMOOTH_EN. SDM Smooth Enable. 0: Disable 1: Enable
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.55 0x0290 PLL_AUDIO1 Bias Register (Default Value: 0x0019_0000)

Offset: 0x0290			Register Name: PLL_AUDIO1_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x19	PLL_CP. PLL bias control.
15:0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.56 0x02A0 PLL_NPU Control Register (Default Value: 0x4010_4500)

Offset: 0x02A0			Register Name: PLL_NPU_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN. PLL Enable. 0: Disable 1: Enable The NPUPLL = 24MHz*N/M1/P0. Note: When DCXO is 26MHz, VE0PLL is 840 MHz by default.
30	R/W	0x1	PLL_LDO_EN. LDO enable. 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.) This bit will take effect only when bit29 is set to 1.
27	R/W	0x0	PLL_OUTPUT_GATE PLL Output Gating Enable. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x02A0			Register Name: PLL_NPU_CTRL_REG
Bit	Read/Write	Default/Hex	Description
26:23	/	/	/
22:20	R/W	0x1	PLL_OUTPUT_DIV PLL Output Div P0 P0=PLL_OUTPUT_DIV + 1 PLL_OUTPUT_DIV is from 0 to 7.
19:16	/	/	/
15:8	R/W	0x45	PLL_N PLL N N= PLL_N +1 PLL_N is from 0 to 254. PLL_N should be no less than 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV PLL Input Div M1 M1=PLL_INPUT_DIV + 1 PLL_INPUT_DIV is from 0 to 1.
0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.57 0x02A4 PLL_NPU Lock Control Register (Default Value: 0x0000_0000)

Offset: 0x02A4			Register Name: PLL_NPU_LOCK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W1C	0x0	PLL_NPU_UNLOCK_STAT PLL_NPU Unlock Status. set 1 to the bit will clear it. 1: Pending 0:No effect
3:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x02A4			Register Name: PLL_NPU_LOCK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	PLL_NPU_UNLOCK_IRQEN PLL_NPU Unlock Interrupt Enable 1: Enable 0: Disable

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.58 0x02A8 PLL_NPU Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x02A8			Register Name: PLL_NPU_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: pulse swallow 01: Triangular (1bit) 10: Triangular (2bit) 11: Triangular (3bit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_DIRECTION. SDM direction 0: UP 1: DOWN
18:17	R/W	0x0	FREQ Frequency 00: 31.5 KHz 01: 32 KHz 10: 32.5 KHz 11: 33 KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.59 0x02AC PLL_NPU Pattern1 Control Register (Default Value: 0x3000_0000)

Offset: 0x02AC			Register Name: PLL_NPU_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x02AC			Register Name: PLL_NPU_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_PI_EN Fraction PI Enable. 0: Disable 1: Enable
30:28	R/W	0x3	PLL_PI_CFG Phase Interpolator bias current control 000: 8uA 001: 16uA 010: 24uA 011: 32uA 100: 40uA 101: 48uA 110: 56uA 111: 64uA
27	R/W	0x0	PLL_SDM_EN PLL SDM Enable. 0: Disable 1: Enable
26	R	0x0	SDM_BUSY. SDM Busy Status. 0: Not Busy 1: Busy Note: When Smooth is enable, need to check SDM_BUSY before update SDM parameters. Cannot update parameters if sdm is busy.
25	R/W	0x0	SMOOTH_EN. SDM Smooth Enable. 0: Disable 1: Enable
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.60 0x02B0 PLL_NPU Bias Register (Default Value: 0x000B_0000)

Offset: 0x02B0			Register Name: PLL_NPU_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0xB	PLL_CP. PLL bias control.
15:0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.61 0x02E0 PLL_DE Control Register (Default Value: 0x4012_5600)

Offset: 0x02E0			Register Name: PLL_DE_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN. PLL Enable. 0: Disable. 1: Enable. for application, DEPLL4X = InputFreq *N/M1/P0. DEPLL3X = InputFreq *N/M1/P1. Note: When DCXO is 26MHz, DEPLL4X is 1044 MHz by default, and DEPLL4X is 696 MHz by default.
30	R/W	0x1	PLL_LDO_EN. LDO enable. 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x0	PLL_OUTPUT0_GATE PLL Output0 Gating Enable 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x02E0			Register Name: PLL_DE_CTRL_REG
Bit	Read/Write	Default/Hex	Description
26	R/W	0x0	PLL_OUTPUT1_GATE PLL Output1 Gating Enable. 0: Disable 1: Enable
25:23	/	/	/
22:20	R/W	0x1	PLL_OUTPUT0_DIV. PLL Output Div P0. P0=PLL_OUTPUT0_DIV + 1 PLL_OUTPUT0_DIV is from 0 to 7.
19	/	/	/
18:16	R/W	0x2	PLL_OUTPUT1_DIV. PLL Output Div P1. P1=PLL_OUTPUT1_DIV + 1 PLL_OUTPUT1_DIV is from 0 to 7.
15:8	R/W	0x56	PLL_N PLL N. N= PLL_N +1 PLL_N is from 0 to 254. PLL_N should be no less than 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV. PLL Input Div M1. M1=PLL_INPUT_DIV + 1 PLL_INPUT_DIV is from 0 to 1.
0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.62 0x02E4 PLL_DE Lock Control Register (Default Value: 0x0000_0000)

Offset: 0x02E4			Register Name: PLL_DE_LOCK_CTRL_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x02E4			Register Name: PLL_DE_LOCK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W1C	0x0	PLL_DE_UNLOCK_STAT PLL_DE Unlock Status. set 1 to the bit will clear it. 1: Pending 0: No effect
3:1	/	/	/
0	R/W	0x0	PLL_DE_UNLOCK_IRQEN PLL_DE Unlock Interrupt Enable 1: Enable 0: Disable

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.63 0x02E8 PLL_DE Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x02E8			Register Name: PLL_DE_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: pulse swallow 01: Triangular (1bit) 10: Triangular (2bit) 11: Triangular (3bit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_DIRECTION. SDM direction. 0: UP 1: DOWN
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.64 0x02EC PLL_DE Pattern1 Control Register (Default Value: 0x3000_0000)

Offset: 0x02EC			Register Name: PLL_DE_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_PI_EN Fraction PI Enable. 0: Disable 1: Enable
30:28	R/W	0x3	PLL_PI_CFG Phase Interpolator bias current control 000: 8uA 001: 16uA 010: 24uA 011: 32uA 100: 40uA 101: 48uA 110: 56uA 111: 64uA
27	R/W	0x0	PLL_SDM_EN PLL SDM Enable. 0: Disable 1: Enable
26	R	0x0	SDM_BUSY. SDM Busy Status. 0: Not Busy 1: Busy Note: When Smooth is enable, need to check SDM_BUSY before update SDM parameters. Cannot update parameters if sdm is busy.
25	R/W	0x0	SMOOTH_EN. SDM Smooth Enable. 0: Disable 1: Enable
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit [0]).

4.1.6.65 0x02F0 PLL_DE Bias Register (Default Value: 0x0015_0000)

Offset: 0x02F0			Register Name: PLL_DE_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x15	PLL_CP. PLL bias control.
15:0	/	/	/

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[0]).

4.1.6.66 0x0500 AHB Clock Register (Default Value: 0x0000_0000)

Offset: 0x0500			Register Name: AHB_CLK_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: SYS_CLK24M 01: RTC_32K 10: RC16M 11: PERI0_600M_BUS Note: The clock MUX provides glitch-free switching and supports dynamic configuration. AHB_CLK = Clock Source/M.
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31. Note: The clock DIV provides glitch-free switching and supports dynamic configuration.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[1]).

4.1.6.67 0x0510 APB0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0510			Register Name: APB0_CLK_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0510			Register Name: APB0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: SYS_CLK24M 01: RTC_32K 10: RC16M 11: PERI0_600M_BUS Note: The clock MUX provides glitch-free switching and supports dynamic configuration. APB0_CLK = Clock Source/M.
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31. Note: The clock DIV provides glitch-free switching and supports dynamic configuration.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[1]).

4.1.6.68 0x0518 APB1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0518			Register Name: APB1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: SYS_CLK24M 01: RTC_32K 10: RC16M 11: PERI0_600M_BUS Note: The clock MUX provides glitch-free switching and supports dynamic configuration. APB1_CLK = Clock Source/M.
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31. Note: The clock DIV provides glitch-free switching and supports dynamic configuration.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[1]).

4.1.6.69 0x0538 APB_UART Clock Register (Default Value: 0x0000_0000)

Offset: 0x0538			Register Name: APB_UART_CLK_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: RTC_32K 010: RC16M 011: PERI0_600M_BUS 100: PERI0_480M_BUS Note: The clock MUX provides glitch-free switching and supports dynamic configuration. APB_UART_CLK = Clock Source/M.
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31. Note: The clock DIV provides glitch-free switching and supports dynamic configuration.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[1]).

4.1.6.70 0x0540 TRACE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0540			Register Name: TRACE_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TRACE_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON TRACE_CLK = Clock Source/M.
30:27	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0540			Register Name: TRACE_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: RTC_32K 010: RC16M 011: PERI0_300M 100: PERI0_400M Note: The clock MUX provides glitch-free switching and supports dynamic configuration.
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31. Note: The clock DIV provides glitch-free switching and supports dynamic configuration.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[1]).

4.1.6.71 0x0560 GIC Clock Register (Default Value: 0x8000_0000)

Offset: 0x0560			Register Name: GIC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	GIC_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON GIC_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: RTC_32K 010: PERI0_600M 011: PERI0_480M 100: PERI0_400M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.72 0x0568 CPU_PERI Clock Register (Default Value: 0x8000_0000)

Offset: 0x0568			Register Name: CPU_PERI_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	CPU_PERI_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON CPU_PERI_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: RTC_32K 010: PERI0_600M 011: PERI0_480M 100: PERI0_400M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.73 0x0574 ITS0 Bus Gating Reset Register (Default Value: 0x0001_0002)

Offset: 0x0574			Register Name: ITS0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x1	ITS_PCIE0_RST. ITS_PCIE0 Reset 0: Assert 1: De-assert
15:2	/	/	/
1	R/W	0x1	ITS_PCIE0_ACLK_GATING. Gating Clock for ITS_PCIE0 ACLK 0: Mask 1: Pass
0	/	/	/

4.1.6.74 0x0580 NSI Clock Register (Default Value: 0xC000_0000)

Offset: 0x0580	Register Name: NSI_CLK_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	NSI_CLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON NSI CLK = Clock Source/M.
30	R/W	0x1	NSI_RST. NSI Reset. 0: Assert 1: De-assert
29	/	/	/
28	R/W	0x0	NSI_DFS_EN. NSI Clock Dynamic Frequency Scaling Enable. 0: Disable 1: Enable
27	R/WAC	0x0	NSI_UPD. NSI Clock Configuration 0 update. 0: Invalid 1: Valid Note: Set this bit will validate Configuration 0. It will be auto cleared after the Configuration 0 is valid. dram req/ack signals are supported. When nsi_upd signal is set to 1, nsi_clk_sel/nsi_div1 will be updated.
26:24	R/W	0x0	NSI_CLK_SEL. Clock Source Select 000: SYS_CLK24M 001: DDRPLL 010: PERI0_800M 011: PERI0_600M 100: PERI0_480M 101: DEPLL3X Note: The clock MUX provides glitch-free switching and supports dynamic configuration.
23:5	/	/	/
4:0	R/W	0x0	NSI_DIV1. Factor M M= NSI_DIV1 + 1. FACTOR M is from 0 to 31. Note: The clock DIV provides glitch-free switching and supports dynamic configuration.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[2]).

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.75 0x0584 NSI Bus Gating Reset Register (Default Value: 0x0001_0001)

Offset: 0x0584			Register Name: NSI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x1	NSI_CFG_RST. NSI Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x1	NSI_CFG_GATING. Gating Clock for NSI_CFG 0: Mask 1: Pass

4.1.6.76 0x0588 MBUS Clock Register (Default Value: 0x8000_0000)

Offset: 0x0588			Register Name: MBUS_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	MBUS_CLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON MBUS_CLK = Clock Source/M.
30:29	/	/	/
28	R/W	0x0	MBUS_DFS_EN. MBUS CLK Dynamic Frequency Scaling Enable. 0: Disable 1: Enable
27	R/WAC	0x0	MBUS_UPD. MBUS Clock Configuration 0 update. 0: Invalid 1: Valid Note: Set this bit will validate Configuration 0. It will be auto cleared after the Configuration 0 is valid. When mbus_upd signal is set to 1, mbus_clk_sel/mbus_div1 will be updated.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0588			Register Name: MBUS_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	MBUS_CLK_SEL. Clock Source Select 000: SYS_CLK24M 001: PERI0_600M 010: DDRPLL 011: PERI0_480M 100: PERI0_400M 101: NPUPLL Note: The clock MUX provides glitch-free switching and supports dynamic configuration.
23:5	/	/	/
4:0	R/W	0x0	MBUS_DIV1. Factor M M= IOMMU_DIV1 + 1. FACTOR M is from 0 to 31. Note: The clock DIV provides glitch-free switching and supports dynamic configuration.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[2]).

4.1.6.77 0x058C IOMMU0 Bus Gating Reset Register (Default Value: 0x0001_0007)

Offset: 0x058C			Register Name: IOMMU0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x1	IOMMU0_SYS_RST. IOMMU0 System Reset 0: Assert 1: De-assert
15:3	/	/	/
2	R/W	0x1	IOMMU0_SYS_HCLK_GATING. Gating Clock for IOMMU0_SYS_HCLK 0: Mask 1: Pass
1	R/W	0x1	IOMMU0_SYS_PCLK_GATING. Gating Clock for IOMMU0_SYS_PCLK 0: Mask 1: Pass

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x058C			Register Name: IOMMU0_BGR_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x1	IOMMU0_SYS_MCLK_GATING. Gating Clock for IOMMU0_SYS_MCLK 0: Mask 1: Pass

4.1.6.78 0x0594 MSI_LITE0 Bus Gating Reset Register (Default Value: 0x0003_0001)

Offset: 0x0594			Register Name: MSI_LITE0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x1	MSI_LITE0_MBUS_RST. MSI_LITE0 MBUS Reset 0: Assert 1: De-assert
16	R/W	0x1	MSI_LITE0_AHB_RST. MSI_LITE0 REG Config Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x1	MSI_LITE0_GATING. Gating Clock for MSI_LITE0 0: Mask 1: Pass

4.1.6.79 0x059C MSI_LITE1 Bus Gating Reset Register (Default Value: 0x0003_0001)

Offset: 0x059C			Register Name: MSI_LITE1_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x1	MSI_LITE1_MBUS_RST. MSI_LITE1 MBUS Reset 0: Assert 1: De-assert
16	R/W	0x1	MSI_LITE1_AHB_RST. MSI_LITE1 REG Config Reset 0: Assert 1: De-assert
15:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x059C			Register Name: MSI_LITE1_BGR_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x1	MSI_LITE1_GATING. Gating Clock for MSI_LITE1 0: Mask 1: Pass

4.1.6.80 0x05A4 MSI_LITE2 Bus Gating Reset Register (Default Value: 0x0003_0001)

Offset: 0x05A4			Register Name: MSI_LITE2_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x1	MSI_LITE2_MBUS_RST. MSI_LITE2 MBUS Reset 0: Assert 1: De-assert
16	R/W	0x1	MSI_LITE2_AHB_RST. MSI_LITE2 REG Config Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x1	MSI_LITE2_GATING. Gating Clock for MSI_LITE2 0: Mask 1: Pass

4.1.6.81 0x05B4 IOMMU1 Bus Gating Reset Register (Default Value: 0x0001_0007)

Offset: 0x05B4			Register Name: IOMMU1_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x1	IOMMU1_SYS_RST. IOMMU1 System Reset 0: Assert 1: De-assert
15:3	/	/	/
2	R/W	0x1	IOMMU1_SYS_HCLK_GATING. Gating Clock for IOMMU1_SYS_HCLK 0: Mask 1: Pass

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x05B4			Register Name: IOMMU1_BGR_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x1	IOMMU1_SYS_PCLK_GATING. Gating Clock for IOMMU1_SYS_PCLK 0: Mask 1: Pass
0	R/W	0x1	IOMMU1_SYS_MCLK_GATING. Gating Clock for IOMMU1_SYS_MCLK 0: Mask 1: Pass

4.1.6.82 0x05C0 AHB Master Clock Gating Register (Default Value: 0x1101_03FF)

Offset: 0x05C0			Register Name: AHB_MAT_CLK_GATING_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	AHB_MONITOR_EN AHB bus auto clock gating function enable. 1: Enable auto clock gate 0: Disable auto clock gate
30	/	/	/
29	R/W	0x0	SD_MONITOR_EN SD bus auto clock gating function enable. 1: Enable auto clock gate 0: Disable auto clock gate
28	R/W	0x1	CPUS_HCLK_GATE_SW_CFG. CPUS AHB Clock Gate Enable. 0: Disable 1: Enable
27:25	/	/	/
24	R/W	0x1	STORE_AHB_GATE_SW_CFG. STORE AHB Clock Gate Enable. 0: Disable 1: Enable
23:17	/	/	/
16	R/W	0x1	MSILITE0_AHB_GATE_SW_CFG. MSILITE0 AHB Clock Gate Enable. 0: Disable 1: Enable
15:10	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x05C0			Register Name: AHB_MAT_CLK_GATING_REG
Bit	Read/Write	Default/Hex	Description
9	R/W	0x1	USB0_USB1_SYS_AHB_GATE_SW_CFG. USB2.0 (USB0_USB1) SYS AHB Clock Gate Enable. 0: Disable 1: Enable
8	R/W	0x1	SERDES_AHB_GATE_SW_CFG. SERDES AHB Clock Gate Enable. 0: Disable 1: Enable
7	R/W	0x1	GPU0_AHB_GATE_SW_CFG GPU0 AHB Clock Gate Enable 0: Disable 1: Enable
6	R/W	0x1	NPU_AHB_GATE_SW_CFG. NPU AHB Clock Gate Enable 0: Disable 1: Enable
5	R/W	0x1	DE_AHB_GATE_SW_CFG. DE AHB Clock Gate Enable 0: Disable 1: Enable
4	R/W	0x1	VID_OUT1_AHB_GATE_SW_CFG. Video Out1 AHB Clock Gate Enable 0: Disable 1: Enable
3	R/W	0x1	VID_OUT0_AHB_GATE_SW_CFG Video Out0 AHB Clock Gate Enable 0: Disable 1: Enable
2	R/W	0x1	VID_IN_AHB_GATE_SW_CFG Video in AHB Clock Gate Enable 0: Disable 1: Enable
1	R/W	0x1	VE_ENC_AHB_GATE_SW_CFG. VE_ENC AHB Clock Gate Enable 0: Disable 1: Enable
0	R/W	0x1	VE_DEC_AHB_GATE_SW_CFG. VE DEC AHB Clock Gate Enable 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[1]).

4.1.6.83 0x05E0 MBUS Master Clock Gating Register (Default Value: 0xF105_5803)

Offset: 0x05E0			Register Name: MBUS_MAT_CLK_GATING_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	MSILITE2_MBUS_GATE_SW_CFG. MSILITE2 MBUS Clock Gate Enable. 0: Disable 1: Enable
30	R/W	0x1	STORE_MBUS_GATE_SW_CFG. STORE MBUS Clock Gate Enable. 0: Disable 1: Enable
29	R/W	0x1	MSILITE0_MBUS_GATE_SW_CFG. MSILITE0 MBUS Clock Gate Enable. 0: Disable 1: Enable
28	R/W	0x1	SERDES_MBUS_GATE_SW_CFG. SERDES MBUS Clock Gate Enable. 0: Disable 1: Enable
27:25	/	/	/
24	R/W	0x1	VID_IN_MBUS_GATE_SW_CFG. VID_IN MBUS Clock Gate Enable 0: Disable 1: Enable
23:19	/	/	/
18	R/W	0x1	NPU_MBUS_GATE_SW_CFG. NPU MBUS Clock Gate Enable 0: Disable 1: Enable
17	/	/	/
16	R/W	0x1	GPU0_MBUS_GATE_SW_CFG. GPU0 MBUS Clock Gate Enable 0: Disable 1: Enable
15	/	/	/
14	R/W	0x1	VE_DEC_MBUS_GATE_SW_CFG. VE_DEC MBUS Clock Gate Enable 0: Disable 1: Enable
13	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x05E0			Register Name: MBUS_MAT_CLK_GATING_REG
Bit	Read/Write	Default/Hex	Description
12	R/W	0x1	VE_ENC0_MBUS_GATE_SW_CFG. VE_ENC0 MBUS Clock Gate Enable 0: Disable 1: Enable
11	R/W	0x1	DESYS_MBUS_GATE_SW_CFG. DESYS MBUS Clock Gate Enable 0: Disable 1: Enable
10:2	/	/	/
1	R/W	0x1	IOMMU1_MBUS_GATE_SW_CFG. IOMMU1 MBUS Clock Gate Enable. 0: Disable 1: Enable
0	R/W	0x1	IOMMU0_MBUS_GATE_SW_CFG. IOMMU0 MBUS Clock Gate Enable. 0: Disable 1: Enable

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[2]).

4.1.6.84 0x05E4 MBUS Gate Enable Register (Default Value: 0x0000_0000)

Offset: 0x05E4			Register Name: MBUS_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x0	VE_DEC_MCLK_EN. Gating MBUS Clock for VE_DEC 0: Mask 1: Pass
17:12	/	/	/
11	R/W	0x0	GMAC0_MCLK_EN. Gating AXI Clock for GMAC0. 0: Mask 1: Pass
10	/	/	/
9	R/W	0x0	ISP_MCLK_EN. Gating MBUS Clock for ISP 0: Mask 1: Pass

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x05E4			Register Name: MBUS_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
8	R/W	0x0	CSI_MCLK_EN. Gating MBUS Clock for CSI 0: Mask 1: Pass
7:6	/	/	/
5	R/W	0x0	NAND_MCLK_EN. Gating AXI Clock for NAND. 0: Mask 1: Pass
4	/	/	/
3	R/W	0x0	DMA1_MCLK_EN. Gating AXI Clock for DMA1. 0: Mask 1: Pass
2	R/W	0x0	CE_MCLK_EN. Gating AXI Clock for CE. 0: Mask 1: Pass
1	R/W	0x0	VE_ENC0_MCLK_EN. Gating MBUS Clock for VE_ENC0 0: Mask 1: Pass
0	R/W	0x0	DMA0_MCLK_EN. Gating MBUS Clock for DMA0. 0: Mask 1: Pass

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[2]).

4.1.6.85 0x0704 DMA0 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0704			Register Name: DMA0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DMA0_RST DMA0 Reset 0: Assert 1: De-assert
15:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0704			Register Name: DMA0_BGR_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	DMA0_GATING. Gating Clock for DMA0 0: Mask 1: Pass

Note: DMA0 working clock sources from AHB_CLK.

4.1.6.86 0x070C DMA1 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x070C			Register Name: DMA1_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DMA1_RST. DMA1 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DMA1_GATING. Gating Clock for DMA1 0: Mask 1: Pass

Note: DMA1 working clock sources from AHB_CLK.

4.1.6.87 0x0724 SPINLOCK Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0724			Register Name: SPINLOCK_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	SPINLOCK_RST. SPINLOCK Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	SPINLOCK_GATING. Gating Clock for SPINLOCK 0: Mask 1: Pass

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.88 0x0744 MSGBOX0 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0744			Register Name: MSGBOX0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	MSGBOX0_RST. MSGBOX_CPUX Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	MSGBOX0_GATING. Gating Clock for MSGBOX_CPUX 0: Mask 1: Pass

4.1.6.89 0x0784 PWM0 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0784			Register Name: PWM0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	PWM0_RST. PWM0 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	PWM0_GATING. Gating Clock for PWM0 0: Mask 1: Pass

4.1.6.90 0x078C PWM1 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x078C			Register Name: PWM1_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	PWM1_RST. PWM1 Reset 0: Assert 1: De-assert
15:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x078C			Register Name: PWM1_BGR_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	PWM1_GATING. Gating Clock for PWM1 0: Mask 1: Pass

4.1.6.91 0x07A4 DBGSYS Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x07A4			Register Name: DBGSYS_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DBGSYS_RST. DBGSYS Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DBGSYS_GATING. Gating Clock for DBGSYS 0: Mask 1: Pass

Note: DBGSYS working clock sources from SYS_CLK24M.

4.1.6.92 0x07AC SYSDAP Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x07AC			Register Name: SYSDAP_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	SYSDAP_RST. SYSDAP Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	SYSDAP_GATING. Gating Clock for DRAM 0: Mask 1: Pass

Note: The register is a secure register by default in the secure mode, which can be only accessed by secure hosts. Its security control is set by the CCMU_SEC_SWITCH_REG (bit[1]).

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.93 0x0800 TIMER0_CLK0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0800			Register Name: TIMER0_CLK0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TIMER0_CLK0_CLK_GATING Gating Clock. 0: Disable 1: Enable TIMER0_CLK0_CLK=Clock Source/P.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: RC16M 010: RTC_32K 011: PERI0_200M 100: DCXO The clock source of TIMER0_CLK0 clock input is 24M/RC 16M/32K/200M/DCXO.
23:3	/	/	/
2:0	R/W	0x0	FACTOR_P. Factor P 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 Select the pre-scale of clock source.

4.1.6.94 0x0804 TIMER0_CLK1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0804			Register Name: TIMER0_CLK1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TIMER0_CLK1_CLK_GATING Gating Clock. 0: Disable 1: Enable TIMER0_CLK1_CLK=Clock Source/P.
30:27	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0804			Register Name: TIMER0_CLK1_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: RC16M 010: RTC_32K 011: PERI0_200M 100: DCXO The clock source of TIMER0_CLK1 clock input is 24M/RC 16M/32K/200M/DCXO.
23:3	/	/	/
2:0	R/W	0x0	FACTOR_P. Factor P 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 Select the pre-scale of clock source.

4.1.6.95 0x0808 TIMER0_CLK2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0808			Register Name: TIMER0_CLK2_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TIMER0_CLK2_CLK_GATING Gating Clock. 0: Disable 1: Enable TIMER0_CLK2_CLK=Clock Source/P.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000:SYS_CLK24M 001:RC16M 010: RTC_32K 011: PERI0_200M 100: DCXO The clock source of TIMER0_CLK2 clock input is 24M/RC 16M/32K/200M/DCXO.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0808			Register Name: TIMER0_CLK2_CLK_REG
Bit	Read/Write	Default/Hex	Description
23:3	/	/	/
2:0	R/W	0x0	FACTOR_P. Factor P 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 Select the pre-scale of clock source.

4.1.6.96 0x080C TIMER0_CLK3 Clock Register (Default Value: 0x0000_0000)

Offset: 0x080C			Register Name: TIMER0_CLK3_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TIMER0_CLK3_CLK_GATING Gating Clock. 0: Disable 1: Enable TIMER0_CLK3_CLK=Clock Source/P.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: RC16M 010: RTC_32K 011: PERI0_200M 100: DCXO The clock source of TIMER0_CLK3 clock input is 24M/RC16M/32K/200M/DCXO.
23:3	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x080C			Register Name: TIMER0_CLK3_CLK_REG
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x0	FACTOR_P. Factor P 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 Select the pre-scale of clock source.

4.1.6.97 0x0810 TIMER0_CLK4 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0810			Register Name: TIMER0_CLK4_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TIMER0_CLK4_CLK_GATING Gating Clock. 0: Disable 1: Enable TIMER0_CLK4_CLK=Clock Source/P.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: RC16M 010: RTC_32K 011: PERI0_200M 100: DCXO The clock source of TIMER0_CLK4 clock input is 24M/RC 16M/32K/200M/DCXO.
23:3	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0810			Register Name: TIMER0_CLK4_CLK_REG
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x0	FACTOR_P. Factor P 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 Select the pre-scale of clock source.

4.1.6.98 0x0814 TIMER0_CLK5 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0814			Register Name: TIMER0_CLK5_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TIMER0_CLK5_CLK_GATING Gating Clock. 0: Disable 1: Enable TIMER0_CLK5_CLK=Clock Source/P.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: RC16M 010: RTC_32K 011: PERI0_200M 100: DCXO The clock source of TIMER0_CLK5 clock input is 24M/RC 16M/32K/200M/DCXO.
23:3	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0814			Register Name: TIMER0_CLK5_CLK_REG
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x0	FACTOR_P. Factor P 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 Select the pre-scale of clock source.

4.1.6.99 0x0818 TIMER0_CLK6 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0818			Register Name: TIMER0_CLK6_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TIMER0_CLK6_CLK_GATING Gating Clock. 0: Disable 1: Enable TIMER0_CLK6_CLK=Clock Source/P.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: RC16M 010: RTC_32K 011: PERI0_200M 100: DCXO The clock source of TIMER0_CLK6 clock input is 24M/RC 16M/32K/200M/DCXO.
23:3	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0818			Register Name: TIMER0_CLK6_CLK_REG
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x0	FACTOR_P. Factor P 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 Select the pre-scale of clock source.

4.1.6.100 0x081C TIMER0_CLK7 Clock Register (Default Value: 0x0000_0000)

Offset: 0x081C			Register Name: TIMER0_CLK7_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TIMER0_CLK7_CLK_GATING Gating Clock. 0: Disable 1: Enable TIMER0_CLK7_CLK=Clock Source/P.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000:SYS_CLK24M 001:RC16M 010: RTC_32K 011: PERI0_200M 100: DCXO The clock source of TIMER0_CLK7 clock input is 24M/RC 16M/32K/200M/DCXO.
23:3	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x081C			Register Name: TIMER0_CLK7_CLK_REG
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x0	FACTOR_P. Factor P 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 Select the pre-scale of clock source.

4.1.6.101 0x0820 TIMER0_CLK8 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0820			Register Name: TIMER0_CLK8_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TIMER0_CLK8_CLK_GATING Gating Clock. 0: Disable 1: Enable TIMER0_CLK8_CLK=Clock Source/P.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: RC16M 010: RTC_32K 011: PERI0_200M 100: DCXO The clock source of TIMER0_CLK8 clock input is 24M/RC 16M/32K/200M/DCXO.
23:3	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0820			Register Name: TIMER0_CLK8_CLK_REG
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x0	FACTOR_P. Factor P 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 Select the pre-scale of clock source.

4.1.6.102 0x0824 TIMER0_CLK9 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0824			Register Name: TIMER0_CLK9_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TIMER0_CLK9_CLK_GATING Gating Clock. 0: Disable 1: Enable TIMER0_CLK9_CLK=Clock Source/P.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: RC16M 010: RTC_32K 011: PERI0_200M 100: DCXO The clock source of TIMER0_CLK9 clock input is 24M/RC 16M/32K/200M/DCXO.
23:3	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0824			Register Name: TIMER0_CLK9_CLK_REG
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x0	FACTOR_P. Factor P 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 Select the pre-scale of clock source.

4.1.6.103 0x0850 TIMER0 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0850			Register Name: TIMER0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	TIMER0_RST. TIMER0 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	TIMER0_GATING. Gating Clock for TIMER0 0: Mask 1: Pass

4.1.6.104 0x0A00 DE0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A00			Register Name: DE0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DE0_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON DE0_CLK = Clock Source/M.
30:27	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0A00			Register Name: DE0_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: DEPLL3X 001: DEPLL4X 010: PERI0_480M 011: PERI0_400M 100: PERI0_300M 101: VIDEO0PLL4X 110: VIDEO2PLL4X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.105 0x0A04 DE0 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A04			Register Name: DE0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DE0_RST. DE0 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DE0_GATING. Gating Clock for DE0 0: Mask 1: Pass

4.1.6.106 0x0A20 DI Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A20			Register Name: DI_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DI_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON DI_CLK = Clock Source/M.
30:27	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0A20			Register Name: DI_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PERI0_600M 001: PERI0_480M 010: PERI0_400M 011: VIDEO0PLL4X 100: VIDEO2PLL4X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.107 0x0A24 DI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A24			Register Name: DI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DI_RST. DI Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DI_GATING. Gating Clock for DI 0: Mask 1: Pass

4.1.6.108 0x0A40 G2D Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A40			Register Name: G2D_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	G2D_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON G2D_CLK = Clock Source/M.
30:27	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0A40			Register Name: G2D_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PERI0_300M 001: PERI0_400M 010: VIDEO0PLL4X 011: VIDEO2PLL4X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.109 0x0A44 G2D Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A44			Register Name: G2D_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	G2D_RST. G2D Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	G2D_GATING. Gating Clock for G2D 0: Mask 1: Pass

4.1.6.110 0x0A60 EINK Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A60			Register Name: EINK_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	EINK_CLK_GATING. EINK Gating Clock 0: Clock is OFF 1: Clock is ON EINK_CLK = Clock Source/M.
30:27	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0A60			Register Name: EINK_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PERI0_480M 001: PERI0_400M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.111 0x0A64 EINK PANEL Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A64			Register Name: EINK_PANEL_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	EINK_PANEL_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON EINK_PANEL_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: VIDEO0PLL4X 001: VIDEO0PLL3X 010: VIDEO1PLL4X 011: VIDEO1PLL3X 100: PERI0_300M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.112 0x0A6C EINK Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A6C			Register Name: EINK_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0A6C			Register Name: EINK_BGR_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	EINK_RST. EINK Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	EINK_GATING. Gating Clock for EINK 0: Mask 1: Pass

4.1.6.113 0x0A74 DE_SYS Bus Gating Reset Register (Default Value: 0x0001_0000)

Offset: 0x0A74			Register Name: DE_SYS_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x1	DE_SYS_RST. DE_SYS Reset 0: Assert 1: De-assert
15:0	/	/	/

4.1.6.114 0x0A80 VE_ENC0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A80			Register Name: VE_ENC0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VE_ENC0_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON VE_ENC0_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: VE0PLL 001: VE1PLL 010: PERI0_800M 011: PERI0_600M 100: PERI0_480M 101: DEPLL3X 110: NPUPLL

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0A80			Register Name: VE_ENC0_CLK_REG
Bit	Read/Write	Default/Hex	Description
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.115 0x0A88 VE_DEC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A88			Register Name: VE_DEC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VE_DEC_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON VE_DEC_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: VE1PLL 001: VE0PLL 010: PERI0_800M 011: PERI0_600M 100: PERI0_480M 101: DEPLL3X 110: NPUPLL
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.116 0x0A8C VE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A8C			Register Name: VE_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x0	VE_DEC_RST. VE_DEC Reset 0: Assert 1: DE-assert

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0A8C			Register Name: VE_BGR_REG
Bit	Read/Write	Default/Hex	Description
17	/	/	/
16	R/W	0x0	VE_ENC0_RST. VE _ENC0 Reset 0: Assert 1: DE-assert
15:3	/	/	/
2	R/W	0x0	VE_DEC_GATING. Gating Clock for VE_DEC 0: Mask 1: Pass
1	/	/	/
0	R/W	0x0	VE_ENC0_GATING. Gating Clock for VE_ENC0 0: Mask 1: Pass

4.1.6.117 0x0AC0 CE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0AC0			Register Name: CE_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CE_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON CE_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: PERI0_400M 010: PERI0_600M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 15.

Note: ce_clk2m_rc clock is derived from a one-eight frequency division of RC16M.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.118 0x0AC4 CE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0AC4			Register Name: CE_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	CE_SYS_RST. CE_SYS Reset 0: Assert 1: De-assert
16	R/W	0x0	CE_RST. CE Reset 0: Assert 1: De-assert
15:2	/	/	/
1	R/W	0x0	CE_SYS_GATING. Gating Clock for CE_SYS 0: Mask 1: Pass
0	R/W	0x0	CE_GATING. Gating Clock for CE 0: Mask 1: Pass

4.1.6.119 0x0B00 NPU Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B00			Register Name: NPU_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	NPU_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON NPU_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: NPUPLL 001: PERI0_800M 010: PERI0_600M 011: PERI0_480M 100: VE0PLL 101: VE1PLL 110: DEPLL3X
23:5	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0B00			Register Name: NPU_CLK_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.120 0x0B04 NPU Bus Gating Reset Register (Default Value: 0x0008_0000)

Offset: 0x0B04			Register Name: NPU_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19	R/W	0x1	NPU_SRAM_RST. NPU SRAM Reset 0: Assert 1: De-assert
18	R/W	0x0	NPU_AHB_RST. NPU AHB Reset 0: Assert 1: De-assert
17	R/W	0x0	NPU_AXI_RST. NPU AXI Reset 0: Assert 1: De-assert
16	R/W	0x0	NPU_CORE_RST. NPU CORE Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	NPU_GATING. Gating Clock for NPU 0: Mask 1: Pass

4.1.6.121 0x0B20 GPU0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B20			Register Name: GPU0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	GPU0_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON GPU0_CLK = Clock Source*((16-M)/16)...

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0B20			Register Name: GPU0_CLK_REG
Bit	Read/Write	Default/Hex	Description
30:28	/	/	/
27	R/WAC	0x0	GPU0_UPD. GPU0 CLK Configuration 0 update. 0: Invalid 1: Valid Note: Setting this bit will validate Configuration 0. It will be auto cleared after the Configuration 0 is valid. This bit supports gpu0 req/ack signals. When gpu0_update signal is set to 1, gpu0_clk_sel/gpu0_div will be updated.
26:24	R/W	0x0	GPU0_CLK_SEL. Clock Source Select. 000: GPUPLL 001: PERI0_800M 010: PERI0_600M 011: PERI0_400M 100: PERI0_300M 101: PERI0_200M Note: It supports glitch-free switching.
23:4	/	/	/
3:0	R/W	0x0	GPU0_DIV1 Factor M. 0000: Not mask 0001: mask 1 cycle at 16 cycles 0010: mask 2 cycles at 16 cycles 0011: mask 3 cycles at 16 cycles ..... 1111: mask 15 cycles at 16 cycles

4.1.6.122 0x0B24 GPU0 Gating Reset Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0B24			Register Name: GPU0_GATING_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	GPU0_RST. GPU0 Reset. 0: Assert 1: De-assert
15:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0B24			Register Name: GPU0_GATING_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	GPU0_GATING. Gating Clock for GPU0. 0: Mask 1: Pass

4.1.6.123 0x0C00 DRAM0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C00			Register Name: DRAM0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DRAM0_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON DRAM0_CLK = Clock Source/M.
30:28	/	/	/
27	R/WAC	0x0	DRAM0_UPD. DRAM0 CLK Configuration 0 update. 0: Invalid 1: Valid Note: Set this bit will validate Configuration 0. It will be auto cleared after the Configuration 0 is valid. It supports dram req/ack signals. When dram0_upd signal is set to 1, dram0_clk_sel/dram0_div1/dram0_ddrclk_sel will be updated.
26:24	R/W	0x0	DRAM0_CLK_SEL. Clock Source Select 000: DDRPLL 001: PERI1_800M 010: PERI1_600M 011: DEPLL3X 100: NPUPLL Note: The clock MUX provides glitch-free switching and supports dynamic configuration.
23:17	/	/	/
16	R/W	0x0	DRAM0_DDRCLK_SEL DDRCLK Source Select 0: From Phy 1: DRAM0_CLK*8 Note: When DRAM0_CLK is less than 83M, the bit is set to 1.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0C00			Register Name: DRAM0_CLK_REG
Bit	Read/Write	Default/Hex	Description
15:5	/	/	/
4:0	R/W	0x0	DRAM0_DIV1. Factor M M= DRAM0_DIV1 + 1. FACTOR M is from 0 to 31. Note: The clock DIV provides glitch-free switching and supports dynamic configuration.

Note: The ratio of hdr0_clk and external memory clock alters from 1:2 to 1:4.

In the DDR normal working mode, DRAM0_DDRCLK_SEL is 0 by default, and external memory clock source is HY PLL.

In The DDR low-frequency working mode, DRAM0_DDRCLK_SEL should be set as 1. In this scene, PHY PLL is gated, and external memory clock source is ddr0_clk whose frequency should be 667M. Then, hdr0_clk (AM0_CLK) is ddr0_clk/8=83M.

4.1.6.124 0x0C0C DRAM0 Bus Gating Reset Register (Default Value: 0x0000_0001)

Offset: 0x0C0C			Register Name: DRAM0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DRAM0_RST. DRAM0 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x1	DRAM0_GATING. Gating Clock for DRAM0 0: Mask 1: Pass

4.1.6.125 0x0C80 NAND0 CLK0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C80			Register Name: NAND0_CLK0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	NAND0_CLK0_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON NAND0_CLK0_CLK = Clock Source/M.
30:27	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0C80			Register Name: NAND0_CLK0_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: PERI0_400M 010: PERI0_300M 011: PERI1_400M 100: PERI1_300M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 15.

4.1.6.126 0x0C84 NAND0 CLK1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C84			Register Name: NAND0_CLK1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	NAND0_CLK1_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON NAND0_CLK1_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: PERI0_400M 010: PERI0_300M 011: PERI1_400M 100: PERI1_300M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 15.

4.1.6.127 0x0C8C NAND0 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0C8C			Register Name: NAND0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0C8C			Register Name: NAND0_BGR_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	NAND0_RST NAND0 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	NAND0_GATING. Gating Clock for NAND0 0: Mask 1: Pass

4.1.6.128 0x0D00 SMHC0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0D00			Register Name: SMHC0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SMHC0_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON SMHC0_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: PERI0_400M 010: PERI0_300M 011: PERI1_400M 100: PERI1_300M
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N. Factor N N= FACTOR_N +1. FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.129 0x0D0C SMHC0 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0D0C	Register Name: SMHC0_BGR_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	SMHC0_RST. SMHC0 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	SMHC0_GATING. Gating Clock for SMHC0 0: Mask 1: Pass

4.1.6.130 0x0D10 SMHC1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0D10			Register Name: SMHC1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SMHC1_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON SMHC1_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: PERI0_400M 010: PERI0_300M 011: PERI1_400M 100: PERI1_300M
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1. FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.131 0x0D1C SMHC1 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0D1C	Register Name: SMHC1_BGR_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	SMHC1_RST. SMHC1 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	SMHC1_GATING. Gating Clock for SMHC1 0: Mask 1: Pass

4.1.6.132 0x0D20 SMHC2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0D20			Register Name: SMHC2_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SMHC2_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON SMHC2_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: PERI0_800M 010: PERI0_600M 011: PERI1_800M 100: PERI1_600M
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N. Factor N N= FACTOR_N +1. FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.133 0x0D2C SMHC2 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0D2C	Register Name: SMHC2_BGR_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	SMHC2_RST SMHC2 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	SMHC2_GATING. Gating Clock for SMHC2 0: Mask 1: Pass

4.1.6.134 0x0D30 SMHC3 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0D30			Register Name: SMHC3_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SMHC3_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON SMHC3_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: PERI0_800M 010: PERI0_600M 011: PERI1_800M 100: PERI1_600M
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N. Factor N N= FACTOR_N +1. FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.135 0x0D3C SMHC3 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0D3C	Register Name: SMHC3_BGR_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	SMHC3_RST. SMHC3 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	SMHC3_GATING. Gating Clock for SMHC3 0: Mask 1: Pass

4.1.6.136 0x0D80 UFS_AXI Clock Register (Default Value: 0x0000_0000)

Offset: 0x0D80			Register Name: UFS_AXI_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	UFS_AXI_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON UFS_AXI_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PERI0_300M 001: PERI0_200M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.137 0x0D84 UFS_CFG Clock Register (Default Value: 0x8000_0018)

Offset: 0x0D84			Register Name: UFS_CFG_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	UFS_CFG_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON UFS_CFG_CLK = Clock Source/M.
30:27	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0D84			Register Name: UFS_CFG_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PERI0_480M 001: DCXO
23:5	/	/	/
4:0	R/W	0x18	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.138 0x0D8C UFS Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0D8C			Register Name: UFS_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19	R/W	0x0	UFS_CORE_RST. UFS CORE Reset 0: Assert 1: De-assert
18	R/W	0x0	UFS_PHY_RST. UFS PHY Reset 0: Assert 1: De-assert
17	R/W	0x0	UFS_AXI_RST. UFS AXI Reset 0: Assert 1: De-assert
16	R/W	0x0	UFS_RST. UFS Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	UFS_GATING. Gating Clock for UFS 0: Mask 1: Pass

4.1.6.139 0x0D90 UFS Reference Clock Enable Register (Default Value: 0x0000_0000)

Offset: 0x0D90	Register Name: UFS_REF_CLK_EN_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	UFS_REF_CLK_EN. UFS Reference clock enable from application layer. The register should be configured based on the reference clock. 0: Use the internal reference clock 1: Use the external reference clock NOTE: The signal is the ref_clk_en_app in the UFS.

4.1.6.140 0x0E00 UART0 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0E00			Register Name: UART0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	UART0_RST. UART0 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	UART0_GATING. Gating Clock for UART0 0: Mask 1: Pass

NOTE: UART0 working clock sources from APB_UART.

4.1.6.141 0x0E04 UART1 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0E04			Register Name: UART1_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	UART1_RST. UART1 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	UART1_GATING. Gating Clock for UART1 0: Mask 1: Pass

NOTE: UART1 working clock sources from APB_UART.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.142 0x0E08 UART2 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0E08			Register Name: UART2_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	UART2_RST. UART2 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	UART2_GATING. Gating Clock for UART2 0: Mask 1: Pass

NOTE: UART2 working clock sources from APB_UART.

4.1.6.143 0x0E0C UART3 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0E0C			Register Name: UART3_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	UART3_RST. UART3 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	UART3_GATING. Gating Clock for UART3 0: Mask 1: Pass

NOTE: UART3 working clock sources from APB_UART.

4.1.6.144 0x0E10 UART4 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0E10			Register Name: UART4_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	UART4_RST. UART4 Reset 0: Assert 1: De-assert
15:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0E10			Register Name: UART4_BGR_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	UART4_GATING. Gating Clock for UART4 0: Mask 1: Pass

NOTE: UART4 working clock sources from APB_UART.

4.1.6.145 0x0E14 UART5 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0E14			Register Name: UART5_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	UART5_RST. UART5 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	UART5_GATING. Gating Clock for UART5 0: Mask 1: Pass

NOTE: UART5 working clock sources from APB_UART.

4.1.6.146 0x0E18 UART6 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0E18			Register Name: UART6_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	UART6_RST. UART6 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	UART6_GATING. Gating Clock for UART6 0: Mask 1: Pass

NOTE: UART6 working clock sources from APB_UART.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.147 0x0E80 TWI0 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0E80			Register Name: TWI0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	TWI0_RST. TWI0 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	TWI0_GATING. Gating Clock for TWI0 0: Mask 1: Pass

NOTE: TWI0 working clock sources from APB1.

4.1.6.148 0x0E84 TWI1 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0E84			Register Name: TWI1_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	TWI1_RST. TWI1 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	TWI1_GATING. Gating Clock for TWI1 0: Mask 1: Pass

NOTE: TWI1 working clock sources from APB1.

4.1.6.149 0x0E88 TWI2 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0E88			Register Name: TWI2_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	TWI2_RST. TWI2 Reset 0: Assert 1: De-assert
15:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0E88			Register Name: TWI2_BGR_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	TWI2_GATING. Gating Clock for TWI2 0: Mask 1: Pass

NOTE: TWI2 working clock sources from APB1.

4.1.6.150 0x0E8C TWI3 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0E8C			Register Name: TWI3_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	TWI3_RST. TWI3 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	TWI3_GATING. Gating Clock for TWI3 0: Mask 1: Pass

NOTE: TWI3 working clock sources from APB1.

4.1.6.151 0x0E90 TWI4 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0E90			Register Name: TWI4_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	TWI4_RST. TWI4 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	TWI4_GATING. Gating Clock for TWI4 0: Mask 1: Pass

NOTE: TWI4 working clock sources from APB1.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.152 0x0E94 TWI5 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0E94			Register Name: TWI5_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	TWI5_RST. TWI5 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	TWI5_GATING. Gating Clock for TWI5 0: Mask 1: Pass

NOTE: TWI5 working clock sources from APB1.

4.1.6.153 0x0E98 TWI6 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0E98			Register Name: TWI6_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	TWI6_RST. TWI6 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	TWI6_GATING. Gating Clock for TWI6 0: Mask 1: Pass

NOTE: TWI6 working clock sources from APB1.

4.1.6.154 0x0E9C TWI7 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0E9C			Register Name: TWI7_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	TWI7_RST. TWI7 Reset 0: Assert 1: De-assert
15:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0E9C			Register Name: TWI7_BGR_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	TWI7_GATING. Gating Clock for TWI7 0: Mask 1: Pass

NOTE: TWI7 working clock sources from APB1.

4.1.6.155 0x0EA0 TWI8 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0EA0			Register Name: TWI8_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	TWI8_RST. TWI8 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	TWI8_GATING. Gating Clock for TWI8 0: Mask 1: Pass

NOTE: TWI8 working clock sources from APB1.

4.1.6.156 0x0EA4 TWI9 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0EA4			Register Name: TWI9_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	TWI9_RST TWI9 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	TWI9_GATING. Gating Clock for TWI9 0: Mask 1: Pass

NOTE: TWI9 working clock sources from APB1.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.157 0x0EA8 TWI10 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0EA8			Register Name: TWI10_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	TWI10_RST. TWI10 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	TWI10_GATING. Gating Clock for TWI10 0: Mask 1: Pass

NOTE: TWI10 working clock sources from APB1.

4.1.6.158 0x0EAC TWI11 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0EAC			Register Name: TWI11_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	TWI11_RST. TWI11 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	TWI11_GATING. Gating Clock for TWI11 0: Mask 1: Pass

NOTE: TWI11 working clock sources from APB1.

4.1.6.159 0x0EB0 TWI12 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0EB0			Register Name: TWI12_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	TWI12_RST. TWI12 Reset 0: Assert 1: De-assert
15:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0EB0			Register Name: TWI12_BGR_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	TWI12_GATING. Gating Clock for TWI12 0: Mask 1: Pass

NOTE: TWI12 working clock sources from APB1.

4.1.6.160 0x0F00 SPI0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0F00			Register Name: SPI0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SPI0_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON SPI0_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000:SYS_CLK24M 001: PERI0_300M 010: PERI0_200M 011: PERI1_300M 100: PERI1_200M 101: PERI0_480M 110: PERI1_480M 111:DCXO
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N. Factor N N= FACTOR_N +1. FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.161 0x0F04 SPI0 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0F04	Register Name: SPI0_BGR_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	SPI0_RST. SPI0 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	SPI0_GATING. Gating Clock for SPI0 0: Mask 1: Pass

4.1.6.162 0x0F08 SPI1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0F08			Register Name: SPI1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SPI1_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON SPI1_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000:SYS_CLK24M 001: PERI0_300M 010: PERI0_200M 011: PERI1_300M 100: PERI1_200M 101: PERI0_480M 110: PERI1_480M 111:DCXO
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N. Factor N N= FACTOR_N +1. FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.163 0x0F0C SPI1 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0F0C			Register Name: SPI1_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	SPI1_RST. SPI1 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	SPI1_GATING. Gating Clock for SPI1 0: Mask 1: Pass

4.1.6.164 0x0F10 SPI2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0F10			Register Name: SPI2_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SPI2_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON SPI2_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000:SYS_CLK24M 001: PERI0_300M 010: PERI0_200M 011: PERI1_300M 100: PERI1_200M 101: PERI0_480M 110: PERI1_480M 111:DCXO
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N. Factor N N= FACTOR_N +1. FACTOR_N is from 0 to 31.
7:5	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0F10			Register Name: SPI2_CLK_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.165 0x0F14 SPI2 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0F14			Register Name: SPI2_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	SPI2_RST. SPI2 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	SPI2_GATING. Gating Clock for SPI2 0: Mask 1: Pass

4.1.6.166 0x0F18 SPIF Clock Register (Default Value: 0x0000_0000)

Offset: 0x0F18			Register Name: SPIF_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SPIF_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON SPIF_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000:SYS_CLK24M 001: PERI0_400M 010: PERI0_300M 011: PERI1_400M 100: PERI1_300M 101: PERI0_160M 110: PERI1_160M 111:DCXO
23:13	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0F18			Register Name: SPIF_CLK_REG
Bit	Read/Write	Default/Hex	Description
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1. FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.167 0x0F1C SPIF Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0F1C			Register Name: SPIF_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	SPIF_RST. SPIF Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	SPIF_GATING. Gating Clock for SPIF 0: Mask 1: Pass

4.1.6.168 0x0F20 SPI3 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0F20			Register Name: SPI3_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SPI3_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON SPI3_CLK = Clock Source/M/N.
30:27	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0F20			Register Name: SPI3_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000:SYS_CLK24M 001: PERI0_300M 010: PERI0_200M 011: PERI1_300M 100: PERI1_200M 101: PERI0_480M 110: PERI1_480M 111:DCXO
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N. Factor N N= FACTOR_N +1. FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.169 0x0F24 SPI3 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0F24			Register Name: SPI3_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	SPI3_RST. SPI3 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	SPI3_GATING. Gating Clock for SPI3 0: Mask 1: Pass

4.1.6.170 0x0FC0 GPADC0_24M Clock Register (Default Value: 0x0000_0000)

Offset: 0x0FC0			Register Name: GPADC0_24M_CLK_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0FC0			Register Name: GPADC0_24M_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	GPADC0_24M_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON GPADC0_24M_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: DCXO
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.171 0x0FC4 GPADC0 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0FC4			Register Name: GPADC0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	GPADC0_RST. GPADC0 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	GPADC0_GATING. Gating Clock for GPADC0 0: Mask 1: Pass

4.1.6.172 0x0FE4 THS0 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0FE4			Register Name: THS0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	THS0_RST. THS0 Reset 0: Assert 1: DE-assert

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0FE4			Register Name: THS0_BGR_REG
Bit	Read/Write	Default/Hex	Description
15:1	/	/	/
0	R/W	0x0	THS0_GATING. Gating Clock for THS0 0: Mask 1: Pass

4.1.6.173 0x1000 IRRX Clock Register (Default Value: 0x0000_0000)

Offset: 0x1000			Register Name: IRRX_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	IRRX_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON IRRX_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: RTC_32K 001:SYS_CLK24M 010:DCXO
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.174 0x1004 IRRX Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x1004			Register Name: IRRX_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	IRRX_RST. IRRX Reset 0: Assert 1: De-assert
15:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1004			Register Name: IRRX_BGR_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	IRRX_GATING. Gating Clock for IRRX 0: Mask 1: Pass

4.1.6.175 0x1008 IRTX Clock Register (Default Value: 0x0000_0000)

Offset: 0x1008			Register Name: IRTX_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	IRTX_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON IRTX_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: PERI1_600M 010: DCXO
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.176 0x100C IRTX Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x100C			Register Name: IRTX_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	IRTX_RST. IRTX Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	IRTX_GATING. Gating Clock for IRTX 0: Mask 1: Pass

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.177 0x1024 LRADC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x1024			Register Name: LRADC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	LRADC_RST. LRADC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	LRADC_GATING. Gating Clock for LRADC 0: Mask 1: Pass

4.1.6.178 0x1200 I2SPCM0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x1200			Register Name: I2SPCM0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	I2SPCM0_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON I2SPCM0_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: AUDIO0PLL4X 001: AUDIO1PLL_DIV2 010: AUDIO1PLL_DIV5 011: PERI0_200M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.179 0x120C I2SPCM0 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x120C			Register Name: I2SPCM0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x120C			Register Name: I2SPCM0_BGR_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	I2SPCM0_RST. I2SPCM0 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	I2SPCM0_GATING. Gating Clock for I2SPCM0 0: Mask 1: Pass

4.1.6.180 0x1210 I2SPCM1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x1210			Register Name: I2SPCM1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	I2SPCM1_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON I2SPCM1_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: AUDIO0PLL4X 001: AUDIO1PLL_DIV2 010: AUDIO1PLL_DIV5 011: PERI0_200M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.181 0x121C I2SPCM1 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x121C			Register Name: I2SPCM1_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x121C			Register Name: I2SPCM1_BGR_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	I2SPCM1_RST. I2SPCM1 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	I2SPCM1_GATING. Gating Clock for I2SPCM1 0: Mask 1: Pass

4.1.6.182 0x1220 I2SPCM2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x1220			Register Name: I2SPCM2_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	I2SPCM2_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON I2SPCM2_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: AUDIO0PLL4X 001: AUDIO1PLL_DIV2 010: AUDIO1PLL_DIV5 011: PERI0_200M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.183 0x1224 I2SPCM2_ASRC Clock Register (Default Value: 0x0000_0000)

Offset: 0x1224			Register Name: I2SPCM2_ASRC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	I2SPCM2_ASRC_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON I2SPCM2_ASRC_CLK = Clock Source/M.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1224			Register Name: I2SPCM2_ASRC_CLK_REG
Bit	Read/Write	Default/Hex	Description
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: AUDIO0PLL4X 001: AUDIO1PLL_DIV2 010: AUDIO1PLL_DIV5 011: PERI0_300M 100: PERI1_300M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31

4.1.6.184 0x122C I2SPCM2 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x122C			Register Name: I2SPCM2_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	I2SPCM2_RST. I2SPCM2 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	I2SPCM2_GATING. Gating Clock for I2SPCM2 0: Mask 1: Pass

4.1.6.185 0x1230 I2SPCM3 Clock Register (Default Value: 0x0000_0000)

Offset: 0x1230			Register Name: I2SPCM3_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	I2SPCM3_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON I2SPCM3_CLK = Clock Source/M.
30:27	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1230			Register Name: I2SPCM3_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: AUDIO0PLL4X 001: AUDIO1PLL_DIV2 010: AUDIO1PLL_DIV5 011: PERI0_200M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.186 0x123C I2SPCM3 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x123C			Register Name: I2SPCM3_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	I2SPCM3_RST. I2SPCM3 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	I2SPCM3_GATING. Gating Clock for I2SPCM3 0: Mask 1: Pass

4.1.6.187 0x1240 I2SPCM4 Clock Register (Default Value: 0x0000_0000)

Offset: 0x1240			Register Name: I2SPCM4_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	I2SPCM4_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON I2SPCM4_CLK = Clock Source/M.
30:27	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1240			Register Name: I2SPCM4_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: AUDIO0PLL4X 001: AUDIO1PLL_DIV2 010: AUDIO1PLL_DIV5 011: PERI0_200M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.188 0x124C I2SPCM4 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x124C			Register Name: I2SPCM4_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	I2SPCM4_RST. I2SPCM4 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	I2SPCM4_GATING. Gating Clock for I2SPCM4 0: Mask 1: Pass

4.1.6.189 0x1280 OWA TX Clock Register (Default Value: 0x0000_0000)

Offset: 0x1280			Register Name: OWA_TX_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	OWA_TX_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON OWA_TX_CLK = Clock Source/M.
30:27	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1280			Register Name: OWA_TX_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: AUDIO0PLL4X 001: AUDIO1PLL_DIV2 010: AUDIO1PLL_DIV5
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.190 0x1284 OWA RX Clock Register (Default Value: 0x0000_0000)

Offset: 0x1284			Register Name: OWA_RX_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	OWA_RX_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON OWA_RX_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: Reserved 001: Reserved 010: PERI0_400M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.191 0x128C OWA Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x128C			Register Name: OWA_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x128C			Register Name: OWA_BGR_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	OWA_RST. OWA Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	OWA_GATING. Gating Clock for OWA 0: Mask 1: Pass

4.1.6.192 0x12C0 DMIC Clock Register (Default Value: 0x0000_0000)

Offset: 0x12C0			Register Name: DMIC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DMIC_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON DMIC_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: AUDIO0PLL4X 001: AUDIO1PLL_DIV2 010: AUDIO1PLL_DIV5
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.193 0x12CC DMIC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x12CC			Register Name: DMIC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DMIC_RST DMIC Reset 0: Assert 1: De-assert

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x12CC			Register Name: DMIC_BGR_REG
Bit	Read/Write	Default/Hex	Description
15:1	/	/	/
0	R/W	0x0	DMIC_GATING. Gating Clock for DMIC 0: Mask 1: Pass

4.1.6.194 0x1300 USB0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x1300			Register Name: USB0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	USB0_CLKEN. Gating Clock for USB0 HOST OHCI. 0: Clock is OFF 1: Clock is ON
30	R/W	0x0	USB0_PHY_RSTN. USB0 PHY Reset. 0: Assert 1: De-assert
29:26	/	/	/
25:24	R/W	0x0	USB0_CLK12M_SEL USB0 HOST OHCI 12M Source Select. 000: 12M divided from 48MHz 001: 12M divided from SYS_CLK24M 010: RTC_32K 011: RC16M
23:0	/	/	/

4.1.6.195 0x1304 USB0 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x1304			Register Name: USB0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	USB0_DEVICE_RST. USB0 DEVICE Reset 0: Assert 1: De-assert
23:21	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1304			Register Name: USB0_BGR_REG
Bit	Read/Write	Default/Hex	Description
20	R/W	0x0	USB0_EHCI_RST. USB0 HOST EHCI Reset 0: Assert 1: De-assert
19:17	/	/	/
16	R/W	0x0	USB0_OHCI_RST. USB0 HOST OHCI Reset 0: Assert 1: De-assert
15:9	/	/	/
8	R/W	0x0	USB0_DEVICE_GATING. Gating Clock for USB0 DEVICE 0: Mask 1: Pass
7:5	/	/	/
4	R/W	0x0	USB0_EHCI_GATING. Gating Clock for USB0 HOST EHCI 0: Mask 1: Pass
3:1	/	/	/
0	R/W	0x0	USB0_OHCI_GATING. Gating Clock for USB0 HOST OHCI 0: Mask 1: Pass

4.1.6.196 0x1308 USB1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x1308			Register Name: USB1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	USB1_CLKEN. Gating Clock for USB1 HOST OHCI. 0: Clock is OFF 1: Clock is ON
30	R/W	0x0	USB1_PHY_RSTN. USB1 PHY Reset. 0: Assert 1: De-assert
29:26	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1308			Register Name: USB1_CLK_REG
Bit	Read/Write	Default/Hex	Description
25:24	R/W	0x0	USB1_CLK12M_SEL USB1 HOST OHCI 12M Source Select. 000: 12M divided from 48MHz 001: 12M divided from SYS_CLK24M 010: RTC_32K 011: RC16M
23:0	/	/	/

4.1.6.197 0x130C USB1 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x130C			Register Name: USB1_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20	R/W	0x0	USB1_EHCI_RST. USB1 HOST EHCI Reset 0: Assert 1: De-assert
19:17	/	/	/
16	R/W	0x0	USB1_OHCI_RST. USB1 HOST OHCI Reset 0: Assert 1: De-assert
15:5	/	/	/
4	R/W	0x0	USB1_EHCI_GATING. Gating Clock for USB1 HOST EHCI 0: Mask 1: Pass
3:1	/	/	/
0	R/W	0x0	USB1_OHCI_GATING. Gating Clock for USB1 HOST OHCI 0: Mask 1: Pass

4.1.6.198 0x1340 USB0_USB1_REF Clock Register (Default Value: 0x8000_0000)

Offset: 0x1340			Register Name: USB0_USB1_REF_CLK_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1340			Register Name: USB0_USB1_REF_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	USB0_USB1_REF_CLK_GATING. Gating Reference Clock for USB0/USB1 0: Clock is OFF 1: Clock is ON USB0_USB1_REF_CLK = Clock Source.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: DCXO
23:0	/	/	/

4.1.6.199 0x1348 USB2_U2_REF Clock Register (Default Value: 0x0000_0000)

Offset: 0x1348			Register Name: USB2_U2_REF_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	USB2_U2_REF_CLK_GATING. Gating Reference Clock for USB2.0 in USB2 Gating Clock. 0: Clock is OFF 1: Clock is ON USB2_U2_REF_CLK = Clock Source.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: DCXO
23:0	/	/	/

4.1.6.200 0x1350 USB2_SUSPEND Clock Register (Default Value: 0x0000_0000)

Offset: 0x1350			Register Name: USB2_SUSPEND_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	USB2_SUSPEND_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON USB2_SUSPEND_CLK = Clock Source/M.
30:25	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1350			Register Name: USB2_SUSPEND_CLK_REG
Bit	Read/Write	Default/Hex	Description
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 0: RTC_32K 1: SYS_CLK24M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.201 0x1354 USB2_MF Clock Register (Default Value: 0x0000_0000)

Offset: 0x1354			Register Name: USB2_MF_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	USB2_MF_CLK_GATING. USB2 Microframe Clock Gating. 0: Clock is OFF 1: Clock is ON USB2_MF_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: PERI0_300M 010: DCXO
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.202 0x135C USB2 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x135C			Register Name: USB2_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	USB2_RST. USB2 Reset 0: Assert 1: De-assert

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x135C			Register Name: USB2_BGR_REG
Bit	Read/Write	Default/Hex	Description
15:0	/	/	/

4.1.6.203 0x1360 USB2_U3_UTMI Clock Register (Default Value: 0x0000_0000)

Offset: 0x1360			Register Name: USB2_U3_UTMI_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	USB2_U3_UTMI_CLK_GATING. USB2_U3_UTMI Clock Gating. 0: Clock is OFF 1: Clock is ON USB2_U3_UTMI_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: PERI0_300M 010: DCXO
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.204 0x1364 USB2_U2_PIPE Clock Register (Default Value: 0x0000_0000)

Offset: 0x1364			Register Name: USB2_U2_PIPE_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	USB2_U2_PIPE_CLK_GATING. USB2 Microframe Clock Gating. 0: Clock is OFF 1: Clock is ON USB2_U2_PIPE_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: PERI0_480M 010: DCXO
23:5	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1364			Register Name: USB2_U2_PIPE_CLK_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.205 0x1380 PCIE0_AUX Clock Register (Default Value: 0x0000_0000)

Offset: 0x1380			Register Name: PCIE0_AUX_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PCIE0_AUX_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON PCIE0_AUX_CLK = Clock Source/M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 0: SYS_CLK24M 1: RTC_32K
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.206 0x1384 PCIE0_AXI_SLV Clock Register (Default Value: 0x0000_0000)

Offset: 0x1384			Register Name: PCIE0_AXI_SLV_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PCIE0_AXI_SLV_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON PCIE0_AXI_SLV_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PERI0_600M 001: PERI0_480M 010: PERI0_400M

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1384			Register Name: PCIE0_AXI_SLV_CLK_REG
Bit	Read/Write	Default/Hex	Description
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.207 0x138C PCIE0 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x138C			Register Name:PCIE0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	PCIE0_RST. PCIE0 Reset 0: Assert 1: De-assert
16	R/W	0x0	PCIE0_PWRUP_RST. PCIE0 POWER_UP Reset 0: Assert 1: De-assert
15:0	/	/	/

4.1.6.208 0x13C0 SERDES_PHY_CFG Clock Register (Default Value: 0x0000_0000)

Offset: 0x13C0			Register Name: SERDES_PHY_CFG_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SERDES_PHY_CFG_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON SERDES_PHY_CFG_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: PERI0_600M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor MFACTOR_M is from 0 to 31.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.209 0x13C4 SERDES Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x13C4			Register Name: SERDES_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	SERDES_RST. SERDES Reset 0: Assert 1: DE-assert
15:0	/	/	/

4.1.6.210 0x1400 GMAC_PTP Clock Register (Default Value: 0x0000_0000)

Offset: 0x1400			Register Name: GMAC_PTP_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	GMAC_PTP_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON GMAC_PTP_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000:SYS_CLK24M 001: PERI0_200M 010:DCXO
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.211 0x1410 GMAC0_PHY Clock Register (Default Value: 0x0000_0000)

Offset: 0x1410			Register Name: GMAC0_PHY_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	GMAC0_PHY_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON GMAC0_PHY_CLK =PERI0_150M/M.
30:5	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1410			Register Name: GMAC0_PHY_CLK_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.212 0x141C GMAC0 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x141C			Register Name: GMAC0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	GMAC0_AXI_RST. GMAC0 AXI Reset 0: Assert 1: De-assert
16	R/W	0x0	GMAC0_RST. GMAC0 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	GMAC0_GATING. Gating Clock for GMAC0 0: Mask 1: Pass

4.1.6.213 0x1500 VO0_TCONLCD0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x1500			Register Name: VO0_TCONLCD0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VO0_TCONLCD0_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON VO0_TCONLCD0_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: VIDEO0PLL4X 001: VIDEO1PLL4X 010: VIDEO2PLL4X 011:PERI0PLL2X

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1500			Register Name: VO0_TCONLCD0_CLK_REG
Bit	Read/Write	Default/Hex	Description
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.214 0x1504 VO0_TCONLCD0 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x1504			Register Name: VO0_TCONLCD0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	VO0_TCONLCD0_RST. VO0_TCON LCD0 Reset 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	VO0_TCONLCD0_GATING. Gating Clock for VO0_TCON LCD0 0: Mask 1: Pass

4.1.6.215 0x1508 VO0_TCONLCD1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x1508			Register Name: VO0_TCONLCD1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VO0_TCONLCD1_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON VO0_TCONLCD1_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: VIDEO0PLL4X 001: VIDEO1PLL4X 010: VIDEO2PLL4X 011: PERI0PLL2X
23:5	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1508			Register Name: VO0_TCONLCD1_CLK_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 15.

4.1.6.216 0x150C VO0_TCONLCD1 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x150C			Register Name: VO0_TCONLCD1_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	VO0_TCONLCD1_RST. VO0_TCON LCD1 Reset 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	VO0_TCONLCD1_GATING Gating Clock for VO0_TCON LCD1 0: Mask 1: Pass

4.1.6.217 0x1544 LVDS0 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x1544			Register Name: LVDS0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	LVDS0_RST. LVDS0 Reset 0: Assert 1: De-assert
15:0	/	/	/

4.1.6.218 0x154C LVDS1 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x154C			Register Name: LVDS1_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	LVDS1_RST. LVDS1 Reset 0: Assert 1: De-assert

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x154C			Register Name: LVDS1_BGR_REG
Bit	Read/Write	Default/Hex	Description
15:0	/	/	/

4.1.6.219 0x1580 DSI0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x1580			Register Name: DSI0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DSI0_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON DSI0_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000:SYS_CLK24M 001: PERI0_200M 010: PERI0_150M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.220 0x1584 DSI0 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x1584			Register Name: DSI0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DSI0_RST. DSI0 Reset 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	DSI0_GATING. Gating Clock for DSI0 0: Mask 1: Pass

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.221 0x1588 DSI1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x1588			Register Name: DSI1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DSI1_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON DSI1_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: PERI0_200M 010: PERI0_150M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.222 0x158C DSI1 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x158C			Register Name: DSI1_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DSI1_RST. DSI1 Reset 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	DSI1_GATING. Gating Clock for DSI1 0: Mask 1: Pass

4.1.6.223 0x15C0 COMBPHY0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x15C0			Register Name: COMBPHY0_CLK_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x15C0			Register Name: COMBPHY0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	COMBPHY0_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON COMBPHY0_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: VIDEO0PLL4X 001: VIDEO1PLL4X 010: VIDEO2PLL4X 011: PERI0PLL2X 100: VIDEO0PLL3X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.224 0x15C4 COMBPHY1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x15C4			Register Name: COMBPHY1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	COMBPHY1_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON COMBPHY1_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: VIDEO0PLL4X 001: VIDEO1PLL4X 010: VIDEO2PLL4X 011: PERI0PLL2X 100: VIDEO0PLL3X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.225 0x1604 TCONTV0 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x1604			Register Name: TCONTV0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	TCONTV0_RST. TCONTV0 Reset 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	TCONTV0_GATING. Gating Clock for TCONTV0 0: Mask 1: Pass

4.1.6.226 0x160C TCONTV1 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x160C			Register Name: TCONTV1_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	TCONTV1_RST. TCONTV1 Reset 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	TCONTV1_GATING. Gating Clock for TCONTV1 0: Mask 1: Pass

4.1.6.227 0x1640 EDP_TV Clock Register (Default Value: 0x0000_0000)

Offset: 0x1640			Register Name: EDP_TV_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	EDP_TV_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON EDP_TV_CLK = Clock Source/M/N.
30:27	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1640			Register Name: EDP_TV_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: VIDEO0PLL4X 001: VIDEO1PLL4X 010: VIDEO2PLL4X 011: PERI0PLL2X
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1. FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.228 0x164C EDP Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x164C			Register Name: EDP_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	EDP_RST EDP Reset 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	EDP_GATING. Gating Clock for EDP 0: Mask 1: Pass

4.1.6.229 0x1680 HDMI CEC Clock Register (Default Value: 0x0000_0000)

Offset: 0x1680			Register Name: HDMI_CEC_CLK_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1680			Register Name: HDMI_CEC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HDMI_CEC_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON HDMI_REF_CLK = Clock Source.
30	R/W	0x0	PERI_GATING. Gating PERIPLL Clock. 0: Clock is OFF 1: Clock is ON
29:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: RTC_32K 001: HDMI_CEC_CLK32K,PERI0PLL2X/36621=32.768kHz
23:0	/	/	/

4.1.6.230 0x1684 HDMI_TV Clock Register (Default Value: 0x0000_0000)

Offset: 0x1684			Register Name: HDMI_TV_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HDMI_TV_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON HDMI_TV_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: VIDEO0PLL4X 001: VIDEO1PLL4X 010: VIDEO2PLL4X 011: PERI0PLL2X
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N. Factor N N= FACTOR_N +1. FACTOR_N is from 0 to 31.
7:5	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1684			Register Name: HDMI_TV_CLK_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.231 0x168C HDMI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x168C			Register Name: HDMI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x0	HDMI_HDCP_RST. HDMI_HDCP Reset 0: Assert 1: De-assert
17	R/W	0x0	HDMI_SUB_RST. HDMI_SUB Reset 0: Assert 1: De-assert
16	R/W	0x0	HDMI_MAIN_RST. HDMI_MAIN Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	HDMI_GATING. Gating Clock for HDMI 0: Mask 1: Pass

4.1.6.232 0x1690 HDMI SFR Clock Register (Default Value: 0x0000_0000)

Offset: 0x1690			Register Name: HDMI_SFR_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HDMI_SFR_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON HDMI_SFR_CLK = Clock Source.
30:27	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1690			Register Name: HDMI_SFR_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: DCXO
23:0	/	/	/

4.1.6.233 0x1694 HDCP ESM Clock Register (Default Value: 0x0000_0000)

Offset: 0x1694			Register Name: HDCP_ESM_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HDCP_ESM_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON HDCP_ESM_CLK = PERI0_300M.
30:0	/	/	/

4.1.6.234 0x16C4 DPSS_TOP0 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x16C4			Register Name: DPSS_TOP0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DPSS_TOP0_RST. DPSS_TOP0 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DPSS_TOP0_GATING. Gating Clock for DPSS_TOP0 0: Mask 1: Pass

4.1.6.235 0x16CC DPSS_TOP1 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x16CC			Register Name: DPSS_TOP1_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x16CC			Register Name: DPSS_TOP1_BGR_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	DPSS_TOP1_RST. DPSS_TOP1 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DPSS_TOP1_GATING. Gating Clock for DPSS_TOP1 0: Mask 1: Pass

4.1.6.236 0x16E4 VIDEO_OUT0 Bus Gating Reset Register (Default Value: 0x0001_0000)

Offset: 0x16E4			Register Name: VIDEO_OUT0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x1	VIDEO_OUT0_RST. VIDEO_OUT0 Reset 0: Assert 1: DE-assert
15:0	/	/	/

4.1.6.237 0x16EC VIDEO_OUT1 Bus Gating Reset Register (Default Value: 0x0001_0000)

Offset: 0x16EC			Register Name: VIDEO_OUT1_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x1	VIDEO_OUT1_RST. VIDEO_OUT1 Reset 0: Assert 1: DE-assert
15:0	/	/	/

4.1.6.238 0x1700 LEDC Clock Register (Default Value: 0x0000_0000)

Offset: 0x1700			Register Name: LEDC_CLK_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1700			Register Name: LEDC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LEDC_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON LEDC_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: PERI0_600M 010: DCXO
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.239 0x1704 LEDC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x1704			Register Name: LEDC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	LEDC_RST. LEDC Reset 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	LEDC_GATING. Gating Clock for LEDC 0: Mask 1: Pass

4.1.6.240 0x1744 DSC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x1744			Register Name: DSC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1744			Register Name: DSC_BGR_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	DSC_RST. DSC Reset 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	DSC_GATING. Gating Clock for DSC 0: Mask 1: Pass

4.1.6.241 0x1800 CSI Master0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x1800			Register Name: CSI_MASTER0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CSI_MASTER0_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON CSI_MASTER0_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: VIDEO0PLL4X 010: VIDEO0PLL3X 011: VIDEO1PLL4X 100: VIDEO1PLL3X 101: VIDEO2PLL4X 110: VIDEO2PLL3X
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N. Factor N N= FACTOR_N +1. FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.242 0x1804 CSI Master1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x1804			Register Name: CSI_MASTER1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CSI_MASTER1_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON CSI_MASTER1_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: VIDEO0PLL4X 010: VIDEO0PLL3X 011: VIDEO1PLL4X 100: VIDEO1PLL3X 101: VIDEO2PLL4X 110: VIDEO2PLL3X
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N. Factor N N= FACTOR_N +1. FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.243 0x1808 CSI Master2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x1808			Register Name: CSI_MASTER2_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CSI_MASTER2_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON CSI_MASTER2_CLK = Clock Source/M/N.
30:27	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1808			Register Name: CSI_MASTER2_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: VIDEO0PLL4X 010: VIDEO0PLL3X 011: VIDEO1PLL4X 100: VIDEO1PLL3X 101: VIDEO2PLL4X 110: VIDEO2PLL3X
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N. Factor N N= FACTOR_N +1. FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.244 0x1840 CSI Clock Register (Default Value: 0x0000_0003)

Offset: 0x1840			Register Name: CSI_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CSI_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON CSI_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: VIDEO2PLL4X 001: DEPLL4X 010: PERI0_480M 011: PERI0_400M 100: PERI0_600M 101: VIDEO0PLL4X 110: VIDEO1PLL4X
23:5	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1840			Register Name: CSI_CLK_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x3	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.245 0x1844 CSI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x1844			Register Name: CSI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	CSI_RST. CSI Reset 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	CSI_GATING. Gating Clock for CSI 0: Mask 1: Pass

4.1.6.246 0x1860 ISP Clock Register (Default Value: 0x0000_0003)

Offset: 0x1860			Register Name: ISP_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	ISP_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON ISP_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: VIDEO2PLL4X 001: PERI0_480M 010: PERI0_400M 011: PERI0_600M 100: VIDEO0PLL4X 101: VIDEO1PLL4X
23:5	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1860			Register Name: ISP_CLK_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x3	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.247 0x1884 VIDEO_IN Bus Gating Reset Register (Default Value: 0x0001_0000)

Offset: 0x1884			Register Name: VIDEO_IN_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x1	VIDEO_IN_RST VIDEO_IN Reset 0: Assert 1: DE-assert
15:0	/	/	/

4.1.6.248 0x1904 DDRPLL Gate Enable Register (Default Value: 0x0001_0001)

Offset: 0x1904			Register Name: DDRPLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x1	DDRPLL_GATE_SW_CFG. DDRPLL Clock Gate Enable. 0: Disable 1: Enable
15:1	/	/	/
0	R/W	0x1	DDRPLL_AUTO_GATE_EN. DDRPLL Clock Auto Gate Enable. 0: Auto 1: No-Auto

4.1.6.249 0x1908 PERI0PLL Gate Enable Register (Default Value: 0x8FFF_0FFF)

Offset: 0x1908			Register Name: PERI0PLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	PERI0_300M_DSP_GATE_EN. PERI0_300M for DSP Clock Gate Enable. 0: Disable 1: Enable
30:28	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1908			Register Name: PERI0PLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
27	R/W	0x1	PERI0PLL2X_GATE_SW_CFG. PERI0PLL2X Clock Gate Enable. 0: Disable 1: Enable
26	R/W	0x1	PERI0_800M_GATE_SW_CFG. PERI0 800M Clock Gate Enable. 0: Disable 1: Enable
25	R/W	0x1	PERI0_600M_GATE_SW_CFG. PERI0 600M Clock Gate Enable. 0: Disable 1: Enable
24	R/W	0x1	PERI0_480M_GATE_ALL_CFG. PERI0 480M Clock Gate Enable. 0: Disable 1: Enable
23	R/W	0x1	PERI0_480M_GATE_SW_CFG. PERI0 480M Clock Gate Enable. 0: Disable 1: Enable
22	R/W	0x1	PERI0_160M_GATE_SW_CFG. PERI0 160M Clock Gate Enable. 0: Disable 1: Enable
21	R/W	0x1	PERI0_300M_GATE_ALL_CFG. PERI0 300M Clock Gate Enable. 0: Disable 1: Enable
20	R/W	0x1	PERI0_300M_GATE_SW_CFG. PERI0 300M Clock Gate Enable. 0: Disable 1: Enable
19	R/W	0x1	PERI0_150M_GATE_SW_CFG. PERI0 150M Clock Gate Enable. 0: Disable 1: Enable
18	R/W	0x1	PERI0_400M_GATE_ALL_CFG. PERI0 400M Clock Gate Enable. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1908			Register Name: PERI0PLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
17	R/W	0x1	PERI0_400M_GATE_SW_CFG. PERI0 400M Clock Gate Enable. 0: Disable 1: Enable
16	R/W	0x1	PERI0_200M_GATE_SW_CFG. PERI0 200M Clock Gate Enable. 0: Disable 1: Enable
15:12	/	/	/
11	R/W	0x1	PERI0PLL2X_AUTO_GATE_EN. PERI0PLL2X Clock Auto Gate Enable. 0: Auto 1: No-Auto
10	R/W	0x1	PERI0_800M_AUTO_GATE_EN. PERI0 800M Clock Auto Gate Enable. 0: Auto 1: No-Auto
9	R/W	0x1	PERI0_600M_AUTO_GATE_EN. PERI0 600M Clock Auto Gate Enable. 0: Auto 1: No-Auto
8	R/W	0x1	PERI0_480M_AUTO_GATE_EN_ALL. PERI0 480M Clock Auto Gate Enable. 0: Auto 1: No-Auto
7	R/W	0x1	PERI0_480M_AUTO_GATE_EN. PERI0 480M Clock Auto Gate Enable. 0: Auto 1: No-Auto
6	R/W	0x1	PERI0_160M_AUTO_GATE_EN. PERI0 160M Clock Auto Gate Enable. 0: Auto 1: No-Auto
5	R/W	0x1	PERI0_300M_AUTO_GATE_EN_ALL. PERI0 300M Clock Auto Gate Enable. 0: Auto 1: No-Auto
4	R/W	0x1	PERI0_300M_AUTO_GATE_EN. PERI0 300M Clock Auto Gate Enable. 0: Auto 1: No-Auto

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1908			Register Name: PERI0PLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
3	R/W	0x1	PERI0_150M_AUTO_GATE_EN. PERI0 150M Clock Auto Gate Enable. 0: Auto 1: No-Auto
2	R/W	0x1	PERI0_400M_AUTO_GATE_EN_ALL. PERI0 400M Clock Auto Gate Enable All. 0: Auto 1: No-Auto
1	R/W	0x1	PERI0_400M_AUTO_GATE_EN. PERI0 400M Clock Auto Gate Enable. 0: Auto 1: No-Auto
0	R/W	0x1	PERI0_200M_AUTO_GATE_EN. PERI0 200M Clock Auto Gate Enable. 0: Auto 1: No-Auto

4.1.6.250 0x190C PERI1PLL Gate Enable Register (Default Value: 0x8FFF_0FFF)

Offset: 0x190C			Register Name: PERI1PLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	PERI1_300M_DSP_GATE_EN. PERI1_300M for DSP Clock Gate Enable. 0: Disable 1: Enable
30:28	/	/	/
27	R/W	0x1	PERI1_800M_GATE_SW_CFG. PERI1 800M Clock Gate Enable. 0: Disable 1: Enable
26	R/W	0x1	PERI1_600M_GATE_ALL_CFG. PERI1 600M Clock Gate Enable. 0: Disable 1: Enable
25	R/W	0x1	PERI1_600M_GATE_SW_CFG. PERI1 600M Clock Gate Enable. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x190C			Register Name: PERI1PLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
24	R/W	0x1	PERI1_480M_GATE_ALL_CFG. PERI1 480M Clock Gate Enable. 0: Disable 1: Enable
23	R/W	0x1	PERI1_480M_GATE_SW_CFG. PERI1 480M Clock Gate Enable. 0: Disable 1: Enable
22	R/W	0x1	PERI1_160M_GATE_SW_CFG. PERI1 160M Clock Gate Enable. 0: Disable 1: Enable
21	R/W	0x1	PERI1_300M_GATE_ALL_CFG. PERI1 300M Clock Gate Enable. 0: Disable 1: Enable
20	R/W	0x1	PERI1_300M_GATE_SW_CFG. PERI1 300M Clock Gate Enable. 0: Disable 1: Enable
19	R/W	0x1	PERI1_150M_GATE_SW_CFG. PERI1 150M Clock Gate Enable. 0: Disable 1: Enable
18	R/W	0x1	PERI1_400M_GATE_ALL_CFG. PERI1 400M Clock Gate Enable. 0: Disable 1: Enable
17	R/W	0x1	PERI1_400M_GATE_SW_CFG. PERI1 400M Clock Gate Enable. 0: Disable 1: Enable
16	R/W	0x1	PERI1_200M_GATE_SW_CFG. PERI1 200M Clock Gate Enable. 0: Disable 1: Enable
15:12	/	/	/
11	R/W	0x1	PERI1_800M_AUTO_GATE_EN. PERI1 800M Clock Auto Gate Enable. 0: Auto 1: No-Auto

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x190C			Register Name: PERI1PLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
10	R/W	0x1	PERI1_600M_AUTO_GATE_EN_ALL. PERI1 600M Clock Auto Gate Enable. 0: Auto 1: No-Auto
9	R/W	0x1	PERI1_600M_AUTO_GATE_EN. PERI1 600M Clock Auto Gate Enable. 0: Auto 1: No-Auto
8	R/W	0x1	PERI1_480M_AUTO_GATE_EN_ALL. PERI1 480M Clock Auto Gate Enable. 0: Auto 1: No-Auto
7	R/W	0x1	PERI1_480M_AUTO_GATE_EN. PERI1 480M Clock Auto Gate Enable. 0: Auto 1: No-Auto
6	R/W	0x1	PERI1_160M_AUTO_GATE_EN. PERI1 160M Clock Auto Gate Enable. 0: Auto 1: No-Auto
5	R/W	0x1	PERI1_300M_AUTO_GATE_EN_ALL. PERI1 300M Clock Auto Gate Enable. 0: Auto 1: No-Auto
4	R/W	0x1	PERI1_300M_AUTO_GATE_EN. PERI1 300M Clock Auto Gate Enable. 0: Auto 1: No-Auto
3	R/W	0x1	PERI1_150M_AUTO_GATE_EN. PERI1 150M Clock Auto Gate Enable. 0: Auto 1: No-Auto
2	R/W	0x1	PERI1_400M_AUTO_GATE_EN_ALL. PERI1 400M Clock Auto Gate Enable All. 0: Auto 1: No-Auto
1	R/W	0x1	PERI1_400M_AUTO_GATE_EN. PERI1 400M Clock Auto Gate Enable. 0: Auto 1: No-Auto

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x190C			Register Name: PERI1PLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x1	PERI1_200M_AUTO_GATE_EN. PERI1 200M Clock Auto Gate Enable. 0: Auto 1: No-Auto

4.1.6.251 0x1910 VIDEOPLL Gate Enable Register (Default Value: 0x0077_0077)

Offset: 0x1910			Register Name: VIDEOPLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
31:23	/	/	/
22	R/W	0x1	VIDEO2PLL3X_GATE_SW_CFG. VIDEO2PLL3X Clock Gate Enable. 0: Disable 1: Enable
21	R/W	0x1	VIDEO1PLL3X_GATE_SW_CFG. VIDEO1PLL3X Clock Gate Enable. 0: Disable 1: Enable
20	R/W	0x1	VIDEO0PLL3X_GATE_SW_CFG. VIDEO0PLL3X Clock Gate Enable. 0: Disable 1: Enable
19	/	/	/
18	R/W	0x1	VIDEO2PLL4X_GATE_SW_CFG. VIDEO2PLL4X Clock Gate Enable. 0: Disable 1: Enable
17	R/W	0x1	VIDEO1PLL4X_GATE_SW_CFG. VIDEO1PLL4X Clock Gate Enable. 0: Disable 1: Enable
16	R/W	0x1	VIDEO0PLL4X_GATE_SW_CFG. VIDEO0PLL4X Clock Gate Enable. 0: Disable 1: Enable
15:7	/	/	/
6	R/W	0x1	VIDEO2PLL3X_AUTO_GATE_EN. VIDEO2PLL3X Clock Auto Gate Enable. 0: Auto 1: No-Auto

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1910			Register Name: VIDEOPLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
5	R/W	0x1	VIDEO1PLL3X_AUTO_GATE_EN. VIDEO1PLL3X Clock Auto Gate Enable. 0: Auto 1: No-Auto
4	R/W	0x1	VIDEO0PLL3X_AUTO_GATE_EN. VIDEO0PLL3X Clock Auto Gate Enable. 0: Auto 1: No-Auto
3	/	/	/
2	R/W	0x1	VIDEO2PLL4X_AUTO_GATE_EN. VIDEO2PLL4X Clock Auto Gate Enable. 0: Auto 1: No-Auto
1	R/W	0x1	VIDEO1PLL4X_AUTO_GATE_EN. VIDEO1PLL4X Clock Auto Gate Enable. 0: Auto 1: No-Auto
0	R/W	0x1	VIDEO0PLL4X_AUTO_GATE_EN. VIDEO0PLL4X Clock Auto Gate Enable. 0: Auto 1: No-Auto

4.1.6.252 0x1914 GPUPLL Gate Enable Register (Default Value: 0x0001_0001)

Offset: 0x1914			Register Name: GPUPLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x1	GPU0PLL_GATE_SW_CFG. GPU0PLLClock Gate Enable. 0: Disable 1: Enable
15:1	/	/	/
0	R/W	0x1	GPU0PLL_AUTO_GATE_EN. GPU0PLL Clock Auto Gate Enable. 0: Auto 1: No-Auto

4.1.6.253 0x1918 VEPLL Gate Enable Register (Default Value: 0x0003_0003)

Offset: 0x1918	Register Name: VEPLL_GATE_EN_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x1	VE1PLL_GATE_SW_CFG. VE1PLLClock Gate Enable. 0: Disable 1: Enable
16	R/W	0x1	VE0PLL_GATE_SW_CFG. VE0PLLClock Gate Enable. 0: Disable 1: Enable
15:2	/	/	/
1	R/W	0x1	VE1PLL_AUTO_GATE_EN. VE1PLL Clock Auto Gate Enable. 0: Auto 1: No-Auto
0	R/W	0x1	VE0PLL_AUTO_GATE_EN. VE0PLL Clock Auto Gate Enable. 0: Auto 1: No-Auto

4.1.6.254 0x191C AUDIOPLL Gate Enable Register (Default Value: 0x0007_0007)

Offset: 0x191C			Register Name: AUDIOPLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x1	AUDIO1PLL_DIV5_GATE_SW_CFG. AUDIO1PLL_DIV5 Gate Enable. 0: Disable 1: Enable
17	R/W	0x1	AUDIO1PLL_DIV2_GATE_SW_CFG. AUDIO1PLL_DIV2 Gate Enable. 0: Disable 1: Enable
16	R/W	0x1	AUDIO0PLL4X_GATE_SW_CFG. AUDIO0PLL4X Gate Enable. 0: Disable 1: Enable
15:3	/	/	/
2	R/W	0x1	AUDIO1PLL_DIV5_AUTO_GATE_EN. AUDIO1PLL_DIV5 Clock Auto Gate Enable. 0: Auto 1: No-Auto

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x191C			Register Name: AUDIOPLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x1	AUDIO1PLL_DIV2_AUTO_GATE_EN. AUDIO1PLL_DIV2 Clock Auto Gate Enable. 0: Auto 1: No-Auto
0	R/W	0x1	AUDIO0PLL4X_AUTO_GATE_EN. AUDIO0PLL4X Clock Auto Gate Enable. 0: Auto 1: No-Auto

4.1.6.255 0x1920 NPUPLL Gate Enable Register (Default Value: 0x0001_0001)

Offset: 0x1920			Register Name: NPUPLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x1	NPUPLL_GATE_SW_CFG. NPUPLL Gate Enable. 0: Disable 1: Enable
15:1	/	/	/
0	R/W	0x1	NPUPLL_AUTO_GATE_EN. NPUPLL Clock Auto Gate Enable. 0: Auto 1: No-Auto

4.1.6.256 0x1928 DEPLL Gate Enable Register (Default Value: 0x0003_0003)

Offset: 0x1928			Register Name: DEPLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x1	DEPLL3X_GATE_SW_CFG. DEPLL3X Clock Gate Enable. 0: Disable 1: Enable
16	R/W	0x1	DEPLL4X_GATE_SW_CFG. DEPLL4X Clock Gate Enable. 0: Disable 1: Enable
15:2	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1928			Register Name: DEPLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x1	DEPLL3X_AUTO_GATE_EN. DEPLL3X Clock Auto Gate Enable. 0: Auto 1: No-Auto
0	R/W	0x1	DEPLL4X_AUTO_GATE_EN. DEPLL4X Clock Auto Gate Enable. 0: Auto 1: No-Auto

4.1.6.257 0x1984 DDRPLL Gate Status Register (Default Value: 0x0001_0000)

Offset: 0x1984			Register Name: DDRPLL_GATE_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R	0x1	DDRPLL_GATE_STAT. DDRPLL Clock Gate Status. 0: Disable 1: Enable
15:0	/	/	/

4.1.6.258 0x1988 PERI0PLL Gate Status Register (Default Value: 0x0FFF_0000)

Offset: 0x1988			Register Name: PERI0PLL_GATE_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R	0x1	PERI0PLL2X_GATE_STAT. PERI0PLL2X Clock Gate Status. 0: Disable 1: Enable
26	R	0x1	PERI0_800M_GATE_STAT. PERI0 800M Clock Gate Status. 0: Disable 1: Enable
25	R	0x1	PERI0_600M_GATE_STAT. PERI0 600M Clock Gate Status. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1988			Register Name: PERI0PLL_GATE_STAT_REG
Bit	Read/Write	Default/Hex	Description
24	R	0x1	PERI0_480M_GATE_ALL_STAT. PERI0 480M Clock Gate Status. 0: Disable 1: Enable
23	R	0x1	PERI0_480M_GATE_STAT. PERI0 480M Clock Gate Status. 0: Disable 1: Enable
22	R	0x1	PERI0_160M_GATE_STAT. PERI0 160M Clock Gate Status. 0: Disable 1: Enable
21	R	0x1	PERI0_300M_GATE_ALL_STAT. PERI0 300M Clock Gate Status. 0: Disable 1: Enable
20	R	0x1	PERI0_300M_GATE_STAT. PERI0 300M Clock Gate Status. 0: Disable 1: Enable
19	R	0x1	PERI0_150M_GATE_STAT. PERI0 150M Clock Gate Status. 0: Disable 1: Enable
18	R	0x1	PERI0_400M_GATE_ALL_STAT. PERI0 400M Clock Gate Status. 0: Disable 1: Enable
17	R	0x1	PERI0_400M_GATE_STAT. PERI0 400M Clock Gate Status. 0: Disable 1: Enable
16	R	0x1	PERI0_200M_GATE_STAT. PERI0 200M Clock Gate Status. 0: Disable 1: Enable
15:0	/	/	/

4.1.6.259 0x198C PERI1PLL Gate Status Register (Default Value: 0x0FFF_0000)

Offset: 0x198C	Register Name: PERI1PLL_GATE_STAT_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R	0x1	PERI1_800M_GATE_STAT. PERI1 800M Clock Gate Status. 0: Disable 1: Enable
26	R	0x1	PERI1_600M_GATE_ALL_STAT. PERI1 600M Clock Gate Status. 0: Disable 1: Enable
25	R	0x1	PERI1_600M_GATE_STAT. PERI1 600M Clock Gate Status. 0: Disable 1: Enable
24	R	0x1	PERI1_480M_GATE_ALL_STAT. PERI1 480M Clock Gate Status. 0: Disable 1: Enable
23	R	0x1	PERI1_480M_GATE_STAT. PERI1 480M Clock Gate Status. 0: Disable 1: Enable
22	R	0x1	PERI1_160M_GATE_STAT. PERI1 160M Clock Gate Status. 0: Disable 1: Enable
21	R	0x1	PERI1_300M_GATE_ALL_STAT. PERI1 300M Clock Gate Status. 0: Disable 1: Enable
20	R	0x1	PERI1_300M_GATE_STAT. PERI1 300M Clock Gate Status. 0: Disable 1: Enable
19	R	0x1	PERI1_150M_GATE_STAT. PERI1 150M Clock Gate Status. 0: Disable 1: Enable
18	R	0x1	PERI1_400M_GATE_ALL_STAT. PERI1 400M Clock Gate Status. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

17	R	0x1	PERI1_400M_GATE_STAT. PERI1 400M Clock Gate Status. 0: Disable 1: Enable
16	R	0x1	PERI1_200M_GATE_STAT. PERI1 200M Clock Gate Status. 0: Disable 1: Enable
15:0	/	/	/

4.1.6.260 0x1990 VIDEOPLL Gate Status Register (Default Value: 0x0077_0000)

Offset: 0x1990			Register Name: VIDEOPLL_GATE_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:23	/	/	/
22	R	0x1	VIDEO2PLL3X_GATE_STAT. VIDEO2PLL3X Clock Gate Status. 0: Disable 1: Enable
21	R	0x1	VIDEO1PLL3X_GATE_STAT. VIDEO1PLL3X Clock Gate Status. 0: Disable 1: Enable
20	R	0x1	VIDEO0PLL3X_GATE_STAT. VIDEO0PLL3X Clock Gate Status. 0: Disable 1: Enable
19	/	/	/
18	R	0x1	VIDEO2PLL4X_GATE_STAT. VIDEO2PLL4X Clock Gate Status. 0: Disable 1: Enable
17	R	0x1	VIDEO1PLL4X_GATE_STAT. VIDEO1PLL4X Clock Gate Status. 0: Disable 1: Enable
16	R	0x1	VIDEO0PLL4X_GATE_STAT. VIDEO0PLL4X Clock Gate Status. 0: Disable 1: Enable
15:0	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.261 0x1994 GPUPLL Gate Status Register (Default Value: 0x0001_0000)

Offset: 0x1994			Register Name: GPUPLL_GATE_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R	0x1	GPU0PLL_GATE_STAT. GPU0PLL Clock Gate Status. 0: Disable 1: Enable
15:0	/	/	/

4.1.6.262 0x1998 VEPLL Gate Status Register (Default Value: 0x0003_0000)

Offset: 0x1998			Register Name: VEPLL_GATE_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R	0x1	VE1PLL_GATE_STAT. VE1PLL Clock Gate Status. 0: Disable 1: Enable
16	R	0x1	VE0PLL_GATE_STAT. VE0PLL Clock Gate Status. 0: Disable 1: Enable
15:0	/	/	/

4.1.6.263 0x199C AUDIOPLL Gate Status Register (Default Value: 0x0007_0000)

Offset: 0x199C			Register Name: AUDIOPLL_GATE_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R	0x1	AUDIO1PLL_DIV5_GATE_STAT. AUDIO1PLL_DIV5 Clock Gate Status. 0: Disable 1: Enable
17	R	0x1	AUDIO1PLL_DIV2_GATE_STAT. AUDIO1PLL_DIV2 Clock Gate Status. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x199C			Register Name: AUDIOPLL_GATE_STAT_REG
Bit	Read/Write	Default/Hex	Description
16	R	0x1	AUDIO0PLL4X_GATE_STAT. AUDIO0PLL4X Clock Gate Status. 0: Disable 1: Enable
15:0	/	/	/

4.1.6.264 0x19A0 NPUPLL Gate Status Register (Default Value: 0x0001_0000)

Offset: 0x19A0			Register Name: NPUPLL_GATE_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R	0x1	NPUPLL_GATE_STAT. NPUPLL Clock Gate Status. 0: Disable 1: Enable
15:0	/	/	/

4.1.6.265 0x19A8 DEPLL Gate Status Register (Default Value: 0x0003_0000)

Offset: 0x19A8			Register Name: DEPLL_GATE_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R	0x1	DEPLL3X_GATE_STAT. DEPLL3X Clock Gate Status. 0: Disable 1: Enable
16	R	0x1	DEPLL4X_GATE_STAT. DEPLL4X Clock Gate Status. 0: Disable 1: Enable
15:0	/	/	/

4.1.6.266 0x1A00 CLK24M Gate Enable Register (Default Value: 0x0000_0008)

Offset: 0x1A00			Register Name: CLK24M_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1A00			Register Name: CLK24M_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
3	R/W	0x1	RES_DCAP_24M_GATE_EN. RES_DCAP 24M Clock Gate Enable. 0: Disable 1: Enable
2:0	/	/	/

4.1.6.267 0x1B00 CM VI Enable Configuration Register (Default Value: 0x0002_0000)

Offset: 0x1B00			Register Name: CM_VI_CFG_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17:16	R	0x2	CM_VI_STATUS CM VI Status 01: Power OFF 10: Power ON
15:1	/	/	/
0	R/W	0x0	CM_VI_MODULE_MODE CM VI module mode 0: Disable 1: Enable

4.1.6.268 0x1B04 CM DESYS Enable Configuration Register (Default Value: 0x0002_0000)

Offset: 0x1B04			Register Name: CM_DESYS_CFG_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17:16	R	0x2	CM_DESYS_STATUS CM DESYS Status 01: Power OFF 10: Power ON
15:1	/	/	/
0	R/W	0x0	CM_DESYS_MODULE_MODE CM DESYS module mode 0: Disable 1: Enable

4.1.6.269 0x1B10 CM VE_DEC Enable Configuration Register (Default Value: 0x0002_0000)

Offset: 0x1B10			Register Name: CM_VE_DEC_CFG_REG
Bit	R/W	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1B10			Register Name: CM_VE_DEC_CFG_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17:16	R	0x2	CM_VE_DEC_STATUS CM VE_DEC Status 01: Power OFF 10: Power ON
15:1	/	/	/
0	R/W	0x0	CM_VE_DEC_MODULE_MODE CM VE_DEC module mode 0: Disable 1: Enable

4.1.6.270 0x1B14 CM VE_ENC Enable Configuration Register (Default Value: 0x0002_0000)

Offset: 0x1B14			Register Name: CM_VE_ENC_CFG_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17:16	R	0x2	CM_VE_ENC_STATUS CM VE_ENC Status 01: Power OFF 10: Power ON
15:1	/	/	/
0	R/W	0x0	CM_VE_ENC_MODULE_MODE CM VE_ENC module mode 0: Disable 1: Enable

4.1.6.271 0x1B1C CM NPU Enable Configuration Register (Default Value: 0x0002_0000)

Offset: 0x1B1C			Register Name: CM_NPU_CFG_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17:16	R	0x2	CM_NPU_STATUS CM NPU Status 01: Power OFF 10: Power ON
15:1	/	/	/
0	R/W	0x0	CM_NPU_MODULE_MODE CM NPU module mode 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.272 0x1B28 CM PCIE0 Enable Configuration Register (Default Value: 0x0002_0000)

Offset: 0x1B28			Register Name: CM_PCIE0_CFG_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17:16	R	0x2	CM_PCIE0_STATUS CM PCIE0 Status 01: Power OFF 10: Power ON
15:1	/	/	/
0	R/W	0x0	CM_PCIE0_MODULE_MODE CM PCIE0 module mode 0: Disable 1: Enable

4.1.6.273 0x1B30 CM USB2 Enable Configuration Register (Default Value: 0x0002_0000)

Offset: 0x1B30			Register Name: CM_USB2_CFG_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17:16	R	0x2	CM_USB2_STATUS CM USB2 Status 01: Power OFF 10: Power ON
15:1	/	/	/
0	R/W	0x0	CM_USB2_MODULE_MODE CM USB2 module mode 0: Disable 1: Enable

4.1.6.274 0x1B34 CM VO Enable Configuration Register (Default Value: 0x0002_0000)

Offset: 0x1B34			Register Name: CM_VO_CFG_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17:16	R	0x2	CM_VO_STATUS CM VO Status 01: Power OFF 10: Power ON
15:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1B34			Register Name: CM_VO_CFG_REG
Bit	R/W	Default/Hex	Description
0	R/W	0x0	CM_VO_MODULE_MODE CM VO module mode 0: Disable 1: Enable

4.1.6.275 0x1B38 CM VO1 Enable Configuration Register (Default Value: 0x0002_0000)

Offset: 0x1B38			Register Name: CM_VO1_CFG_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17:16	R	0x2	CM_VO1_STATUS CM VO1 Status 01: Power OFF 10: Power ON
15:1	/	/	/
0	R/W	0x0	CM_VO1_MODULE_MODE CM VO1 module mode 0: Disable 1: Enable

4.1.6.276 0x1C00 APB2JTAG Clock Register (Default Value: 0x0000_0000)

Offset: 0x1C00			Register Name: APB2JTAG_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	APB2JTAG_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON APB2JTAG_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: SYS_CLK24M 001: RTC_32K 010: RC16M 011: PERI0_480M 100: PERI1_480M 101: PERI0_200M 110: PERI1_200M
23:5	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1C00			Register Name: APB2JTAG_CLK_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.

Note: apb2jtag_clk frequency should be no more than 200M.

4.1.6.277 0x1C04 APB2JTAG Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x1C04			Register Name: APB2JTAG_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	APB2JTAG_RST. APB2JTAG Reset 0: Assert 1: DE-assert
15:0	/	/	/

4.1.6.278 0x1F00 CCMU Security Switch Register (Default Value: 0x0000_0000)

Offset: 0x1F00			Register Name: CCMU_SEC_SWITCH_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	MBUS_SEC. MBUS clock register security. 0: Secure 1: Non-secure
1	R/W	0x0	BUS_SEC. Bus relevant registers security. 0: Secure 1: Non-secure
0	R/W	0x0	PLL_SEC. PLL relevant registers security. 0: Secure 1: Non-secure

4.1.6.279 0x1F10 SYSDAP REQ Control Register (Default Value: 0x0000_0001)

Offset: 0x1F10			Register Name: SYSDAP_REQ_CTRL_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1F10			Register Name: SYSDAP_REQ_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	SYSDAP_REQ_ENABLE. 0: Disable 1: Enable Note: enable sysdap set req to control ce and dapsys clock and reset

4.1.6.280 0x1F20 PLL Configuration0 Register (Default Value: 0x0000_0000)

Offset: 0x1F20			Register Name: PLL_CFG0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PLL_CONFIG0 PLL Control Reserved Register

4.1.6.281 0x1F24 PLL Configuration1 Register (Default Value: 0x0000_0000)

Offset: 0x1F24			Register Name: PLL_CFG1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PLL_CONFIG1 PLL Control Reserved Register

4.1.6.282 0x1F28 PLL Configuration2 Register (Default Value: 0x0000_0000)

Offset: 0x1F28			Register Name: PLL_CFG2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PLL_CONFIG2 PLL Control Reserved Register

4.1.6.283 0x1F30 CCMU FANOUT CLOCK GATE Register (Default Value: 0x0000_0000)

Offset: 0x1F30			Register Name: CCMU_FAN_GATE_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	CLK25M_EN. Gating for CLK25M. 0: Clock is OFF 1: Clock is ON

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1F30			Register Name: CCMU_FAN_GATE_REG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	CLK16M_EN. Gating for CLK16M. 0: Clock is OFF 1: Clock is ON
1	R/W	0x0	CLK12M_EN. Gating for CLK12M. 0: Clock is OFF 1: Clock is ON
0	R/W	0x0	CLK24M_EN. Gating for CLK24M. 0: Clock is OFF 1: Clock is ON

4.1.6.284 0x1F34 CLK27M FANOUT Register (Default Value: 0x0000_0000)

Offset: 0x1F34			Register Name: CLK27M_FAN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CLK27M_EN. Gating for CLK27M. 0: Clock is OFF 1: Clock is ON SCLK=Clock Source/M/N.
30:26	/	/	/
25:24	R/W	0x0	CLK27M_SCR_SEL. Clock Source Select. 000: VIDEO0PLL4X 001: VIDEO1PLL4X 010: VIDEO2PLL4X
23:13	/	/	/
12:8	R/W	0x0	CLK27M_DIV1. Factor N. N= FACTOR_N +1. FACTOR_M is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	CLK27M_DIV0. Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.6.285 0x1F38 PCLK FANOUT Register (Default Value: 0x0000_0000)

Offset: 0x1F38			Register Name: CLK_FAN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PCLK_DIV_EN. Gating for PCLK. 0: Clock is OFF 1: Clock is ON PCLK = APB0_CLK/M/N.
30:10	/	/	/
9:5	R/W	0x0	PCLK_DIV1. Factor N. N= FACTOR_N +1. FACTOR_N is from 0 to 31.
4:0	R/W	0x0	PCLK_DIV. Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

4.1.6.286 0x1F3C CCMU FANOUT Register (Default Value: 0x0000_0000)

Offset: 0x1F3C			Register Name: CCMU_FAN_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	CLK_FANOUT3_EN. Gating for CLK_FANOUT3. 0: Clock is OFF 1: Clock is ON
23	R/W	0x0	CLK_FANOUT2_EN. Gating for CLK_FANOUT2. 0: Clock is OFF 1: Clock is ON
22	R/W	0x0	CLK_FANOUT1_EN. Gating for CLK_FANOUT1. 0: Clock is OFF 1: Clock is ON
21	R/W	0x0	CLK_FANOUT0_EN. Gating for CLK_FANOUT0. 0: Clock is OFF 1: Clock is ON
20:12	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1F3C			Register Name: CCMU_FAN_REG
Bit	Read/Write	Default/Hex	Description
11:9	R/W	0x0	CLK_FANOUT3_SEL. Clock Fanout3 Select. 000: CLK32K_FANOUT (From SYSRTC) 001: CLK12M (From SYS_CLK24M/2) 010: CLK16M (From PERI0_160M/10) 011: CLK24M (From SYS_CLK24M) 100: CLK25M (From PERI0_150M/6) 101: CLK27M 110: PCLK The above seven clock can be selected to output through clock fanout3.
8:6	R/W	0x0	CLK_FANOUT2_SEL. Clock Fanout2 Select. 000: CLK32K_FANOUT (From SYSRTC) 001: CLK12M (From SYS_CLK24M/2) 010: CLK16M (From PERI0_160M/10) 011: CLK24M (From SYS_CLK24M) 100: CLK25M (From PERI0_150M/6) 101: CLK27M 110: PCLK The above seven clock can be selected to output through clock fanout2.
5:3	R/W	0x0	CLK_FANOUT1_SEL. Clock Fanout1 Select. 000: CLK32K_FANOUT (From SYSRTC) 001: CLK12M (From SYS_CLK24M/2) 010: CLK16M (From PERI0_160M/10) 011: CLK24M (From SYS_CLK24M) 100: CLK25M (From PERI0_150M/6) 101: CLK27M 110: PCLK The above seven clock can be selected to output through clock fanout1.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1F3C			Register Name: CCMU_FAN_REG
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x0	CLK_FANOUT0_SEL. Clock Fanout0 Select. 000: CLK32K_FANOUT (From SYSRTC) 001: CLK12M (From SYS_CLK24M/2) 010: CLK16M (From PERI0_160M/10) 011: CLK24M (From SYS_CLK24M) 100: CLK25M (From PERI0_150M/6) 101: CLK27M 110: PCLK The above seven clock can be selected to output through clock fanout0.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.2 Power Reset Clock Management (PRCM)

4.2.1 Overview

The Power Reset Clock Management (PRCM) module provides a versatile supporting multiple power-management techniques and manages the gating and enabling of the clocks to the device modules in CPUS domain.

The system-level reset management provides correct reset routing and sequencing when one or more devices are stacked together in the same package. The device-level reset management provides reset routing to relevant devices.

The PRCM has the following features:

- CPUS Clock Configuration
- APBS Clock Configuration
- CPUS Module Clock Configuration
- CPUS Module BUS Gating and Reset
- RAM configure Control

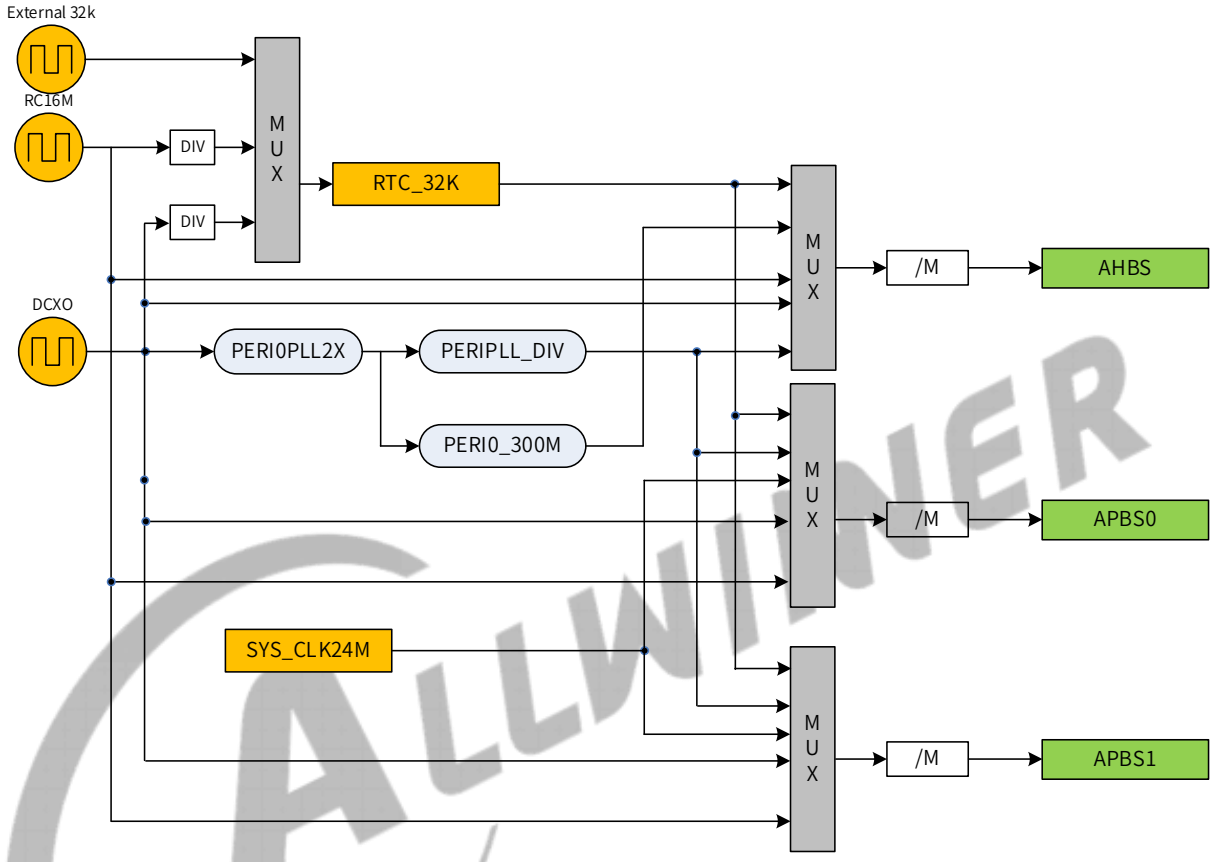
Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.2.2 Functional Description

4.2.2.1 Bus Clock Tree

The following figures show the diagram of the Bus Clock Tree Diagram.

Figure 4-3 Bus Clock Tree Diagram

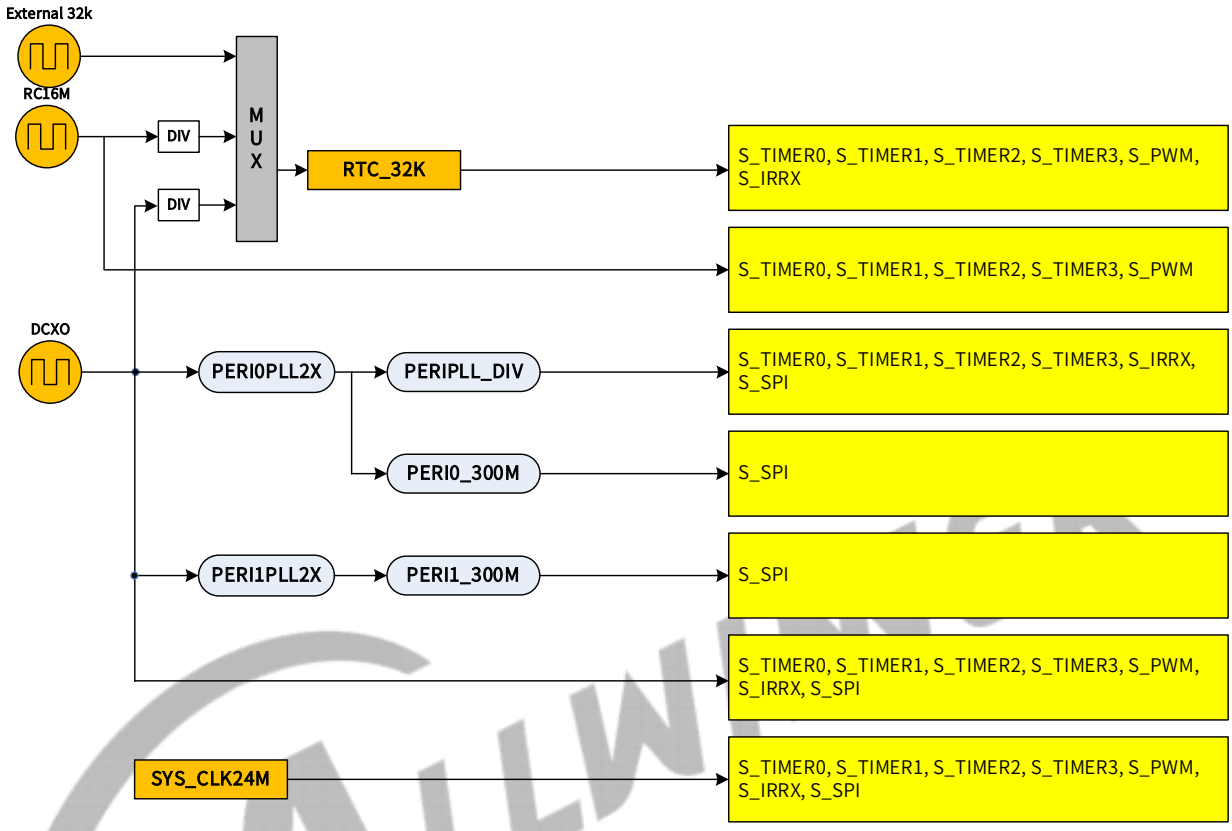


Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.2.2.2 Module Clock Tree

The following figures show a block diagram of the clock tree Diagram in CPUS domain.

Figure 4-4 Module Clock Tree Diagram



4.2.3 Programming Guidelines

4.2.3.1 Bus Clock Configuration

The bus clock supports dynamic switching, but the switching process needs to obey the following two rules.

- To switch from a lower frequency to a higher frequency: configure the frequency division factor first, and then switch the clock source.
- To switch from a higher frequency to a lower frequency: switch the clock source first, and then set the frequency division factor.

The bus frequencies are as follows.

- **AHBS:** The typical frequency is 200 MHz.
- **APBS0:** The typical frequency is 100 MHz.
- **APBS1:** The typical frequency is 24 MHz.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.2.3.2 Module Clock Configuration

For the bus gating reset register of a module, the reset bit is de-asserted first, and then the gating clock is enabled to avoid potential problems caused by the asynchronous release of the reset signal.

For all module clocks, configure the clock sources and frequency division factors first, and then write 1 to the gating clock. For the configuration order of the clock source and frequency division factor, follow the rules below:

- To switch from a lower frequency to a higher frequency: set the frequency division factor first, and then configure the clock source.
- To switch from a higher frequency to a lower frequency: configure the clock source first, and then set the frequency division factor.

4.2.4 Register List

The PRCM module includes two groups of registers:

Module Name	Base Address
STBY_PRCM	0x07010000

Register Name	Offset	Description
AHBS_CLK_REG	0x0000	AHBS Clock Register
APBS0_CLK_REG	0x000C	APBS0 Clock Register
APBS1_CLK_REG	0x0010	APBS1 Clock Register
S_TIMER0_CLK_REG	0x0100	S_TIMER0 Clock Register
S_TIMER1_CLK_REG	0x0104	S_TIMER1 Clock Register
S_TIMER2_CLK_REG	0x0108	S_TIMER2 Clock Register
S_TIMER3_CLK_REG	0x010C	S_TIMER3 Clock Register
S_TIMER_BGR_REG	0x011C	S_TIMER BUS GATING RESET Register
S_TWD_BGR_REG	0x012C	S_TWD BUS GATING RESET Register
S_PWM_CLK_REG	0x0130	S_PWM Clock Register
S_PWM_BGR_REG	0x013C	S_PWM BUS GATING RESET Register
S_SPI_CLK_REG	0x0150	S_SPI Clock Register
S_SPI_BGR_REG	0x015C	S_SPI BUS GATING RESET Register
S_MBOX_BGR_REG	0x017C	S_MBOX BUS GATING RESET Register
S_UART_BGR_REG	0x018C	S_UART BUS GATING RESET Register
S_TWI_BGR_REG	0x019C	S_TWI BUS GATING RESET Register
S_PPU_BGR_REG	0x01AC	S_PPU BUS GATING RESET Register
S_TZMA_BGR_REG	0x01B0	S_TZMA GATING RESET Register
S_CPUS_BIST_BGR_REG	0x01BC	S_CPUS_BIST BUS GATING RESET Register
S_IRRX_CLK_REG	0x01C0	S_IRRX Clock Register
S_IRRX_BGR_REG	0x01CC	S_IRRX BUS GATING RESET Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
RTC_BGR_REG	0x020C	RTC BUS GATING RESET Register
RISCV_24M_CLK_REG	0x0210	RISCV_24M Clock Register
RISCV_BGR_REG	0x021C	RISCV BUS GATING RESET Register
S_CPUCFG_BGR_REG	0x022C	S_CPUCFG BUS GATING RESET Register
PRCM_SEC_SWITCH_REG	0x0290	PRCM Security Switch Register
CPUX_ISO_CONFIG_REG	0x0294	CPUX Isolation Configuration Register
NMI_INT_CTRL_REG	0x0320	NMI Interrupt Control Register
NMI_INT_EN_REG	0x0324	NMI Interrupt Enable Register
NMI_INT_PEND_REG	0x0328	NMI Interrupt Pending Register
DEV_BUS_AUTOG_CTRL_REG	0x0338	DEV_BUS_AUTOG_CTRL Register
BUS_ACG_REG	0x033C	Bus Auto Clock Gating Register
MSRAMOC_CTRL_REG	0x0360	MSRAMOC Control Register
AHBS_RDY_TOUT_CTRL_REG	0x0368	AHBS Ready Timeout Control Register
JTAG_PAD_SEL_REG	0x037C	JTAG PAD Select Configuration Register
CPUX_ISO_EN_REG	0x03A0	CPUX ISO Enable Register
CRY_CONFIG_REG	0x03E0	Crypt Configuration Register
CRY_KEY_REG	0x03E4	Crypt Key Register
CRY_EN_REG	0x03E8	Crypt Enable Register

4.2.5 Register Description

4.2.5.1 0x0000 AHBS Clock Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: AHBS_CLK_REG
Bit	R/W	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	AHBS_CLK_SRC_SEL AHBS Clock Source Select 000: DCXO 001: RTC_32K 010: RC16M 011: PERIPLL_DIV (200MHz) 100: PERI0_300M Others: / AHBS_HCLK = Clock Source/M.
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Note: In the security mode, the register is a secure register by default, which can be only accessed by the secure host. The AHBS security control is realized by the bit0 in the 0x0290 register.

4.2.5.2 0x000C APBS0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: APBS0_CLK_REG
Bit	R/W	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	APBS0_CLK_SRC_SEL. APBS0 Clock Source Select. 000: DCXO 001: RTC_32K 010: RC16M 011: PERIPLL_DIV (200MHz) 100: SYS_CLK24M Others: / APBS0_CLK = Clock Source/M.
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31

Note: In the security mode, the register is a secure register by default, which can be only accessed by the secure host. The APBS0 security control is realized by the bit0 in the 0x0290 register.

4.2.5.3 0x0010 APBS1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: APBS1_CLK_REG
Bit	R/W	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	APBS1_CLK_SRC_SEL. APBS1 Clock Source Select. 000: DCXO 001: RTC_32K 010: RC16M 011: PERIPLL_DIV (200MHz) 100: SYS_CLK24M Others:/ APBS1_CLK = Clock Source/ M.
23:5	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0010			Register Name: APBS1_CLK_REG
Bit	R/W	Default/Hex	Description
4:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 31

Note: In the security mode, the register is a secure register by default, which can be only accessed by the secure host. The APBS1 security control is realized by the bit0 in the 0x0290 register.

4.2.5.4 0x0100 S_TIMER0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: S_TIMER0_CLK_REG
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	CLK_SRC_SEL. S_TIMER0 clock source select. 000: DCXO 001: RTC_32K 010: RC16M 011: PERIPLL_DIV (200MHz) 100: SYS_CLK24M
3:1	R/W	0x0	S_TIMER0_CLK_DIVN. Select the pre-scale of S_TIMER0 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 S_TIMER0_CLK = Clock Source/S_TIMER0_CLK_DIVN.
0	R/W	0x0	S_TIMER0_CLK_GATING Clock gating of S_TIMER0 0: Disable; 1: Enable

4.2.5.5 0x0104 S_TIMER1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: S_TIMER1_CLK_REG
Bit	R/W	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0104			Register Name: S_TIMER1_CLK_REG
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	CLK_SRC_SEL. S_TIMER1 clock source select. 000: DCXO 001: RTC_32K 010: RC16M 011: PERIPLL_DIV (200MHz) 100: SYS_CLK24M
3:1	R/W	0x0	S_TIMER1_CLK_DIVN. Select the pre-scale of S_TIMER1 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 S_TIMER1_CLK = Clock Source/S_TIMER1_CLK_DIVN.
0	R/W	0x0	S_TIMER1_CLK_GATING. Clock gating of S_TIMER1 0: Disable 1: Enable

4.2.5.6 0x0108 S_TIMER2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: S_TIMER2_CLK_REG
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	CLK_SRC_SEL. S_TIMER2 clock source select. 000: DCXO 001: RTC_32K 010: RC16M 011: PERIPLL_DIV (200MHz) 100: SYS_CLK24M

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0108			Register Name: S_TIMER2_CLK_REG
Bit	R/W	Default/Hex	Description
3:1	R/W	0x0	S_TIMER2_CLK_DIVN. Select the pre-scale of S_TIMER2 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 S_TIMER2_CLK = Clock Source/S_TIMER2_CLK_DIVN.
0	R/W	0x0	S_TIMER2_CLK_GATING. Clock gating of S_TIMER2 0: Disable 1: Enable

4.2.5.7 0x010C S_TIMER3 Clock Register (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: S_TIMER3_CLK_REG
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	CLK_SRC_SEL. S_TIMER3 clock source select. 000: DCXO 001: RTC_32K 010: RC16M 011: PERIPLL_DIV (200MHz) 100: SYS_CLK24M
3:1	R/W	0x0	S_TIMER3_CLK_DIVN. Select the pre-scale of S_TIMER3 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 S_TIMER3_CLK = Clock Source/S_TIMER3_CLK_DIVN.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x010C			Register Name: S_TIMER3_CLK_REG
Bit	R/W	Default/Hex	Description
0	R/W	0x0	S_TIMER3_CLK_GATING. Clock gating of S_TIMER3 0: Disable 1: Enable

4.2.5.8 0x011C S_TIMER BUS GATING RESET Register (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: S_TIMER_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	S_TIMER_RST. S_TIMER Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	S_TIMER_GATING. Gating Clock for S_TIMER. 0: Mask 1: Pass

4.2.5.9 0x012C S_TWD BUS GATING RESET Register (Default Value: 0x0000_0001)

Offset: 0x012C			Register Name: S_TWD_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	S_TWD_GATING. Gating Clock for S_TWD. 0: Mask 1: Pass

Note: The register is fixed to be a secure register.

4.2.5.10 0x0130 S_PWM Clock Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: S_PWM_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	S_PWM_CLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0130			Register Name: S_PWM_CLK_REG
Bit	Read/Write	Default/Hex	Description
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: DCXO 01: RTC_32K 10: RC16M 11: SYS_CLK24M S_PWM_CLK = Clock Source
23:0	/	/	/

4.2.5.11 0x013C S_PWM BUS GATING RESET Register (Default Value: 0x0000_0000)

Offset: 0x013C			Register Name: S_PWM_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	S_PWM_RST R_ PWM Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	S_PWM_GATING. Gating bus Clock for R_ PWM 0: Mask 1: Pass

4.2.5.12 0x0150 S_SPI Clock Register (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: S_SPI_CLK_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock. 0: Clock is OFF 1: Clock is ON S_SPI_CLK = Clock Source/M/N.
30:27	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0150			Register Name: S_SPI_CLK_REG
Bit	R/W	Default/Hex	Description
26:24	R/W	0x0	S_SPI_CLK_SRC_SEL. S_SPI Clock Source Select. 000: DCXO 001: PERIPLL_DIV (200MHz) 010: PERI0_300M 011: PERI1_300M 100: SYS_CLK24M
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N Factor N. N= FACTOR_N +1. FACTOR_N is from 0 to 31
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31

4.2.5.13 0x015C S_SPI BUS GATING RESET Register (Default Value: 0x0000_0000)

Offset: 0x015C			Register Name: S_SPI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	S_SPI_RST S_SPI Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	S_SPI_GATING. Gating Clock for S_SPI 0: Mask 1: Pass

4.2.5.14 0x017C S_MBOX BUS GATING RESET Register (Default Value: 0x0000_0000)

Offset: 0x017C			Register Name: S_MBOX_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x017C			Register Name: S_MBOX_BGR_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	S_MBOX_RST. S_MBOX Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	S_MBOX_GATING. Gating Clock for S_MBOX 0: Mask 1: Pass

4.2.5.15 0x018C S_UART BUS GATING RESET Register (Default Value: 0x0000_0000)

Offset: 0x018C			Register Name: S_UART_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	S_UART1_RST. S_UART1 Reset. 0: Assert 1: De-assert
16	R/W	0x0	S_UART0_RST. S_UART0 Reset. 0: Assert 1: De-assert
15:2	/	/	/
1	R/W	0x0	S_UART1_GATING. Gating Clock for S_UART1 0: Mask 1: Pass
0	R/W	0x0	S_UART0_GATING. Gating Clock for S_UART0 0: Mask 1: Pass

4.2.5.16 0x019C S_TWI BUS GATING RESET Register (Default Value: 0x0000_0000)

Offset: 0x019C			Register Name: S_TWI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x019C			Register Name: S_TWI_BGR_REG
Bit	Read/Write	Default/Hex	Description
18	R/W	0x0	S_TWI2_RST. S_TWI2 Reset. 0: Assert 1: De-assert
17	R/W	0x0	S_TWI1_RST. S_TWI1 Reset. 0: Assert 1: De-assert
16	R/W	0x0	S_TWI0_RST. S_TWI0 Reset. 0: Assert 1: De-assert
15:3	/	/	/
2	R/W	0x0	S_TWI2_GATING. Gating Clock for S_TWI2 0: Mask 1: Pass
1	R/W	0x0	S_TWI1_GATING. Gating Clock for S_TWI1 0: Mask 1: Pass
0	R/W	0x0	S_TWI0_GATING. Gating Clock for S_TWI0 0: Mask 1: Pass

4.2.5.17 0x01AC S_PPU BUS GATING RESET Register (Default Value: 0x0000_0001)

Offset: 0x01AC			Register Name: S_PPU_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	S_PPU_GATING. Gating Clock for S_PPU (PCK600). 0: Mask 1: Pass

4.2.5.18 0x01B0 S_TZMA GATING RESET Register (Default Value: 0x0000_0000)

Offset: 0x01B0			Register Name: S_TZMA_BGR_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x01B0			Register Name: S_TZMA_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	S_TZMA_GATING. Gating Clock for S_TZMA 0: Mask 1: Pass

4.2.5.19 0x01BC S_CPUS_BIST BUS GATING RESET Register (Default Value: 0x0000_0000)

Offset: 0x01BC			Register Name: S_CPUS_BIST_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	S_CPUS_BIST_GATING. Gating Clock for S_CPUS_BIST 0: Mask 1: Pass

4.2.5.20 0x01C0 S_IRRX Clock Register (Default Value: 0x0000_0000)

Offset: 0x01C0			Register Name: S_IRRX_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock. 0: Clock is OFF 1: Clock is ON S_IRRX_CLK = Clock Source/M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 00: RTC_32K 01: DCXO 10:SYS_CLK24M 11:/
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.2.5.21 0x01CC S_IRRX BUS GATING RESET Register (Default Value: 0x0000_0000)

Offset: 0x01CC			Register Name: S_IRRX_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	S_IRRX_RST S_IRRX Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	S_IRRX_GATING Gating Clock for S_IRRX 0: Mask 1: Pass

4.2.5.22 0x020C RTC BUS GATING RESET Register (Default Value: 0x0001_0001)

Offset: 0x020C			Register Name: RTC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x1	RTC_RST. RTC Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x1	RTC_GATING. Gating Clock for RTC. 0: Mask 1: Pass

4.2.5.23 0x0210 RISCV_24M Clock Register (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: RISCV_24M_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	RISCV_CLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON RISCV_24M_CLK = Clock Source.
30:26	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0210			Register Name: RISCV_24M_CLK_REG
Bit	Read/Write	Default/Hex	Description
25:24	R/W	0x0	RISCV_24M_CLK_SEL. Clock Source Select. 00: DCXO 01: RTC_32K 10: CLK16M_RC 11:/
23:0	/	/	/

4.2.5.24 0x021C RISCV BUS GATING RESET Register (Default Value: 0x0000_0000)

Offset: 0x021C			Register Name: RISCV_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	RISCV_CFG_RST. RISCV_CFG Reset. 0: Assert 1: De-assert
15:2	/	/	/
1	R/W	0x0	RISCV_CFG_GATING. Gating bus Clock for RISCV_CFG. 0: Clock is OFF 1: Clock is ON
0	R/W	0x0	RISCV_GATING. Gating bus Clock for RISCV. 0: Clock is OFF 1: Clock is ON

4.2.5.25 0x022C S_CPUCFG BUS GATING RESET Register (Default Value: 0x0001_0001)

Offset: 0x022C			Register Name: S_CPUCFG_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x1	S_CPUCFG_RST. S_CPUCFG Reset. 0: Assert 1: De-assert
15:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x022C			Register Name: S_CPUCFG_BGR_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x1	S_CPUCFG_GATING. Gating Clock for S_CPUCFG. 0: Mask 1: Pass

4.2.5.26 0x0290 PRCM Security Switch Register (Default Value: 0x0000_0000)

Offset: 0x0290			Register Name: PRCM_SEC_SWITCH_REG
Bit	R/W	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	POWER_SEC Power secure Power relevant registers' security, if the system is in non-security mode, this related registers are always non-security. 0: Secure 1: Non-secure Including: VDD_SYS power domain reset register, system domain power control register.
1	R/W	0x0	PLL_SEC PLL Secure PLL control relevant registers' security, if the system is in non-security mode, this related register are always non-security. 0: Secure 1: Non-secure Including: PLL control register 0/1.
0	R/W	0x0	CPUS BUS_CLK_SEC CPUS BUS Clock Secure CPUS BUS clock relevant registers' security, if the system is in non-security mode, this related register are always non-security. 0: Secure 1: Non-secure Including: AHBS configuration register, APBS0 configuration register, APBS1 configuration register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Note: In the security mode, the register is a secure register by default, which can be only accessed by the secure host. In the non-security mode, the secure control becomes invalid.

4.2.5.27 0x0294 CPUX Isolation Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0294			Register Name: CPUX_ISO_CONFIG_REG
Bit	R/W	Default/Hex	Description
31:14	/	/	/
13	R/W	0x0	CPUX_TZMA_ISO_EN CPUX TZMA Isolation Enable 0: Disable 1: Enable
12	R/W	0x0	CPUX_TWD_ISO_EN CPUX TWD Isolation Enable 0: Disable 1: Enable
11	R/W	0x0	CPUX_TWI2_ISO_EN CPUX TWI2 Isolation Enable 0: Disable 1: Enable
10	R/W	0x0	CPUX_TWI1_ISO_EN CPUX TWI1 Isolation Enable 0: Disable 1: Enable
9	R/W	0x0	CPUX_TWI0_ISO_EN CPUX TWI0 Isolation Enable 0: Disable 1: Enable
8	/	/	/
7	R/W	0x0	CPUX_UART1_ISO_EN CPUX UART1 Isolation Enable 0: Disable 1: Enable
6	R/W	0x0	CPUX_UART0_ISO_EN CPUX UART0 Isolation Enable 0: Disable 1: Enable
5	R/W	0x0	CPUX_GPIO_ISO_EN CPUX GPIO Isolation Enable 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0294			Register Name: CPUX_ISO_CONFIG_REG
Bit	R/W	Default/Hex	Description
4	R/W	0x0	CPUX_IRRX_ISO_EN CPUX IRRX Isolation Enable 0: Disablek 1: Enable
3	R/W	0x0	CPUX_PWM_ISO_EN CPUX PWM Isolation Enable 0: Disable 1: Enable
2	/	/	/
1	R/W	0x0	CPUX_SPI_ISO_EN. CPUX SPI Isolation Enable. 0: Disable 1: Enable
0	R/W	0x0	CPUX_RTC_ISO_EN CPUX RTC Isolation Enable 0: Disable 1: Enable

4.2.5.28 0x0320 NMI Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0320			Register Name: NMI_INT_CTRL_REG
Bit	R/W	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	NMI_SRC_TYPE. External NMI Interrupt Source Type. External NMI pins will trigger alarm signals if system is powered down. (NMI_SRC_TYPE is need to config before NMI irq is enable) 00: Low level sensitive 01: Negative edge trigged 10: High level sensitive 11: Positive edge sensitive

4.2.5.29 0x0324 NMI Interrupt Enable Register (Default Value: 0x8000_0000)

Offset: 0x0324			Register Name: NMI_INT_EN_REG
Bit	R/W	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0324			Register Name: NMI_INT_EN_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x1	NMI_INPUT_DET_EN NMI Input Detect Enable. 0: Disable 1: Enable
30:2	/	/	/
1	R/W	0x0	NMIIRQ_RV_EN. Interrupt nmi Enable Bits. 0: interrupt is disabled. 1: interrupt is enabled. When the interrupt is enabled, an NMI signal will be sent to RISC-V.
0	R/W	0x0	NMIIRQ_SYS_EN. Interrupt nmi Enable Bits. 0: interrupt is disabled. 1: interrupt is enabled. When the interrupt is enabled, an NMI signal will be sent to CPUX.

4.2.5.30 0x0328 NMI Interrupt Pending Register (Default Value: 0x0000_0000)

Offset: 0x0328			Register Name: NMI_INT_PEND_REG
Bit	R/W	Default/Hex	Description
31:1	/	/	/
0	R/W1C	0x0	NMI_IRQ_PEND. NMI IRQ Pending. Interrupt NMI Pending/Clear Bit. Set 1 to the bit will clear it. (after first enabling NMI irq function, must set this bit to 1 to clear the unexpected pending once) 0: Corresponding interrupt is not pending. 1: Corresponding interrupt is pending.

4.2.5.31 0x0338 DEV_BUS_AUTOG_CTRL Register (Default Value: 0x0000_0010)

Offset: 0x0338			Register Name: DEV_BUS_AUTOG_CTRL_REG
Bit	R/W	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0338			Register Name: DEV_BUS_AUTOG_CTRL_REG
Bit	R/W	Default/Hex	Description
31:24	R/W	0x0	CPUCLK_REC_DLY_TIME When LP mode exits, it is the delay time in the unit of PRCM clock during which OR1200 clock are resumed after peripherals and bus clocks are resumed. 0=256cycle, 1=1cycle,(p), 255=255cycle
23:21	/	/	/
20	R/W	0x0	LPI_OUT_SYNC_EN It is used to configure whether the LPI interface from OR1200 to PRCM is asynchronous or synchronous. 1: Asynchronous 0: Synchronous
19:12	/	/	/
11	R/W	0x0	LPI_IF_EN It is used to configure the LPI interface between OR1200 and PRCM. 1: Enable 0: Disable. When it is not disabled, the state of CPUS will not be transferred to PRCM.
10	R/W	0x0	LPI_IN_SYNC_EN It is used to configure the LPI interface from PRCM to OR1200. 1: Asynchronous 0: Synchronous
9	R/W	0x0	TT_AUTOGATE_EN It is used to enable R1200 ticktimer clock autogate. When it is enabled and pm_tt_o is set to 1, the ticktimer clock will be gated automatically.
8	R/W	0x0	CPU_ICACHE_AUTOGATE_EN It is used to enable the clocks in the OR1200 except ticktimer clock. When it is enabled, and pm_cpu_o and pm_icache_o are set to 1 simultaneously, the clocks of cpu, icache, qmem, and pm will be auto gated. 1: autogate enable 0: autogate disable
7:4	R	0x1	CPUS_LP_STAT pm_ic_gate, pm_cpu_gate, and cactive. It is the low-power state of CPUS, which indicates pm_tt_gate, pm_ic_gate, pm_cpu_gate, and cactive.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0338			Register Name: DEV_BUS_AUTOG_CTRL_REG
Bit	R/W	Default/Hex	Description
3:1	/	/	/
0	R/W	0x0	OR1200_CLKAUTG_EN When OR1200 enters the sleep mode, the auto gate of module bus or working clock will be enabled. 1: Enable 0: Disable

Note: In the security mode, the register is a secure register by default, which can be only accessed by the secure host. The AHBS security control is realized by the bit0 in the 0x0290 register.

4.2.5.32 0x033C Bus Auto Clock Gating Register (Default Value: 0x0000_0000)

Offset: 0x033C			Register Name: BUS_ACG_REG
Bit	R/W	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	AHBS_AUTO_CLK_GATE_EN AHBS bus auto clock gating function enable. 1: Enable auto clock gate 0: Disable auto clock gate
23:1	/	/	/
0	R/W	0x0	BM_ACG_MODE_EN BM Auto Clock Gating Mode Enable. AHBS bus matrix module auto clock gating mode enable, if this bit is 1 and AHBS auto clock gating function is enable, AHBS bus matrix module hclk will close when AHBS bus clock close.

Note: In the security mode, the register is a secure register by default, which can be only accessed by the secure host. Its security control is realized by the bit0 in the 0x0290 register.

4.2.5.33 0x0360 MSRAMOC Control Register (Default Value: 0x0000_0000)

Offset: 0x0360			Register Name: MSRAMOC_CTRL_REG
Bit	R/W	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	MSRAMOC_PORT_HOLD_EN MSRAMOC Port Hold Enable 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0360			Register Name: MSRAMOC_CTRL_REG
Bit	R/W	Default/Hex	Description
0	R/W	0x0	MSRAMOC_ACG_EN MSRAMOC Auto Clock Gating Enable 0: Disable 1: Enable

4.2.5.34 0x0368 AHBS Ready Timeout Control Register (Default Value: 0x0000_0000)

Offset: 0x0368			Register Name: AHBS_RDY_TOUT_CTRL_REG
Bit	R/W	Default/Hex	Description
31:25	/	/	/
24	R/W1C	0x0	AHBS_RDY_TIMEOUT_IRQ_PEND AHBS Hready Time Out Irq Pending. Write 1 Clear
23:9	/	/	/
8	R/W	0x0	AHBS_RDY_TIMEOUT_IRQ_EN. AHBS Hready Time Out Irq Enable. 1: Irq Enable 0: Irq Disable
7	R/W	0x0	AHBS_TIMEOUT_INT_VAL_SEL. AHBS Time Out Interval Value Select. 0: interval_value* 2^10 + 2^10 -1 1: interval_value* 2^16 + 2^16 -1
6:1	R/W	0x0	AHBS_TIMEOUT_CNT_INT_VAL. AHBS Time Out Counter Interval Value.
0	R/W	0x0	AHBS_RDY_TIMEOUT_EN. AHBS Hready Time Out Enable.

4.2.5.35 0x037C JTAG PAD Select Configuration Register (Default Value: 0x0000_0000)

Offset: 0x037C			Register Name: JTAG_PAD_SEL_REG
Bit	R/W	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	CPUS_JTAG_SEL. CPUS JTAG Select. 0: use cpus pad 1: use sys pad for secure debug
0	R/W	0x0	RISCV_JTAG_SEL. RISCV JTAG Select. 0: use cpus pad 1: use sys pad for secure debug

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.2.5.36 0x03A0 CPUX ISO Enable Register (Default Value: 0x0000_0000)

Offset: 0x03A0			Register Name: CPUX_ISO_EN_REG
Bit	R/W	Default/Hex	Description
31:16	W	0x0	KEY_FIELD This field should be filled with 0x1903, and then the bit 0 can be written with the new value.
15:1	/	/	/
0	R/W	0x0	CPUX_ISO_EN CPUX isolation enable. 1: Enable 0: Disable

4.2.5.37 0x03E0 Crypt Configuration Register (Default Value: 0x0000_0000)

Offset: 0x03E0			Register Name: CRY_CONFIG_REG
Bit	R/W	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	KEY_FIELD Key Field. If you want to read or write Crypt Key Register/Crypt Enable Register, you should write 0x1689 in these bits.

4.2.5.38 0x03E4 Crypt Key Register (Default Value: 0x0000_0000)

Offset: 0x03E4			Register Name: CRY_KEY_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	CRY_KEY Crypt Key.

4.2.5.39 0x03E8 Crypt Enable Register (Default Value: 0x0000_0000)

Offset: 0x03E8			Register Name: CRY_EN_REG
Bit	R/	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	CRY_EN Crypt enable. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

5 Processors

5.1 ARM Cortex A76 x2+Cortex A55 x6 Subsystem

5.1.1 Overview

The Cortex-A55 core is a mid-range, low-power core that implements the Armv8-A architecture with support for the Armv8.1-A extension, the Armv8.2-A extension, the RAS extension, the Load acquire (LDAPR) instructions introduced in the Armv8.3-A extension, and the dot product instructions introduced in the Armv8.4-A extension.

The Cortex-A76 core is a high-performance and low-power Arm product that implements the Armv8-A architecture.

The Cortex-A55 core includes the following features

- Core Features
  - Full implementation of the Armv8.2-AA64, A32, and T32 instruction sets.
  - Both the AArch32 and AArch64 execution states at all Exception levels (EL0 to EL3).
  - In-order pipeline with direct and indirect branch prediction.
  - Separate L1 data and instruction side memory systems with a Memory Management Unit (MMU).
  - Supports for Arm TrustZone® technology.
  - Optional Data Engine unit that implements the Advanced SIMD and floating-point architecture support.
  - Optional Cryptographic Extension. This architectural extension is only available if the Data Engine is present.
  - Generic Interrupt Controller (GIC) CPU interface to connect to an external distributor.
  - Generic Timers interface supporting 64-bit count input from an external system counter.
- Cache features
  - Optional unified private L2 cache.
  - L1 and L2 cache protection in the form of Error Correction Code (ECC) or parity on all RAM instances.

The Cortex-A76 core includes the following features:

- Core features
  - 40-bit Physical Address (PA).
  - A Memory Management Unit (MMU).

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- Optional Cryptographic Extension.
- Armv8.4 Dot Product instruction support.
- Superscalar, variable-length, out-of-order pipeline.
- Supports for Arm TrustZone® technology.
- Supports for Page-Based Hardware Attributes (PBHA).
- Reliability, Availability, and Serviceability (RAS) Extension.
- Full implementation of the Armv8.2-A A64, A32, and T32 instruction sets.
- Generic Interrupt Controller (GICv4) CPU interface to connect to an external distributor.
- Generic Timers interface supporting 64-bit count input from an external system counter.
- An integrated execution unit that implements the Advanced SIMD and floating-point architecture support.
- AArch32 Execution state at Exception level EL0 only. AArch64 Execution state at all Exception levels (EL0 to EL3).

- Cache features
  - Separate L1 data and instruction caches.
  - Private, unified data and instruction L2 cache.
  - Optional L1 and L2 memory protection in the form of Error Correcting Code (ECC) or parity on RAM instances which affect functionality.

The DSU includes the following features:

- AMBA ACE5 or AMBA 5 CHI main bus interface.
- Optional 128-bit wide I/O-coherent Accelerator Coherency Port (ACP).
- Optional 64-bit wide device peripheral port.
- Supports for cores with 40-bit, 44-bit, or 48-bit physical addresses.
- Armv8.2-A debug logic or (for compatible cores) Armv8.4-A debug logic.
- Supports Reliability, Availability, and Serviceability (RAS).
- Optional unified 16-way set-associative L3 cache.
- 64-byte cache lines throughout.
- Supports cache partitioning.
- Partial L3 cache power down support.
- Optional cache protection in the form of Error Correcting Code (ECC) on L3 cache RAM instances.
- Snoop Control Unit (SCU).

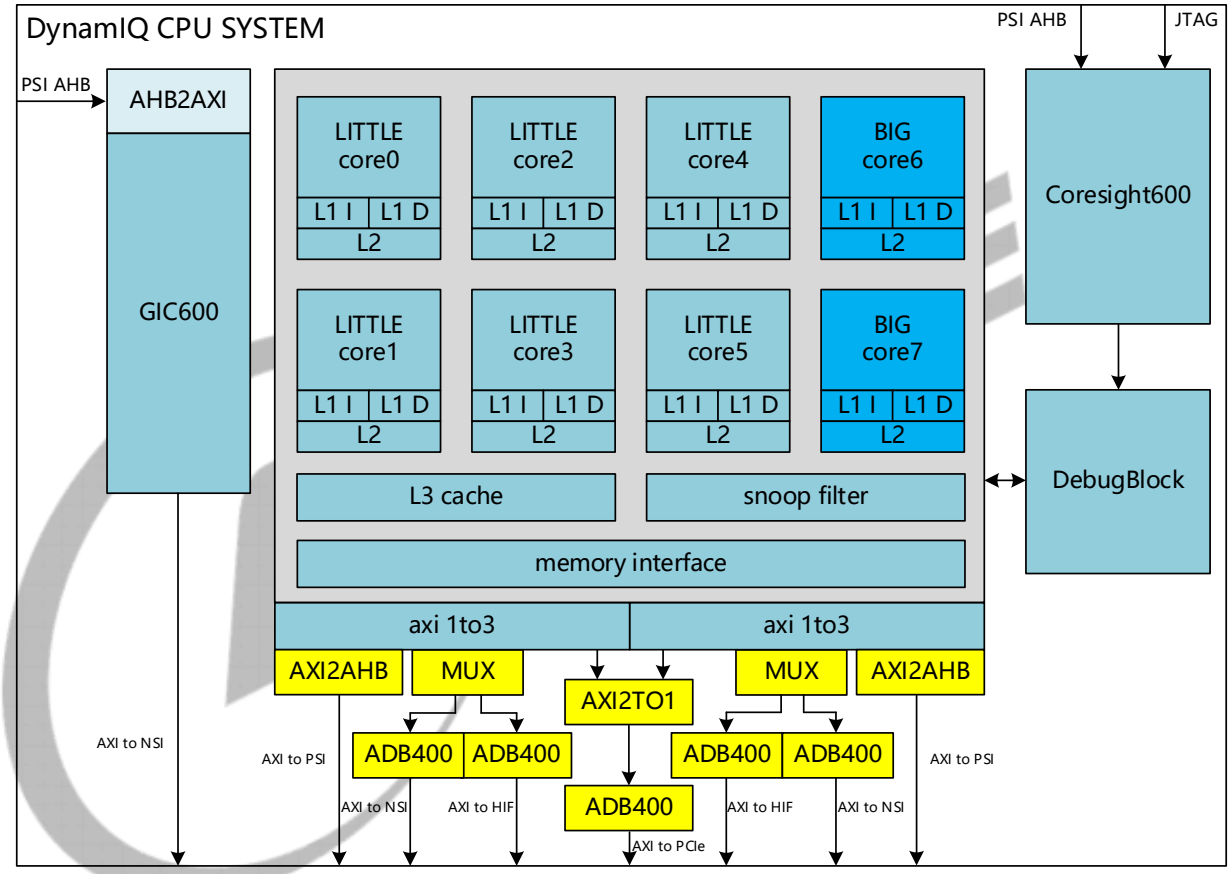
Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- L3 memory system can be clocked at a rate synchronous to the external system interconnect or at integer multiples.
- Armv8.2-A or Armv8.4-A architecture cores supported.
- Supports three types of cores.
- Cores can be clocked at different frequencies.

5.1.2 Block Diagram

The following figure shows the block diagram of CPUX system.

Figure 5-1 CPUX System Block Diagram



5.1.3 Functional Descriptions

5.1.3.1 Cortex-A55 Power Mode

The following table describes the Cortex-A55 Power Mode.

Table 5-1 Cortex-A55 Power Mode

Power Mode	Power Domain		Description
	PDCPU	PDADVSIMD	

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Power Mode	Power Domain		Description
	PDCPU	PDADVSIMD	
Debug Recovery	On	On	Core on. Adanced SIMD and floating-point block on. Block is active.
On	On	On	Core on. Adanced SIMD and floating-point block on. Block is active.
SIMD Dynamic Retention	On	Ret	Core on. Adanced SIMD and floating-point block in retention. Block is active.
Core Dynamic Retention	Ret	Ret	Core retention. Core logic and advanced SIMD and floating-point block in retention. Logic and RAM retention power only.
Off (emulated)	On	On	Core on. Advanced SIMD and floating-point block on. Block is active.
Off	Off	Off	Core off. Power to the block is gated.

5.1.3.2 Cortex-A76 Power Mode

The following table describes the Cortex-A76 Power Mode.

Table 5-2 Cortex-A76 Power Mode

Power Mode	Short Name	PACTIVE bit number	PATATE value	Power Mode Description
Debug recovery	DEBUG_RECOV	-	0b001010	Logic is off (or in reset). RAM state is retained and not invalidated when transitioning to On mode.
On	ON	8	0b001000	All power up.
Core dynamic retention	FULL_RET	5	0b000101	Logic and RAM state are inoperable but retained.
Emulated off	OFF_EMU	1	0b000001	On with Warm reset asserted, debug state is retained and accessible.
OFF	OFF	0 (implicit)	0b000000	All power down.

5.1.3.3 DSU Power Mode

The following table describes the DSU Power Mode.

Table 5-3 DSU Power Mode

Power Mode	Power Mode Description
On	All the cores and DSUs are available.
Functional Retention	L3 cache and snoop filter RAM can enter the retention state when L3 cache isn t accessed.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Power Mode	Power Mode Description
Memory Retention	L3 cache and snoop filter RAM can enter the retention state after cluster powers down. In this mode, cluster should be the only consistent device.
Off	Before powering down, data should be saved, and core or cluster should ensure its own data consistency.

5.1.3.4 PMU

The DynamIQ Shared Unit includes performance monitors that enable you to gather various statistics on the operation of the memory of the cluster during runtime. These provide useful information about the behavior of the cluster that you can use when debugging or profiling code.

The PMU provides six counters. Each counter can count any of the events available in the cluster. The absolute counts that are recorded might vary because of pipeline effects. This has negligible effect except in cases where the counters are enabled for a very short time.

The PMU includes the following interfaces and counters:

Event interface

Events from all other units across the design are provided to the PMU.

System register and APB interface

You can program the PMU registers using the system registers or external APB interface.

Counters

The PMU has 32-bit counters that increment when they are enabled based on events and a 64-bit cycle counter.

PMU register interface

DSU support access to the performance monitor registers from the internal system register interface.

5.1.4 Programming Guidelines

5.1.4.1 PLL Distribution

The whole CPU_SYS includes four PLLs, consisting of CPU_BACK_PLL, CPU_L_PLL, CPU_B_PLL, and CPU_DSU_PLL. The CPU_BACK_PLL is generated by the generic PLL, and the other three PLLs are generated by the linear PLLs.

The primary clock source of core0/core1/core2/core3/core4/core5 is CPU_L_PLL; and their backup clock source is 26MHz, CPU_BACK_PLL, and 1.2 GHz.

The primary clock source of core6/core7 is CPU_B_PLL; and their backup clock source is 26MHz, CPU_BACK_PLL, and 1.2 GHz.

The primary clock source of cluster is CPU_DSU_PLL; and their backup clock source is 26MHz, CPU_BACK_PLL, and 600 MHz.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

The clocks of core and cluster supports dynamic adjustment. The clock ratio of cluster directly influences the latency of access to L3. To meet a great performance, it is recommended that the frequency of cluster should be at least 75% of that of the fastest core.

The ratio between the frequency of cluster master clock and that of output clock of cluster accessing external devices is 1:1 or 2:1. For the specific configuration, refer to CPU_DSU_PLL_CLK_REG (bit[1:0]).

5.1.4.2 Linear PLL Frequency Modulation

There are two kinds of parameters for linear PLL frequency modulation, including the immediate effect type and the manual update type.

The immediate effect type is that the configured values immediately take effect after being written to registers, and the readback value is same to the configured one.

The manual update type is that the configured values need to be updated by additionally writing 1 to update bit in PLLx_CTRL_REG; then the readback value are the updated parameter; or, the readback value will be the original one.

The manual update type of parameters depends on PLLs' output clocks. Therefore, when PLL_EN is not enabled, the update operation is invalid when PLLs don't output clocks.

The PLL parameters influenced by UPDATE operation are PLL_LFM_REG and N in the PLL_CTRL_REG. The interval of two update operations should be no less than 1 us.

Enable PLLs

Follow the steps below to enable PLLs.

Step 1 Set the PLL_LDO_EN in the CPU_L/B/DSU_PLL_CTRL_REG as 1.

Step 2 Set the PLL_OUTPUT_GATE in the CPU_L/B/DSU_PLL_CTRL_REG as 1.

Step 3 Configure N, M1, M0, and P in the CPU_L/B/DSU_PLL_CTRL_REG.

Step 4 Set the PLL_EN in the CPU_L/B/DSU_PLL_CTRL_REG as 1.

Step 5 Set the LOCK_ENABLE in the CPU_L/B/DSU_PLL_CTRL_REG as 1.

Step 6 Set the PLL_UPDATE in the CPU_L/B/DSU_PLL_CTRL_REG as 1.

Step 7 Wait the PLL_UPDATE in the CPU_L/B/DSU_PLL_CTRL_REG to be cleared.

Step 8 Wait the LOCK status in the CPU_L/B/DSU_PLL_CTRL_REG to be 1, and perform the adjustment for three times.

Step 9 After 20 us latency, the PLL is enabled.

Disable PLLs

Follow the steps below to disable PLLs.

Step 1 Set the PLL_OUTPUT_GATE in the CPU_L/B/DSU_PLL_CTRL_REG as 0.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 2 Set the LOCK_ENABLE in the CPU_L/B/DSU_PLL_CTRL_REG as 0.

Step 3 Set the PLL_PLL_EN in the CPU_L/B/DSU_PLL_CTRL_REG as 0.

Step 4 Set the PLL_LDO_EN in the CPU_L/B/DSU_PLL_CTRL_REG as 0.

NOTE

It is not suggested to enable or disable the PLLs during usage, as the PLL enable/disable will lead to the disturbance among PLLs, which will cause system instability. When the clock is not required, it is recommended to set the PLL_OUTPUT_GATE bit in the PLL_CTRL as 0.

PLL Pre-divider Frequency Modulation

The PLL linear frequency modulation supports smooth transition to target N value at a certain modulation rate value without re-locking. However, only the linear frequency modulation of N value is supported. When the pre-divider factor alters, PLL should be re-locked.

When not enabling linear frequency modulation, or when the pre-divider should be adjusted in the condition that liner frequency modulation is enabled. Follow the steps below to perform PLL pre-divider frequency modulation.

Step 1 Set the PLL_OUTPUT_GATE in the CPU_L/B/DSU_PLL_CTRL_REG as 0.

Step 2 Set the LOCK_ENABLE in the CPU_L/B/DSU_PLL_CTRL_REG as 0.

Step 3 Configure N, M1, M0, and P in the CPU_L/B/DSU_PLL_CTRL_REG.

Step 4 Set the LOCK_ENABLE in the CPU_L/B/DSU_PLL_CTRL_REG as 1.

Step 5 Set the PLL_UPDATE in the CPU_L/B/DSU_PLL_CTRL_REG as 1.

Step 6 Set the PLL_UPDATE in the CPU_L/B/DSU_PLL_CTRL_REG as 1.

Step 7 Wait the LOCK_STATUS in the CPU_L/B/DSU_PLL_CTRL_REG to be cleared.

Step 8 Wait 20 us latency.

Step 9 Set the PLL_OUTPUT_GATE in the CPU_L/B/DSU_PLL_CTRL_REG as 1.

PLL Linear Frequency Modulation

The following steps take CPU_L_PLL as an example to perform PLL linear frequency modulation.

Step 1 Set PLL_PLL_EN in the CPU_L_PLL_CTRL_REG as 1, and wait CPU_L_PLL lock state is stable.

Step 2 Set SPR_FREQ_MODE in the CPU_L_PLL_PAT0_CTRL_REG as 10 or 11. Set PLL_PI_EN as 1 and SMOOTH_EN as 0 in the CPU_L_PLL_PAT1_CTRL_REG.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 3 Set PLL_LFM_STEP in the CPU_L_PLL_LFM_REG. STEP is 12 bit. The formula is as below:

FREQ = FCLK*FCLK*STEP/2^17

In the above formula. FREQ is the target modulation rate at the unit of MHz/us. The FCLK is reference clock frequency at the unit of MHz. Thus, the step can be gotten by the formula as below:

STEP = FREQ*2^17/FCLK/FCLK

Step 1 Set the PLL_LFM_EN in the CPU_L_PLL_LFM_REG as 1.

Step 2 Set the PLL_UPDATE in the CPU_L_PLL_CTRL_REG as 1.

Step 3 Wait the PLL_UPDATE in the CPU_L_PLL_CTRL_REG to be 0.

Step 4 Set the PLL_N in the CPU_L_PLL_CTRL_REG and then write 1 to the PLL_UPDATE.

Step 5 Wait the PLL_UPDATE to be 0, indicating the linear frequency modulation completes.

Step 6 To re-configure N value, go back to the step 7.

Step 7 To disable linear frequency modulation, set PLL_LFM_EN in the CPU_L_PLL_LFM_REG as 0, and set PLL_UPDATE in the CPU_L_PLL_CTRL_REG as 1.

5.1.4.3 Generic PLL Frequency Modulation

Enable PLLs

There are two configuration methods. The one is used in the startup phase, during which there is a period of instable clock output once when PLL is enabled. The other is not recommended to be used in the startup phase as there exists glitches when PLL_OUTPUT_GATE is enabled; after PLLs become stable, output clock.

Method 1:

Step 1 Set PLL_LDO_EN in the CPU_BACK_PLL_CTRL_REG as 1.

Step 2 Set PLL_OUTPUT_GATE in the CPU_BACK_PLL_CTRL_REG as 1.

Step 3 Set the values of N, M1, M0, P in the CPU_BACK_PLL_CTRL_REG.

Step 4 Set PLL_EN in the CPU_BACK_PLL_CTRL_REG as 1.

Step 5 Set LOCK_ENABLE in the CPU_BACK_PLL_CTRL_REG as 1.

Step 6 Wait the LOCK status in the CPU_BACK_PLL_CTRL_REG to be 1, and perform the adjustment for three times.

Step 7 After 20 us latency, PLLs can be used.

Method 2:

Step 1 Set PLL_LDO_EN in the CPU_BACK_PLL_CTRL_REG as 1.

Step 2 Set the values of N, M1, M0, P in the CPU_BACK_PLL_CTRL_REG.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 3 Set PLL_EN in the CPU_BACK_PLL_CTRL_REG as 1.

Step 4 Set LOCK_ENABLE in the CPU_BACK_PLL_CTRL_REG as 1.

Step 5 Wait the LOCK status in the CPU_L/B/DSU_PLL_CTRL_REG to be 1, and perform the adjustment for three times.

Step 6 After 20 us latency.

Step 7 Set the PLL_OUTPUT_GATE in the CPU_BACK_PLL_CTRL_REG as 1. Then, PLLs can be used.

NOTE

When more than one channel output exists in PLLs, write 1 to PLL_OUTPUT_GATE for each output clock to be used.

Disable PLLs

Follow the steps below to disable PLLs. Before this, ensure that the PLL clock has been switched to other clock source or closed.

Step 1 Set PLL_OUTPUT_GATE in the CPU_BACK_PLL_CTRL_REG as 0.

Step 2 Set LOCK_ENABLE in the CPU_BACK_PLL_CTRL_REG as 0.

Step 3 Set PLL_EN in the CPU_BACK_PLL_CTRL_REG as 0.

Step 4 Set PLL_LDO_EN in the CPU_BACK_PLL_CTRL_REG as 0.

NOTE

It is not suggested to enable or disable the PLLs during usage, as the PLL enable/disable will lead to the disturbance among PLLs, which will cause system instability. When the clock is not required, it is recommended to set the PLL_OUTPUT_GATE bit in the PLL_CTRL as 0.

PLL Spreading

Step 1 Enable PLLs.

Step 2 Configure the static parameters as below

- SPR_FREQ_MODE is recommended to be 3.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- PLL_PI_EN is recommended to be 1.
- PLL_PI_CFG is recommended to use the default value.
- SMOOTH_EN is recommended to be 0.
- DITHER is recommended to be 0.

Step 3 Configure WAVE_STEP, WAVE_BOT, FREQ, SDM_DIRECTION, FRAC_IN and FRAC_EN in conformity with PLL spreading/fractional divider formulas.

Step 4 Configure SIG_DELT_PAT_EN and other parameters to enable PLL spreading/fractional dividers.

Step 5 To adjust static parameters, configure SIG_DELT_PAT_EN as 0. After SDM_BUSY is 0, go back to step 1.

Step 6 To adjust control parameters when PLL spreading/fractional dividers are enabled, configure WAVE_STEP, WAVE_BOT, FREQ, SDM_DIRECTION, and FRAC_IN.

Step 7 To disable PLL spreading, set SIG_DELT_PAT_EN as 0. To enable PLL spreading next time, judge SDM_BUSY as 0 first.

PLL Frequency Modulation

CAUTION

Before PLL frequency modulation, ensure the PLLs are enabled. It is not recommended to enable/disable during the PLL usage. When the clock is not used, set PLL_OUTPUT_GATE in the CPU_BACK_PLL_CTRL_REG as 0.

The generic PLLs cannot be used during the frequency modulation. Therefore, set PLL_OUTPUT_GATE in the CPU_BACK_PLL_CTRL_REG as 0.

Follow the steps below to perform PLL frequency modulation.

Step 1 Configure N and M factors.

Step 2 Write 0 to LOCK_ENABLE in the CPU_BACK_PLL_CTRL_REG, and then write 1.

Step 3 Wait the LOCK in the CPU_BACK_PLL_CTRL_REG to be 1.

Step 4 Set the PLL_OUTPUT_GATE in the CPU_BACK_PLL_CTRL_REG as 1.

5.1.5 Register list

Module Name	Base Address	Description
CPU_SUBSYS_CTRL	0x08000000	CPU Subsystem Control Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Module Name	Base Address	Description
TIMESTAMP_STA	0x08010000	Timestamp Status Register
TIMESTAMP_CTRL	0x08020000	Timestamp Control Register
CLUSTER_CFG	0x08860000	Cluster Configuration Register
CPU_PLL_CFG	0x08870000	CPU PLL Configuration Register

5.1.5.1 CPU_SUBSYS_CTRL Register List

Register Name	Offset	Description
GENER_CTRL_REG0	0x0000	General Control Register0
CPU_SYS_RST_CTRL	0x000C	CPU Subsystem Reset Control Register
PLL_CTRL_REG0	0x0140	PLL Control Register 0
PLL_CTRL_REG1	0x0144	PLL Control Register 1
CPU_DA_DDR_CTRL_REG	0x0200	CPU Direct Access DDR Control Register
CLU0_CPU0_CTRL_REG	0x1000	Cluster0 CPU0 Control Register
CLU0_RVBARADDR0_L	0x1004	Cluster0 Reset Vector Base Address Register0_L
CLU0_RVBARADDR0_H	0x1008	Cluster0 Reset Vector Base Address Register0_H
CLU0_CPU1_CTRL_REG	0x2000	Cluster0 CPU1 Control Register
CLU0_RVBARADDR1_L	0x2004	Cluster0 Reset Vector Base Address Register1_L
CLU0_RVBARADDR1_H	0x2008	Cluster0 Reset Vector Base Address Register1_H
CLU0_CPU2_CTRL_REG	0x3000	Cluster0 CPU2 Control Register
CLU0_RVBARADDR2_L	0x3004	Cluster0 Reset Vector Base Address Register2_L
CLU0_RVBARADDR2_H	0x3008	Cluster0 Reset Vector Base Address Register2_H
CLU0_CPU3_CTRL_REG	0x4000	Cluster0 CPU3 Control Register
CLU0_RVBARADDR3_L	0x4004	Cluster0 Reset Vector Base Address Register3_L
CLU0_RVBARADDR3_H	0x4008	Cluster0 Reset Vector Base Address Register3_H
CLU0_CPU4_CTRL_REG	0x5000	Cluster0 CPU4 Control Register
CLU0_RVBARADDR4_L	0x5004	Cluster0 Reset Vector Base Address Register4_L
CLU0_RVBARADDR4_H	0x5008	Cluster0 Reset Vector Base Address Register4_H
CLU0_CPU5_CTRL_REG	0x6000	Cluster0 CPU5 Control Register
CLU0_RVBARADDR5_L	0x6004	Cluster0 Reset Vector Base Address Register5_L
CLU0_RVBARADDR5_H	0x6008	Cluster0 Reset Vector Base Address Register5_H
CLU0_CPU6_CTRL_REG	0x7000	Cluster0 CPU6 Control Register
CLU0_RVBARADDR6_L	0x7004	Cluster0 Reset Vector Base Address Register6_L
CLU0_RVBARADDR6_H	0x7008	Cluster0 Reset Vector Base Address Register6_H
CLU0_CPU7_CTRL_REG	0x8000	Cluster0 CPU7 Control Register
CLU0_RVBARADDR7_L	0x8004	Cluster0 Reset Vector Base Address Register7_L
CLU0_RVBARADDR7_H	0x8008	Cluster0 Reset Vector Base Address Register7_H

5.1.5.2 TIMESTAMP_STA Register List

Register Name	Offset	Description
CNT_LOW_REG	0x0000	Counter Low Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
CNT_HI_REG	0x0004	Counter High Register

5.1.5.3 TIMESTAMP_CTRL Register List

Register Name	Offset	Description
TSTAMP_CTRL_REG	0x0000	Timestamp Control Register
CNT_CTRL_LOW_REG	0x0008	Counter Low Register
CNT_CTRL_HI_REG	0x000C	Counter High Register
CNT_FREQID_REG	0x0020	Counter Base Frequency ID Register

5.1.5.4 CLUSTER_CFG Register List

Register Name	Offset	Description
C0_CPU0_CTRL_REG	0x0000	Cluster 0 CPU0 Control Register
C0_CPU0_STATUS0	0x0004	Cluster 0 CPU0 Status0 Register
C0_CPU1_CTRL_REG	0x1000	Cluster 0 CPU1 Control Register
C0_CPU1_STATUS0	0x1004	Cluster 0 CPU1 Status0 Register
C0_CPU2_CTRL_REG	0x2000	Cluster 0 CPU2 Control Register
C0_CPU2_STATUS0	0x2004	Cluster 0 CPU2 Status0 Register
C0_CPU3_CTRL_REG	0x3000	Cluster 0 CPU3 Control Register
C0_CPU3_STATUS0	0x3004	Cluster 0 CPU3 Status0 Register
C0_CPU4_CTRL_REG	0x4000	Cluster 0 CPU4 Control Register
C0_CPU4_STATUS0	0x4004	Cluster 0 CPU4 Status0 Register
C0_CPU5_CTRL_REG	0x5000	Cluster 0 CPU5 Control Register
C0_CPU5_STATUS0	0x5004	Cluster 0 CPU5 Status0 Register
C0_CPU6_CTRL_REG	0x6000	Cluster 0 CPU6 Control Register
C0_CPU6_STATUS0	0x6004	Cluster 0 CPU6 Status0 Register
C0_CPU7_CTRL_REG	0x7000	Cluster 0 CPU7 Control Register
C0_CPU7_STATUS0	0x7004	Cluster 0 CPU7 Status0 Register
C0_RST_CTRL	0x8000	Cluster 0 Reset Control Register
C0_CTRL_REG0	0x8004	Cluster 0 Control Register0
C0_CTRL_REG1	0x8008	Cluster 0 Control Register1
CLK_FORCE_CFG_REG	0x800C	Clk Control Force Configuration Register
CLUSTER_SPRAM_CFG_REG	0x8010	CPU cluster spram memory Configuration Register
CLUSTER_RF2P_CFG_REG	0x8014	CPU cluster rf2p memory Configuration Register
CLUSTER_RFP2P_CFG_REG	0x8018	CPU cluster rfp2p memory Configuration Register
CLUSTER_SYSSPRAM_CFG_REG	0x801C	CPU cluster sysspram memory Configuration Register
DSU_AXI_TH_CFG_REG	0x8020	DSU AXI2TO1 TH Configuration Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
CLU_DSU_STATUS_REG	0x8030	Cluster DSU Status Register
CLU_DSU_RST_CTRL	0x80A4	Cluster DSU reset self release Register
AXI0_MNT_CTRL_REG	0x80B0	DSU AXI0 MONITOR Control Register
AXI0_MNT_PRD_REG	0x80B4	DSU AXI0 MONITOR Period Register
AXI0_MNT_RLTCY_REG	0x80B8	DSU AXI0 MONITOR Read Total Latency Register
AXI0_MNT_WLTCY_REG	0x80BC	DSU AXI0 MONITOR Write Total Latency Register
DSU_AXI0_MNT_RREQ_REG	0x80C0	DSU AXI0 MONITOR Read Request times Register
DSU_AXI0_MNT_WREQ_REG	0x80C4	DSU AXI0 MONITOR Write Request times Register
DSU_AXI0_MNT_RBD_REG	0x80C8	DSU AXI0 MONITOR Read Bandwidth Register
DSU_AXI0_MNT_WBD_REG	0x80CC	DSU AXI0 MONITOR Write Bandwidth Register
DSU_AXI1_MNT_CTRL_REG	0x80D0	DSU AXI1 MONITOR Control Register
DSU_AXI1_MNT_PRD_REG	0x80D4	DSU AXI1 MONITOR Period Register
DSU_AXI1_MNT_RLTCY_REG	0x80D8	DSU AXI1 MONITOR Read Total Latency Register
DSU_AXI1_MNT_WLTCY_REG	0x80DC	DSU AXI1 MONITOR Write Total Latency Register
DSU_AXI1_MNT_RREQ_REG	0x80E0	DSU AXI1 MONITOR Read Request times Register
DSU_AXI1_MNT_WREQ_REG	0x80E4	DSU AXI1 MONITOR Write Request times Register
DSU_AXI1_MNT_RBD_REG	0x80E8	DSU AXI1 MONITOR Read Bandwidth Register
DSU_AXI1_MNT_WBD_REG	0x80EC	DSU AXI1 MONITOR Write Bandwidth Register

5.1.5.5 CPU_PLL_CFG Register List

Register Name	Offset	Description
CPU_BACK_PLL_CTRL_REG	0x0000	CPU_BACK_PLL Control Register
CPU_BACK_PLL_LOCK_CTRL_REG	0x0004	CPU_BACK_PLL lock control Register
CPU_BACK_PLL_PAT0_CTRL_REG	0x0008	CPU_BACK_PLL Pattern0 Control Register
CPU_BACK_PLL_PAT1_CTRL_REG	0x000C	CPU_BACK_PLL Pattern1 Control Register
CPU_BACK_PLL_BIAS_REG	0x0010	CPU_BACK_PLL Bias Register
CPU_L_PLL_CTRL_REG	0x1000	CPU_L_PLL Control Register
CPU_L_PLL_PAT0_CTRL_REG	0x1004	CPU_L_PLL Pattern0 Control Register
CPU_L_PLL_PAT1_CTRL_REG	0x1008	CPU_L_PLL Pattern1 Control Register
CPU_L_PLL_BIAS_REG	0x100C	CPU_L_PLL Bias Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
CPU_L_PLL_TUN0_REG	0x1010	CPU_L_PLL Tuning0 Register
CPU_L_PLL_TUN1_REG	0x1014	CPU_L_PLL Tuning1 Register
CPU_L_PLL_LFM_REG	0x1018	CPU_L_PLL LFM Register
CPU_L_PLL_CLK_REG	0x101C	CPU_L_PLL Clock Register
CPU_L_PLL_GATING_REG	0x1020	CPU_L_PLL Gating Configuration Register
CPU_L_PLL_UNLOCK_IRQEN_REG	0x1024	CPU_L_PLL Unlock IRQ Enable Register
CPU_L_PLL_UNLOCK_STAT_REG	0x1028	CPU_L_PLL Unlock Status Register
CPU_L_PLL_CTRL_STAT_REG	0x102C	CPU_L_PLL Control Status Register
CPU_B_PLL_CTRL_REG	0x2000	CPU_B_PLL Control Register
CPU_B_PLL_PAT0_CTRL_REG	0x2004	CPU_B_PLL Pattern0 Control Register
CPU_B_PLL_PAT1_CTRL_REG	0x2008	CPU_B_PLL Pattern1 Control Register
CPU_B_PLL_BIAS_REG	0x200C	CPU_B_PLL Bias Register
CPU_B_PLL_TUN0_REG	0x2010	CPU_B_PLL Tuning0 Register
CPU_B_PLL_TUN1_REG	0x2014	CPU_B_PLL Tuning1 Register
CPU_B_PLL_LFM_REG	0x2018	CPU_B_PLL LFM Register
CPU_B_PLL_CLK_REG	0x201C	CPU_B_PLL Clock Register
CPU_B_PLL_GATING_REG	0x2020	CPU_B_PLL Gating Configuration Register
CPU_B_PLL_UNLOCK_IRQEN_REG	0x2024	CPU_B_PLL Unlock IRQ Enable Register
CPU_B_PLL_UNLOCK_STAT_REG	0x2028	CPU_B_PLL Unlock Status Register
CPU_B_PLL_CTRL_STAT_REG	0x202C	CPU_B_PLL Control Status Register
CPU_DSU_PLL_CTRL_REG	0x3000	CPU_DSU_PLL Control Register
CPU_DSU_PLL_PAT0_CTRL_REG	0x3004	CPU_DSU_PLL Pattern0 Control Register
CPU_DSU_PLL_PAT1_CTRL_REG	0x3008	CPU_DSU_PLL Pattern1 Control Register
CPU_DSU_PLL_BIAS_REG	0x300C	CPU_DSU_PLL Bias Register
CPU_DSU_PLL_TUN0_REG	0x3010	CPU_DSU_PLL Tuning0 Register
CPU_DSU_PLL_TUN1_REG	0x3014	CPU_DSU_PLL Tuning1 Register
CPU_DSU_PLL_LFM_REG	0x3018	CPU_DSU_PLL LFM Register
CPU_DSU_PLL_CLK_REG	0x301C	CPU_DSU_PLL Clock Register
CPU_DSU_PLL_GATING_REG	0x3020	CPU_DSU_PLL Gating Configuration Register
CPU_DSU_PLL_UNLOCK_IRQEN_REG	0x3024	CPU_DSU_PLL Unlock IRQ Enable Register
CPU_DSU_PLL_UNLOCK_STAT_REG	0x3028	CPU_DSU_PLL Unlock Status Register
CPU_DSU_PLL_CTRL_STAT_REG	0x302C	CPU_DSU_PLL Control Status Register
CPU_SLOW_CLK_SEL_REG	0x3034	CPU Slow Clock Select Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.1.6 CPU_SUBSYS_CTRL Register Description

5.1.6.1 0x0000 General Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name:GENER_CTRL_REG0
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	GICCDISABLE control debug block
0	R/W	0x0	CDBGRSTACK Debug Reset ACK

5.1.6.2 0x000C CPU Subsystem Reset Control Register (Default Value: 0x0000_007F)

Offset: 0x000C			Register Name: CPU_SYS_RST_CTRL
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x1	GIC_DBG_RSTN GIC OUTRE debug Reset. 0: Assert 1: De-assert
5	R/W	0x1	GIC_OUT_RSTN GIC OUTRE Reset. 0: Assert 1: De-assert
4	R/W	0x1	GIC_OUT_MBIST_RSTN GIC OUTER MBIST Reset. 0: Assert 1: De-assert
3	R/W	0x1	COREPLL_RST Corepll Reset. 0: Assert 1: De-assert
2	R/W	0x1	CS_RST CoreSight Reset. 0: Assert 1: De-assert
1	R/W	0x1	PORTRST Jtag portrst. 0: Assert 1: De-assert

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x000C			Register Name: CPU_SYS_RST_CTRL
Bit	Read/Write	Default/Hex	Description
0	R/W	0x1	TRST. Jtag trst. 0: Assert 1: De-assert

5.1.6.3 0x0140 PLL Control Register 0 (Default Value: 0x0000_0007)

Offset: 0x0140			Register Name: PLL_CTRL_REG0
Bit	R/W	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	TEST_CLK_SEL. Test Clock Select. 0: XTAL. 1: External Clock.
23:3	/	/	/
2	R/W	0x1	GM1. XTAL Gain Control Bit1.
1	R/W	0x1	GM0. XTAL Gain Control Bit0.
0	R/W	0x1	PLL_BIAS_EN. PLL Bias Enable. 0: Disable 1: Enable

5.1.6.4 0x0144 PLL Control Register 1 (Default Value: 0x0003_0025)

Offset: 0x0144			Register Name: PLL_CTRL_REG1
Bit	R/W	Default/Hex	Description
31:24	R/W	0x0	KEY_FIELD. Key Field for LDO Enable bit. If the key field value is 0xA7, the bit[23:0] can be modified.
23:19	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0144			Register Name: PLL_CTRL_REG1
Bit	R/W	Default/Hex	Description
18:16	R/W	0x3	PLLVDD_LDO_OUT_CTRL. PLLVDD LDO Output Control 000: 0.81V 001: 0.84V 010: 0.87V 011: 0.9V 100: 0.93V 101: 0.96V 110: 0.99V 111: 1.02V
15:6	/	/	/
5	R/W	0x1	VCO_START_EN vco start enable 0: Disable 1: Enable
4	R/W	0x0	MBIAS_EN. Chip Master Bias Enable 0: From Internal Bias 1: From ADDA Bias
3	R/W	0x0	PLLTEST_EN For Verify (Back door clock PLLTEST enable) Plltest output enable 0: The output clock gate is 0. 1: The output clock sources from PLL or divided from clock source.
2:1	/	/	/
0	R/W	0x1	LDO_EN 0: Disable 1: Enable Note: PLL Power enable (power source from VCC_PLL)

5.1.6.5 0x0200 CPU Direct Access DDR Control Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: CPU_DA_DDR_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	CPU Direct Access DDR Mux Select 0: CPU accesses DDR through NSI 1: CPU accesses DDR through AXI2HIF

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.1.6.6 0x1000 Cluster0 CPU0 Control Register (Default Value: 0x0000_0000)

Offset: 0x1000			Register Name: CLU0_CPU0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	Cluster 0 CPU0 AA64NAA32 Register width state: 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor.

5.1.6.7 0x1004 Cluster0 Reset Vector Base Address Register0_L (Default Value: 0x0000_0000)

Offset: 0x1004			Register Name: CLU0_RVBARADDR0_L
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	RVBARADDR[31:2] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64) of cluster0 CPU0.
1:0	/	/	/

5.1.6.8 0x1008 Cluster0 Reset Vector Base Address Register0_H (Default Value: 0x0000_0000)

Offset: 0x1008			Register Name: CLU0_RVBARADDR0_H
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR[39:32] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64) of cluster0 CPU0.

5.1.6.9 0x2000 Cluster0 CPU1 Control Register (Default Value: 0x0000_0000)

Offset: 0x2000			Register Name: CLU0_CPU1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	Cluster 0 CPU1 AA64NAA32 Register width state 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.1.6.10 0x2004 Cluster0 Reset Vector Base Address Register1_L (Default Value: 0x0000_0000)

Offset: 0x2004			Register Name: CLU0_RVBARADDR1_L
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	RVBARADDR[31:2] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64) of cluster0 CPU1.
1:0	/	/	/

5.1.6.11 0x2008 Cluster0 Reset Vector Base Address Register1_H (Default Value: 0x0000_0000)

Offset: 0x2008			Register Name: CLU0_RVBARADDR1_H
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR[39:32] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64) of cluster0 CPU1.

5.1.6.12 0x3000 Cluster0 CPU2 Control Register (Default Value: 0x0000_0000)

Offset: 0x3000			Register Name: CLU0_CPU2_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	Cluster 0 CPU2 AA64NAA32 Register width state 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor

5.1.6.13 0x3004 Cluster0 Reset Vector Base Address Register2_L (Default Value: 0x0000_0000)

Offset: 0x3004			Register Name: CLU0_RVBARADDR2_L
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	RVBARADDR[31:2] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64) of cluster0 CPU2.
1:0	/	/	/

5.1.6.14 0x3008 Cluster0 Reset Vector Base Address Register2_H (Default Value: 0x0000_0000)

Offset: 0x3008	Register Name: CLU0_RVBARADDR2_H

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR[39:32] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64) of cluster0 CPU2.

5.1.6.15 0x4000 Cluster0 CPU3 Control Register (Default Value: 0x0000_0000)

Offset: 0x4000			Register Name: CLU0_CPU3_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	Cluster 0 CPU3 AA64NAA32 Register width state 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor

5.1.6.16 0x4004 Cluster0 Reset Vector Base Address Register3_L (Default Value: 0x0000_0000)

Offset: 0x4004			Register Name: CLU0_RVBARADDR3_L
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	RVBARADDR[31:2] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64) of cluster0 CPU3.
1:0	/	/	/

5.1.6.17 0x4008 Cluster0 Reset Vector Base Address Register3_H (Default Value: 0x0000_0000)

Offset: 0x4008			Register Name: CLU0_RVBARADDR3_H
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR[39:32] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64) of cluster0 CPU3.

5.1.6.18 0x5000 Cluster0 CPU4 Control Register (Default Value: 0x0000_0000)

Offset: 0x5000			Register Name: CLU0_CPU4_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x5000			Register Name: CLU0_CPU4_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	Cluster 0 CPU4 AA64NAA32 Register width state 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor

5.1.6.19 0x5004 Cluster0 Reset Vector Base Address Register4_L (Default Value: 0x0000_0000)

Offset: 0x5004			Register Name: CLU0_RVBARADDR4_L
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	RVBARADDR[31:2] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64) of cluster0 CPU4.
1:0	/	/	/

5.1.6.20 0x5008 Cluster0 Reset Vector Base Address Register4_H (Default Value: 0x0000_0000)

Offset: 0x5008			Register Name: CLU0_RVBARADDR4_H
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR[39:32] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64) of cluster0 CPU4.

5.1.6.21 0x6000 Cluster0 CPU5 Control Register (Default Value: 0x0000_0000)

Offset: 0x6000			Register Name: CLU0_CPU5_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	Cluster 0 CPU5 AA64NAA32 Register width state: 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor

5.1.6.22 0x6004 Cluster0 Reset Vector Base Address Register5_L (Default Value: 0x0000_0000)

Offset: 0x6004			Register Name: CLU0_RVBARADDR5_L
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x6004			Register Name: CLU0_RVBARADDR5_L
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	RVBARADDR[31:2] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64) of cluster0 CPU5.
1:0	/	/	/

5.1.6.23 0x6008 Cluster0 Reset Vector Base Address Register5_H (Default Value: 0x0000_0000)

Offset: 0x6008			Register Name: CLU0_RVBARADDR5_H
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR[39:32] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64) of cluster0 CPU5.

5.1.6.24 0x7000 Cluster0 CPU6 Control Register (Default Value: 0x0000_0000)

Offset: 0x7000			Register Name: CLU0_CPU6_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	Cluster 0 CPU6 AA64NAA32 Register width state 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor

5.1.6.25 0x7004 Cluster0 Reset Vector Base Address Register6_L (Default Value: 0x0000_0000)

Offset: 0x7004			Register Name: CLU0_RVBARADDR6_L
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	RVBARADDR[31:2] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64) of cluster0 CPU6.
1:0	/	/	/

5.1.6.26 0x7008 Cluster0 Reset Vector Base Address Register6_H (Default Value: 0x0000_0000)

Offset: 0x7008			Register Name: CLU0_RVBARADDR6_H
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x7008			Register Name: CLU0_RVBARADDR6_H
Bit	Read/Write	Default/Hex	Description
7:0	R/W	0x0	RVBARADDR[39:32] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64) of cluster0 CPU6.

5.1.6.27 0x8000 CLuster0 CPU7 Control Register (Default Value: 0x0000_0000)

Offset: 0x8000			Register Name: CLU0_CPU7_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	Cluster 0 CPU7 AA64NAA32 Register width state 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor

5.1.6.28 0x8004 Cluster0 Reset Vector Base Address Register7_L (Default Value: 0x0000_0000)

Offset: 0x8004			Register Name: CLU0_RVBARADDR7_L
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	RVBARADDR[31:2] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64) of cluster0 CPU7.
1:0	/	/	/

5.1.6.29 0x8008 Cluster0 Reset Vector Base Address Register7_H (Default Value: 0x0000_0000)

Offset: 0x8008			Register Name: CLU0_RVBARADDR7_H
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR[39:32] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64) of cluster0 CPU7.

5.1.7 TIMESTAMP_STA Register Description

5.1.7.1 0x0000 Counter Low Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CNT_LOW_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: CNT_LOW_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CNT_LOW_REG. Current value of counter[31:0]

5.1.7.2 0x0004 Counter High Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: CNT_HI_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CNT_HI_REG. Current value of counter[64:32]

5.1.8 TIMESTAMP_CTRL Register Description

5.1.8.1 0x0000 Timestamp Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TSTAMP_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	EN. Timestamp Counter Enable. 0: Disable 1: Enable

5.1.8.2 0x0008 Counter Low Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CNT_CTRL_LOW_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CNT_CTRL_LOW_REG. Current value of counter[31:0]

5.1.8.3 0x000C Counter High Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: CNT_CTRL_HI_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CNT_CTRL_HI_REG. Current value of counter[64:32]

5.1.8.4 0x0020 Counter Base Frequency ID Register (Default Value: 0x0000_0000)

Offset: 0x0020	Register Name: CNT_FREQID_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	FREQ. This register must be programmed to match the clock frequency of the timestamp generator, in ticks per second. For example, in the soc, a 24 MHz clock must program 0x16E3600.

Note: This register just records the fixed frequency value.

5.1.9 CLUSTER_CFG Register Description

5.1.9.1 0x0000 Cluster 0 CPU0 Control Register (Default Value: 0x0000_0001)

Offset: 0x0000			Register Name: C0_CPU0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10	R/W	0x0	CORE0_EXM1_CLR Clear the status of exclusive monitor1 interface
9	R/W	0x0	CORE0_EXM0_CLR Clear the status of exclusive monitor0 interface
8	R/W	0x0	Core0 CRM auto select slow frequency enable 0: Disable auto select. 1: Enable auto select.
7	/	/	/
6	R/W	0x0	CORE0_CFGTE Enable Thumb exceptions, controls the reset value of the SCTLR.TE bit. The options are: 0: TE bit is LOW. 1: TE bit is HIGH.
5	R/W	0x0	CORE0_VINITHI Enable high exception vectors, controls the reset value of the SCTLR.V bit. The options are: 0: Starts exception vectors at address 0x00000000. 1: Starts exception vectors at address 0xFFFF0000.
4	R/W	0x0	CORE0_CFGEND Endianness configuration, controls the reset value of the SCTLR_EL3/SCTLR_S EE bit. The options are: 0: EE bit is LOW. 1: EE bit is HIGH.
3:1	/	/	/
0	R/W	0x1	CORE0_RESET. Cluster CORE0 Reset Assert. 0: Assert 1: De-assert

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.1.9.2 0x0004 Cluster 0 CPU0 Status0 Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: C0_CPU0_STATUS0
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R	0x0	CORE0_DBGRSTREQ Indicates that core0 Debug reset request
15:13	/	/	/
12	R	0x0	CORE0_INSTRRUN Indicates that core0 is in a running state (powered up and not in WFI or WFE low-power states).
11:9	/	/	/
8	R	0x0	CORE0_INSTRRET Indicates that core0 has retired at least one instruction recently.
7:5	/	/	/
4	R	0x0	CORE0_STANDBYWFI. Indicates if Cluster0 CPU0 is in WFI standby mode: 0: Processor is not in WFI standby mode. 1: Processor is in WFI standby mode
3:1	/	/	/
0	R	0x0	CORE0_STANDBYWFE. Indicates if Cluster0 CPU0 is in the WFE standby mode: 0: Processor is not in WFE standby mode 1: Processor is in WFE standby mode

5.1.9.3 0x1000 Cluster 0 CPU1 Control Register (Default Value: 0x0000_0001)

Offset: 0x1000			Register Name: C0_CPU1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10	R/W	0x0	CORE1_EXM1_CLR Clear the status of exclusive monitor1 interface
9	R/W	0x0	CORE1_EXM0_CLR Clear the status of exclusive monitor0 interface
8	R/W	0x0	Core1 CRM auto select slow frequency en. 0: Disable auto select 1: Enable auto select
7	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1000			Register Name: C0_CPU1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	CORE1_CFGTE Enable Thumb exceptions, controls the reset value of the SCTLR.TE bit. The options are: 0: TE bit is LOW. 1: TE bit is HIGH.
5	R/W	0x0	CORE1_VINITHI Enable high exception vectors, controls the reset value of the SCTLR.V bit. The options are: 0: Starts exceptions vectors at address 0x00000000. 1: Starts exceptions vectors at address 0xFFFF0000.
4	R/W	0x0	CORE1_CFGEND Endianness configuration, controls the reset value of the SCTLR_EL3/SCTLR_S EE bit. The options are: 0: EE bit is LOW. 1: EE bit is HIGH.
3:1	/	/	/
0	R/W	0x1	CORE1_RESET. Cluster CORE1 Reset Assert. 0: Assert 1: De-assert

5.1.9.4 0x1004 Cluster 0 CPU1 Status0 Register (Default Value: 0x0000_0000)

Offset: 0x1004			Register Name: C0_CPU1_STATUS0
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R	0x0	CORE1_DBGRSTREQ Indicates that core1 Debug reset request
15:13	/	/	/
12	R	0x0	CORE1_INSTRRUN Indicates that core1 is in a running state (powered up and not in WFI or WFE low-power states).
11:9	/	/	/
8	R	0x0	CORE1_INSTRRET Indicates that core1 has retired at least one instruction recently.
7:5	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1004			Register Name: C0_CPU1_STATUS0
Bit	Read/Write	Default/Hex	Description
4	R	0x0	CORE1_STANDBYWFI. Indicates if Cluster0 CPU1 is in WFI standby mode: 0: Processor not in WFI standby mode. 1: Processor in WFI standby mode
3:1	/	/	/
0	R	0x0	CORE1_STANDBYWFE. Indicates if Cluster0 CPU1 is in the WFE standby mode: 0: Processor not in WFE standby mode 1: Processor in WFE standby mode

5.1.9.5 0x2000 Cluster 0 CPU2 Control Register (Default Value: 0x0000_0001)

Offset: 0x2000			Register Name: C0_CPU2_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10	R/W	0x0	CORE2_EXM1_CLR Clear the status of exclusive monitor1 interface
9	R/W	0x0	CORE2_EXM0_CLR Clear the status of exclusive monitor0 interface
8	R/W	0x0	Core2 CRM auto select slow frequency en. 0: Disable auto select 1: Enable auto select
7	/	/	/
6	R/W	0x0	CORE2_CFGTE Enable Thumb exceptions, controls the reset value of the SCTLR.TE bit. The options are: 0: TE bit is LOW. 1: TE bit is HIGH.
5	R/W	0x0	CORE2_VINITHI Enable high exception vectors, controls the reset value of the SCTLR.V bit. The options are: 0: Starts exceptions vectors at address 0x00000000. 1: Starts exceptions vectors at address 0xFFFF0000.
4	R/W	0x0	CORE2_CFGEND Endianness configuration, controls the reset value of the SCTLR_EL3/SCTLR_S EE bit. The options are: 0: EE bit is LOW. 1: EE bit is HIGH.
3:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x2000			Register Name: C0_CPU2_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x1	CORE2_RESET. Cluster CORE2 Reset Assert. 0: Assert 1: De-assert

5.1.9.6 0x2004 Cluster 0 CPU2 Status0 Register (Default Value: 0x0000_0000)

Offset: 0x2004			Register Name: C0_CPU2_STATUS0
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R	0x0	CORE2_DBGRSTREQ Indicates that core2 Debug reset request
15:13	/	/	/
12	R	0x0	CORE2_INSTRRUN Indicates that core2 is in a running state (powered up and not in WFI or WFE low-power states).
11:9	/	/	/
8	R	0x0	CORE2_INSTRRET Indicates that core2 has retired at least one instruction recently.
7:5	/	/	/
4	R	0x0	CORE2_STANDBYWFI. Indicates if Cluster0 CPU2 is in WFI standby mode: 0: Processor not in WFI standby mode. 1: Processor in WFI standby mode
3:1	/	/	/
0	R	0x0	CORE2_STANDBYWFE. Indicates if Cluster0 CPU2 is in the WFE standby mode: 0: Processor not in WFE standby mode 1: Processor in WFE standby mode

5.1.9.7 0x3000 Cluster 0 CPU3 Control Register (Default Value: 0x0000_0001)

Offset: 0x3000			Register Name: C0_CPU3_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10	R/W	0x0	CORE3_EXM1_CLR Clear the status of exclusive monitor1 interface

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x3000			Register Name: C0_CPU3_CTRL_REG
Bit	Read/Write	Default/Hex	Description
9	R/W	0x0	CORE3_EXM0_CLR Clear the status of exclusive monitor0 interface
8	R/W	0x0	Core3 CRM auto select slow frequency en. 0: Disable auto select 1: Enable auto select
7	/	/	/
6	R/W	0x0	CORE3_CFGTE Enable Thumb exceptions, controls the reset value of the SCTLR.TE bit. The options are: 0: TE bit is LOW. 1: TE bit is HIGH.
5	R/W	0x0	CORE3_VINITHI Enable high exception vectors, controls the reset value of the SCTLR.V bit. The options are: 0: Starts exceptions vectors at address 0x00000000. 1: Starts exceptions vectors at address 0xFFFF0000.
4	R/W	0x0	CORE3_CFGEND Endianness configuration, controls the reset value of the SCTLR_EL3/SCTLR_S EE bit. The options are: 0: EE bit is LOW. 1: EE bit is HIGH.
3:1	/	/	/
0	R/W	0x1	CORE3_RESET. Cluster CORE3 Reset Assert. 0: Assert 1: De-assert

5.1.9.8 0x3004 Cluster 0 CPU3 Status0 Register (Default Value: 0x0000_0000)

Offset: 0x3004			Register Name: C0_CPU3_STATUS0
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R	0x0	CORE3_DBGRSTREQ Indicates that core3 Debug reset request
15:13	/	/	/
12	R	0x0	CORE3_INSTRRUN Indicates that core3 is in a running state (powered up and not in WFI or WFE low-power states).
11:9	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x3004			Register Name: C0_CPU3_STATUS0
Bit	Read/Write	Default/Hex	Description
8	R	0x0	CORE3_INSTRRET Indicates that core3 has retired at least one instruction recently.
7:5	/	/	/
4	R	0x0	CORE3_STANDBYWFI. Indicates if Cluster0 CPU3 is in WFI standby mode: 0: Processor not in WFI standby mode. 1: Processor in WFI standby mode
3:1	/	/	/
0	R	0x0	CORE3_STANDBYWFE. Indicates if Cluster0 CPU3 is in the WFE standby mode: 0: Processor not in WFE standby mode 1: Processor in WFE standby mode

5.1.9.9 0x4000 Cluster 0 CPU4 Control Register (Default Value: 0x0000_0001)

Offset: 0x4000			Register Name: C0_CPU4_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10	R/W	0x0	CORE4_EXM1_CLR Clear the status of exclusive monitor1 interface
9	R/W	0x0	CORE4_EXM0_CLR Clear the status of exclusive monitor0 interface
8	R/W	0x0	Core4 CRM auto select slow frequency en. 0: Disable auto select 1: Enable auto select
7	/	/	/
6	R/W	0x0	CORE4_CFGTE Enable Thumb exceptions, controls the reset value of the SCTLR.TE bit. The options are: 0: TE bit is LOW. 1: TE bit is HIGH.
5	R/W	0x0	CORE4_VINITHI Enable high exception vectors, controls the reset value of the SCTLR.V bit. The options are: 0: Starts exceptions vectors at address 0x00000000. 1: Starts exceptions vectors at address 0xFFFF0000.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x4000			Register Name: C0_CPU4_CTRL_REG
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	CORE4_CFGEND Endianness configuration, controls the reset value of the SCTLR_EL3/SCTLR_S EE bit. The options are: 0: EE bit is LOW. 1: EE bit is HIGH.
3:1	/	/	/
0	R/W	0x1	CORE4_RESET. Cluster CORE4 Reset Assert. 0: Assert 1: De-assert

5.1.9.10 0x4004 Cluster 0 CPU4 Status0 Register (Default Value: 0x0000_0000)

Offset: 0x4004			Register Name: C0_CPU4_STATUS0
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R	0x0	CORE4_DBGRSTREQ Indicates that core4 Debug reset request
15:13	/	/	/
12	R	0x0	CORE4_INSTRRUN Indicates that core4 is in a running state (powered up and not in WFI or WFE low-power states).
11:9	/	/	/
8	R	0x0	CORE4_INSTRRET Indicates that core4 has retired at least one instruction recently.
7:5	/	/	/
4	R	0x0	CORE4_STANDBYWFI. Indicates if Cluster0 CPU4 is in WFI standby mode: 0: Processor not in WFI standby mode. 1: Processor in WFI standby mode
3:1	/	/	/
0	R	0x0	CORE0_STANDBYWFE. Indicates if Cluster0 CPU4 is in the WFE standby mode: 0: Processor not in WFE standby mode 1: Processor in WFE standby mode

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.1.9.11 0x5000 Cluster 0 CPU5 Control Register (Default Value: 0x0000_0001)

Offset: 0x5000			Register Name: C0_CPU5_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10	R/W	0x0	CORE5_EXM1_CLR Clear the status of exclusive monitor1 interface
9	R/W	0x0	CORE5_EXM0_CLR Clear the status of exclusive monitor0 interface
8	R/W	0x0	Core5 CRM auto select slow frequency en. 0: Disable auto select 1: Enable auto select
7	/	/	/
6	R/W	0x0	CORE5_CFGTE Enable Thumb exceptions, controls the reset value of the SCTLR.TE bit. The options are: 0: TE bit is LOW. 1: TE bit is HIGH.
5	R/W	0x0	CORE5_VINITHI Enable high exception vectors, controls the reset value of the SCTLR.V bit. The options are: 0: Starts exceptions vectors at address 0x00000000. 1: Starts exceptions vectors at address 0xFFFF0000.
4	R/W	0x0	CORE5_CFGEND Endianness configuration, controls the reset value of the SCTLR_EL3/SCTLR_S EE bit. The options are: 0: EE bit is LOW. 1: EE bit is HIGH.
3:1	/	/	/
0	R/W	0x1	CORE5_RESET. Cluster CORE5 Reset Assert. 0: Assert 1: De-assert

5.1.9.12 0x5004 Cluster 0 CPU5 Status0 Register (Default Value: 0x0000_0000)

Offset: 0x5004			Register Name: C0_CPU5_STATUS0
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R	0x0	CORE5_DBGRSTREQ Indicates that core1 Debug reset request
15:13	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x5004			Register Name: C0_CPU5_STATUS0
Bit	Read/Write	Default/Hex	Description
12	R	0x0	CORE5_INSTRRUN Indicates that core1 is in a running state (powered up and not in WFI or WFE low-power states).
11:9	/	/	/
8	R	0x0	CORE5_INSTRRET Indicates that core1 has retired at least one instruction recently.
7:5	/	/	/
4	R	0x0	CORE5_STANDBYWFI. Indicates if Cluster0 CPU5 is in WFI standby mode: 0: Processor not in WFI standby mode. 1: Processor in WFI standby mode
3:1	/	/	/
0	R	0x0	CORE1_STANDBYWFE. Indicates if Cluster0 CPU5 is in the WFE standby mode: 0: Processor not in WFE standby mode 1: Processor in WFE standby mode

5.1.9.13 0x6000 Cluster 0 CPU6 Control Register (Default Value: 0x0000_0081)

Offset: 0x6000			Register Name: C0_CPU6_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10	R/W	0x0	CORE6_EXM1_CLR Clear the status of exclusive monitor1 interface
9	R/W	0x0	CORE6_EXM0_CLR Clear the status of exclusive monitor0 interface
8	R/W	0x0	Core6 CRM auto select slow frequency en. 0: Disable auto select 1: Enable auto select
7	R/W	0x1	CORE6_MPMMEN Maximum Power Mitigation Mechanism (MPMM) enable signal. The options are: 0: MPMM disabled 1: MPMM enabled
6	R/W	0x0	CORE6_CFGTE Enable Thumb exceptions, controls the reset value of the SCTLR.TE bit. The options are: 0: TE bit is LOW 1: TE bit is HIGH

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x6000			Register Name: C0_CPU6_CTRL_REG
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	CORE6_VINITHI Enable high exception vectors, controls the reset value of the SCTLR.V bit. The options are: 0: Starts exceptions vectors at address 0x00000000. 1: Starts exceptions vectors at address 0xFFFF0000.
4	R/W	0x0	CORE6_CFGEND Endianness configuration, controls the reset value of the SCTLR_EL3/SCTLR_S EE bit. The options are: 0: EE bit is LOW. 1: EE bit is HIGH.
3:1	/	/	/
0	R/W	0x1	CORE6_RESET. Cluster CORE6 Reset Assert. 0: Assert 1: De-assert

5.1.9.14 0x6004 Cluster 0 CPU6 Status0 Register (Default Value: 0x0000_0000)

Offset: 0x6004			Register Name: C0_CPU6_STATUS0
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R	0x0	CORE6_DBGRSTREQ Indicates that core6 Debug reset request
15:13	/	/	/
12	R	0x0	CORE6_INSTRRUN Indicates that core6 is in a running state (powered up and not in WFI or WFE low-power states).
11:9	/	/	/
8	R	0x0	CORE6_INSTRRET Indicates that core6 has retired at least one instruction recently.
7:5	/	/	/
4	R	0x0	CORE6_STANDBYWFI. Indicates if Cluster0 CPU6 is in WFI standby mode: 0: Processor not in WFI standby mode. 1: Processor in WFI standby mode
3:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x6004			Register Name: C0_CPU6_STATUS0
Bit	Read/Write	Default/Hex	Description
0	R	0x0	CORE2_STANDBYWFE. Indicates if Cluster0 CPU6 is in the WFE standby mode: 0: Processor not in WFE standby mode 1: Processor in WFE standby mode

5.1.9.15 0x7000 Cluster 0 CPU7 Control Register (Default Value: 0x0000_0081)

Offset: 0x7000			Register Name: C0_CPU7_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10	R/W	0x0	CORE7_EXM1_CLR Clear the status of exclusive monitor1 interface
9	R/W	0x0	CORE7_EXM0_CLR Clear the status of exclusive monitor0 interface
8	R/W	0x0	Core7 CRM auto select slow frequency en. 0: Disable auto select 1: Enable auto select
7	R/W	0x1	CORE7_MPMMEN Maximum Power Mitigation Mechanism (MPMM) enable signal. The options are: 0: MPMM disabled. 1: MPMM enabled.
6	R/W	0x0	CORE7_CFGTE Enable Thumb exceptions, controls the reset value of the SCTLR.TE bit. The options are: 0: TE bit is LOW. 1: TE bit is HIGH.
5	R/W	0x0	CORE7_VINITHI Enable high exception vectors, controls the reset value of the SCTLR.V bit. The options are: 0: Starts exceptions vectors at address 0x00000000. 1: Starts exceptions vectors at address 0xFFFF0000.
4	R/W	0x0	CORE7_CFGEND Endianness configuration, controls the reset value of the SCTLR_EL3/SCTLR_S EE bit. The options are: 0: EE bit is LOW. 1: EE bit is HIGH.
3:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x7000			Register Name: C0_CPU7_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x1	CORE7_RESET. Cluster CORE7 Reset Assert. 0: Assert 1: De-assert

5.1.9.16 0x7004 Cluster 0 CPU7 Status0 Register (Default Value: 0x0000_0000)

Offset: 0x7004			Register Name: C0_CPU7_STATUS0
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R	0x0	CORE7_DBGRSTREQ Indicates that core7 Debug reset request
15:13	/	/	/
12	R	0x0	CORE7_INSTRRUN Indicates that core7 is in a running state (powered up and not in WFI or WFE low-power states).
11:9	/	/	/
8	R	0x0	CORE7_INSTRRET Indicates that core7 has retired at least one instruction recently.
7:5	/	/	/
4	R	0x0	CORE7_STANDBYWFI. Indicates if Cluster0 CPU7 is in WFI standby mode: 0: Processor not in WFI standby mode. 1: Processor in WFI standby mode
3:1	/	/	/
0	R	0x0	CORE7_STANDBYWFE. Indicates if Cluster0 CPU7 is in the WFE standby mode: 0: Processor not in WFE standby mode 1: Processor in WFE standby mode

5.1.9.17 0x8000 Cluster 0 Reset Control Register (Default Value: 0x0000_03F1)

Offset: 0x8000			Register Name: C0_RST_CTRL
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
9	R/W	0x1	ATB_RST ATB Reset. The reset signal for DSU atbclk domain. 0: Assert 1: de-assert

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x8000			Register Name: C0_RST_CTRL
Bit	Read/Write	Default/Hex	Description
8	R/W	0x1	MBIST_RST CPUBIST Reset. The reset signal for test. 0: Assert 1: de-assert
7	R/W	0x1	BUS_RST Cluster all other bus bridge Reset 0: Assert 1: De-assert
6	R/W	0x1	PERI_RST Cluster Peri Part Reset 0: Assert 1: De-assert
5	R/W	0x1	APB_RST. Cluster Debug APB part Reset 0: Assert 1: De-assert
4	R/W	0x1	GIC_RST cluster gic inner reset 0: Assert 1: De-assert
3:1	/	/	/
0	R/W	0x1	CLU_RST Cluster reset 0: Assert 1: De-assert

5.1.9.18 0x8004 Cluster 0 Control Register0 (Default Value: 0x0000_0008)

Offset: 0x8004			Register Name: C0_CTRL_REG0
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	BROADCAST_CACHEMAINTPOU Enable broadcasting of cache maintenance operations to the point of unification: 0: Cache maintenance operations DCCMVAU and DC CVAU are not broadcast to other clusters. This is more efficient and can be used if all other clusters are based on Arm Cortex cores. 1: Cache maintenance operations DCCMVAU and DC CVAU are broadcast to other clusters.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x8004			Register Name: C0_CTRL_REG0
Bit	Read/Write	Default/Hex	Description
30	R/W	0x0	BROADCAST_PERSIST. Enable broadcasting of cache clean to the point of persistence operations: 0: DC CVAP instructions are treated the same as DC CVAC. 1: DC CVAP instructions sent as a clean to the point of persistence transaction externally.
29	R/W	0x0	BROADCAST_OUTER. Enable broadcasting of outer shareable transactions: 0: Outer Shareable transactions are not broadcasted externally. 1: Outer Shareable transactions are broadcasted externally.
28	R/W	0x0	BROADCAST_CACHE_MAINT Enable broadcasting of cache maintenance operations to downstream caches: 0: Cache maintenance operations are not broadcasted to downstream caches. 1: Cache maintenance operations are broadcasted to downstream caches.
27:13	/	/	/
12	R/W	0x0	Cluster, CRM auto select slow frequency en. 0: Disable auto select 1: Enable auto select
11:4	/	/	/
3	R/W	0x1	DBGCONNEXTED 0: no use 1: A debugger is connected and so the DebugBlock should be accessed on boot.
2	/	/	/
1	R/W	0x0	CRYPTODISABLE Disables the Cryptographic Extension.
0	R/W	0x0	GICCDISABLE Globally disables the CPU interface logic and routes the external interrupt signals directly to the cores.

5.1.9.19 0x8008 Cluster 0 Control Register1 (Default Value: 0x0000_0000)

Offset: 0x8008			Register Name: C0_CTRL_REG1
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x8008			Register Name: C0_CTRL_REG1
Bit	Read/Write	Default/Hex	Description
0	R/WAC	0x0	EVENTI signaled a WFE wake up event.

5.1.9.20 0x800C Clk Control Force Configuration Register (Default Value: 0x0000_003F)

Offset: 0x800C			Register Name: CLK_FORCE_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x1	BUSCLK2_CC_FORCE 1: busclk2 no gating 0: busclk2 auto gating
4	R/W	0x1	BUSCLK1_CC_FORCE 1: busclk1 no gating 0: busclk1 auto gating
3	R/W	0x1	SCLK_CC_FORCE 1: sclk no gating 0: sclk auto gating
2	R/W	0x1	PCLK_CC_FORCE 1: pclk no gating 0: pclk auto gating
1	R/W	0x1	GICCLK_CC_FORCE 1: gicclk no gating 0: gicclk auto gating
0	R/W	0x1	ATCLK_CC_FORCE 1: atclk no gating 0: atclk auto gating

5.1.9.21 0x8010 CPU cluster spram memory Configuration Register (Default Value: 0x0084_1550)

Offset: 0x8010			Register Name: CLUSTER_SPRAM_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:0	R/W	0x841550	DSU_SPRAM_CFG DSU RF1P and SRAM memory control port

5.1.9.22 0x8014 CPU cluster rf2p memory Configuration Register (Default Value: 0x0000_8435)

Offset: 0x8014			Register Name: CLUSTER_RF2P_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x8014			Register Name: CLUSTER_RF2P_CFG_REG
Bit	Read/Write	Default/Hex	Description
29:0	R/W	0x8435	DSU_RF2P_CFG DSU RF2P memory control port

5.1.9.23 0x8018 CPU cluster rfp2p memory Configuration Register (Default Value: 0x0000_0401)

Offset: 0x8018			Register Name: CLUSTER_RFP2P_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:0	R/W	0x401	DSU_RFP2P_CFG cluster RFP2P control port

5.1.9.24 0x801C CPU cluster sysspram memory Configuration Register (Default Value: 0x00A4_1509)

Offset: 0x801C			Register Name: CLUSTER_SYSSPRAM_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:0	R/W	0xa41509	DSU_SYSSPRAM_CFG cluster SYSSPRAM control port

5.1.9.25 0x8020 DSU AXI2TO1 Th Configuration Register (Default Value: 0x0000_0000)

Offset: 0x8020			Register Name: DSU_AXI_TH_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
23:20	R/W	0x0	AW_TH_1 In the course of write operation, when DSU1 accesses AXI2TO1 master in the PCIe channel, the maximum instructions can be sent consecutively.
19:16	R/W	0x0	AW_TH_0 In the course of write operation, when DSU0 accesses AXI2TO1 master in the PCIe channel, the maximum instructions can be sent consecutively.
15:8	/	/	/
7:4	R/W	0x0	AR_TH_1 In the course of read operation, when DSU1 accesses AXI2TO1 master in the PCIe channel, the maximum instructions can be sent consecutively.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x8020			Register Name: DSU_AXI_TH_CFG_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	AR_TH_0 In the course of write operation, when DSU1 accesses AXI2TO1 master in the PCIe channel, the maximum instructions can be sent consecutively.

5.1.9.26 0x8030 Cluster 0 DSU Status Register (Default Value: 0x0000_0000)

Offset: 0x8030			Register Name: CLU_DSU_STATUS_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R	0x0	EVENTOREQ A *Send Event* (SEV) instruction signals a WFE wake up event to other clusters by asserting the EVENTOREQ output.
15:5	/	/	/
4:0	R	0x0	MEM_PRDYN memory power ack signal

5.1.9.27 0x80A4 Cluster 0 DSU reset self release Register (Default Value: 0x0000_0000)

Offset: 0x80A4			Register Name: CLU_DSU_RST_CTRL
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:8	W/R	0x0	DSU_RST_CTL dsu reset control When it is not 0, dsu_rst will be reset and then released.
7:0	/	/	/

5.1.9.28 0x80B0 DSU AXI0 Monitor Control Register (Default Value: 0x0000_0000)

Offset: 0x80B0			Register Name: DSU_AXI0_MNT_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	WC	0x0	AXI0_MONITOR_CLR AXI0 Monitor function clear 0: Not affect 1: Clear

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x80B0			Register Name: DSU_AXI0_MNT_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	AXI0_MONITOR_EN AXI0 Monitor function enable 0: Not enable 1: Enable

5.1.9.29 0x80B4 DSU AXI0 Monitor Period Register (Default Value: 0x0000_0000)

Offset: 0x80B4			Register Name: DSU_AXI0_MNT_PRD_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	AXI0_PERIOD DSU AXI0 Monitor function monitoring period Unit is cycle

5.1.9.30 0x80B8 DSU AXI0 Monitor Read Total Latency Register (Default Value: 0x0000_0000)

Offset: 0x80B8			Register Name: DSU_AXI0_MNT_RLTCY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	AXI0_LATENCY_R DSU AXI0 Monitor function READ channel total latency Unit is cycle

5.1.9.31 0x80BC DSU AXI0 Monitor Write Total Latency Register (Default Value: 0x0000_0000)

Offset: 0x80BC			Register Name: DSU_AXI0_MNT_WLTCY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	AXI0_LATENCY_W DSU AXI0 Monitor function WRITE channel total latency Unit is cycle

5.1.9.32 0x80C0 DSU AXI0 Monitor Read Request Times Register (Default Value: 0x0000_0000)

Offset: 0x80C0			Register Name: DSU_AXI0_MNT_RREQ_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	AXI0_RREQ_TIME DSU AXI0 Monitor function READ channel total times

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.1.9.33 0x80C4 DSU AXI0 Monitor Write Request Times Register (Default Value: 0x0000_0000)

Offset: 0x80C4			Register Name: DSU_AXI0_MNT_WREQ_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	AXI0_WREQ_TIME DSU AXI0 Monitor function WRITE channel total times

5.1.9.34 0x80C8 DSU AXI0 Monitor Read Bandwidth Register (Default Value: 0x0000_0000)

Offset: 0x80C8			Register Name: DSU_AXI0_MNT_RBD_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	AXI0_BANDWIDTH_R DSU AXI0 Monitor function READ channel Bandwidth Unit is KB

5.1.9.35 0x80CC DSU AXI0 Monitor Write Bandwidth Register (Default Value: 0x0000_0000)

Offset: 0x80CC			Register Name: DSU_AXI0_MNT_WBD_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	AXI0_BANDWIDTH_W DSU AXI0 Monitor function WRITE channel Bandwidth Unit is KB

5.1.9.36 0x80D0 DSU AXI1 Monitor Control Register (Default Value: 0x0000_0000)

Offset: 0x80D0			Register Name: DSU_AXI1_MNT_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	WC	0x0	AXI1_MONITOR_CLR AXI1 Monitor function clear 0: Not affect 1: Clear
0	R/W	0x0	AXI1_MONITOR_EN AXI1 Monitor function enable 0: Not enable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.1.9.37 0x80D4 DSU AXI1 Monitor Period Register (Default Value: 0x0000_0000)

Offset: 0x80D4			Register Name: DSU_AXI1_MNT_PRD_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	AXI1_PERIOD DSU AXI1 Monitor function monitoring period Unit is cycle

5.1.9.38 0x80D8 DSU AXI1 Monitor Read Total Latency Register (Default Value: 0x0000_0000)

Offset: 0x80D8			Register Name: DSU_AXI1_MNT_RLTCY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	AXI1_LATENCY_R DSU AXI1 Monitor function READ channel total latency Unit is cycle

5.1.9.39 0x80DC DSU AXI1 Monitor Write Total Latency Register (Default Value: 0x0000_0000)

Offset: 0x80DC			Register Name: DSU_AXI1_MNT_WLTCY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	AXI1_LATENCY_W DSU AXI1 Monitor function WRITE channel total latency Unit is cycle

5.1.9.40 0x80E0 DSU AXI1 Monitor Read Request Times Register (Default Value: 0x0000_0000)

Offset: 0x80E0			Register Name: DSU_AXI1_MNT_RREQ_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	AXI1_RREQ_TIME DSU AXI1 Monitor function READ channel total times

5.1.9.41 0x80E4 DSU AXI1 Monitor Write Request Times Register (Default Value: 0x0000_0000)

Offset: 0x80E4			Register Name: DSU_AXI1_MNT_WREQ_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	AXI1_WREQ_TIME DSU AXI1 Monitor function WRITE channel total times

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.1.9.42 0x80E8 DSU AXI1 Monitor Read Bandwidth Register (Default Value: 0x0000_0000)

Offset: 0x80E8			Register Name: DSU_AXI1_MNT_RBD_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	AXI1_BANDWIDTH_R DSU AXI1 Monitor function READ channel Bandwidth Unit is KB

5.1.9.43 0x80EC DSU AXI1 Monitor Write Bandwidth Register (Default Value: 0x0000_0000)

Offset: 0x80EC			Register Name: DSU_AXI1_MNT_WBD_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	AXI1_BANDWIDTH_W DSU AXI1 Monitor function WRITE channel Bandwidth Unit is KB

5.1.10 CPU_PLL_CFG Register Description

5.1.10.1 0x0000 CPU_BACK_PLL Control Register (Default Value: 0x4010_4A00)

Offset: 0x0000			Register Name: CPU_BACK_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable The CPU_BACK_PLL = InputFreq*N/M1/P0. When DCXO is 26MHz, CPU_BACK_PLL frequency is 975 MHz by default.
30	R/W	0x1	PLL_LDO_EN LDO enable 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: CPU_BACK_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
28	R	0x0	LOCK PLL Lock Info. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x0	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable
26:23	/	/	/
22:20	R/W	0x1	PLL_OUTPUT_DIV. PLL Output Div P0. P0=PLL_OUTPUT_DIV + 1 PLL_OUTPUT_DIV is from 0 to 7.
19:16	/	/	/
15:8	R/W	0x4A	PLL_N PLL Factor N. N= PLL_N +1 PLL_N is from 0 to 254. PLL_N should be no less than 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV. PLL Input Div M1. M1=PLL_INPUT_DIV + 1 PLL_INPUT_DIV is from 0 to 1.
0	/	/	/

5.1.10.2 0x0004 CPU_BACK_PLL Lock Control Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: CPU_BACK_PLL_LOCK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: CPU_BACK_PLL_LOCK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
4	R/WAC	0x0	CPU_BACK_PLL_UNLOCK_STAT CPU_BACK_PLL Unlock Status. set 1 to the bit will clear it. 1: Pending 0: No effect
3:1	/	/	/
0	R/W	0x0	CPU_BACK_PLL_UNLOCK_IRQEN CPU_BACK_PLL Unlock Interrupt Enable 1: Enable 0: Disable

5.1.10.3 0x0008 CPU_BACK_PLL Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CPU_BACK_PLL_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: pulse swallow 01: Triangular (1bit) 10: Triangular (2bit) 11: Triangular (3bit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_DIRECTION. SDM direction. 0: UP 1: DOWN
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

5.1.10.4 0x000C CPU_BACK_PLL Pattern1 Control Register (Default Value: 0x3000_0000)

Offset: 0x000C	Register Name: CPU_BACK_PLL_PAT1_CTRL_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_PI_EN Fraction PI Enable. 0: Disable 1: Enable
30:28	R/W	0x3	PLL_PI_CFG Phase Interpolator bias current control 000: 4u 001: 12u 010: 20u 011: 28u 100: 36u 101: 44u 110: 52u 111: 60u
27	R/W	0x0	PLL_SDM_EN PLL SDM Enable. 0: Disable 1: Enable
26	R	0x0	SDM_BUSY. SDM Busy Status. 0: Not Busy 1: Busy Note: When Smooth is enable, need to check SDM_BUSY before update SDM parameters. Cannot update parameters if sdm is busy.
25	R/W	0x0	SMOOTH_EN. SDM Smooth Enable. 0: Disable 1: Enable
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

5.1.10.5 0x0010 CPU_BACK_PLL Bias Register (Default Value: 0x0015_0000)

Offset: 0x0010			Register Name: CPU_BACK_PLL_BIAS_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0010			Register Name: CPU_BACK_PLL_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x15	PLL_CP. PLL current bias control.
15:0	/	/	/

5.1.10.6 0x1000 CPU_L_PLL Control Register (Default Value: 0x4080_1400)

Offset: 0x1000			Register Name: CPU_L_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_PLL_EN. PLL Enable. 0: Disable. 1: Enable. The CPU_L_PLL= InputFreq*N/P/(M0*M1). The CPU_L_PLL VCO= InputFreq*N/P. Note: 1) CPU_L_PLL VCO input clock frequency should range from 480 MHz to 2.26 GHz. 2) When DCXO is 26 MHz, the CPU_L_PLL frequency is 520 MHz.
30	R/W	0x1	PLL_LDO_EN. LDO enable. 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock info. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x0	PLL_OUTPUT_GATE PLL Output Gating Enable. 0: Disable 1: Enable
26	R/WAC	0x0	PLL_UPDATE Write q update the cfg to pll, auto clear.
25:24	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1000			Register Name: CPU_L_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
23	R/W	0x1	PLL_NDET. PLL_NDET.
22	R/W	0x0	PLL_TDIV. PLL_TDIV.
21:20	R/W	0x0	PLL_M0. PLL_M0. M0 = PLL_M0 + 1 PLL_FACTOR_M0 is from 0 to 3.
19:16	R/W	0x0	PLL_P PLL PREDIV P P = PLL_P + 1
15:8	R/W	0x14	PLL_N PLL N.PLL N is 4/5/8/9/10/12-255. N= PLL_N. The N value range should satisfy the following formula. 480MHz<=InputFreq*N/P/(M0*M1)<=2260MHz
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4	/	/	/
3:0	R/W	0x0	PLL_M1. PLL_M1. M1 = PLL_M1 + 1 PLL_M1 is from 0 to 15.

5.1.10.7 0x1004 CPU_L_PLL Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x1004			Register Name: CPU_L_PLL_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1004			Register Name: CPU_L_PLL_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: reserve 01: Triangular (1bit) 10: Triangular (2bit) 11: Triangular (3bit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_DIRECTION. SDM direction. 0: UP 1: DOWN
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

5.1.10.8 0x1008 CPU_L_PLL Pattern1 Control Register (Default Value: 0x3000_0000)

Offset: 0x1008			Register Name: CPU_L_PLL_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_PI_EN Fraction PI Enable. 0: Disable 1: Enable
30:28	R/W	0x3	PLL_PI_CFG Phase Interpolator bias current control 000: 4u 001: 12u 010: 20u 011: 28u 100: 36u 101: 44u 110: 52u 111: 60u

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1008			Register Name: CPU_L_PLL_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
27	R/W	0x0	PLL_SDM_EN PLL SDM Enable. 0: Disable 1: Enable
26	R	0x0	SDM_BUSY. SDM Busy Status. 0: Not Busy 1: Busy Note: When Smooth is enable, need to check SDM_BUSY before update SDM parameters. Cannot update parameters if sdm is busy.
25	R/W	0x0	SMOOTH_EN. SDM Smooth Enable. 0: Disable 1: Enable
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

5.1.10.9 0x100C CPU_L_PLL Bias Register (Default Value: 0x0005_0000)

Offset: 0x100C			Register Name: CPU_L_PLL_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x05	PLL_CP. PLL current bias control.
15:0	/	/	/

5.1.10.10 0x1010 CPU_L_PLL Tuning0 Register (Default Value: 0x0000_0000)

Offset: 0x1010			Register Name: CPU_L_PLL_TUN0_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	PLL_LPF_SW. PLL_LPF_SW.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1010			Register Name: CPU_L_PLL_TUN0_REG
Bit	Read/Write	Default/Hex	Description
4:2	/	/	/
1:0	R/W	0x0	PLL_FF_SR PLL_FF_SR

5.1.10.11 0x1014 CPU_L_PLL Tuning1 Register (Default Value: 0x0003_2800)

Offset: 0x1014			Register Name: CPU_L_PLL_TUN1_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_SDM_EN. PLL_SDM_EN.
30	R/W	0x0	PLL_FF_EN. PLL_FF_EN.
29	R/W	0x0	PLL_SS_EN. LL_SS_EN.
28:20	R/W	0x0	PLL_SS_FRAC. PLL_SS_FRAC.
19:12	R/W	0x32	PLL_SS_INT. PLL_SS_INT.
11:0	R/W	0x800	PLL_FRAC PLL_FRAC

5.1.10.12 0x1018 CPU_L_PLL LFM Register (Default Value: 0x4000_0000)

Offset: 0x1018			Register Name: CPU_L_PLL_LFM_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_LFM_EN PLL_LFM_EN 0: Disable 1: Enable
30	R/W	0x1	PLL_LFM_RSTN LFM RSTN bake up
29	R/W	0x0	PLL_LFM_CLK_SEL. LFM CLK Select. 1: ref_clk 0: pll_clk_sdm
28:12	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1018			Register Name: CPU_L_PLL_LFM_REG
Bit	Read/Write	Default/Hex	Description
11:0	R/W	0x1	PLL_LFM_STEP PLL_LFM_STEP LFM frequency = fclk*fclk*step/2^17 fclk is reference clock frequency (MHz). The frequency ramping rate unit is MHz/us. 0x1: 0.00439MHz/us (fclk = 24MHz) 0x2: 0.00879MHz/us (fclk = 24MHz) 0x4: 0.01758MHz/us (fclk = 24MHz) 0x8: 0.03516MHz/us (fclk = 24MHz) 0x10: 0.07031MHz/us (fclk = 24MHz) 0x20: 0.14062MHz/us (fclk = 24MHz) 0x40: 0.28125MHz/us (fclk = 24MHz) 0x80: 0.56250MHz/us (fclk = 24MHz) 0x100: 1.12500MHz/us (fclk = 24MHz) 0x200: 2.25000MHz/us (fclk = 24MHz) 0x400: 4.50000MHz/us (fclk = 24MHz) 0x800: 9.00000MHz/us (fclk = 24MHz)

5.1.10.13 0x101C CPU_L_PLL Clock Register (Default Value: 0x0000_0000)

Offset: 0x101C			Register Name: CPU_L_PLL_CLK_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	CPU_L_PLL_CLK_SEL. Clock Source Select. 000,001,010: CPU_SLOW_CLK 011: CPU_L_PLL/P 100: PERI0PLL_DIV2 101: CPU_BACK_PLL CPU0_5_CLK = Clock Source. Note: The clock MUX provides glitch-free switching and supports dynamic configuration.
23:18	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x101C			Register Name: CPU_L_PLL_CLK_REG
Bit	Read/Write	Default/Hex	Description
17:16	R/W	0x0	CPU_L_PLL_OUT_EXT_DIVP. Factor P. 00: 1 01: 2 10: 4 11: \ When the output clock frequency is less than 288MHz, the factor P can be divided to get the required clock frequency.
15:0	/	/	/

5.1.10.14 0x1020 CPU_L_PLL Gating Configuration Register (Default Value: 0x0000_00001)

Offset: 0x1020			Register Name: CPU_L_PLL_GATING_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	CPU_GATING_FIELD CPU Gating Field If CPU_GATING_FIELD=16 h16AA, configure the signal of bit0.
15:1	/	/	/
0	R/W	0x1	CPU_L_PLL_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON

5.1.10.15 0x1024 CPU_L_PLL Unlock IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x1024			Register Name: CPU_L_PLL_UNLOCK_IRQEN_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
0	R/W	0x0	CPU_L_PLL_UNLOCK_IRQEN CPU_L_PLL Unlock Interrupt Enable 1: Enable 0: Disable

5.1.10.16 0x1028 CPU_L_PLL Unlock Status Register (Default Value: 0x0000_0000)

Offset: 0x1028			Register Name: CPU_L_PLL_UNLOCK_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1028			Register Name: CPU_L_PLL_UNLOCK_STAT_REG
Bit	Read/Write	Default/Hex	Description
0	R/WAC	0x0	CPU_L_PLL_UNLOCK_STAT CPU_L_PLL Unlock Status. set 1 to the bit will clear it. 1: Pending 0: No effect

5.1.10.17 0x102C CPU_L_PLL Control Status Register (Default Value: 0x4080_1400)

Offset: 0x102C			Register Name: CPU_L_PLL_CTRL_STAT_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	PLL_PLL_EN PLL Enable 0: Disable 1: Enable Note: CPU_L_PLL output clock frequency ranges from 480MHz to 3GHz. When the DCXO is 26MHz, CPU_L_PLL output clock frequency is 520MHz by default.
30	R	0x1	PLL_LDO_EN. LDO enable. 0: Disable 1: Enable
29	R	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock info. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R	0x0	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable
26	R	0x0	PLL_UPDATE Write q update the cfg to pll, auto clear.
25:24	/	/	/
23	R	0x1	PLL_NDET
22	R	0x0	PLL_TDIV

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x102C			Register Name: CPU_L_PLL_CTRL_STAT_REG
Bit	Read/Write	Default/Hex	Description
21:20	R	0x0	PLL_M0 M0 = PLL_M0 + 1 PLL_FACTOR_M0 is from 0 to 3.
19:16	R	0x0	PLL_P PLL PREDIV P P = PLL_P + 1
15:8	R	0x14	PLL_N PLL N N= PLL_N+1.
7:6	R	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4	/	/	/
3:0	R	0x0	PLL_M1 PLL_M1 M1 = PLL_M1 + 1 PLL_M1 is from 0 to 15.

5.1.10.18 0x2000 CPU_B_PLL Control Register (Default Value: 0x4080_1400)

Offset: 0x2000			Register Name: CPU_B_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_PLL_EN PLL Enable 0: Disable 1: Enable The CPU_B_PLL= InputFreq*N/P/(M0*M1). The CPU_B_PLL VCO= InputFreq*N/P. Note: CPU_B_PLL VCO output clock frequency ranges from 480MHz~2.26GHz. When the DCXO is 26MHz, CPU_B_PLL output clock frequency is 520MHz by default.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x2000			Register Name: CPU_B_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
30	R/W	0x1	PLL_LDO_EN LDO enable. 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x0	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable
26	R/WAC	0x0	PLL_UPDATE Write q update the cfg to pll, auto clear.
25:24	/	/	/
23	R/W	0x1	PLL_NDET
22	R/W	0x0	PLL_TDIV
21:20	R/W	0x0	PLL_M0 M0 = PLL_M0 + 1 PLL_FACTOR_M0 is from 0 to 3.
19:16	R/W	0x0	PLL_P PLL PREDIV P P = PLL_P + 1.
15:8	R/W	0x14	PLL_N PLL N.PLL N is 4/5/8/9/10/12-255. N= PLL_N The N value range should satisfy the formula as below. 480MHz<=InputFreq*N/P/(M0*M1)<=2260MHz
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x2000			Register Name: CPU_B_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4	/	/	/
3:0	R/W	0x0	PLL_M1. PLL_M1. M1 = PLL_M1 + 1 PLL_M1 is from 0 to 15.

5.1.10.19 0x2004 CPU_B_PLL Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x2004			Register Name: CPU_B_PLL_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: reserve 01: Triangular (1bit) 10: Triangular (2bit) 11: Triangular (3bit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_DIRECTION. SDM direction. 0: UP 1: DOWN
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

5.1.10.20 0x2008 CPU_B_PLL Pattern1 Control Register (Default Value: 0x3000_0000)

Offset: 0x2008			Register Name: CPU_B_PLL_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x2008			Register Name: CPU_B_PLL_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_PI_EN Fraction PI Enable. 0: Disable 1: Enable
30:28	R/W	0x3	PLL_PI_CFG Phase Interpolator bias current control 000: 4u 001: 12u 010: 20u 011: 28u 100: 36u 101: 44u 110: 52u 111: 60u
27	R/W	0x0	PLL_SDM_EN PLL SDM Enable. 0: Disable 1: Enable
26	R	0x0	SDM_BUSY. SDM Busy Status. 0: Not Busy 1: Busy Note: When Smooth is enable, need to check SDM_BUSY before update SDM parameters. Cannot update parameters if sdm is busy.
25	R/W	0x0	SMOOTH_EN. SDM Smooth Enable. 0: Disable 1: Enable
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

5.1.10.21 0x200C CPU_B_PLL Bias Register (Default Value: 0x0005_0000)

Offset: 0x200C	Register Name: CPU_B_PLL_BIAS_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x05	PLL_CP. PLL current bias control.
15:0	/	/	/

5.1.10.22 0x2010 CPU_B_PLL Tuning0 Register (Default Value: 0x0000_0000)

Offset: 0x2010			Register Name: CPU_B_PLL_TUN0_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	PLL_LPF_SW PLL_LPF_SW
4:2	/	/	/
1:0	R/W	0x0	PLL_FF_SR PLL_FF_SR

5.1.10.23 0x2014 CPU_B_PLL Tuning1 Register (Default Value: 0x0003_2800)

Offset: 0x2014			Register Name: CPU_B_PLL_TUN1_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_SDM_EN. PLL_SDM_EN.
30	R/W	0x0	PLL_FF_EN. PLL_FF_EN.
29	R/W	0x0	PLL_SS_EN. LL_SS_EN.
28:20	R/W	0x0	PLL_SS_FRAC. PLL_SS_FRAC.
19:12	R/W	0x32	PLL_SS_INT. PLL_SS_INT.
11:0	R/W	0x800	PLL_FRAC. PLL_FRAC.

5.1.10.24 0x2018 CPU_B_PLL LFM Register (Default Value: 0x4000_0000)

Offset: 0x2018			Register Name: CPU_B_PLL_LFM_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_LFM_EN. PLL_LFM_EN. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x2018			Register Name: CPU_B_PLL_LFM_REG
Bit	Read/Write	Default/Hex	Description
30	R/W	0x1	PLL_LFM_RSTN LFM RSTN bake up.
29	R/W	0x0	PLL_LFM_CLK_SEL. LFM CLK Select. 1: ref_clk 0: pll_clk_sdm
28:12	/	/	/
11:0	R/W	0x1	PLL_LFM_STEP. PLL_LFM_STEP. LFM frequency = fclk*fclk*step/2^17. fclk is reference clock frequency (MHz). The frequency ramping rate unit is MHz/us. 0x1: 0.00439MHz/us (fclk = 24MHz) 0x2: 0.00879MHz/us (fclk = 24MHz) 0x4: 0.01758MHz/us (fclk = 24MHz) 0x8: 0.03516MHz/us (fclk = 24MHz) 0x10: 0.07031MHz/us (fclk = 24MHz) 0x20: 0.14062MHz/us (fclk = 24MHz) 0x40: 0.28125MHz/us (fclk = 24MHz) 0x80: 0.56250MHz/us (fclk = 24MHz) 0x100: 1.12500MHz/us (fclk = 24MHz) 0x200: 2.25000MHz/us (fclk = 24MHz) 0x400: 4.50000MHz/us (fclk = 24MHz) 0x800: 9.00000MHz/us (fclk = 24MHz)

5.1.10.25 0x201C CPU_B_PLL Clock Register (Default Value: 0x0000_0000)

Offset: 0x201C			Register Name: CPU_B_PLL_CLK_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	CPU_B_PLL_CLK_SEL. Clock Source Select. 000, 001, 010: CPU_SLOW_CLK 011: CPU_B_PLL/P 100: PERI0PLL_DIV2 101: CPU_BACK_PLL CPU6_7_CLK = Clock Source Note: The clock MUX provides glith-free switching and supports dynamic configuration.
23:18	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x201C			Register Name: CPU_B_PLL_CLK_REG
Bit	Read/Write	Default/Hex	Description
17:16	R/W	0x0	CPU_B_PLL_OUT_EXT_DIVP. Factor P. 00: 1 01: 2 10: 4 11: \ When the output clock frequency is less than 288MHz, the factor P can be divided to get the required clock frequency.
15:0	/	/	/

5.1.10.26 0x2020 CPU_B_PLL Gating Configuration Register (Default Value: 0x0000_00001)

Offset: 0x2020			Register Name: CPU_B_PLL_GATING_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	CPU_GATING_FIELD CPU Gating Field If CPU_GATING_FIELD=16 h16AA, configure the signal of bit0.
15:1	/	/	/
0	R/W	0x1	CPU_B_PLL_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON

5.1.10.27 0x2024 CPU_B_PLL Unlock IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x2024			Register Name: CPU_B_PLL_UNLOCK_IRQEN_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
0	R/W	0x0	CPU_B_PLL_UNLOCK_IRQEN CPU_B_PLL Unlock Interrupt Enable 1: Enable 0: Disable

5.1.10.28 0x2028 CPU_B_PLL Unlock Status Register (Default Value: 0x0000_0000)

Offset: 0x2028			Register Name: CPU_B_PLL_UNLOCK_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x2028			Register Name: CPU_B_PLL_UNLOCK_STAT_REG
Bit	Read/Write	Default/Hex	Description
0	R/WAC	0x0	CPU_B_PLL_UNLOCK_STAT CPU_B_PLL Unlock Status. set 1 to the bit will clear it. 1: Pending 0: No effect

5.1.10.29 0x202C CPU_B_PLL Control Status Register (Default Value: 0x4080_1400)

Offset: 0x202C			Register Name: CPU_B_PLL_CTRL_STAT_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	PLL_PLL_EN. PLL Enable. 0: Disable. 1: Enable. The CPU_B_PLL= InputFreq*N/P/(M0*M1). Note: CPU_B_PLL output clock frequency ranges from 480MHz to 2.26GHz. When the DCXO is 26MHz, CPU_B_PLL output clock frequency is 520MHz by default.
30	R	0x1	PLL_LDO_EN. LDO enable. 0: Disable 1: Enable
29	R	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock info. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R	0x0	PLL_OUTPUT_GATE PLL Output Gating Enable. 0: Disable 1: Enable
26	R	0x0	PLL_UPDATE Write q update the cfg to pll, auto clear.
25:24	/	/	/
23	R	0x1	PLL_NDET. PLL_NDET.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x202C			Register Name: CPU_B_PLL_CTRL_STAT_REG
Bit	Read/Write	Default/Hex	Description
22	R	0x0	PLL_TDIV. PLL_TDIV.
21:20	R	0x0	PLL_M0. PLL_M0. M0 = PLL_M0 + 1 PLL_FACTOR_M0 is from 0 to 3.
19:16	R	0x0	PLL_P. PLL PREDIV P. P = PLL_P + 1.
15:8	R	0x14	PLL_N PLL N. N= PLL_N+1.
7:6	R	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4	/	/	/
3:0	R	0x0	PLL_M1. PLL_M1. M1 = PLL_M1 + 1 PLL_M1 is from 0 to 15.

5.1.10.30 0x3000 CPU_DSU_PLL Control Register (Default Value: 0x4080_1400)

Offset: 0x3000			Register Name: CPU_DSU_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_PLL_EN. PLL Enable. 0: Disable. 1: Enable. The CPU_DSU_PLL= InputFreq*N/P/(M0*M1). The CPU_DSU_PLL VCO= InputFreq*N/P. Note: CPU_B_PLL VCO output clock frequency ranges from 480MHz~2.26GHz. When the DCXO is 26 MHz, CPU_B_PLL output clock frequency is 520 MHz by default.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x3000			Register Name: CPU_DSU_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
30	R/W	0x1	PLL_LDO_EN. LDO enable. 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock info. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x0	PLL_OUTPUT_GATE PLL Output Gating Enable. 0: Disable 1: Enable
26	R/WAC	0x0	PLL_UPDATE Write q update the cfg to pll, auto clear.
25:24	/	/	/
23	R/W	0x1	PLL_NDET. PLL_NDET.
22	R/W	0x0	PLL_TDIV. PLL_TDIV.
21:20	R/W	0x0	PLL_M0. PLL_M0. M0 = PLL_M0 + 1 PLL_FACTOR_M0 is from 0 to 3.
19:16	R/W	0x0	PLL_P. PLL PREDIV P. P = PLL_P + 1.
15:8	R/W	0x14	PLL_N PLL N.PLL N is 4/5/8/9/10/12-255. N= PLL_N. The N value range should satisfy the formula as below. 480MHz<=InputFreq*N/P/(M0*M1)<=2260MHz
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x3000			Register Name: CPU_DSU_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4	/	/	/
3:0	R/W	0x0	PLL_M1. PLL_M1. M1 = PLL_M1 + 1 PLL_M1 is from 0 to 15.

5.1.10.31 0x3004 CPU_DSU_PLL Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x3004			Register Name: CPU_DSU_PLL_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: reserve 01: Triangular (1bit) 10: Triangular (2bit) 11: Triangular (3bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_DIRECTION SDM direction 0: UP 1: DOWN
18:17	R/W	0x0	FREQ Frequency 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

5.1.10.32 0x3008 CPU_DSU_PLL Pattern1 Control Register (Default Value: 0x3000_0000)

Offset: 0x3008			Register Name: CPU_DSU_PLL_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x3008			Register Name: CPU_DSU_PLL_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_PI_EN Fraction PI Enable. 0: Disable 1: Enable
30:28	R/W	0x3	PLL_PI_CFG Phase Interpolator bias current control 000: 4u 001: 12u 010: 20u 011: 28u 100: 36u 101: 44u 110: 52u 111: 60u
27	R/W	0x0	PLL_SDM_EN PLL SDM Enable. 0: Disable 1: Enable
26	R	0x0	SDM_BUSY SDM Busy Status 0: Not Busy 1: Busy Note: When Smooth is enable, need to check SDM_BUSY before update SDM parameters. Cannot update parameters if sdm is busy.
25	R/W	0x0	SMOOTH_EN SDM Smooth Enable 0: Disable 1: Enable
24	R/W	0x0	DITHER_EN Dither Enable
23:21	/	/	/
20	R/W	0x0	FRAC_EN Fraction Enable
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN Fraction In

5.1.10.33 0x300C CPU_DSU_PLL Bias Register (Default Value: 0x0005_0000)

Offset: 0x300C	Register Name: CPU_DSU_PLL_BIAS_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x05	PLL_CP PLL current bias control.
15:0	/	/	/

5.1.10.34 0x3010 CPU_DSU_PLL Tuning0 Register (Default Value: 0x0000_0000)

Offset: 0x3010			Register Name: CPU_DSU_PLL_TUN0_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	PLL_LPF_SW PLL_LPF_SW
4:2	/	/	/
1:0	R/W	0x0	PLL_FF_SR PLL_FF_SR

5.1.10.35 0x3014 CPU_DSU_PLL Tuning1 Register (Default Value: 0x0003_2800)

Offset: 0x3014			Register Name: CPU_DSU_PLL_TUN1_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_SDM_EN PLL_SDM_EN
30	R/W	0x0	PLL_FF_EN PLL_FF_EN
29	R/W	0x0	PLL_SS_EN LL_SS_EN
28:20	R/W	0x0	PLL_SS_FRAC PLL_SS_FRAC
19:12	R/W	0x32	PLL_SS_INT PLL_SS_INT
11:0	R/W	0x800	PLL_FRAC PLL_FRAC

5.1.10.36 0x3018 CPU_DSU_PLL LFM Register (Default Value: 0x4000_0000)

Offset: 0x3018			Register Name: CPU_DSU_PLL_LFM_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_LFM_EN. PLL_LFM_EN. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x3018			Register Name: CPU_DSU_PLL_LFM_REG
Bit	Read/Write	Default/Hex	Description
30	R/W	0x1	PLL_LFM_RSTN LFM RSTN bake up.
29	R/W	0x0	PLL_LFM_CLK_SEL. LFM CLK Select. 1: ref_clk 0: pll_clk_sdm
28:12	/	/	/
11:0	R/W	0x1	PLL_LFM_STEP. PLL_LFM_STEP. LFM frequency = fclk*fclk*step/2^17. fclk is reference clock frequency (MHz). The frequency ramping rate unit is MHz/us. 0x1: 0.00439MHz/us (fclk = 24MHz) 0x2: 0.00879MHz/us (fclk = 24MHz) 0x4: 0.01758MHz/us (fclk = 24MHz) 0x8: 0.03516MHz/us (fclk = 24MHz) 0x10: 0.07031MHz/us (fclk = 24MHz) 0x20: 0.14062MHz/us (fclk = 24MHz) 0x40: 0.28125MHz/us (fclk = 24MHz) 0x80: 0.56250MHz/us (fclk = 24MHz) 0x100: 1.12500MHz/us (fclk = 24MHz) 0x200: 2.25000MHz/us (fclk = 24MHz) 0x400: 4.50000MHz/us (fclk = 24MHz) 0x800: 9.00000MHz/us (fclk = 24MHz)

5.1.10.37 0x301c CPU_DSU_PLL Clock Register (Default Value: 0x0000_0105)

Offset: 0x301c			Register Name: CPU_DSU_PLL_CLK_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x301c			Register Name: CPU_DSU_PLL_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CPU_CLK_SEL. Clock Source Select. 000,001,010: CPU_SLOW_CLK 011: CPU_DSU_PLL/P 100: CPU0PLL 101: PERI0_600M DSU_CLK = Clock Source. CPU_AXI Clock = DSU_CLK/M. CPU_APB Clock= DSU_CLK/N. CPU_GIC Clock=DSU_CLK/M1. Note: The clock MUX provides glith-free switching and supports dynamic configuration.
23:18	/	/	/
17:16	R/W	0x0	CPU_DSU_PLL_OUT_EXT_DIVP. Factor P. 00: 1 01: 2 10: 4 11: \ When the output clock frequency is less than 288MHz, the factor P can be divided to get the required clock frequency.
15:10	/	/	/
9:8	R/W	0x1	DSU_APB_DIV_CFG. Factor N. (N = FACTOR_N +1) FACTOR_N only supports 1 and 3. Note: The clock MUX provides glith-free switching and supports dynamic configuration.
7:4	/	/	/
3:2	R/W	0x1	DSU_PERI_DIV_CFG. Factor M1:(M= FACTOR_M1 +1) FACTOR_M1 only supports 1 and 3. Note: The clock DIV provides glith-free switching and supports dynamic configuration.
1:0	R/W	0x1	DSU_AXI_DIV_CFG. Factor M:(M= FACTOR_M +1) FACTOR_M only supports 0, 1, and 3. Note: The clock DIV provides glith-free switching and supports dynamic configuration.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.1.10.38 0x3020 CPU_DSU_PLL Gating Configuration Register (Default Value: 0x0000_0001)

Offset: 0x3020			Register Name: CPU_DSU_PLL_GATING_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	CPU_GATING_FIELD CPU Gating Field If CPU_GATING_FIELD=16 h16AA, configure the signal of bit[15:0].
15:5	/	/	/
4	R/W	0x0	DSU_PPU_SW_GATE_EN DSU PPU Control Enable 0: Disable 1: Enable
3:1	/	/	/
0	R/W	0x1	DSU_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON

5.1.10.39 0x3024 CPU_DSU_PLL Unlock IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x3024			Register Name: CPU_DSU_PLL_UNLOCK_IRQEN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	CPU_DSU_PLL_UNLOCK_IRQEN CPU_DSU_PLL Unlock Interrupt Enable 1: Enable 0: Disable

5.1.10.40 0x3028 CPU_DSU_PLL Unlock Status Register (Default Value: 0x0000_0000)

Offset: 0x3028			Register Name: CPU_DSU_PLL_UNLOCK_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/WAC	0x0	CPU_DSU_PLL_UNLOCK_STAT CPU_DSU_PLL Unlock Status. set 1 to the bit will clear it. 1: Pending 0: No effect

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.1.10.41 0x302C CPU_DSU_PLL Control Status Register (Default Value: 0x4080_1400)

Offset: 0x302C			Register Name: CPU_DSU_PLL_CTRL_STAT_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	PLL_PLL_EN. PLL Enable. 0: Disable. 1: Enable. The CPU_DSU_PLL= InputFreq*N/P/(M0*M1). Note: CPU_B_PLL output clock frequency ranges from 480MHz to 2.26GHz. When the DCXO is 26 MHz, CPU_B_PLL output clock frequency is 520 MHz by default.
30	R	0x1	PLL_LDO_EN LDO enable 0: Disable 1: Enable
29	R	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R	0x0	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable
26	R	0x0	PLL_UPDATE Write q update the cfg to pll, auto clear.
25:24	/	/	/
23	R	0x1	PLL_NDET PLL_NDET
22	R	0x0	PLL_TDIV PLL_TDIV
21:20	R	0x0	PLL_M0 PLL_M0 M0 = PLL_M0 + 1 PLL_FACTOR_M0 is from 0 to 3.
19:16	R	0x0	PLL_P PLL PREDIV P. P = PLL_P + 1.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x302C			Register Name: CPU_DSU_PLL_CTRL_STAT_REG
Bit	Read/Write	Default/Hex	Description
15:8	R	0x14	PLL_N PLL N. N= PLL_N+1. The N value range should satisfy the formula as below. 480MHz<=InputFreq*N/P/(M0*M1)<=2260MHz
7:6	R	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4	/	/	/
3:0	R	0x0	PLL_M1 PLL_M1 M1 = PLL_M1 + 1 PLL_M1 is from 0 to 15.
7:0	/	/	/

5.1.10.42 0x3034 CPU Slow Clock Select Register (Default Value: 0x0000_0000)

Offset: 0x3034			Register Name: CPU_SLOW_CLK_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	CPU_SLOW_CLK_SEL Clock select 00: DCXO 01: CLK32K 10: CLK16M_RC CPU_SLOW_CLK=Clock select

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.2 RISC-V E902 Subsystem

5.2.1 Overview

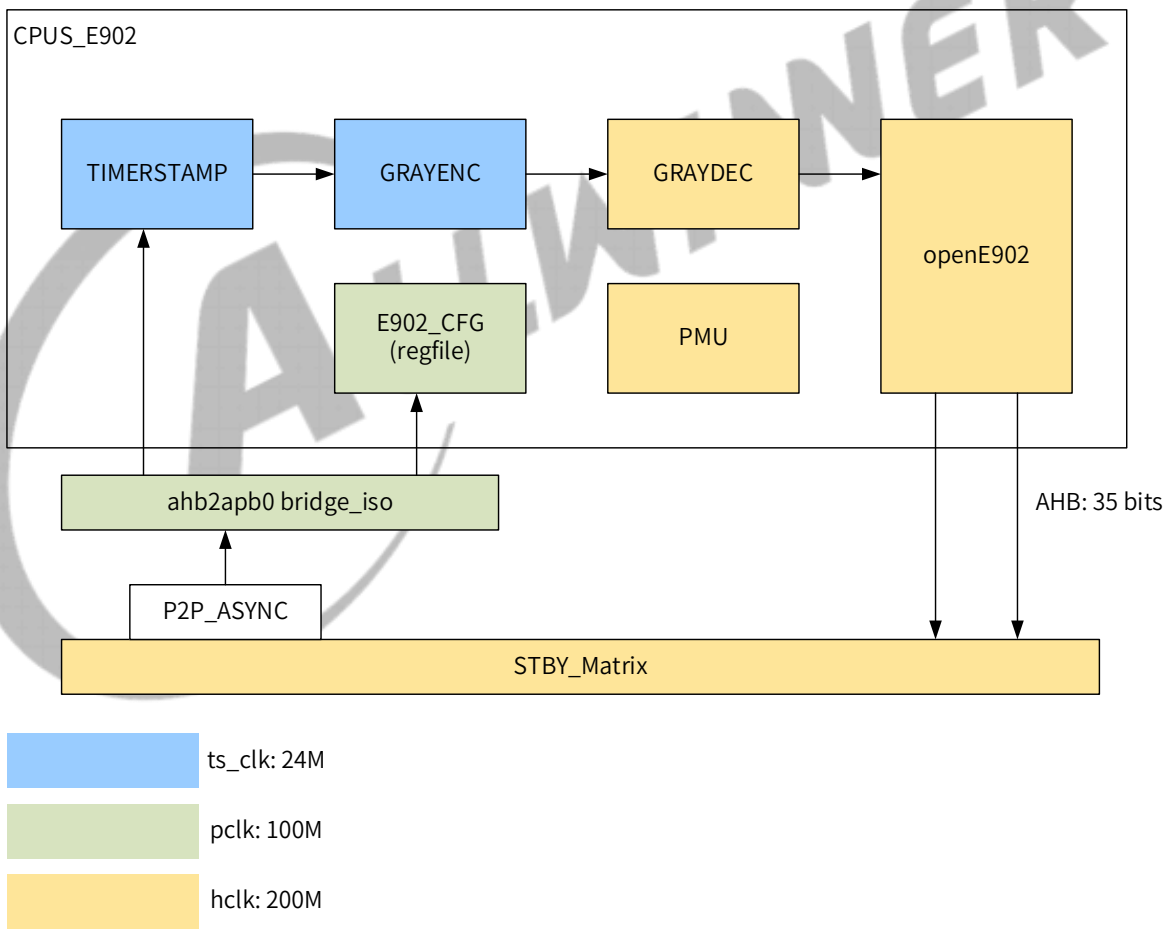
The RISC-V system includes RISC IP core and related peripheral devices (CPUs_E902_CFG, TIMERSTAMP, TIMER_GRAYDEC, TIMER_GRAYENC, and so on), which is able to be interconnected to CPUX system by STBY AHB Matrix.

The RISC-V system has the following features:

Configurable start address via software

- Separate TIMERSTAMP supports counting immediately after reset is released.
- Supports the access to 16GB DRAM.

5.2.2 Block Diagram



5.2.3 Register List

Module Name	Base Address	Comments

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

E902_CFG	0x07032000	

Register Name	Offset	Description
E902_AUTO_GATING_REG	0x0004	E902 Auto Gating Register
E902_DDR_REMAP_REG	0x0020	E902 DDR Remap Register
E902_TS_TMODE_SEL_REG	0x0040	E902 Timestamp Test Mode Select Register
E902_WAKEUP_IRQ_NUM_REG	0x0060	E902 Wakeup IRQ Number Register
E902_WAKEUP_MASK0_REG	0x0064	E902 Wakeup Mask0 Register
E902_WAKEUP_MASK1_REG	0x0068	E902 Wakeup Mask1 Register
E902_PAD_LPMD_REG	0x0080	E902 Low Power Mode Register
E902_RST_START_ADDR_REG	0x0204	E902 RST Start Address Register

5.2.4 Register Description

5.2.4.1 0x0004 E902 Auto Gating Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: E902_AUTO_GATING_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	E902_AUTOGATE_EN The auto gating control of E902_core is used for module consumption reduction. 0: Disable auto gating 1: Reserved

5.2.4.2 0x0020 E902 DDR Remap Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: E902_DDR_REMAP_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	E902_DDR_REMAP. E902 DRAM Access Addr(0x0_8000_0000~0x0_BFFF_FFFF) Remap Control. 0000: No remap DRAM Space 1G - 2G 0x0_8000_0000~0x0_BFFF_FFFF --->no remap 0001: DRAM Space 2G - 3G 0x0_8000_0000~0x0_BFFF_FFFF ---> 0x0_C000_0000~0x0_FFFF_FFFF 0010: DRAM Space 3G - 4G 0x0_8000_0000~0x0_BFFF_FFFF --->

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0020			Register Name: E902_DDR_REMAP_REG
Bit	Read/Write	Default/Hex	Description
			0x1_0000_0000~0x1_3FFF_FFFF 0011: DRAM Space 4G - 5G 0x0_8000_0000~0x0_BFFF_FFFF ---> 0x1_4000_0000~0x1_7FFF_FFFF 0100: DRAM Space 5G - 6G 0x0_8000_0000~0x0_BFFF_FFFF ---> 0x1_8000_0000~0x1_BFFF_FFFF 0101: DRAM Space 6G - 7G 0x0_8000_0000~0x0_BFFF_FFFF ---> 0x1_C000_0000~0x1_FFFF_FFFF 0110: DRAM Space 7G - 8G 0x0_8000_0000~0x0_BFFF_FFFF ---> 0x2_0000_0000~0x2_3FFF_FFFF 0111: DRAM Space 8G - 9G 0x0_8000_0000~0x0_BFFF_FFFF ---> 0x2_4000_0000~0x2_7FFF_FFFF 1000: DRAM Space 9G - 10G 0x0_8000_0000~0x0_BFFF_FFFF ---> 0x2_8000_0000~0x2_BFFF_FFFF 1001: DRAM Space 10G - 11G 0x0_8000_0000~0x0_BFFF_FFFF ---> 0x2_C000_0000~0x2_FFFF_FFFF 1010: DRAM Space 11G - 12G 0x0_8000_0000~0x0_BFFF_FFFF ---> 0x3_0000_0000~0x3_3FFF_FFFF 1011: DRAM Space 12G - 13G 0x0_8000_0000~0x0_BFFF_FFFF ---> 0x3_4000_0000~0x3_7FFF_FFFF 1100: DRAM Space 13G - 14G 0x0_8000_0000~0x0_BFFF_FFFF ---> 0x3_8000_0000~0x3_BFFF_FFFF 1101: DRAM Space 14G - 15G 0x0_8000_0000~0x0_BFFF_FFFF ---> 0x3_C000_0000~0x3_FFFF_FFFF 1110: DRAM Space 15G - 16G 0x0_8000_0000~0x0_BFFF_FFFF ---> 0x4_0000_0000~0x4_3FFF_FFFF 1111: No remap DRAM Space 1G - 2G 0x0_8000_0000~0x0_BFFF_FFFF --->no remap

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.2.4.3 0x0040 E902 Timestamp Test Mode Select Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: E902_TS_TMODE_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	E902_TS_TEST_MODE_EN. E902 Timestamp Test Mode Enable. 0: Normal Mode 1:Test Mode
0	/	/	/

Note: In the test mode, this Counter Low/Hi registers will count simultaneously.

5.2.4.4 0x0060 E902 Wakeup IRQ Number Register (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: E902_WAKEUP_IRQ_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
6:0	R	0x0	E902_WAKEUP_IRQ_SEQ. Recording First Wakeup IRQ number, only takes effect when register E902_AUTOGATE_EN is enable.

5.2.4.5 0x0064 E902 Wakeup Mask0 Register (Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: E902_WAKEUP_MASK0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	WP_MASK0. Wakeup Mask0.

Note: The 0x64 and 0x68 registers correspond to 64 interrupt wakeup enable, which are disabled by default. When some interrupt can be waked up, the corresponding bit should be set to 1. The MASK0 bit0 indicates the interrupt number 16.

5.2.4.6 0x0068 E902 Wakeup Mask1 Register (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: E902_WAKEUP_MASK1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	WP_MASK1. Wakeup Mask1.

Note: The 0x64 and 0x68 registers correspond to 64 interrupt wakeup enable, which are disabled by default. When some interrupt can be waked up, the corresponding bit should be set to 1. The MASK1 bit0 indicates the interrupt number 48.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.2.4.7 0x0080 E902 Low Power Mode Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: E902_PAD_LPMD_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R	0x3	E902_PAD_LPMD_B The states in low-power mode sysio_pad_lpmd_b[1:0] will be altered when the processor executes WFI instructions. 00: Deep sleep 00: Light sleep 10: Reserved 11: Normal working mode

5.2.4.8 0x0204 E902 RST Start Address Register (Default Value: 0x4001_4000)

Offset: 0x0204			Register Name: E902_RST_START_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x40014000	E902_RST_START_ADDR bit0 is fixed to 0, and cannot be written.

Note: It is the running PC address when E902 reset is released. Before this, configure the register as dynamic configuration is not supported.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.3 NPU

The NPU has the following features.

- Primary APIs
  - OpenVX 1.3
  - OpenVX 1.2 Neural Network Extension
  - OpenCL 3.0/1.2
- Additional APIs
  - VivanteVX
  - Vivante Extensions for OpenCL
  - Vivante Extensions for OpenVX
  - Vivante Extensions for Convolutional Neural Networks
- Enhanced Vision Instructions
  - EVIS 1 and EVIS 2 Instruction Sets
- Drivers
  - OpenVX 1.3
  - OpenCL 3.0/1.2
- Primary operating systems
  - Embedded Linux
  - Android 11.0/10.0/9.0/8.0
- Parallel processing units
  - Programmable Scalable Ultra-threaded execution unit (SIMD4: transcendental, ctl-flow)
  - One instruction issue per PPU per clock; IEEE 32-bit floating-point pipeline supports long instructions
- Code and data memory location restrictions
  - Unrestricted; arbitrary memory reads and writes

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

6 Interprocessor Communication

6.1 Message Box (MSGBOX)

6.1.1 Overview

The Message Box (MSGBOX) provides interrupt communication mechanism for microprocessors.

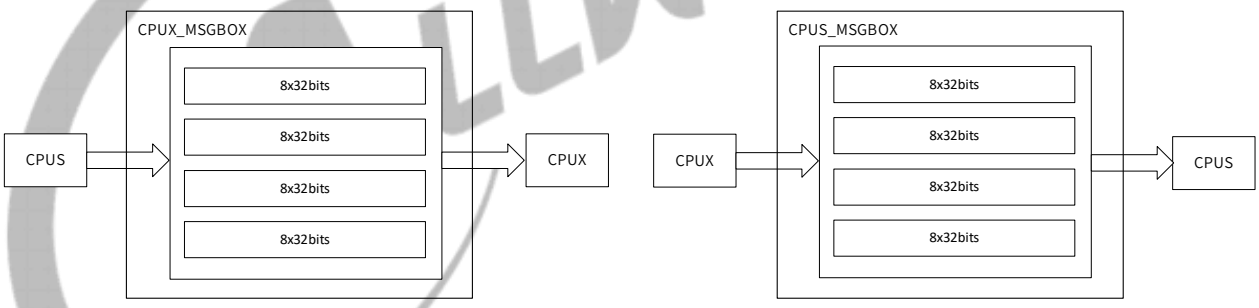
The MSGBOX has the following features:

- Supports two CPUs to transmit information through one-way channels. Each CPU has a MSGBOX and can only read or write in one communication
  - CPUX_MSGBOX: CPUS write, CPUX read
  - CPUS_MSGBOX: CPUX write, CPUS read
- The channel between two CPUs has 4 channels, and the FIFO depth of each is 8x32 bits.

6.1.2 Block Diagram

The following figure shows the block diagram of the message box.

Figure 6-1 Message Box Block Diagram



Each CPU has 4 channels. The two channels can be configured to be secure by software, the other two channels can be configured to be non-secure by software. The two secure channels or two non-secure channels can be configured as one synchronous box (Sending a message requires a response) or one asynchronous box (Sending a message requires no response).

6.1.3 Clock Sources

The MSGBOX is mounted on AHB. Before accessing the MSGBOX registers, you need to de-assert the MSGBOX reset signal on AHB bus and then open the MSGBOX gating signal on AHB bus.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.1.4 Functional Description

6.1.4.1 Interrupt

Each channel can independently configure the interrupt enable bit. A read interrupt will be generated when the channel is not empty, while a write interrupt will be generated when the channel is not full. For each CPU, all channels can generate read interrupts, that is, if only a channel is non-full, the read interrupt will be generated. The channel that generates interrupts can be queried by the interrupt status register.

6.1.4.2 FIFO Status

When channel FIFO is non-full, the MSGBOX_FIFO_STATUS_REG [0]is 0. At the moment, the FIFO can be written.

When channel FIFO is full, the MSGBOX_FIFO_STATUS_REG [0] is 1. At the moment, if FIFO is written again, the previous data will be covered.

6.1.4.3 Transmitter/Receiver Mode

At the same channel, user1 is fixed as transmitter, user0 is fixed as receiver.

6.1.5 Programming Guidelines

6.1.5.1 Check the Transfer Status via the Interrupt

Follow the steps below to check the transfer status:

Step 1 Enable the interrupts: Configure the interrupt enable bits of transmitter/receiver through MSGBOX_RD_IRQ_EN_REG/MSGBOX_WR_IRQ_EN_REG.

Step 2 Check the IRQ status of the corresponding queue through MSGBOX_RD_IRQ_STATUS_REG/MSGBOX_WR_IRQ_STATUS_REG.

- If the FIFO is not full, the channel will generate a transmission interrupt to remind the transmitter to transmit data. Write data to the FIFO in the interrupt handler, then clear the pending bit of the transmitter in MSGBOX_WR_IRQ_STATUS_REG and the enable bit of the transmitter in MSGBOX_WR_IRQ_EN_REG.
- If the FIFO is filled with new data, the channel generates a reception interrupt to remind the receiver to receive data. Read data from the FIFO in interrupt handler, then clear the pending bit of the receiver in MSGBOX_RD_IRQ_STATUS_REG and the enable bit of the receiver in MSGBOX_RD_IRQ_EN_REG.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.1.5.2 Check the Transfer Status via the FIFO

Follow the steps below to check the FIFO status of the corresponding queue:

- If the FIFO is not full, the transmitter fills the FIFO with 8*32 bits.
- If the FIFO is full, the receiver reads the FIFO data, and reads MSGBOX_FIFO_STATUS_REG to acquire the current FIFO data amount and the FIFO data amount before reading to ensure that no data is dropped.

6.1.5.3 Transmit/Receive Message

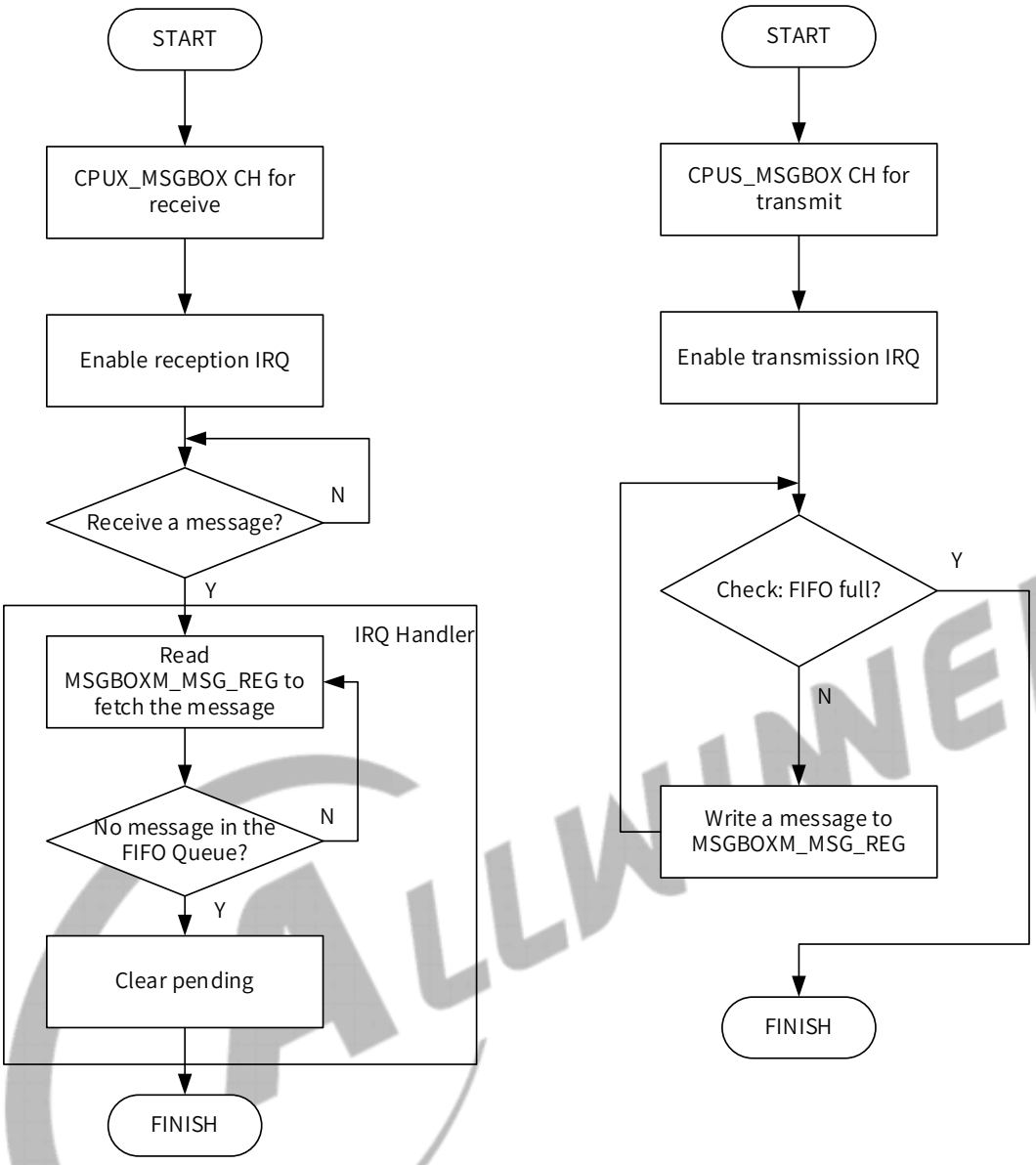
The following figure takes the example of CPUX_MSGBOX and CPUS_MSGBOX to show the message transmitting and receiving of CPUs.

CPUX_MSGBOX: Receiving message

CPUS_MSGBOX: Transmitting message

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 6-2 The Communication Process between CPUX_MSGBOX and CPUS_MSGBOX



6.1.6 Register List

Module Name	Base Address
MBOX_CPUX	0x03004000
MBOX_CPUS	0x07094000

Parameter	Description	Value
N	The number of other CPUs communicating with the CPU	0
P	The channel number of two CPUs	0-3

MSGBOX	CPU	The Value of N

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

MSGBOX	CPU	The Value of N
MBOX_CPUX	CPUS->CPUX	N=0
MBOX_CPUS	CPUX->CPUS	N=0

Register Name	Offset	Description
MSGBOX_RD_IRQ_EN_REG	0x0020+N*0x0100 (N=0)	MSGBOX Read IRQ Enable Register
MSGBOX_RD_IRQ_STATUS_REG	0x0024+N*0x0100 (N=0)	MSGBOX Read IRQ Status Register
MSGBOX_WR_IRQ_EN_REG	0x0030+N*0x0100 (N=0)	MSGBOX Write IRQ Enable Register
MSGBOX_WR_IRQ_STATUS_REG	0x0034+N*0x0100 (N=0)	MSGBOX Write IRQ Status Register
MSGBOX_DEBUG_REG	0x0040+N*0x0100 (N=0)	MSGBOX Debug Register
MSGBOX_FIFO_STATUS_REG	0x0050+N*0x0100+P*0x0004 (N=0)(P=0~3)	MSGBOX FIFO Status Register
MSGBOX_MSG_STATUS_REG	0x0060+N*0x0100+P*0x0004 (N=0)(P=0~3)	MSGBOX Message Status Register
MSGBOX_MSG_REG	0x0070+N*0x0100+P*0x0004 (N=0)(P=0~3)	MSGBOX Message Queue Register
MSGBOX_WR_INT_THRESHOLD_REG	0x0080+N*0x0100+P*0x0004 (N=0)(P=0~3)	MSGBOX Write IRQ Threshold Register

6.1.7 Register Description

6.1.7.1 0x0020+N*0x0100 (N=0) MSGBOX Read IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0020+N*0x0100 (N=0)			Register Name: MSGBOX_RD_IRQ_EN_REG
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6	R/W	0x0	RECEPTION_MQ3_IRQ_EN Reception Channel3 Interrupt Enable 0: Disable 1: Enable (It will notify user 0 by interrupts when Message Queue 3 has received a new message.)
5	/	/	/
4	R/W	0x0	RECEPTION_MQ2_IRQ_EN Reception Channel2 Interrupt Enable 0: Disable 1: Enable (It will notify user 0 by interrupts when Message Queue 2 has received a new message.)

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0020+N*0x0100 (N=0)			Register Name: MSGBOX_RD_IRQ_EN_REG
Bit	R/W	Default/Hex	Description
3	/	/	/
2	R/W	0x0	RECEPTION_MQ1_IRQ_EN Reception Channel1 Interrupt Enable 0: Disable 1: Enable (It will notify user 0 by interrupts when Message Queue 1 has received a new message.)
1	/	/	/
0	R/W	0x0	RECEPTION_MQ0_IRQ_EN Reception Channel0 Interrupt Enable 0: Disable 1: Enable (It will notify user 0 by interrupt when Message Queue 0 has received a new message.)

6.1.7.2 0x0024+N*0x0100 (N=0) MSGBOX Read IRQ Status Register (Default Value: 0x0000_0000)

Offset: 0x0024+N*0x0100 (N=0)			Register Name: MSGBOX_RD_IRQ_STATUS_REG
Bit	R/W	Default/Hex	Description
31:3	/	/	/
6	R/W	0x0	RECEPTION_MQ3_IRQ_PEND Reception Channel3 Interrupt Pending 0: No effect 1: Pending. This bit will be pending for user 0 when Message Queue 3 has received a new message. Setting 1 to this bit will clear it.
5	/	/	/
4	R/W	0x0	RECEPTION_MQ2_IRQ_PEND Reception Channel2 Interrupt Pending 0: No effect 1: Pending. This bit will be pending for user 0 when Message Queue 2 has received a new message. Setting 1 to this bit will clear it.
3	/	/	/
2	R/W	0x0	RECEPTION_MQ1_IRQ_PEND Reception Channel1 Interrupt Pending 0: No effect 1: Pending. This bit will be pending for user 0 when Message Queue 1 has received a new message. Setting 1 to this bit will clear it.
1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0024+N*0x0100 (N=0)			Register Name: MSGBOX_RD_IRQ_STATUS_REG
Bit	R/W	Default/Hex	Description
0	R/W	0x0	RECEPTION_MQ0_IRQ_PEND Reception Channel0 Interrupt Pending 0: No effect 1: Pending. This bit will be pending for user 0 when Message Queue 0 has received a new message. Setting 1 to this bit will clear it.

6.1.7.3 0x0030+N*0x0100 (N=0) MSGBOX Write IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0030+N*0x0100 (N=0)			Register Name: MSGBOX_WR_IRQ_EN_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TRANSMIT_MQ3_IRQ_EN Transmit Channel3 Interrupt Enable 0: Disable 1: Enable (It will notify user 1 by interrupts when Message Queue 3 empty level reach the configured threshold.)
6	/	/	/
5	R/W	0x0	TRANSMIT_MQ2_IRQ_EN Transmit Channel2 Interrupt Enable 0: Disable 1: Enable (It will notify user 1 by interrupt when Message Queue 2 empty level reach the configured threshold.)
4	/	/	/
3	R/W	0x0	TRANSMIT_MQ1_IRQ_EN Transmit Channel1 Interrupt Enable 0: Disable 1: Enable (It will notify user 1 by interrupt when Message Queue 1 empty level reach the configured threshold.)
2	/	/	/
1	R/W	0x0	TRANSMIT_MQ0_IRQ_EN. Transmit Channel0 Interrupt Enable 0: Disable 1: Enable (It will notify user 1 by interrupt when Message Queue 0 empty level reach the configured threshold.)
0	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.1.7.4 0x0034+N*0x0100 (N=0) MSGBOX Write IRQ Status Register (Default Value: 0x0000_0000)

Offset: 0x0034+N*0x0100 (N=0)			Register Name: MSGBOX_WR_IRQ_STATUS_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TRANSMIT_MQ3_IRQ_PEND Transmit Channel3 Interrupt Pending 0: No effect 1: Pending. This bit will be pending for user 1 when Message Queue 3 empty level reach the configured threshold. Setting 1 to this bit will clear it.
6	/	/	/
5	R/W	0x0	TRANSMIT_MQ2_IRQ_PEND Transmit Channel2 Interrupt Pending 0: No effect 1: Pending. This bit will be pending for user 1 when Message Queue 2 empty level reach the configured threshold. Setting 1 to this bit will clear it.
4	/	/	/
3	R/W	0x0	TRANSMIT_MQ1_IRQ_PEND. Transmit Channel1 Interrupt Pending. 0: No effect 1: Pending. This bit will be pending for user 1 when Message Queue 1 empty level reach the configured threshold. Setting 1 to this bit will clear it.
2	/	/	/
1	R/W	0x0	TRANSMIT_MQ0_IRQ_PEND Transmit Channel0 Interrupt Pending 0: No effect 1: Pending. This bit will be pending for user 1 when Message Queue 0 empty level reach the configured threshold. Setting 1 to this bit will clear it.
0	/	/	/

6.1.7.5 0x0040+N*0x0100 (N=0) MSGBOX Debug Register (Default Value: 0x0000_0000)

Offset: 0x0040+N*0x0100 (N=0)			Register Name: MSGBOX_DEBUG_REG
Bit	R/W	Default/Hex	Description
31:12	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0040+N*0x0100 (N=0)			Register Name: MSGBOX_DEBUG_REG
Bit	R/W	Default/Hex	Description
11:8	R/W	0x0	FIFO_CTRL FIFO Control MQ[7:0] Control. In the debug mode, the corresponding FIFO channel will disable and only one register space valid for a message exchange. 0: Normal Mode 1: Disable the corresponding FIFO (Clear FIFO)
7:1	/	/	/
0	R/W	0x0	DEBUG_MODE Debug Mode In the Debug Mode, each user can transmit messages to itself through each Message Queue. 0: Normal Mode 1: Debug Mode

6.1.7.6 0x0050+N*0x0100+P*0x0004(N=0) (P=0~3) MSGBOX FIFO Status Register (Default Value: 0x0000_0000)

Offset: 0x0050+N*0x0100+P*0x0004 (N=0) (P=0~3)			Register Name: MSGBOX_FIFO_STATUS_REG
Bit	R/W	Default/Hex	Description
31: 1	/	/	/
0	R	0x0	FIFO_NOT_AVA_FLAG FIFO is not available flag 0: The Message FIFO queue empty level reached the configured threshold 1: The Message FIFO queue empty level is not reached the configured threshold This FIFO status register has the status related to the message queue.

6.1.7.7 0x0060+N*0x0100+P*0x0004 (N=0) (P=0~3) MSGBOX Message Status Register (Default Value: 0x0000_0000)

Offset: 0x0060+N*0x0100+P*0x0004 (N=0) (P=0~3)			Register Name: MSGBOX_MSG_STATUS_REG
Bit	R/W	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0060+N*0x0100+P*0x0004 (N=0) (P=0~3)			Register Name: MSGBOX_MSG_STATUS_REG
Bit	R/W	Default/Hex	Description
3:0	R	0x0	MSG_NUM Message Number Number of unread messages in the message queue. Here, limited to eight messages per message queue. 0000: There is no message in the message FIFO queue. 0001: There is 1 message in the message FIFO queue. 0010: There are 2 messages in the message FIFO queue. 0011: There are 3 messages in the message FIFO queue. 0100: There are 4 messages in the message FIFO queue. 0101: There are 5 messages in the message FIFO queue. 0110: There are 6 messages in the message FIFO queue. 0111: There are 7 messages in the message FIFO queue. 1000: There are 8 messages in the message FIFO queue. 1001~1111:/

6.1.7.8 0x0070+N*0x0100+P*0x0004 (N=0) (P=0~3) MSGBOX Message Queue Register (Default Value: 0x0000_0000)

Offset: 0x0070+N*0x0100+P*0x0004 (N=0) (P=0~3)			Register Name: MSGBOX_MSG_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	MSG_QUE The message register stores the to-be-read message of the message FIFO queue. Reading will remove the message from the FIFO queue.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.1.7.9 0x0080+N*0x0100+P*0x0004 (N=0) (P=0~3) MSGBOX Write IRQ Threshold Register (Default Value: 0x0000_0000)

Offset: 0x0080+N*0x0100+P*0x0004 (N=0) (P=0~3)			Register Name: MSGBOX_WR_INT_THRESHOLD_REG
Bit	R/W	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	MSG_WR_INT_THRESHOLD_CFG Configure the FIFO empty level to trigger the write interrupt for user1. 00: 7 01: 6 10: 4 11: 0

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.2 Spinlock

6.2.1 Overview

The spinlock provides hardware synchronization mechanism in multi-core systems. With the lock operation, the spinlock prevents multiple processors from handling the sharing data simultaneously and thus ensure the coherence of data.

The spinlock has the following features:

- Supports 32 lock units
- Two kinds of lock status: locked and unlocked
- Lock time of the processor is predictable (less than 200 cycles)

6.2.2 Clock Sources

The spinlock is mounted on AHB. Before accessing the spinlock registers, you need to de-assert the reset signal on AHB bus and then open the corresponding gating signal on AHB bus.

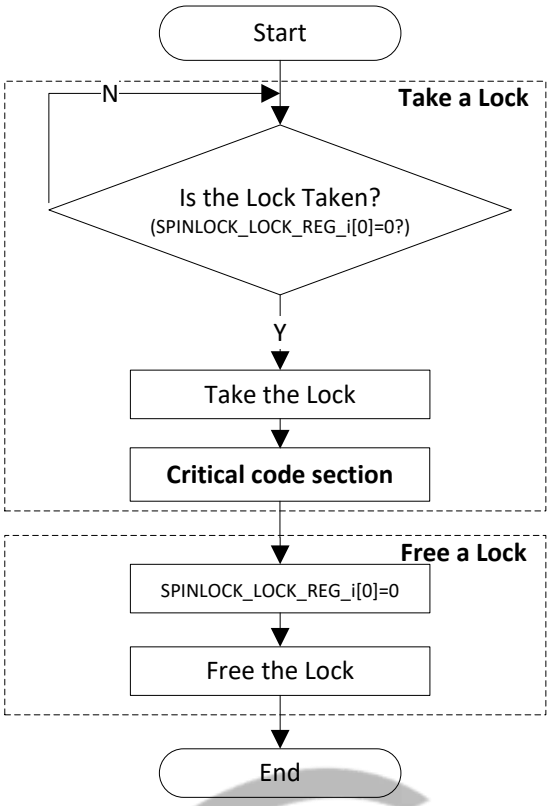
6.2.3 Functional Description

6.2.3.1 Typical Application

The following figure shows how to take and release spinlock. A processor locks spinlock0 before executing specific codes, and then unlocks the codes. After the lock is free, other processors can read or write the data.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 6-3 Take and Free Spinlock



6.2.3.2 Spinlock State Machine

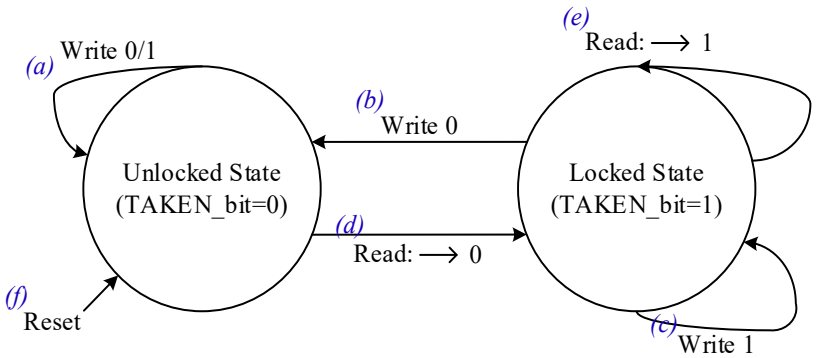
When a processor uses spinlock, it needs to acquire the spinlock status through SPINLOCK_STATUS_REG.

Reading operation: When the return value is 0, it indicates that the spinlock enters the locked status; reading this status bit again can return 1, it indicates that the spinlock is the locked status.

Writing operation: When the spinlock is in the locked status, writing 0 can convert the spinlock to the unlocked status, the writing operation for other status is invalid.

The following figure shows the spinlock state machine.

Figure 6-4 Spinlock State Machine



a) When the spinlock is in the unlocked state, writing 0/1 has no effect;

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

b) When the spinlock is in the locked state, writing 0 can convert the corresponding spinlock to the unlocked state;

c) When the spinlock is in the locked state, writing 1 has no effect;

d) When the spinlock is in the unlocked state, reading the bit can return 0 (it indicates spinlock enters into the locked state);

e) When the spinlock is in the locked state, reading the bit can return 1 (it indicates spinlock is in the locked state);

f) After reset, the spinlock is in the unlock state by default.

6.2.4 Programming Guidelines

6.2.4.1 Switching Spinlock Status

Follow the steps below to switch the lock status of a spinlock between the locked and unlocked statuses.

Step 1 When the read value from SPINLOCKN_LOCK_REG (N=0–31) is 0, the spinlock comes into the locked status.

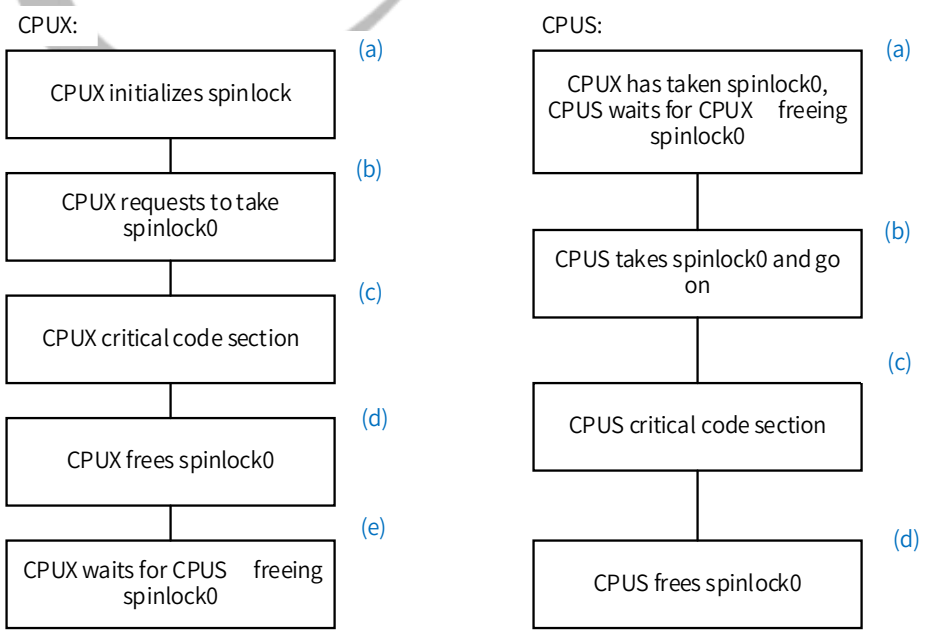
Step 2 Execute the application codes, and the status of SPINLOCK_STATUS_REG is 1.

Step 3 Write 0 to SPINLOCKN_LOCK_REG (N=0–31), the spinlock converts into the unlocked status, and the corresponding spinlock is released.

6.2.4.2 Taking/Freeing Spinlock

Take the synchronization between CPUX and CPUS with Spinlock as an example, the CPUX and CPUS perform the following steps.

Figure 6-5 CPUX and CPUS Taking/Freeing Spinlock0 Process



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

CPUX:

a) The CPUX initializes Spinlock.

b) Check lock register0 (SPINLOCK_STATUS_REG) status. If it is taken, check until CPUX frees spinlock0 and then request to take spinlock0. Otherwise, retry until the lock register0 is taken.

c) Execute CPUX critical code.

d) After executing CPUX critical code, the CPUX frees spinlock0.

e) Enable spinlock0 irq.

f) Clear spinlock0 irq pending.

g) While CPUS acquired spinlock0 authorization, CPUX waits for CPUS freeing spinlock0.

CPUS:

a) If the CPUX has taken spinlock0, the CPUS waits for CPUX to free spinlock0.

b) The CPUS requests to take spinlock0. If it fails, retry until the lock register0 is taken.

c) Execute CPUS critical code.

d) After executing CPUS critical code, the CPUS frees spinlock0.

e) Enable spinlock0 irq.

f) Clear spinlock0 irq pending.

The following codes are for reference.

----------CPUX----------

Step 1 CPUX initializes Spinlock

```
put_wvalue(SPINLOCK_BGR_REG,0x00010000);
put_wvalue(SPINLOCK_BGR_REG,0x00010001);
```

Step 2 CPUX requests to take spinlock0

```
rdata=readl(SPINLOCK_STATUS_REG);          //Check lock register0 status
if (rdata != 0) rdata=readl(SPINLOCK_LOCK_REG);   //If it fails, retry till lock register0 is taken
```

---------- CPUX critical code section ----------

Step 3 CPU0 frees spinlock0

```
writel (0, SPINLOCK_LOCK_REG);          //CPU0 frees spinlock0     n= 0
```

Step 4 Enable spinlock0 irq.

```
writel (0x1, SPINLOCK_IRQ_EN_REG);
```

Step 5 Clear spinlock0 irq pending.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

writel (0x1, SPINLOCK_IRQ_STA_REG);

Step 6 CPU0 waits for CPU1' freeing spinlock0

while((readl(SPINLOCK_STATUS_REG)&0x1)== 1); //CPU0 waits for CPU1 freeing spinlock0

----------CPUS----------

Step 1 CPUX has taken spinlock0, CPUS waits for CPUX' freeing spinlock0

while(readl(SPINLOCK_STATUS_REG) = 1); //CPUS waits for CPUX freeing spinlock0

Step 2 CPUS takes spinlock0 and go on

rdata=readl(SPINLOCK_LOCK_REG); //Request to take spinlock0

if (rdata != 0) rdata=readl(SPINLOCK_LOCK_REG); //If it fails, retry till lock register0 is taken

---------- **CPUS critical code section** ----------

Step 3 CPUS frees spinlock0

writel (0, SPINLOCK_LOCK_REG); //CPUS frees spinlock0

Step 4 Enable spinlock0 irq.

writel (0x1, SPINLOCK_IRQ_EN_REG);

Step 5 Clear spinlock0 irq pending.

writel (0x1, SPINLOCK_IRQ_STA_REG);

6.2.4.3 Processing Interrupt

The spinlock generates an interrupt when a lock is freed (the lock status converts from the locked status to the unlocked status).

Follow the steps below to process the interrupt:

Step 1 Configure the interrupt enable bit of the corresponding spinlock in SPINLOCK_IRQ_EN_REG to enable the interrupt.

Step 2 The spinlock generates an interrupt when its status converts from the locked status to the unlocked status, and the corresponding bit of the SPINLOCK_IRQ_STA_REG turns to 1.

Step 3 Execute the interrupt handle function and clear the pending bit.

6.2.5 Register List

Module Name	Base Address
SPINLOCK	0x03005000

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
SPINLOCK_SYSTATUS_REG	0x0000	SpinLock System Status Register
SPINLOCK_STATUS_REG	0x0010	SpinLock Status Register
SPINLOCK_IRQ_EN_REG	0x0020	SpinLock Interrupt Enable Register
SPINLOCK_IRQ_STA_REG	0x0040	SpinLock Interrupt Status Register
SPINLOCK_LOCKID0_REG	0x0080	SpinLock Lockid0 Register
SPINLOCK_LOCKID1_REG	0x0084	SpinLock Lockid1 Register
SPINLOCK_LOCKID2_REG	0x0088	SpinLock Lockid2 Register
SPINLOCK_LOCKID3_REG	0x008C	SpinLock Lockid3 Register
SPINLOCK_LOCKID4_REG	0x0090	SpinLock Lockid4 Register
SPINLOCKN_LOCK_REG	0x0100+n*0x0004 (n=0~31)	SpinLock Register n

6.2.6 Register Description

6.2.6.1 0x0000 Spinlock System Status Register (Default Value: 0x1000_0000)

Offset: 0x0000			Register Name: SPINLOCK_SYSTATUS_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R	0x1	LOCKS_NUM Number of lock registers implemented 00: This instance has 256 lock registers 01: This instance has 32 lock registers 10: This instance has 64 lock registers 11: This instance has 128 lock registers
27:9	/	/	/
8	R	0x0	IU0 Use Flag0 In-Use flag0, covering lock register0-31. 0: All lock register 0-31 are in the Not Taken state. 1: At least one of the lock register 0-31 is in the Taken state.
7:0	/	/	/

6.2.6.2 0x0010 SpinLock Status Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SPINLOCK_STATUS_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0010			Register Name: SPINLOCK_STATUS_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	LOCK_REG_STATUS SpinLock Reg Status 0: The Spinlock is free 1: The Spinlock is taken Spinlock 0~31 bit.

6.2.6.3 0x0020 SpinLock Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SPINLOCK_IRQ_EN_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	LOCK_IRQ_EN SpinLock interrupt enable 0: Disable 1: Enable

6.2.6.4 0x0040 SpinLock Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: SPINLOCK_IRQ_STA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W1C	0x0	LOCK_IRQ _STATUS SpinLock interrupt status 0: No effect 1: Pending Writing 1 will clear this bit.

6.2.6.5 0x0080 SpinLock Lockid0 Register (Default Value: 0x7777_7777)

Offset: 0x0080			Register Name: SPINLOCK_LOCKID0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x77777777	LOCKID0

6.2.6.6 0x0084 SpinLock Lockid1 Register (Default Value: 0x7777_7777)

Offset: 0x0084			Register Name: SPINLOCK_LOCKID1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x77777777	LOCKID1

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.2.6.7 0x0088 SpinLock Lockid2 Register (Default Value: 0x7777_7777)

Offset: 0x0088			Register Name: SPINLOCK_LOCKID2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x77777777	LOCKID2

6.2.6.8 0x008C SpinLock Lockid3 Register (Default Value: 0x7777_7777)

Offset: 0x008C			Register Name: SPINLOCK_LOCKID3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x77777777	LOCKID3

6.2.6.9 0x0090 SpinLock Lockid4 Register (Default Value: 0x7777_7777)

Offset: 0x0090			Register Name: SPINLOCK_LOCKID4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x77777777	LOCKID4

6.2.6.10 0x0100+n*0x0004 (n=0~31) SpinLock Register n (Default Value: 0x0000_0000)

Offset: 0x0100+n*0x0004 (n=0~31)			Register Name: SPINLOCKN_LOCK_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	TAKEN. Lock State. Read 0x0: The lock was previously Not Taken (free). The requester is granted the lock. Write 0x0: Set the lock to Not Taken (free). Read 0x1: The lock was previously Taken. The requester is not granted the lock and must retry. Write 0x1: No update to the lock value.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

7 Thermal Sensor

7.1 Thermal Sensor Controller (THS)

7.1.1 Overview

The thermal sensors are common elements in wide range of modern system on chips (SoCs) platform. The thermal sensors are used to constantly monitor the temperature on the chip.

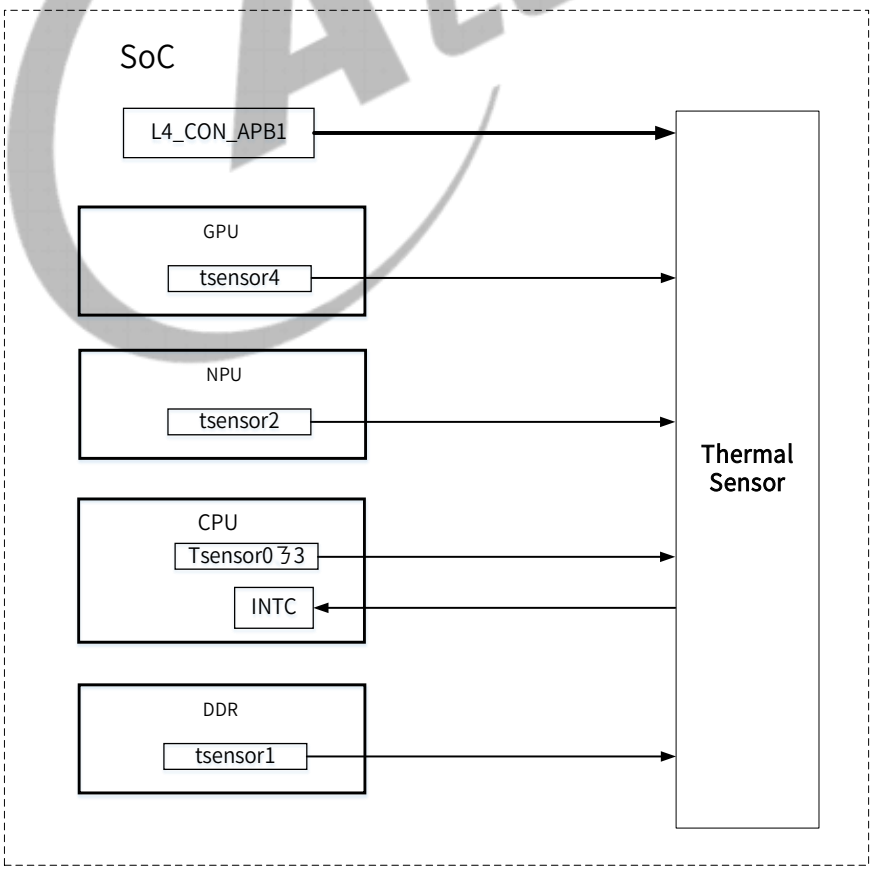
The SoC embeds five thermal sensors in possible hot spots on the die. Sensor0 is located in the CPUB; sensor1 is located in the DDR; sensor2 is located in the NPU; sensor3 is located in the CPUL; sensor4 is located in the GPU. These thermal sensors generate interrupt to lower temperature via DVFS, on reaching a certain thermal threshold.

The THS has the following features:

- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt
- Supports ±3℃ error limit from 60 to 125℃ and ±5℃ from -40 to 60℃

7.1.2 Environment Diagram

The following figures show the environment diagram of the THS.

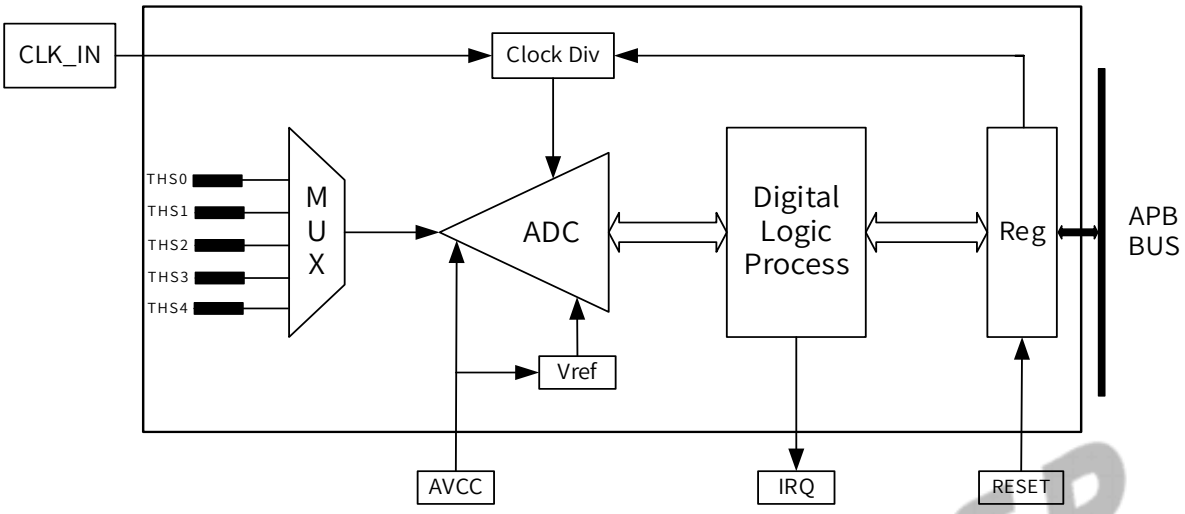


Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.1.3 Block Diagram

The following figures show the block diagram of the THS.

Figure 7-1 THS Block Diagram



7.1.4 Clock Sources

The following table describes the clock sources of THS. For clock setting, configurations, and gating information, refer to the section CCU.

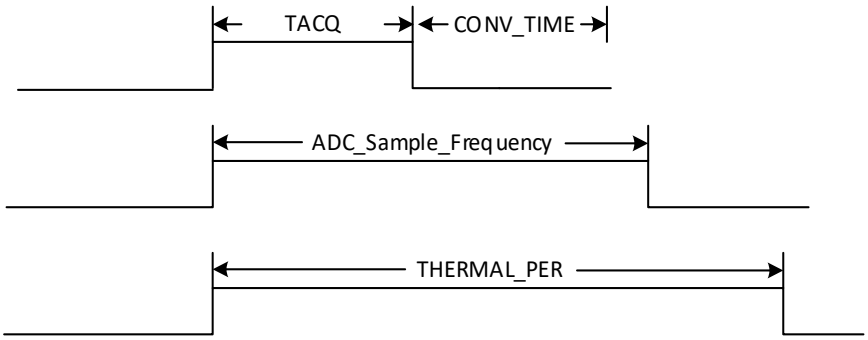
Module	Clock Sources	Description
THS	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.
	DCXO	The external high-frequency crystal oscillator. Its frequency is 26 MHz.

7.1.5 Functional Description

7.1.5.1 Timing Requirements

The following figure shows the timing requirements for the THS module.

Figure 7-2 Thermal Sensor Timing Requirement



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

CLK_IN = 24 MHz

CONV_TIME (Conversion Time) = 1/24 MHz x 14 Cycles = 0.583 us

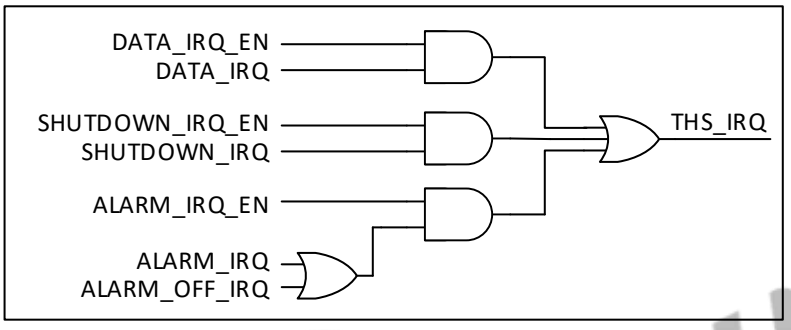
TACQ > 1/24 MHz x 24 Cycles

THERMAL_PER > ADC_Sample_Frequency > TACQ + CONV_TIME

7.1.5.2 Interrupts

The THS module has four interrupt sources: DATA_IRQ, SHUTDOWN_IRQ, ALARM_IRQ, and ALARM_OFF_IRQ. The following figure shows thermal sensor interrupt sources.

Figure 7-3 Thermal Sensor Controller Interrupt Source



DATA_IRQ

The interrupt is generated when the measured sensor_data is updated.

SHUTDOWN_IRQ

The interrupt is generated when the temperature is higher than the shutdown threshold.

ALARM_IRQ

The interrupt is generated when the temperature is higher than the Alarm_Threshold.

ALARM_OFF_IRQ

The interrupt is generated when the temperature is lower than the Alarm_Off_Thershold. It is triggered at the falling edge.

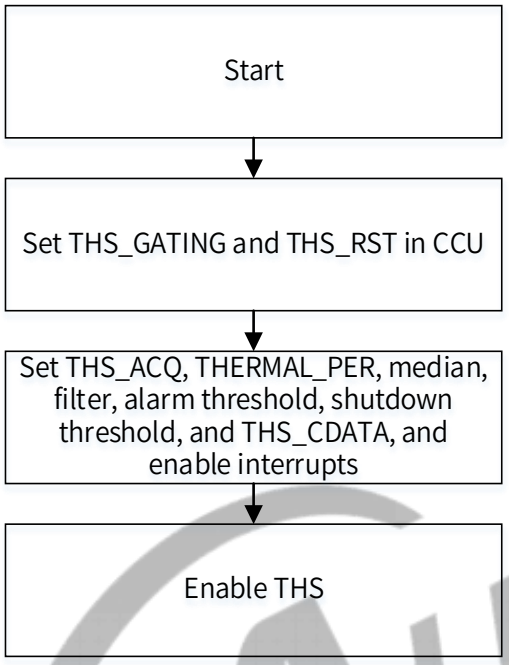
Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.1.6 Programming Guidelines

7.1.6.1 Initialization

The following takes THS0 as an example to explicit the THS initialization, query mode, interrupt mode.

Figure 7-4 THS Initialization



In the final test (FT) stage, the THS is calibrated through the ambient temperature, and the calibration value is written in the SID module. The following table shows the THS information in the SID.

Table 7-1 THS Information in the SID

Base Address: 0x14	Register Name: THS
Bit	Description
31:28	The highest 4 bits of the Audio_bias calibration value.
27:16	The calibration value of the T-sensor.
15:12	The lowest 4 bits of the Audio_bias calibration value.
11:0	The value of the ambient temperature.

Before enabling THS, read eFuse value and write the value to THS0_CDATA.

Query Mode

the following takes THS0 as an example, THS1-4 are the same.

Step 1 Write 0x1 to the bit [16] of THS_BGR_REG to dessert the reset.

Step 2 Write 0x1 to the bit [0] of THS_BGR_REG to open the THS clock.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 3 Write 0x2F to the bit [15:0] of THS_CTRL to set the ADC acquire time.

Step 4 Write 0x1DF to the bit [31:16] of THS_CTRL to set the ADC sample frequency divider.

Step 5 Write 0x3A to the bit [31:12] of THS_PER to set the THS work period.

Step 6 Write 0x1 to the bit [2] of THS_FILTER to enable the temperature convert filter.

Step 7 Write 0x1 to the bit [1:0] of THS_FILTER to select the filter type.

Step 8 Read THS eFuse value from SID, then write the eFuse value to TSENSORn_CDATA to calibrate THS.

Step 9 Write 0x1 to the bit [0] 0f THS_EN to enable THS.

Step 10 Read the bit [0] of THS_DATA_INTS. If it is 1, the temperature conversion is complete.

Step 11 Read the bit [11:0] of THS0_DATA, and calculate the THS temperature based on section

Interrupt Mode

The following takes THs0 as an example, THS1-4 are the same.

Step 1 Write 0x1 to the bit16 of THS_BGR_REG to dessert the reset.

Step 2 Write 0x1 to the bit0 of THS_BGR_REG to open the THS clock.

Step 3 Write 0x2F to the bit [15:0] of THS_CTRL to set the ADC acquire time.

Step 4 Write 0x1DF to the bit [31:16] of THS_CTRL to set the ADC sample frequency divider.

Step 5 Write 0x3A to the bit [31:12] of THS_PER to set the THS work period.

Step 6 Write 0x1 to the bit2 of THS_FILTER to enable the temperature convert filter.

Step 7 Write 0x1 to the bit [1:0] of THS_FILTER to select the filter type.

Step 8 Read THS eFuse value from SID, and then write the eFuse value to TSENSORn_CDATA to calibrate THS.

Step 9 Write 0x1 to the bit [0] of THS_DATA_INTC to enable the interrupt of THS.

Step 10 Set GIC interface based on IRQ 71.

Step 11 Put the interrupt handler address into the interrupt vector table.

Step 12 Write 0x1 to the bit [0] 0f THS_EN to enable THS.

Step 13 Read the bit [0] of THS_DATA_INTS. If it is 1, the temperature conversion is complete.

Step 14 Read the bit [11:0] of THS0_DATA, and calculate the THS temperature based on section

7.1.7 Register List

Module Name	Base Address
THS	0x02522000

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
THS_CTRL	0x0000	THS Control Register
THS_EN	0x0004	THS Enable Register
THS_PER	0x0008	THS Period Control Register
THS_DATA_INTC	0x0010	THS Data Interrupt Control Register
THS_SHUT_INTC	0x0014	THS Shut Interrupt Control Register
THS_ALARM_INTC	0x0018	THS Alarm Interrupt Control Register
THS_DATA_INTS	0x0020	THS Data Interrupt Status Register
THS_SHUT_INTS	0x0024	THS Shut Interrupt Status Register
THS_ALARMO_INTS	0x0028	THS Alarm off Interrupt Status Register
THS_ALARM_INTS	0x002C	THS Alarm Interrupt Status Register
THS_FILTER	0x0030	THS Median Filter Control Register
THS0_ALARM_CTRL	0x0040	THS0 Alarm threshold Control Register
THS1_ALARM_CTRL	0x0044	THS1 Alarm threshold Control Register
THS2_ALARM_CTRL	0x0048	THS2 Alarm threshold Control Register
THS3_ALARM_CTRL	0x004C	THS3 Alarm threshold Control Register
THS4_ALARM_CTRL	0x0050	THS4 Alarm threshold Control Register
THS0_THS1_SHUTDOWN_CTRL	0x0080	THS0_THS1 Shutdown threshold Control Register
THS2_THS3_SHUTDOWN_CTRL	0x0084	THS2_THS3 Shutdown threshold Control Register
THS4_SHUTDOWN_CTRL	0x0088	THS4 Shutdown threshold Control Register
THS0_THS1_CDATA	0x00A0	THS0_THS1 Calibration Data
THS2_THS3_CDATA	0x00A4	THS2_THS3Calibration Data
THS4_CDATA	0x00A8	THS4 Calibration Data
THS0_DATA	0x00C0	THS0 Data Register
THS1_DATA	0x00C4	THS1 Data Register
THS2_DATA	0x00C8	THS2 Data Register
THS3_DATA	0x00CC	THS3 Data Register
THS4_DATA	0x00D0	THS4 Data Register

7.1.8 Register Description

7.1.8.1 0x0000 THS Control Register (Default Value: 0x01DF_002F)

Offset: 0x0000			Register Name: THS_CTRL
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x1DF	TACQ ADC acquire time, default (2uS) CLK_IN/(n+1)
15:0	R/W	0x2F	Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.1.8.2 0x0004 THS Enable Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: THS_EN
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W	0x0	THS4_EN Enable temperature measurement sensor4 0: Disable 1: Enable
3	R/W	0x0	THS3_EN Enable temperature measurement sensor3 0: Disable 1: Enable
2	R/W	0x0	THS2_EN Enable temperature measurement sensor2 0: Disable 1: Enable
1	R/W	0x0	THS1_EN Enable temperature measurement sensor1 0: Disable 1: Enable
0	R/W	0x0	THS0_EN Enable temperature measurement sensor0 0: Disable 1: Enable

7.1.8.3 0x0008 THS Period Control Register (Default Value: 0x0003_A000)

Offset: 0x0008			Register Name: THS_PER
Bit	Read/Write	Default/Hex	Description
31:12	R/W	0x3A	THERMAL_PER Temperature measurement period,default (10ms) 4096*(n+1)/CLK_IN
11:0	/	/	/

7.1.8.4 0x0010 THS Data Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: THS_DATA_INTC
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0010			Register Name: THS_DATA_INTC
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	THS4_DATA_IRQ_EN Selects Temperature measurement data of sensor4 0: Disable 1: Enable
3	R/W	0x0	THS3_DATA_IRQ_EN Selects Temperature measurement data of sensor3 0: Disable 1: Enable
2	R/W	0x0	THS2_DATA_IRQ_EN Selects Temperature measurement data of sensor2 0: Disable 1: Enable
1	R/W	0x0	THS1_DATA_IRQ_EN Selects Temperature measurement data of sensor1 0: Disable 1: Enable
0	R/W	0x0	THS0_DATA_IRQ_EN Selects Temperature measurement data of sensor0 0: Disable 1: Enable

7.1.8.5 0x0014 THS Shut Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: THS_SHUT_INTC
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W	0x0	SHUT_INT4_EN Selects shutdown interrupt for sensor4 0: Disable 1: Enable
3	R/W	0x0	SHUT_INT3_EN Selects shutdown interrupt for sensor3 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: THS_SHUT_INTC
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	SHUT_INT2_EN Selects shutdown interrupt for sensor2 0: Disable 1: Enable
1	R/W	0x0	SHUT_INT1_EN Selects shutdown interrupt for sensor1 0: Disable 1: Enable
0	R/W	0x0	SHUT_INT0_EN Selects shutdown interrupt for sensor0 0: Disable 1: Enable

7.1.8.6 0x0018 THS Alarm Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: THS_ALARM_INTC
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W	0x0	ALARM_INT4_EN Selects Alarm interrupt for sensor4 0: Disable 1: Enable
3	R/W	0x0	ALARM_INT3_EN Selects Alarm interrupt for sensor3 0: Disable 1: Enable
2	R/W	0x0	ALARM_INT2_EN Selects Alarm interrupt for sensor2 0: Disable 1: Enable
1	R/W	0x0	ALARM_INT1_EN Selects Alarm interrupt for sensor1 0: Disable 1: Enable
0	R/W	0x0	ALARM_INT0_EN Selects Alarm interrupt for sensor0 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.1.8.7 0x0020 THS Data Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: THS_DATA_INTS
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W1C	0x0	THS4_DATA_IRQ_STS Data interrupt status for sensor4 Write '1' to clear this interrupt.
3	R/W1C	0x0	THS3_DATA_IRQ_STS Data interrupt status for sensor3 Write '1' to clear this interrupt.
2	R/W1C	0x0	THS2_DATA_IRQ_STS Data interrupt status for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	THS1_DATA_IRQ_STS Data interrupt status for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	THS0_DATA_IRQ_STS Data interrupt status for sensor0 Write '1' to clear this interrupt.

7.1.8.8 0x0024 THS Shut Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: THS_SHUT_INTS
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W1C	0x0	SHUT_INT4_STS Shutdown interrupt status for sensor4 Write '1' to clear this interrupt.
3	R/W1C	0x0	SHUT_INT3_STS Shutdown interrupt status for sensor3 Write '1' to clear this interrupt.
2	R/W1C	0x0	SHUT_INT2_STS Shutdown interrupt status for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	SHUT_INT1_STS Shutdown interrupt status for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	SHUT_INT0_STS Shutdown interrupt status for sensor0 Write '1' to clear this interrupt.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.1.8.9 0x0028 THS Alarm off Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: THS_ALARMO_INTS
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W1C	0x0	ALARM_OFF4_STS Alarm interrupt off pending for sensor4 Write '1' to clear this interrupt.
3	R/W1C	0x0	ALARM_OFF3_STS Alarm interrupt off pending for sensor3 Write '1' to clear this interrupt.
2	R/W1C	0x0	ALARM_OFF2_STS Alarm interrupt off pending for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	ALARM_OFF1_STS Alarm interrupt off pending for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	ALARM_OFF0_STS Alarm interrupt off pending for sensor0 Write '1' to clear this interrupt.

7.1.8.10 0x002C THS Alarm Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: THS_ALARM_INTS
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W1C	0x0	ALARM_INT4_STS Alarm interrupt pending for sensor4 Write '1' to clear this interrupt.
3	R/W1C	0x0	ALARM_INT3_STS Alarm interrupt pending for sensor3 Write '1' to clear this interrupt.
2	R/W1C	0x0	ALARM_INT2_STS Alarm interrupt pending for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	ALARM_INT1_STS Alarm interrupt pending for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	ALARM_INT0_STS Alarm interrupt pending for sensor0 Write '1' to clear this interrupt.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.1.8.11 0x0030 THS Median Filter Control Register (Default Value: 0x0000_0001)

Offset: 0x0030			Register Name: THS_FILTER
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	FILTER_EN Filter Enable 0: Disable 1: Enable
1:0	R/W	0x1	FILTER_TYPE Average Filter Type 00: 2 01: 4 10: 8 11: 16

7.1.8.12 0x0040 THS0 Alarm Threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x0040			Register Name: THS0_ALARM_CTRL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5A0	ALARM0_T_HOT Thermal sensor0 Alarm Threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM0_T_HYST Thermal sensor0 Alarm threshold for hysteresis temperature

7.1.8.13 0x0044 THS1 Alarm Threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x0044			Register Name: THS1_ALARM_CTRL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5A0	ALARM1_T_HOT Thermal sensor1 Alarm Threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM1_T_HYST Thermal sensor1 Alarm threshold for hysteresis temperature

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.1.8.14 0x0048 THS2 Alarm Threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x0048			Register Name: THS2_ALARM_CTRL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5A0	ALARM2_T_HOT Thermal sensor2 Alarm Threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM2_T_HYST Thermal sensor2 Alarm threshold for hysteresis temperature

7.1.8.15 0x004C THS3 Alarm Threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x004C			Register Name: THS3_ALARM_CTRL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5A0	ALARM3_T_HOT Thermal sensor3 Alarm Threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM3_T_HYST Thermal sensor3 Alarm threshold for hysteresis temperature

7.1.8.16 0x0050 THS4 Alarm Threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x0050			Register Name: THS4_ALARM_CTRL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5A0	ALARM4_T_HOT Thermal sensor4 Alarm Threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM4_T_HYST Thermal sensor4 Alarm threshold for hysteresis temperature

7.1.8.17 0x0080 THS0_THS1 Shutdown Threshold Control Register (Default Value: 0x04E9_04E9)

Offset: 0x0080	Register Name: THS0_THS1_SHUTDOWN_CTRL

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
27:16	R/W	0x4E9	SHUT1_T_HOT Thermal sensor1 Shutdown Threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x4E9	SHUT0_T_HOT Thermal sensor0 Shutdown Threshold for hot temperature

7.1.8.18 0x0084 THS2_THS3 Shutdown Threshold Control Register (Default Value: 0x0000_04E9)

Offset: 0x0084			Register Name: THS2_THS3_SHUTDOWN_CTRL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x4E9	SHUT3_T_HOT Thermal sensor3 Shutdown Threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x4E9	SHUT2_T_HOT Thermal sensor2 Shutdown Threshold for hot temperature

7.1.8.19 0x0088 THS4 Shutdown Threshold Control Register (Default Value: 0x0000_04E9)

Offset: 0x0088			Register Name: THS4_SHUTDOWN_CTRL
Bit	Read/Write	Default/Hex	Description
27:12	/	/	/
11:0	R/W	0x4E9	SHUT4_T_HOT Thermal sensor4 Shutdown Threshold for hot temperature

7.1.8.20 0x00A0 THS0_THS1 Calibration Data (Default Value: 0x0800_0800)

Offset: 0x00A0			Register Name: THS0_THS1_CDATA
Bit	Read/Write	Default/Hex	Description
27:16	R/W	0x800	THS1_CDATA Thermal Sensor1 calibration data
15:12	/	/	/
11:0	R/W	0x800	THS0_CDATA Thermal Sensor0 calibration data

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.1.8.21 0x00A4 THS2_THS3 Calibration Data (Default Value: 0x0000_0800)

Offset: 0x00A4			Register Name: THS2_THS3_CDATA
Bit	Read/Write	Default/Hex	Description
27:16	R/W	0x800	THS3_CDATA Thermal Sensor3 calibration data
15:12	/	/	/
11:0	R/W	0x800	THS2_CDATA Thermal Sensor2 calibration data

7.1.8.22 0x00A8 THS4 Calibration Data (Default Value: 0x0000_0800)

Offset: 0x00A8			Register Name: THS4_CDATA
Bit	Read/Write	Default/Hex	Description
27:12	/	/	/
11:0	R/W	0x800	THS4_CDATA Thermal Sensor4 calibration data

7.1.8.23 0x00C0 THS0 Data Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: THS0_DATA
Bit	Read/Write	Default/Hex	Description
32:12	/	/	/
11:0	R	0x0	THS0_DATA Temperature measurement data of sensor0

7.1.8.24 0x00C4 THS1 Data Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: THS1_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x0	THS1_DATA Temperature measurement data of sensor1

7.1.8.25 0x00C8 THS2 Data Register (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: THS2_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x0	THS2_DATA Temperature measurement data of sensor2

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.1.8.26 0x00CC THS3 Data Register (Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: THS3_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x0	THS3_DATA Temperature measurement data of sensor3

7.1.8.27 0x00D0 THS4 Data Register (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: THS4_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x0	THS4_DATA Temperature measurement data of sensor4

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

8 Timers

8.1 Timer0

8.1.1 Overview

The Timer0 supports timing, counting, and interrupt output.

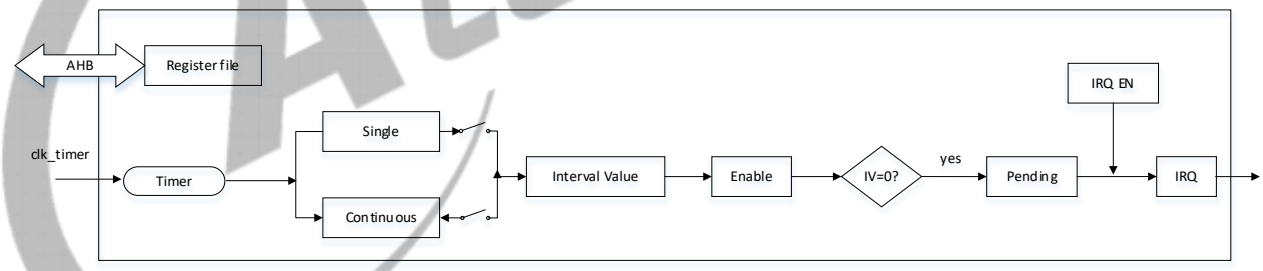
The Timer module has the following features:

- Supports configuring timer registers through AHB interface
- Count clock can be switched between RTC_32K, DCXO, SYS_CLK24M, PERI0_200M, and RC16M through PRCM/CCU
- Programmable 56-bit down timer
- Supports two count modes: continuous mode and single mode
- Generates an interrupt when the count value is decreased to 0

8.1.2 Block Diagram

The following figure shows the block diagram of timer1.

Figure 8-1 Timer1 Block Diagram



8.1.3 Clock Sources

The following table describes the clock sources of Timer0. For clock setting, configurations, and gating information, refer to the section CCU or PRCM.

Module	Clock Sources	Description
Timer0_CPUX	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.
	RC16M	The on-chip oscillator. Its frequency is 16MHz by default.
	RTC_32K	Its frequency is 32.768 KHz by default.
	PERI0_200M	Its frequency is 200 MHz by default.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Module	Clock Sources	Description
	DCXO	The external high-frequency crystal oscillator. Its frequency is 26 MHz.
Timer0_CPUS	DCXO	The external high-frequency crystal oscillator. Its frequency is 26 MHz.
	RTC_32K	Its frequency is 32.768 KHz by default.
	RC16M	The on-chip oscillator. Its frequency is 16MHz by default.
	PERIPLL_DIV	Its frequency is 200 MHz by default.
	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.

8.1.4 Functional Descriptions

8.1.4.1 Count Time Calculation

$$T = \frac{\{TIMER_IVH, TIMER_IVL\} - \{TIMER_CVH, TIMER_CVL\}}{f_{clk_timer}}$$

Where,

TIMER_IVH is the higher 24 bits of the interval value that is configured by the lower 24 bits of the TIMER_IVH_REG.

TIMER_IVL is the lower 32 bits of the interval value that is configured by the TIMER_IVL_REG.

TIMER_CVH is the higher 24 bits of the current value that is configured by the lower 24 bits of the TIMER_CVH_REG.

TIMER_CVL is the lower 32bits of the current value that is configured by the TIMER_CVL_REG.

fclk_timer is the frequency of timer clock source.

8.1.4.2 Count Modes

The timer is a 56-bit down counter. The counter value is decremented by 1 on each rising edge of the timer clock. The timer has two count modes: the single count mode and the periodic mode. You can configure the count modes via the TIMER_CTRL_REG(bit[7]).

- Continuous Mode

In the continuous mode, the timer will reload data from the Timer Interval Value and generate an interrupt when the counter is decreased to 0. Then, it restarts another round of counting.

- Single Mode

In the single mode, the timer will stop counting and generate an interrupt after the counter decreases to 0. It restarts counting only when the interval value is reloaded.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

8.1.5 Programming Guidelines

8.1.5.1 Initialization

Refer to the following steps to initialize the timer.

Step 1 Configure the timer parameters including the clock sources and timing modes by writing to TIMER_CTRL_REG. There is no sequence requirement for these parameter configurations.

Step 2 Write the interval value.

a) Write to TIMER_IVL_REG and TIMER_IVH_REG to configure the interval values of the timer.

b) Write to TIMER_CTRL_REG (bit[1]) to load the interval value to the timer. If the bit is 1, no write operation is permitted; if the bit is 0, reload succeeds.

Step 3 Write to TIMER_CTRL_REG(bit[0]) to start the timer. Read TIMER_CVL_REG and TIMER_CVH_REG to get the current value of the timer.

NOTE

When performing read or write operations on the current value registers, operate TIMER_CVL_REG register before TIMER_CVH_REG register.

8.1.5.2 Interrupt Processing

Refer to the following steps to process the interrupt:

Step 1 Write to the corresponding interrupt in TIMER_IRQ_REG. The timer will generate an interrupt once the count value reaches 0.

Step 2 After the software program enters the interrupt process, write to the pending bit of the corresponding interrupts in TIMER_STA_REG to clear the interrupt pending.

Step 3 Resume the interrupt and continue to execute the interrupted process.

8.1.6 Register List

Module Name	Base Address	Comment
Timer0_CPUX	0x03009000	
Timer0_CPUS	0x07091000	Timer_CPUS register is the same with TIMER0_CPUX.

Register Name	Offset	Description
TIMER_IRQ_REG	0x0000	Timer IRQ Enable Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
TIMER_STA_REG	0x0004	Timer Status Register
TIMER_SEC_REG	0x0008	Timer Secure Register
TIMER_CTRL_REG	0x0020+0x0020*N	Timer Control Register
TIMER_IVL_REG	0x0024+0x0020*N	Timer Low Interval Value Register
TIMER_CVL_REG	0x0028+0x0020*N	Timer Low Current Value Register
TIMER_IVH_REG	0x002C+0x0020*N	Timer High Interval Value Register
TIMER_CVH_REG	0x0030+0x0020*N	Timer High Current Value Register
TIMER_CV_READ_SEL_REG	0x0034+0x0020*N	Timer Current Value Read Select Register

NOTE

For Timer0_CPUX, N ranges from 0 to 9. For Timer0_CPUS, N ranges from 0 to 3.

8.1.7 Register Description

8.1.7.1 0x0000 Timer IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TIMER_IRQ_REG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:0	R/W	0x0	TIMER_IRQ_EN Timer (0~NUM-1) Interrupt Enable 1: Enable 0: Disable Note: The specific number is decided by the number of timers in different domains.

8.1.7.2 0x0004 Timer Status Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: TIMER_STA_REG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:0	R/WC	0x0	TIMER_IRQ_STAT Timer (0~NUM-1) Status 1: Pending 0: No effect Note: The specific number is decided by the number of timers in different domains.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

8.1.7.3 0x0008 Timer Secure Register (Default Value: 0x0000_03FF)

Offset: 0x0008			Register Name: TIMER_SEC_REG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:0	R/W	0x3FF	TIMER_SECURE Timer (0~NUM-1) Secure Control 1: Secure 0: Non-secure Note: The specific number is decided by the number of timers in different domains.

8.1.7.4 0x0020+0x0020*N Timer Control Register (Default Value: 0x0000_0000)

Offset: 0x0020+0x0020*N			Register Name: TIMER_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TIMER_MODE Timer Mode 0: Continuous mode. When interval value is reached, the timer will restart another round of counting automatically. 1: Single mode. When interval value is reached, the timer will stop counting.
6:2	/	/	/
1	R/W	0x0	TIMER_RELOAD. Timer 0 Reload. 0: No effect 1: Reload timer 0 Interval value After the bit is set, it cannot be written again before it s cleared automatically.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0020+0x0020*N			Register Name: TIMER_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	TIMER_EN. Timer 0 Enable. 0: Stop/Pause 1: Start If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to 0 , the current value counter will pause. Wait for at least 2 cycles, and then the start bit can be set to 1. In the pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value. The reload bit and the enable bit should be set to 1 at the same time.

8.1.7.5 0x0024+0x0020*N Timer Low Interval Value Register (Default Value: 0x0000_0000)

Offset: 0x0024+0x0020*N			Register Name:TIMER_IVL_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TIMER_IVL Timer Interval Value bit[31:0] Register

8.1.7.6 0x0028+0x0020*N Timer Low Current Value Register (Default Value: 0x0000_0000)

Offset: 0x0028+0x0020*N			Register Name: TIMER_CVL_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TIMER_CVL Timer Current Value bit[31:0] Register

NOTE

The current value register is a 56-bit register. When read or write the current value, the TIMER_CVL should be read or write first.

8.1.7.7 0x002C+0x0020*N Timer High Interval Value Register (Default Value: 0x0000_0000)

Offset: 0x002C+0x0020*N	Register Name: TIMER_IVH_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	TIMER_IVH Timer Interval Value bit[55:32] Register

8.1.7.8 0x0030+0x0020*N Timer High Current Value Register (Default Value: 0x0000_0000)

Offset: 0x0030+0x0020*N			Register Name: TIMER_CVH_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	TIMER_CVH Timer Current Value bit[55:32] Register

8.1.7.9 0x0034+0x0020*N Timer Current Value Read Select Register (Default Value: 0x0000_0000)

Offset: 0x0034+0x0020*N			Register Name: TIMER_CV_READ_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	TIMER_CV_READ_SEL Timer Read Current Value. 0: The Frequency of hclk must be faster than 2 times of tclk. 1: The Frequency of hclk and tclk are unlimited.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

8.2 Timer1

8.2.1 Overview

The Timer1 supports the timing, counting, and interrupt output.

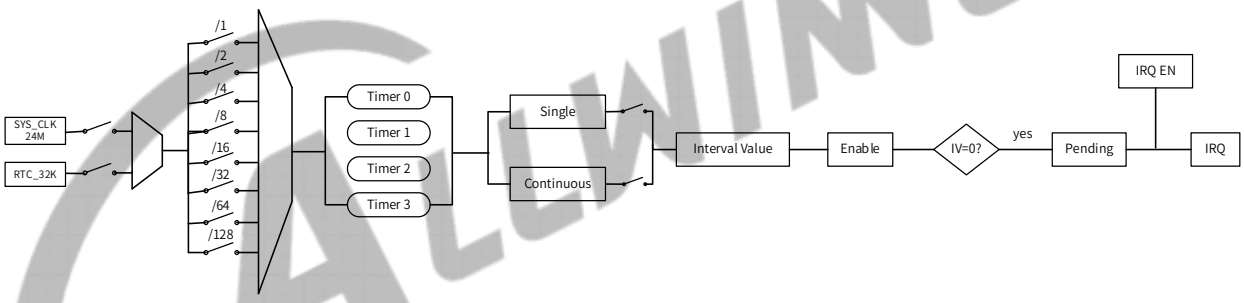
The Timer module has the following features:

- Count clock can be switched between RTC_32K and SYS_CLK24M
- Configurable eight pre-scaler coefficients
- Programmable 32-bit down timer
- Supports two count modes: continuous mode and single mode
- Generates an interrupt when the count is decreased to 0

8.2.2 Block Diagram

The following figure shows the block diagram for the timer.

Figure 8-2 Block Diagram for the Timer



8.2.3 Clock Sources

The following table describes the clock sources of Timer1. For clock setting, configurations, and gating information, refer to the section CCU.

Module	Clock Sources	Description
Timer1_CPUX	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.
	RTC_32K	Its frequency is 32.768 KHz by default.

8.2.4 Functional Descriptions

8.2.4.1 Count Time Calculation

$$\frac{\text{TMR0_INTV_VALUE_REG - TMR0_CUR_VALUE_REG}}{\text{TMR0_CLK_SRC}} \times \text{TMR0_CLK_PRES}$$

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Where,

TMR0_INTV_VALUE_REG is the timer interval value.

TMR0_CUR_VALUE_REG is the timer current count value.

TMR0_CLK_SRC is the timer clock source.

TMR0_CLK_PRES is the timer clock frequency division.

8.2.4.2 Count Modes

The timer is a 32-bit down counter. The counter value is decremented by 1 on each rising edge of the timer clock. The timer has two count modes: the single mode and the continuous mode. You can configure the count modes via the TMRn_CTRL_REG (bit[7]).

- Continuous Mode

In the continuous mode, the timer will reload data from the Timer Interval Value and generate an interrupt when the counter is decreased to 0. Then, it restarts another round of counting.

- Single Mode

In the single mode, the timer will stop counting and generate an interrupt after the counter decreases to 0. It restarts counting only when the interval value is reloaded.

8.2.5 Programming Guidelines

8.2.5.1 Initialization

Refer to the following steps to initialize the timer:

Step 1 Configure the timer parameters including the clock sources and timing modes by writing to TMRn_CTRL_REG. There is no sequence requirement for these parameter configurations.

Step 2 Write the interval value.

a) Write to TMRn_INTV_VALUE_REG to configure the interval values of the timer.

b) Write to TMRn_CTRL_REG to load the interval value to the timer. If the bit is 1, no write operation is permitted; if the bit is 0, reload succeeds.

Step 3 Write to TMRn_CTRL_REG to start the timer. Read TMRn_CUR_VALUE_REG to get the current value of the timer.

8.2.5.2 Interrupt Processing

Refer to the following steps to process the interrupt:

Step 1 Write to the corresponding interrupt in TMR_IRQ_EN_REG. The timer will generate an interrupt once the count value reaches 0.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 2 After the software program enters the interrupt process, write to the pending bit of the corresponding interrupts in TMR_IRQ_STA_REG to clear the interrupt pending.

Step 3 Resume the interrupt and continue to execute the interrupted process.

8.2.6 Register List

Module Name	Base Address	Comment
Timer1_CPUX	0x02052000	

Register Name	Offset	Description
TMR_IRQ_EN_REG	0x0000	Timer IRQ Enable Register
TMR_IRQ_STA_REG	0x0004	Timer IRQ Status Register
TMR0_CTRL_REG	0x0010	Timer 0 Control Register
TMR0_INTV_VALUE_REG	0x0014	Timer 0 Interval Value Register
TMR0_CUR_VALUE_REG	0x0018	Timer 0 Current Value Register
TMR1_CTRL_REG	0x0020	Timer 1 Control Register
TMR1_INTV_VALUE_REG	0x0024	Timer 1 Interval Value Register
TMR1_CUR_VALUE_REG	0x0028	Timer 1 Current Value Register
TMR2_CTRL_REG	0x0030	Timer 2 Control Register
TMR2_INTV_VALUE_REG	0x0034	Timer 2 Interval Value Register
TMR2_CUR_VALUE_REG	0x0038	Timer 2 Current Value Register
TMR3_CTRL_REG	0x0040	Timer 3 Control Register
TMR3_INTV_VALUE_REG	0x0044	Timer 3 Interval Value Register
TMR3_CUR_VALUE_REG	0x0048	Timer 3 Current Value Register

8.2.7 Register Description

8.2.7.1 0x0000 Timer IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TMR_IRQ_EN_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: TMR_IRQ_EN_REG
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	TMR3_IRQ_EN Timer 3 Interrupt Enable 0: Disable 1: Enable
2	R/W	0x0	TMR2_IRQ_EN Timer 2 Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	TMR1_IRQ_EN Timer 1 Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	TMR0_IRQ_EN Timer 0 Interrupt Enable 0: Disable 1: Enable

8.2.7.2 0x0004 Timer IRQ Status Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: TMR_IRQ_STA_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W1C	0x0	TMR3_IRQ_PEND Timer 3 IRQ Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending, timer 1 interval value is reached
2	R/W1C	0x0	TMR2_IRQ_PEND Timer 2 IRQ Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending, timer 1 interval value is reached
1	R/W1C	0x0	TMR1_IRQ_PEND Timer 1 IRQ Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending, timer 1 interval value is reached
0	R/W1C	0x0	TMR0_IRQ_PEND Timer 0 IRQ Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending, timer 0 interval value is reached

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

8.2.7.3 0x0010 Timer 0 Control Register (Default Value: 0x0000_0004)

Offset: 0x0010			Register Name: TMR0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TMR0_MODE Timer 0 mode 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR0_CLK_PRES Select the prescaler of timer 0 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR0_CLK_SRC Timer0 Clock Source. 00: RTC_32K 01: SYS_CLK24M 10: / 11: /
1	R/W	0x0	TMR0_RELOAD Timer 0 Reload. 0: No effect 1: Reload timer 0 Interval value After the bit is set, it cannot be written again before it's cleared automatically.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0010			Register Name: TMR0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	TMR0_EN Timer 0 Enable 0: Stop/Pause 1: Start If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

8.2.7.4 0x0014 Timer 0 Interval Value Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: TMR0_INTV_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR0_INTV_VALUE Timer 0 Interval Value

Note: The value setting should consider the system clock and the timer clock source.

8.2.7.5 0x0018 Timer 0 Current Value Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: TMR0_CUR_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR0_CUR_VALUE Timer 0 Current Value

Note: Timer 0 current value is a 32-bit down-counter (from interval value to 0).

8.2.7.6 0x0020 Timer 1 Control Register (Default Value: 0x0000_0004)

Offset: 0x0020			Register Name: TMR1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0020			Register Name: TMR1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	TMR1_MODE Timer 1 mode 0: Periodic mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR1_CLK_PRES Select the prescaler of timer 1 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR1_CLK_SRC Timer1 Clock Source 00: RTC_32K 01: SYS_CLK24M 10: / 11: /
1	R/W	0x0	TMR1_RELOAD Timer 1 Reload 0: No effect 1: Reload timer 1 Interval value After the bit is set, it cannot be written again before it's cleared automatically.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0020			Register Name: TMR1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	TMR1_EN Timer 1 Enable 0: Stop/Pause 1: Start If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

8.2.7.7 0x0024 Timer 1 Interval Value Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: TMR1_INTV_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR1_INTV_VALUE Timer 1 Interval Value

Note: The value setting should consider the system clock and the timer clock source.

8.2.7.8 0x0028 Timer 1 Current Value Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name:TMR1_CUR_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR1_CUR_VALUE Timer 1 Current Value

Note: Timer 1 current value is a 32-bit down-counter (from interval value to 0).

8.2.7.9 0x0030 Timer 2 Control Register (Default Value: 0x0000_0004)

Offset: 0x0030			Register Name: TMR2_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0030			Register Name: TMR2_CTRL_REG
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	TMR2_MODE Timer 2 mode 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR2_CLK_PRES Select the prescaler of timer 0 clock source 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR2_CLK_SRC Timer2 Clock Source 00: RTC_32K 01: SYS_CLK24M 10: / 11: /
1	R/W	0x0	TMR2_RELOAD Timer 2 Reload 0: No effect 1: Reload timer 2 Interval value After the bit is set, it cannot be written again before it's cleared automatically.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0030			Register Name: TMR2_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	TMR2_EN Timer 2 Enable 0: Stop/Pause 1: Start If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

8.2.7.10 0x0034 Timer 2 Interval Value Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: TMR2_INTV_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR2_INTV_VALUE Timer 2 Interval Value

Note: the value setting should consider the system clock and the timer clock source.

8.2.7.11 0x0038 Timer 2 Current Value Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: TMR2_CUR_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR2_CUR_VALUE Timer 2 Current Value

Note: Timer 2 current value is a 32-bit down-counter (from interval value to 0).

8.2.7.12 0x0040 Timer 3 Control Register (Default Value: 0x0000_0004)

Offset: 0x0040			Register Name: TMR3_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0040			Register Name: TMR3_CTRL_REG
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	TMR3_MODE Timer 3 mode 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR3_CLK_PRES Select the prescaler of timer 3 clock source 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR3_CLK_SRC Timer3 Clock Source 00: RTC_32K 01: SYS_CLK24M 10: / 11: /
1	R/W	0x0	TMR3_RELOAD Timer 3 Reload 0: No effect 1: Reload timer 3 Interval value After the bit is set, it cannot be written again before it's cleared automatically.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0040			Register Name: TMR3_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	TMR3_EN Timer 3 Enable 0: Stop/Pause 1: Start If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

8.2.7.13 0x0044 Timer 3 Interval Value Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: TMR3_INTV_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR3_INTV_VALUE Timer 3 Interval Value

Note: the value setting should consider the system clock and the timer clock source.

8.2.7.14 0x0048 Timer 3 Current Value Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: TMR3_CUR_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR3_CUR_VALUE Timer 3 Current Value

Note: Timer 3 current value is a 32-bit down-counter (from interval value to 0).

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

8.3 Watchdog Timer (WDT)

8.3.1 Overview

Watchdog Timer is used to transmit a reset signal to reset the entire system after an exception occurs.

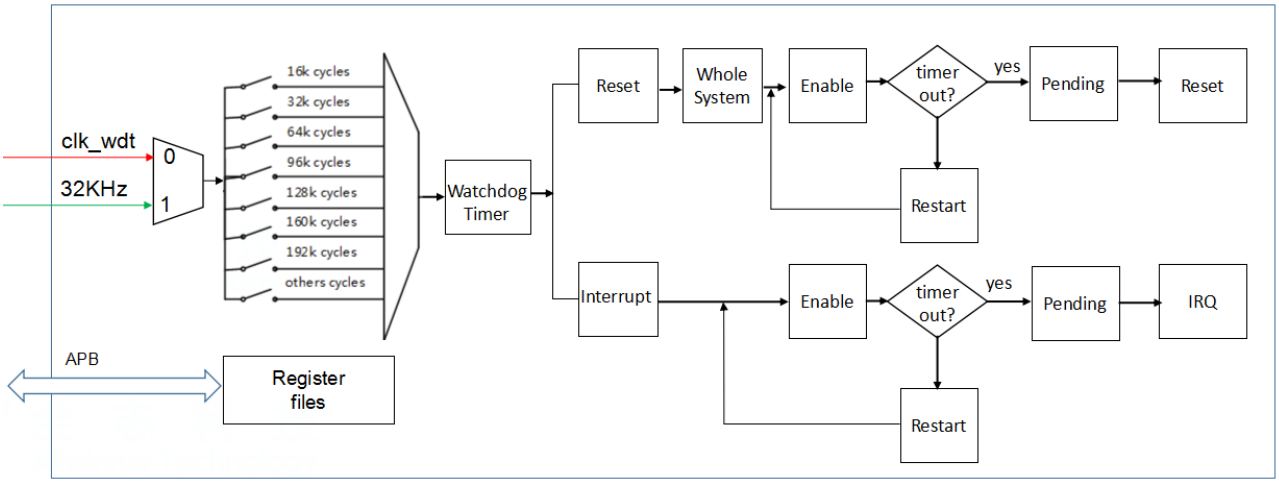
The It has the following features:

- Two clock sources selectable: RTC_32K and DCXO/750
- Includes a 32-bit up counter and a 12-bit down counter
- Configurable 12 initial values
- Supports generating timeout interrupts
- Supports generating reset signals
- Supports timer restart

8.3.2 Block Diagram

The following figure shows the functional block diagram of the watchdog module.

Figure 8-3 Watchdog Block Diagram



8.3.3 Functional Descriptions

The watchdog timer includes a 32-bit up counter and a 12-bit down counter. The counter value is increased or decreased by 1 on each rising edge of the count clock. For the down counter, it only works in the reset mode.

The watchdog timer has two operating modes: interrupt mode and reset mode.

- Interrupt mode

Write 2 b10 to WDT_CFG_REG (bit[1:0]). When the up counter value reaches the WDT_INTERVAL_VALUE set by the WDT_MODE_REG, an interrupt will be generated if WDT_IRQ_EN_REG (bit[0]) is set to 1.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- Reset mode

Write 2'b01 to WDT_CFG_REG (bit[1:0]). When the up counter value reaches the WDT_INTERVAL_VALUE set by the WDT_MODE_REG, a reset signal will be generated to reset the entire system. The period of pulling the reset signal to low is controlled by a down counter value, which is congifured by WDT_OCFG_REG (bit[11:0]).

The clock sources of WDT can be selected from CLK_32K and DCXO/750(26MHz/750) by configuring WDT_CFG_REG (bit[8]).

The WDT will restart counting by setting 1 to WDT_CTRL_REG (bit[0]) and setting 0xA57 to WDT_CTRL_REG (bit[12:1]).

8.3.4 Programming Guidelines

8.3.4.1 Initialization

Follow the steps below to initialize the watchdog timer:

Step 1 Configure the WDT_CFG_REG (bit[1:0]) to set the generation of the interrupts or the output of reset signal.

Step 2 Configure the WDT_MODE_REG (bit [7:4]) to configure the initial count value.

Step 3 Write 1 to WDT_MODE_REG (bit [0]) to enable the watchdog timer.

8.3.4.2 Interrupt Processing

Follow the steps below to process the interrupt:

Step 1 Write 1 to the WDT_IRQ_EN_REG (bit[0]) to enable the interrupt.

Step 2 After entering the interrupt process, write 1 to the WDT_IRQ_STAT (bit[0]) to clear the interrupt pending, and then process the interrupt.

Step 3 Resume the interrupt and continue to execute the interrupted process.

8.3.4.3 Watchdog Timer Reset

In the following instance making configurations for Watchdog: Configure clock source as DCXO/750, configure Interval Value as 1s and configure Watchdog Configuration as to whole system. This instance indicates that reset system after 1s.

```
writel (0x16AA_003F, WDT_OCFG_REG)                    //Set reset pulse width to 2ms
writel (0x16AA0001, WDT_CFG_REG)                      //To whole system
writel (0x16AA0010, WDT_MODE_REG)                     //Interval Value set 1s
writel ((readl(WDT_MODE_REG)|(1<<0), WDT_MODE_REG)    //Enable Watchdog
```

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

8.3.4.4 Watchdog Timer Restart

In the following instance making configurations for Watchdog:

Configure Interval Value as 1s and Configure Watchdog to reset whole system. If the time of other codes is larger than 1s, watchdog will reset the whole system. In the sentence of time of other codes inside 1s, watchdog will be restarted if the configuration of restart watchdog is implemented (normal feed dog process), and watchdog should be configured as restart after changing the interval value. Below are the procedures for Normally feed dog and Change the interval value.

1. Normally feed dog process

```
//Configure reset pulse width 2ms
writel(readl(WDT_OCFG_REG) & (~(0xFF << 0)) | (0x3F << 0) | (0x16AA << 16), WDT_OCFG_REG);
writel(readl(WDT_CFG_REG) & (~(0x1 << 0)) | (0x1 << 0), WDT_CFG_REG)          //To whole system
writel(readl(WDT_MODE_REG) & (~(0xF << 4)) | (0x1 << 4), WDT_MODE_REG) //Interval Value set 1s
writel(readl(WDT_MODE_REG) & (~(0x1 << 0)) | (0x1 << 0), WDT_MODE_REG) //Enable Watchdog
----other codes---
//Writel 0xA57 at Key Field and Restart Watchdog
writel(readl(WDT_CTRL_REG) | (0xA57 << 1) & (~(0x1 << 0)) | (0x1 << 0), WDT_CTRL_REG);
```

2. Change WDT Interval value

```
//Configure reset pulse width 2ms
writel(readl(WDT_OCFG_REG) & (~(0xFF << 0)) | (0x3F << 0) | (0x16AA << 16), WDT_OCFG_REG );
writel(readl(WDT_CFG_REG) & (~(0x1 << 0)) | (0x1 << 0), WDT_CFG_REG)    //To whole system
writel(readl(WDT_MODE_REG) & (~(0xF << 4)) | (0x1 << 4), WDT_MODE_REG) //Interval Value set 1s
writel(readl(WDT_MODE_REG) & (~(0x1 << 0)) | (0x1 << 0), WDOG_MODE_REG) //Enable Watchdog
----other codes---
writel(readl(WDT_MODE_REG) & (~(0xF << 4)), WDT_MODE_REG)    //Interval Value set 1s
//Writel 0xA57 at Key Field and Restart Watchdog
writel(readl(WDT_CTRL_REG) | (0xA57 << 1) & (~(0x1 << 0)) | (0x1 << 0), WDT_CTRL_REG)
```

8.3.5 Register List

Module Name	Base Address	Comments
WDT0_CPUX	0x02050000	
WDT_CPUS	0x07021000	WDT_CPUS register is the same with WDT0_CPUX

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
WDT_IRQ_EN_REG	0x0000	WDT IRQ Enable Register
WDT_IRQ_STAT_REG	0x0004	WDT Status Register
WDT_SRST_REG	0x0008	WDT Software Reset Register
WDT_CTRL_REG	0x000C	WDT Control Register
WDT_CFG_REG	0x0010	WDT Configuration Register
WDT_MODE_REG	0x0014	WDT Mode Register
WDT_OCFG_REG	0x0018	WDT Output Configuration Register

8.3.6 Register Description

8.3.6.1 0x0000 WDT IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: WDT_IRQ_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	WDT_IRQ_EN WDT Interrupt Enable 1: Enable 0: Disable

8.3.6.2 0x0004 WDT Status Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: WDT_IRQ_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/WAC	0x0	WDT Status WDT IRQ Pending. Setting 1 to the bit will clear it. 1: Pending. WDT interval value is reached. 0: No effect

8.3.6.3 0x0008 WDT Software Reset Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: WDT_SRST_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	KEY Field This field should be filled with 0x16AA, and then the bit 0 can be written with the new value.
15:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: WDT_SRST_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	Soft Reset Enable 0: De-assert 1: Reset System If this bit is used for system reset, the watchdog timer functions should be disabled.

8.3.6.4 0x000C WDT Control Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: WDT_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:1	W	0x0	Watchdog Key Field This bit should be written at value 0xA57. Writing any other value in this field aborts the write operation.
0	R/W1S	0x0	Watchdog Restart 0: No effect 1: Restart the Watchdog 0

8.3.6.5 0x0010 WDT Configuration Register (Default Value: 0x0000_0001)

Offset: 0x0010			Register Name: WDT_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	KEY_FIELD Key Field. This field should be filled with 0x16AA, and then the bit 15:0 can be written with the new value.
15:8	/	/	/
8	R/W	0x0	WDT Clock select 0: RTC_32K 1: DCXO/750
7:2	/	/	/
1:0	R/W	0x1	WDT Configuration 00: to E902 core (only for WDT_CPUS) 01: to whole system 10: only interrupt 11: /

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

8.3.6.6 0x0014 WDT Mode Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: WDT_MODE_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	KEY_FIELD Key Field. This field should be filled with 0x16AA, and then the bit 15:0 can be written with the new value.
15:8	/	/	/
7:4	R/W	0x0	WDT Interval Value. Watchdog clock source is DCXO/750. If the clock source is turned off, WDT will not work. 0000: 16k cycles (0.5s) 0001: 32k cycles (1s) 0010: 64k cycles (2s) 0011: 96k cycles (3s) 0100: 128k cycles (4s) 0101: 160K cycles (5s) 0110: 192k cycles (6s) 0111: 256k cycles (8s) 1000: 320k cycles (10s) 1001: 384k cycles (12s) 1010: 448k cycles (14s) 1011: 512k cycles (16s) 1100: / 1101: / 1110: / 1111: /
3:1	/	/	
0	R/W	0x0	Watchdog Enable. 0: Disable 1: Enable

8.3.6.7 0x0018 WDT Output Configuration Register (Default Value: 0x0000_001F)

Offset: 0x0018			Register Name: WDT_OCFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	KEY_FIELD Key Field. This field should be filled with 0x16AA, and then the bit 11:0 can be written with the new value.
15:12	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0018			Register Name: WDT_OCFG_REG
Bit	Read/Write	Default/Hex	Description
11:0	R/W	0x1F	WDT OUTPUT CONFIG WDT Reset Valid Time Configuration T=1/32ms*(N+1) Default 1ms

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

9 RTC

9.1 RTC

9.1.1 Overview

The Real Time Clock (RTC) is used to implement the time counter and the timing wakeup functions. The RTC can display the year, month, day, week, hour, minute, second in real time. With the independent power, the RTC can still work when system powers off.

The RTC has the following features:

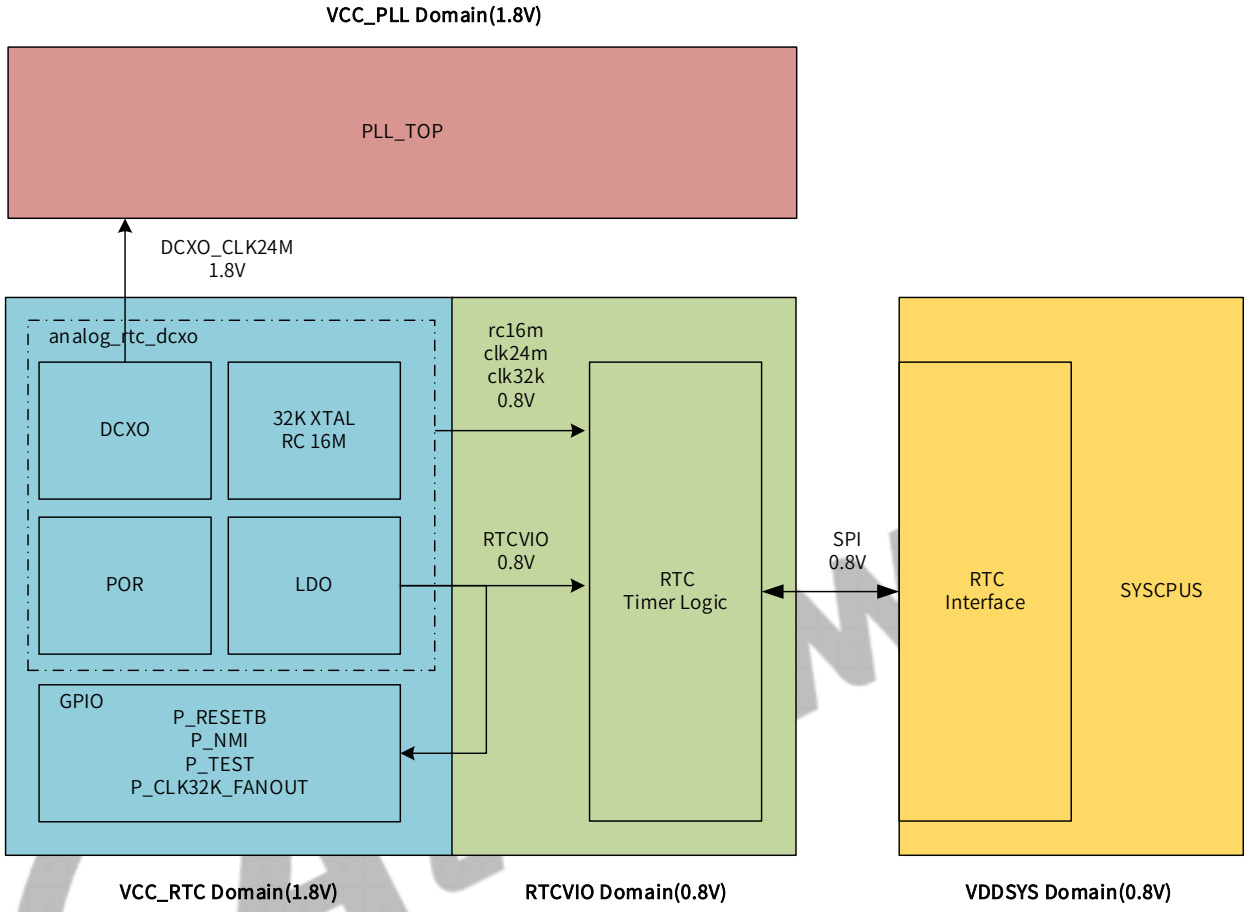
- Embedded with a 16-bit day counter, a 5-bit hour counter, a 6-bit minute counter, and a 6-bit second counter
- Externally connect to 32.768 kHz low-frequency oscillator for counting clock
- 1 kHz counting frequency
- Configurable initial value by software anytime
- Supports generating interrupt and waking up the external devices with the timing alarms function
- Supports fanout function of internal 32K clock
- 8 general-purpose registers for storing the power-off information in the VDD_RTC power domain
- Multiple special registers for recording the BROM information in the VDD_CPUS power domain

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.1.2 Block Diagram

The following figure shows the block diagram of the RTC.

Figure 9-1 RTC Block Diagram



9.1.3 External Signals

Table 9-1 RTC External Signals

Signal Name	Description	Type
X32KIN	Clock Input of 32.768 kHz Crystal	AI
X32KOUT	Clock Output of 32.768 kHz Crystal	AO
X32KFOUT	32.768 kHz clock Fanout	AO,OD
VCC-RTC	Power Supply for RTC	P
RTC-VIO	Digital Power Supply for RTC	P

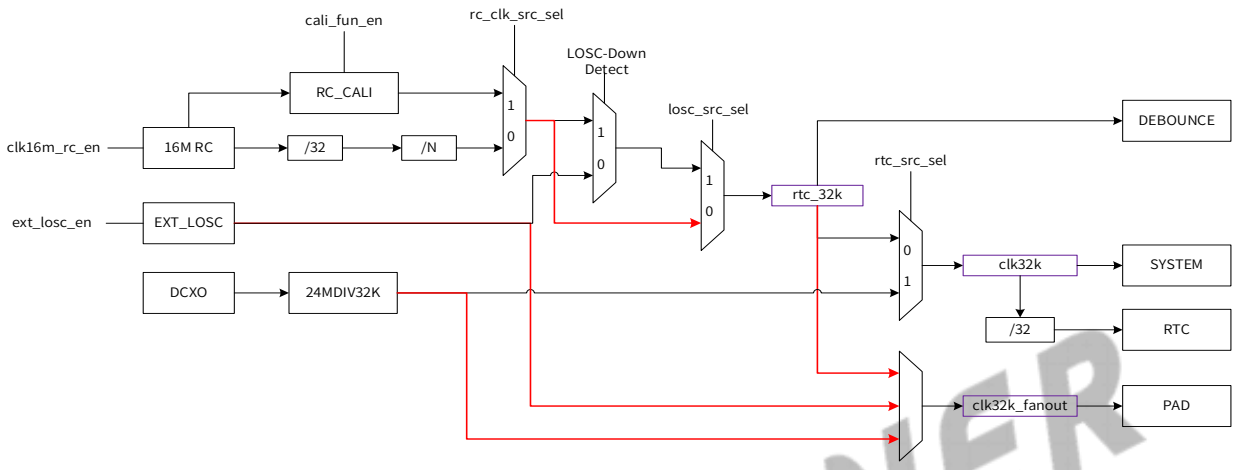
Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.1.4 Functional Descriptions

9.1.4.1 RTC Clock Tree

The following figure shows the clock tree of the RTC.

Figure 9-2 RTC Clock Tree



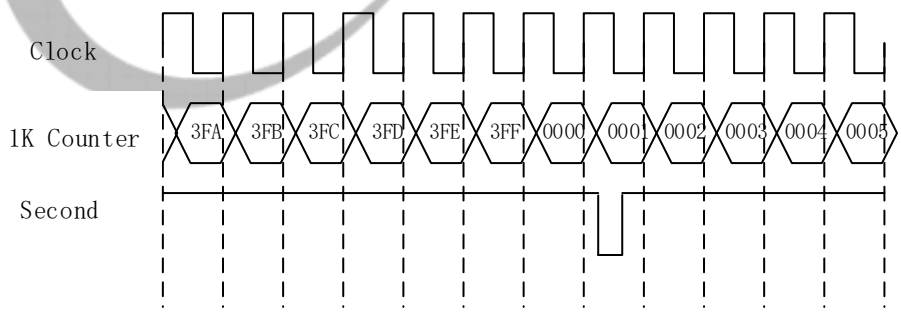
The RTC clock sources can be selected from the 32K divided from Internal RC, external low-frequency oscillator, or DCXO.

The auto clock source switch depends on LOSC detection. When there is no clock for LOSC, the RTC clock source will be switched to Internal RC.

The clock sources of RTC_32K_FANOUT and system 32K can be selected from the 32K divided from Internal RC, external low-frequency oscillator, or DCXO.

9.1.4.2 Real Time Clock

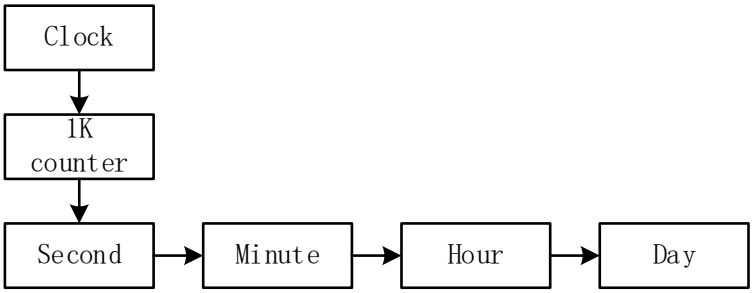
Figure 9-3 RTC Counter



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

The 1 kHz counter adds 1 on each rising edge of the clock. When the sampling clock number reaches 0x3FF, 1 kHz counter restarts to count from 0, and the second counter adds 1. The step structure of 1 kHz counter is as follows.

Figure 9-4 RTC 1 kHz Counter Step Structure



According to above implementation, the changing range of each counter is as follows.

Table 9-2 RTC Counter Changing Range

Counter	Range
Second	0 to 59
Minute	0 to 59
Hour	0 to 23
Day	0 to 65535 (The year, month, day need be transformed by software according to day counter)

CAUTION

As there is no error correction mechanism in the hardware, each counter configuration should not exceed a reasonable counting range.

9.1.4.3 Alarm 0

The ALARM0_CUR_VLU_REG is a 32bit number which adds 1 each second. When Alarm0irq is enabled, read the value of the ALARM0_CUR_VLU_REG, add n seconds, and write to the ALARM0_DAY_SET_REG. N seconds later, the value of ALARM0_CUR_VLU_REG is the same to that of ALARM0_DAY_SET_REG. Then, the Alarm0irq will be triggered.

9.1.4.4 Power-off Information Storage

The RTC provides eight 32-bit general purpose register to store power-off information.

Because VCC-RTC always holds non-power-off state after VCC-RTC cold starts, when the system is in shutdown or standby scene, the CPU can judge software process by the storing information.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

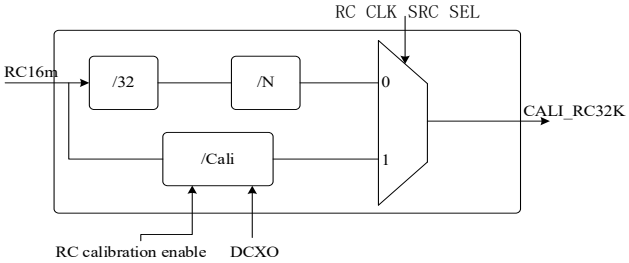
9.1.4.5 VDD-RTC

The RTC module has a LDO, the input source of the LDO is VCC_RTC, the output of the LDO is RTC_VIO, the value of RTC_VIO is adjustable, the RTC_VIO is mainly used for internal digital logic.

9.1.4.6 RC Calibration

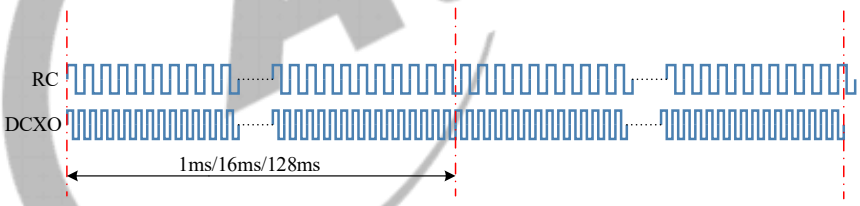
RC calibration circuit is shown as below. Whether to output the calibrated RC clock is decided by RC_Cali_SEL.

Figure 9-5 RC Calibration Circuit



The following figure shows the principle of RC calibration. The DCXO is taken as the reference clock to compute the counter number M in the RC clock within 1 ms, 16 ms, or 128 ms. As a result, the accurate frequency of the internal RC can be obtained; then, it will be divided by 32.768KHz to get the division ratio K of 32.768 KHz divided from RC clock; at last, the RC16M is divided by ratio K to get the frequency of 32.768 KHz. It should be reminded that the principle of RC calibration is to let output frequency is 32.768 KHz but not let input frequency is 16MHz.

Figure 9-6 RC and DCXO Waveform



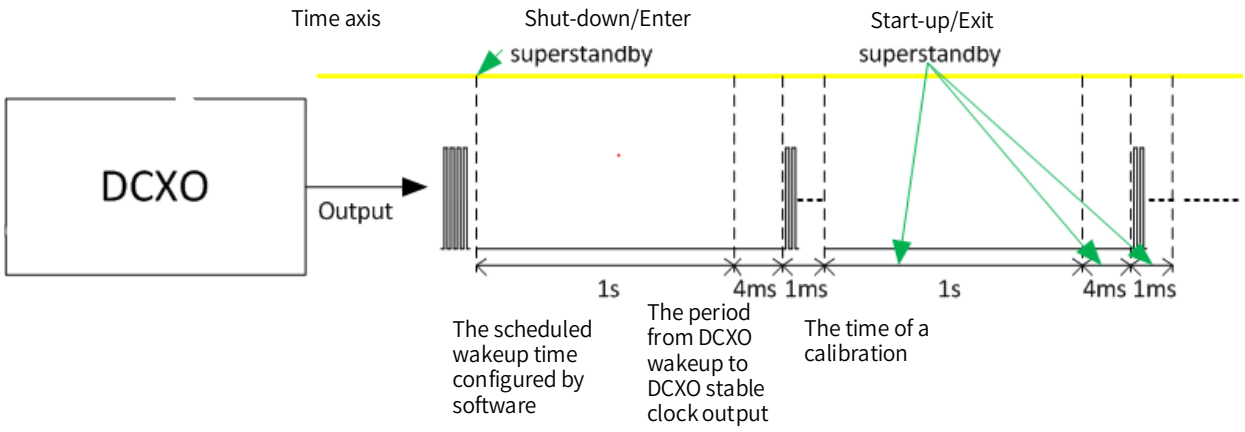
9.1.4.7 DCXO Scheduled Wake-up

The DCXO scheduled wakeup circuit includes two controls, which are the scheduled wakeup hardware automatic enable and the scheduled wakeup time length configured by software.

The scheduled wakeup means that DCXO circuit is waked up every 1s-60s in the scene of super standby or shutdown to output clock for 32K calibration; generally, the ambient temperature alters slightly within several seconds. Afterwards, DCXO circuit is switched off for a period, which is the scheduled wakeup time length configured by software. The period from DCXO wakeup to DCXO stable clock output is 3ms-4ms. If the scheduled wakeup function is disabled, DCXO circuit will keep working. The DCXO schedule wake-up diagram is shown as below.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 9-7 DCXO Scheduled wake-up diagram



In the scene of shutdown or super standby, the time of a calibration consists of the scheduled wakeup time configured by software plus the period from DCXO wakeup to DCXO stable clock output and the time of a calibration. In the above figure, the scheduled wakeup time is 1s; the actual value can be configured by software. The period from DCXO wakeup to DCXO stable clock output is theoretically 4ms; the actual value is based on the IC verifications. Among the three periods, startup or super standby exit will not lead to DCXO anomalies.

The DCXO enable signal and DCXO scheduled wakeup signal are in an OR relationship, and they do not conflict.

The intervals of operations on DCXO enable and disable should be at least 4ms.

9.1.5 Programming Guidelines

9.1.5.1 RTC Clock Source Select

To select from RTC clock sources, follow the steps as below.

a) Set LOSC_CTRL_REG [bit1] as 1 to select the divided clock whose RTC internal clock source is DCXO.

b) Set LOSC_CTRL_REG [bit1] as 0 to select the divided clock whose RTC internal clock source is External 32K or RC16M.

c) Use clock source auto switch when External 32K is lost.

Step 1 Set LOSC_CTRL_REG [bit14] as 1. When External 32K is lost, 32k clk source will be auto changed to RC.

Step 2 Set LOSC_CTRL_REG [bit4] as 1 to enable external 32768Hz crystal.

Step 3 Set LOSC_CTRL_REG [bit15] as 0 enable External 32K auto switch function.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 4 Read LOSC_AUTO_SWT_STA_REG [bit2] for three times. It is 0, indicating External 32K startup succeeds.

Step 5 Set LOSC_CTRL_REG [bit1] as 1.

Step 6 Read LOSC_AUTO_SWT_STA_REG [bit0]. If it is 1, indicating the RTC clock source has been switched to External 32K.

Step 7 Set LOSC_CTRL_REG [bit0] as 0 to select the divided clock whose RTC internal clock source is RC16M.

NOTE

When External 32K is disabled, the divided clock of RC16M will be selected whether LOSC_CTRL_REG [bit0] is written to 0 or 1.

d) Do not use clock source auto switch when External 32K is lost.

Step 1 Set LOSC_CTRL_REG [bit15] as 1 to disable External 32K auto switch function.

Step 2 Set LOSC_CTRL_REG [bit14] as 0. When External 32K is lost, 32k clk source won't be auto changed to RC.

Step 3 Set LOSC_CTRL_REG [bit0] as 0 to select the divided clock whose RTC internal clock source is RC16M.

Step 4 Set LOSC_CTRL_REG [bit0] as 1 to select the divided clock whose RTC internal clock source is External 32K.

NOTE

After External 32K auto switch function is disabled, both RC16M and External 32K should be enabled as whether 32K clock exists cannot be guaranteed in this scene.

9.1.5.2 Real Time Setting

Write the current time to RTC_DAY_REG and RTC_HH_MM_SS_REG.

NOTE

The bit [8:7] of LOSC_CTRL_REG is should be set to 0 before the next time configuration.

Here are the basic code samples.

For example, set time to 21st, 07:08:09 and read it.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

RTC_DAY_REG = 0x00000015;

RTC_HH_MM_SS_REG = 0x00070809; //0000 0000 000|0 0000(Hour) 00|00 0000(Minute) 00|00 0000(Second)

Read (RTC_DAY_REG);

Read (RTC_HH_MM_SS_REG);

9.1.5.3 Alarm0 Setting

Step 1 Enable alram0 interrupt by writing 1 to ALARM0_IRQ_EN.

Step 2 Write the count-down day, hour, minute, second number to ALARM0_DAY_SET_REG, ALARM0_CUR_VLU_REG, and ALARM0_CONFIG_REG.

Step 3 Enable alarm0 function by writing 1 to ALARM0_ENABLE_REG, then the software can query alarm count value in real time by ALARM0_DAY_SET_REG and ALARM0_CUR_VLU_REG. When the setting time is reached, ALARM0_IRQ_STA_REG is set to 1 to generate an interrupt.

Step 4 After entering the interrupt process, write 0 to the ALARM0_IRQ_STA_REG to clear the interrupt pending, and execute the interrupt process.

Step 5 Resume the interrupt and continue to execute the interrupted process.

Step 6 The power-off wakeup is generated via SoC hardware and PMU, the software only needs to set the pending condition of alarm0, and set ALARM0_CONFIG_REG to 1.

9.1.5.4 DCXO Frequency

The SoC supports three kinds of high-frequency oscillator, whose pull up/down status are input by two external PADs, DCXO_ST0 and DCXO_ST1. The two PADs status are weak pull-up by default. When external pins float or connect to power, the PAD input signal is 1. When external pins are grounded, the PAD input signal is 0. When the two PADs are combined, the oscillator status are as follows.

2'b00: 24M oscillator (UFS uses external 26M oscillator)

2'b01: 19.2M oscillator

2'b10: 26M oscillator

2'b11: 24M oscillator (UFS uses external 19.2M oscillator)

The status of DCXO_ST PAD can be read by the XO_CTRL0_REG (bit[15:14]). To avoid external interference, perform read operation for three times and ensure the read values are consistent.

As DCXO PAD status are weak pull up by default. When external pins are grounded, a leakage path will be formed. Therefore, if DCXO_ST0 and DCXO_ST1 status is 00 when the power-up completes, it indicates the external pins are grounded. In this condition, the DCXO PAD will be configured as 0 in the XO_CTRL1_REG(bit[11:8]) to avoid power leakage.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.1.5.5 PHY Reference Clock

On the SoC, DCXO outputs two independent reference clocks. One is for UFS and the other is for COMBO PHY0, COMBO PHY1, and HDMI. The clock gating is put on each analog PHY reference clock entrance. Therefore, the reference clock can be closed.

These PHY reference clock gating is controlled by XO_CTRL1_REG (bit[5:4]) and XO_CTRL1_REG (bit[1:0]) and default to be closed. Write 1 to corresponding bits to enable reference clock. The configuration principles are shown as below.

- If the PHY reference clock is supplied by external PADs, the internal reference clock gating is configured as 0 to disable clock.
- If the PHY reference clock is supplied by DCXO, the internal reference clock gating is 1 to enable clock.

The reference clocks of UFS, COMBO PHY0, COMBO PHY1 are controlled by both RTC gating and clock request of each module. For details, see the section of each module.

9.1.6 Register List

Module Name	Base Address
RTC	0x07090000

Register Name	Offset	Description
LOSC_CTRL_REG	0x0000	LOSC Control Register
LOSC_AUTO_SWT_STA_REG	0x0004	LOSC Auto Switch Status Register
INTOSC_CLK_PRESCAL_REG	0x0008	Internal OSC Clock Prescaler Register
INTOSC_CLK_AUTO_CALI_REG	0x000C	Internal OSC Clock Auto Calibration Register
RTC_DAY_REG	0x0010	RTC Year-Month-Day Register
RTC_HH_MM_SS_SET_REG	0x0014	RTC Hour-Minute-Second Register
ALARM0_DAY_SET_REG	0x0020	Alarm 0 Day Set Register
ALARM0_CUR_VLU_REG	0x0024	Alarm 0 Counter Current Value Register
ALARM0_ENABLE_REG	0x0028	Alarm 0 Enable Register
ALARM0_IRQ_EN	0x002C	Alarm 0 IRQ Enable Register
ALARM0_IRQ_STA_REG	0x0030	Alarm 0 IRQ Status Register
ALARM0_CONFIG_REG	0x0050	Alarm 0 Config Register
CLK32K_FOUT_CTRL_GATING_REG	0x0060	RTC_32K Fanout Control register
GP_DATA_REGn	0x0100+N*0x0004 (N=0~7)	General Purpose Register
XO_CTRL_WP_REG	0x015C	DCXO Control Write Protect Register
XO_CTRL_REG	0x0160	DCXO Control Register
CALI_CTRL_REG	0x0164	Calibration Control Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
XO_GATING_REG	0x016C	DCXO Gating Ctrl Register
VDD_RTC_REG	0x0190	VDD RTC Regulation Register
IC_CHARA_REG	0x01F0	IC Characteristic Register
VDD_OFF_GATING_CTRL_REG	0x01F4	VDD Off Gating Control Register
EFUSE_HV_PWRSWT_CTRL_REG	0x0204	Efuse High Voltage Power Switch Control Register
RTC_SPI_CLK_CTRL_REG	0x0310	RTC SPI Clock Control Register

NOTE

The registers whose offset is less than 0x0300 are in VDD_RTC Power Domain. The registers whose offset is no less than 0x0300 are in VDD_SYS Power Domain.

9.1.7 Register Description

9.1.7.1 0x0000 LOSC Control Register (Default Value: 0x0000_4010)

Offset: 0x0000			Register Name: LOSC_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	KEY_FIELD KEY Field This field should be filled with 0x16AA, and then the bit 0 and bit 1 can be written with the new value.
15	R/W	0x0	LOSC_AUTO_SWT_FUNCTION LOSC auto switch function disable 0: Enable 1: Disable
14	R/W	0x1	LOSC_AUTO_SWT_32K_SEL_EN LOSC auto switch 32K clk source select enable. 0: Disable. When losc is lost, 32k clk source will not change to RC 1: Enable. When losc is lost, 32k clk source will change to RC (LOSC_SRC_SEL will be changed from 1 to 0)
13:9	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: LOSC_CTRL_REG
Bit	Read/Write	Default/Hex	Description
8	R	0x0	RTC_HHMMSS_ACCE RTC Hour Minute Second access. After writing the RTC HH-MM-SS register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC HH-MM-SS register, the HH-MM-SS register will be refreshed for at most one second. Note: Time can be configured only when this bit is 0.
7	R	0x0	RTC_DAY_ACCE RTC DAY access After writing the RTC DAY register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC DAY register, the DAY register will be refreshed for at most one second. Note: Time can be configured only when this bit is 0.
6:5	/	/	/
4	R/W	0x1	EXT_LOSC_EN External 32768Hz Crystal Enable 0: Disable 1: Enable
3:2	R/W	0x0	EXT_LOSC_GSM External 32.768Hz Crystal GSM When GSM is altered, 32K oscillation circuit will arise transient instability. If the Auto Switch is enabled, it is possible that the clock source will switch from 32K to RC16M. GSM will influence the time of 32K oscillation starting. Namely, the larger the GSM value is, the shorter the oscillation starting is. Therefore, it is not necessary or recommended to alter GSM value. To alter GSM value, disable the Auto Switch and delay 50us. Then alter GSM, and switch the clock sourcing from RC16M to 32K. 00: Low 01: Reserved 10: Reserved 11: High

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: LOSC_CTRL_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	RTC_SRC_SEL RTC_TIMER Clock Source Select 0: LOSC_SRC 1: 24MDIV32K Before switching, ensure that the 24MDIV32K is enabled. Namely, the bit16 of 32K_FANOUT_GATING_REG is set to 1.
0	R/W	0x0	LOSC_SRC_SEL LOSC Clock Source Select N is the value of Internal OSC Clock Prescaler register. 0: Low Frequency Clock from 16M RC 1: External 32.768KHz OSC.

Note: The internal OSC frequency is about 16MHz.

9.1.7.2 0x0004 LOSC Auto Switch Status Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: LOSC_AUTO_SWT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R	0x0	EXT_LOSC_STA Work only when AUTO SWITCH function is enable. 0: External 32.768k OSC work normally. 1: External 32.768k OSC work abnormally.
1	R/W1C	0x0	LOSC_AUTO_SWT_PEND LOSC auto switch pending. 0: No effect 1: Auto switches pending, means LOSC_SRC_SEL is changed from 1 to 0.
0	R	0x0	LOSC_SRC_SEL_STA Checking LOSC Clock Source Status. N is the value of Internal OSC Clock Prescaler register. 0: Low Frequency Clock from 16M RC 1: External 32.768KHz OSC

9.1.7.3 0x0008 Internal OSC Clock Prescaler Register (Default Value: 0x0000_000F)

Offset: 0x0008	Register Name: INTOSC_CLK_PRESCAL_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4:0	R/W	0xF	INTOSC_32K_CLK_PRESCAL Internal OSC 32K Clock Prescaler value N. The clock output = Internal RC/32 / N. 0x0: 1 0x1: 2 0x2: 3 ..... 0x1F: 32

9.1.7.4 0x000C Internal OSC Clock Auto Calibration Register (Default Value: 0x7A00_0000)

Offset: 0x000C			Register Name: INTOSC_CLK_AUTO_CALI_REG
Bit	Read/Write	Default/Hex	Description
31:22	R	0x1E8	32k calibration integer divide factor
21:5	R	0x0	32k calibration decimal divide factor
4	R/W	0x0	Calibration Function Clk16M_RC_enable 0: Auto gating 1: Soft bypass
3:2	R/W	0x0	RC Calibration Precise Selection 00: 1 ms calibration precise 01: 16 ms calibration precise 10: 128 ms calibration precise
1	R/W	0x0	RC calibration enable 0: Close Calibration circuit 1: Open Calibration circuit
0	R/W	0x0	RC CLK SRC SEL Select the RTC 32k clock source from normal RC or Calibrated RC: 0: Normal RC 1: Calibrated RC

9.1.7.5 0x0010 RTC Year-Month-DAY Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: RTC_DAY_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	UDF	DAY Set DAY Range from 0~65535

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.1.7.6 0x0014 RTC Hour-Minute-Second Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: RTC_HH_MM_SS_SET_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	UDF	HOUR Set Hour Range from 0~23
15:14	/	/	/
13:8	R/W	UDF	MINUTE Set Minute Range from 0~59
7:6	/	/	/
5:0	R/W	UDF	SECOND Set second Range from 0~59

9.1.7.7 0x0020 Alarm 0 Day Set Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: ALARM0_DAY_SET_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	ALARM0_COUNTER Alarm 0 Counter is Based on Day.

9.1.7.8 0x0024 Alarm 0 Counter Current Value Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: ALARM0_CUR_VLU_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	UDF	HOUR Current hour Range from 0~23
15:14	/	/	/
13:8	R/W	UDF	MINUTE Current minute Range from 0~59
7:6	/	/	/
5:0	R/W	UDF	SECOND Current second Range from 0~59

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.1.7.9 0x0028 Alarm 0 Enable Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: ALARM0_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	ALM_0_EN Alarm 0 Enable 0: Disable 1: Enable

9.1.7.10 0x002C Alarm 0 IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: ALARM0_IRQ_EN
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	ALARM0_IRQ_EN Alarm 0 IRQ Enable 0: Disable 1: Enable

9.1.7.11 0x0030 Alarm 0 IRQ Status Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: ALARM0_IRQ_STA_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W1C	0x0	ALARM0_IRQ_PEND Alarm 0 IRQ Pending bit 0: No effect 1: Pending. Alarm 0 counter value is reached If alarm 0 irq enable is set to 1. The pending bit will be sent to the interrupt controller.

9.1.7.12 0x0050 Alarm 0 Config Register (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: ALARM0_CONFIG_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	ALARM0_WAKEUP Configuration of alarm wake up output 0: Disable alarm wake up output 1: Enable alarm wake up output

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.1.7.13 0x0060 RTC_32K Fanout Control Register (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: CLK32K_FOUT_CTRL_GATING_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DCXO_TO_32K_DIVIDER_ENABLE DCXO to 32k divider enable 1: Enable the DCXO 24m to 32k divider circuit 0: Disable the DCXO 24m to 32k divider circuit
15:3	/	/	/
2:1	R/W	0x0	LOSC_OUT_SRC_SEL Losc out source select. 00: RTC_32K (select by RC_CLK_SRC_SEL & LOSC_SRC_SEL) 01: LOSC 10: DCXO divided 32K
0	R/W	0x0	LOSC_OUT_GATING Losc out gating enable. Configuration of LOSC output, and no LOSC output by default. 0: Mask LOSC output gating 1: Enable LOSC output gating

9.1.7.14 0x0100+N*0x0004 (N=0~7) General Purpose Register (Default Value: 0x0000_0000)

Offset: 0x0100+N*0x0004 (N=0~7)			Register Name: GP_DATA_REGn
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	GP_DATA Data.

Note: general purpose register 0~7 value can be stored if the VDD_RTC is larger than 0.7v.

9.1.7.15 0x015C DCXO Control Write Protect Register (Default Value: 0x0000_0000)

Offset: 0x015C			Register Name: XO_CTRL_WP_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x015C			Register Name: XO_CTRL_WP_REG
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x0	Key Filed Write protect for XO_CTRL0_REG (0x0160) Write this field as 0x16AA before configuring XO_CTRL_REG(0x0160) and this field will be automatically cleared to 0 after XO_CTRL_REG is configured.

9.1.7.16 0x0160 DCXO Control0 Register (Default Value: 0x983F_10F7)

Offset: 0x0160			Register Name: XO_CTRL0_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	CLK_REQ_ENB Clk req enable 0: Enable DCXO wake up function 1: Disable DCXO wake up function
30:29	/	/	/
28	R	0x1	DCXO_STABLE_STS DCXO Stable Status 0: No stable 1: Stable
27:24	R/W	0x8	DCXO_ICTRL DCXO current control value
23	/	/	/
22:16	R/W	0x3F	DCXO_TRIM DCXO cap array value. cap cell is 55fF
15:14	R	0x0	DCXO_ST DCXO Status. 00: 24M 01: 19.2M 10: 26M 11: 24M
13	R	0x1	SYSRST_STAT System Reset Status 0: Assert 1: De-assert
12:8	R/W	0x10	DCXO_BG DCXO bandgap output voltage
7	R/W	0x1	DCXO_LDO_INRUSHB DCXO LDO driving capacity signal active high

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0160			Register Name: XO_CTRL0_REG
Bit	Read/Write	Default/Hex	Description
6	R/W	0x1	XTAL_MODE Xtal mode enable signal active high 0x0 for external clk input mode 0x1 for normal mode
5:4	R/W	0x3	DCXO_RFCLK_ENHANCE DCXO rfclk enhance Enhance driving capacity of output OUT_RF_REFCLK, 0x0 for 5pF, 0x1 for 10pF, 0x2 for 15pF, 0x3 for 20pF
3	/	/	/
2	R/W	0x1	RSTO_DLY_SEL RSTO delay select. For Debug Use Only, Can t config to 0 in normal state.
1	R/W	0x1	DCXO_EN DCXO enable 1: Enable 0: Disable
0	R/W	0x1	CLK16M_RC_EN Clock RC16M enable 1: Enable 0: Disable To ensure a steady clock source for the reset debounce circuit, some register configurations are required. When the SoC is powered on for the first time, the reset debounce circuit uses the 32k clock divided by RC16M by default. When the SoC is powered off, read corresponding bits to check whether EXT32K works normally. If yes, switch the clock source of debounce circuit to EXT32K and then close RC16M. If there is no EXT32K or external RTC, software will check whether EXT32K works normally then perform switching operation; or software will not switch off RC16M.

9.1.7.17 0x0164 Calibration Control Register (Default Value: 0x0000_0043)

Offset: 0x0164			Register Name: CALI_CTRL_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0164			Register Name: CALI_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	WAKEUP_DCXO_EN Wake up DCXO circuit enable
30:17	/	/	/
16	R/W	0x0	WAKEUP_READY_SLEEP_MODE Calibration wake up ready sleep mode, it must be set before 0x164 bit31 WAKEUP_DCXO_EN is set to 1. 0: Disable 1: Enable
15:12	R/W	0x0	TIMER FOR READY SLEEP Total timer for ready sleep 0x00: 15s 0x01: 30s 0x02: 45s 0x03: 60s 0x04: 90s 0x05: 120s 0x06: 150s Others: /
11:8	R/W	0x0	WAKEUP_CNT FOR READY SLEEP Wake up counter for ready sleep 0x00: 250ms 0x01: 500ms 0x02: 750ms 0x03: 1s 0x04: 1.25s 0x05: 1.5s 0x06: 1.75s 0x07: 2s 0x08: 2.25s 0x09: 2.5s 0x0A: 2.75s 0x0B: 3s 0x0C: 3.25s 0x0D: 3.5s 0x0E: 3.75s 0x0F: 4s

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0164			Register Name: CALI_CTRL_REG
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0x4	WAKEUP_CNT FOR SLEEP Wake up counter for sleep 0x00: 250ms 0x01: 500ms 0x02: 1s 0x03: 10s 0x04: 60s 0x05: 120s 0x06: 180s 0x07: 240s 0x08: 300s 0x09: 360s 0x0A: 420s 0x0B: 480s 0x0C: 540s 0x0D: 600s 0x0E: 1200s 0x0F: 1800s
3:0	R/W	0x3	WAIT DCXO SEL Select for DCXO active after DCXO enable 0x0: 1ms 0x1:2ms 0x2:3ms 0x3:4ms ... 0xF: 16ms

9.1.7.18 0x016C DCXO Control1 Register (Default Value: 0x0000_0500)

Offset: 0x016C			Register Name: XO_CTRL1_REG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:10	R/W	0x1	DCXO_ST1_PULL DCXO_ST1 Pull_up or down Select 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x016C			Register Name: XO_CTRL1_REG
Bit	Read/Write	Default/Hex	Description
9:8	R/W	0x1	DCXO_ST0_PULL DCXO_ST0 Pull_up or down Select 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
7:6	/	/	/
5	R/W	0x0	DCXO_SERDES1_GATING DCXO for SERDES COMBOPHY1 gating enable 0: Disable 1: Enable
4	R/W	0x0	DCXO_SERDES0_GATING DCXO for SERDES COMBOPHY0 gating enable 0: Disable 1: Enable
3	/	/	/
2	/	/	/
1	R/W	0x0	DCXO_HDMI_GATING DXCO for HDMI gating enable 0: Disable 1: Enable
0	R/W	0x0	DCXO_UFS_GATING DXCO for UFS gating enable 0: Disable 1: Enable

Note: This register's writing operation is not protected by the 0x015C register.

9.1.7.19 0x0190V DD RTC Regulation Register (Default Value: 0x0000_0003)

Offset: 0x0190			Register Name: VDD_RTC_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W	0x0	V_SEL VDD select 0: Resistance divider 1: Band gap
3	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0190			Register Name: VDD_RTC_REG
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x3	VDD_RTC_REGU RTC VIO voltage select These bits are useful for regulating the RTC_VIO from 0.65 V to 1.3 V: 0x0: 1.0 V 0x1: 0.65 V 0x2: 0.7 V 0x3: 0.8 V 0x4: 0.9 V 0x5: 1.1 V 0x6: 1.2 V 0x7: 1.3 V RTC-VIO is the VDD_RTC voltage.

9.1.7.20 0x01F0 IC Characteristic Register (Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: IC_CHARA_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	KEY_FIELD Write protect It should be written at value 0x16AA. Writing any other value in this field aborts the write operation.
15:0	R/W	0x0	ID_DATA IC_CHARA Return 0x16AA only if the KEY_FIELD is set as 0x16AA when read those bits, otherwise return 0x0.

9.1.7.21 0x01F4 VDD Off Gating Control Register (Default Value: 0x0000_0029)

Offset: 0x01F4			Register Name: VDD_OFF_GATING_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	KEY_FIELD Write protect. This field should be filled with 0x16AA, and then the bit 15 can be configured.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x01F4			Register Name: VDD_OFF_GATING_CTRL_REG
Bit	Read/Write	Default/Hex	Description
15	WAC	0x0	PWROFF_GAT_RTC_CFG. Power off gating control signal. When using vdd_sys to RTC isolation software control, write 1 to this bit. it will only be cleared by resetb release. (For Debug Use Only)
14:12	/	/	/
11:4	R/W	0x2	VCCIO_DET_SPARE VCCIO detect spare bit[7:5]: reserved bit6]: Select the default oscillator (1-band gap), which is the bandgap reference bit[4]: bypass debounce circuit 0: bypass 1: no bypass bit[3]: Enable control 0: Disable vccio detector 1: Force detector output bit[2:0]: Level adjustment 000: Detection threshold is 2.5 V 001: Detection threshold is 2.6 V 010: Detection threshold is 2.7 V 011: Detection threshold is 2.8 V 100: Detection threshold is 2.9 V 101: Detection threshold is 3 V 110~111: N/A
3	R/W	0x1	POR_RST_OUT_EN POR reset output enable 0: Disable 1: Enable
2	/	/	/
1	R/W	0x0	VDDSYS_DET_BYPASS_EN VDDSYS detect bypass enable. 0: Not bypass 1: Bypass
0	R/W	0x1	VCCIO_DET_BYPASS_EN VCCIO detect bypass enable. 0: Not bypass 1: Bypass

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.1.7.22 0x0204 Efuse High Voltage Power Switch Control Register (Default Value: 0x0000_0000)

Offset: 0x0204			Register Name: EFUSE_HV_PWRSWT_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	EFUSE_1P8V_POWER_SWITCH_CONTROL EFUSE power switch control 1: Open power switch 0: Close power switch

9.1.7.23 0x0310 RTC SPI Clock Control Register (Default Value: 0x0000_0013)

Offset: 0x0310			Register Name: RTC_SPI_CLK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	RTC_SPI_GATE_EN RTC Reg CFG SPI Clock Gating 0: Gating 1: Not Gating Note: Before configuring the RTC registers in the always-on domain, configure the division of SPI clock first, and then open the gating.
30:5	/	/	/
4:0	R/W	0x13	RTC_SPI_DIV RTC Reg CFG SPI Clock Divider M Actual SPI Clock = AHBS/(M+1),(0~31) AHBS default Freq is 400MHz, SPI Clock default Freq is 20MHz Note: SPI clock frequency cannot be larger than 50MHz, or the RTC registers will be abnormal.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

10 I/O Memory Management Unit

The I/O Memory management unit (IOMMU) is designed for the specific memory requirements of products. It maps the virtual address of peripherals accessing memory to the physical address. The IOMMU allows multiple ways to manage the location of physical address, and it can map the physical address which has potentially conflict to allocate memory space for different processes, and also allow the application of non-continuous address to map to continuous virtual address space.

MMU-600 contains the following key components:

- Two IOMMUs
  - iommu0 supports master0-3: USB0_USB1, CSI, ISP, VE_ENC
  - iommu1 supports master0-5: VE_MBUS0, VE_MBUS1, DE0, DI, G2D, EINK
- Supports mapping virtual address to physical address by hardware
- Each IOMMU supports concurrent address mapping in host modules
- Each IOMMU supports 16G space address mapping
- Each IOMMU supports maximum 15 masters
- Supports independent bypass, prefetch, and interrupt handling for masters
- Supports two-level TLBs. Each master has its own L1 TLB, while the masters in one IOMMU share a L2 TLB.
- Supports complete flush and local invalidation for TLB
- Supports triggering PTW behaviors in case of a cache miss
- Supports authorization check
- Supports 4K protection of MBUS protocol; not support that of AXI host port

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11 Memory Controllers

11.1 SDRAM controller (DRAMC)

The DRAMC has the following features:

- 32-bit LPDDR4/LPDDR4x/LPDDR5 SDRAM
- Clock frequency up to 2133 MHz for LPDDR4 and LPDDR4x
- Clock frequency up to 2400 MHz for LPDDR5
- Supports Dynamic Frequency Setting(DFS) via hardware
- Supports multiple Low Power Modes
- Supports the read-modify-write function
- Supports flip chip package
- Supports VPR/VPW command processing
- Supports DBYTE mapping and CA mapping
- Supports DVFSC only for LPDDR5
- Supports PPR only for LPDDR4 and LPDDR5

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.2 Universal Flash Storage Host Controller (UFSHC)

The Universal Flash Storage protocol developed by JEDEC is aimed to define UFS electrical interface and UFS device. UFS electrical interface is a general-purpose serial communication bus; and UFS device is a general-purpose data storage and communication medium. UFSHC is the UFS host controller compatible with UFS protocol. In the chip, the UFSHC is composed of Synopsys UFS3.0, UniPro1.8, and MPHY4.1.

The UFSHC has the following features:

- Supports Scatter/Gather DMA
- Preconfigures up to 32 task requests and 8 task management requests
- Supports various UPIU data packets (32B~65535B)
- Supports system host to program and access the 32-bit AHB slave interface
- Supports DMA data transmission through the 128-bit AXI master interface.
- Supports the following UFS2.0 features:
  - Supports HS-G3, up to 5.8Gbps theoretically in the high-speed mode.
  - Symmetrical 2RX-2TX lanes
- Supports the following UFS3.0 features:
  - Supports HS-G4, up to 11.6Gbps theoretically in the high-speed mode.
  - Supports PA_INIT error codes in UECDL register
  - Supports QOS indication of TX, RX and PA_INIT in the UECDL register
- Supports 40-bit RMMI data interface
- Supports MPHY rate mode
  - High speed: Gear 1/2/3/4 (Rate A or B)
  - Low speed: PWM Gear 1/2/3/4

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.3 SD/MMC Host Controller (SMHC)

11.3.1 Overview

The SMHC (SD-MMC Host controller) can be configured to support Secure Digital memory (SD Memory), UHS-I Card, Secure Digital I/O (SDIO), Multimedia Cards (MMC), and eMMC.

The SMHC has the following features:

- Four SD/MMC host controller (SMHC) interfaces
  - SMHC0, compliant with the protocol Secure Digital Memory (SD3.0)
  - SMHC1, compliant with the protocol Secure Digital I/O (SDIO3.0)
  - SMHC2 and SMHC3, compliant with the protocol Multimedia Card (eMMC5.1)
  - Supports one SD (Verson1.0 to 3.0) or MMC (Verson3.3 to 5.1)
- The SMHC0 and the SMHC1 support the following:
  - 1-bit or 4-bit data width
  - Maximum performance:
    - SDR mode 200 MHz@1.8 V IO pad
    - DDR mode 50 MHz@1.8 V IO pad
    - SDR mode 50 MHz@3.3 V IO pad
- The SMHC2 and the SMHC3 supports the following:
  - 1-bit, 4-bit, or 8-bit data width
  - Maximum performance
    - SDR mode 200 MHz@1.8V IO pad
    - DDR mode 200 MHz@1.8V IO pad
    - DDR mode 50 MHz@3.3V IO pad
    - SDR mode 50 MHz@3.3V IO pad
- Supports block size of 1 to 65535 bytes
- Supports hardware CRC generation and error detection
- Supports eMMC boot operation and alternative boot operation
- Supports command queue for eMMC V5.1 device
- Supports host pull-up control
- Supports Command Completion signals and interrupts to host processor, and Command Completion signal disable
- Programmable baud rate
- Supports descriptor-based internal DMA controller

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- Internal 1K Bytes FIFO for data transfer

11.3.2 Block Diagram

The following figures show the block diagrams of the SMHC.

Figure 11-1 SMHC 0-2 Block Diagram

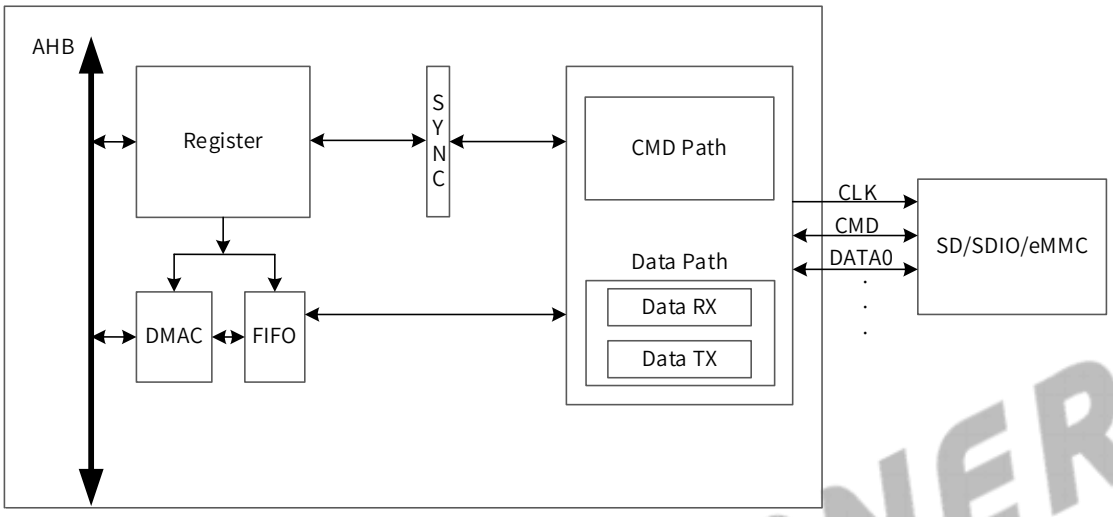
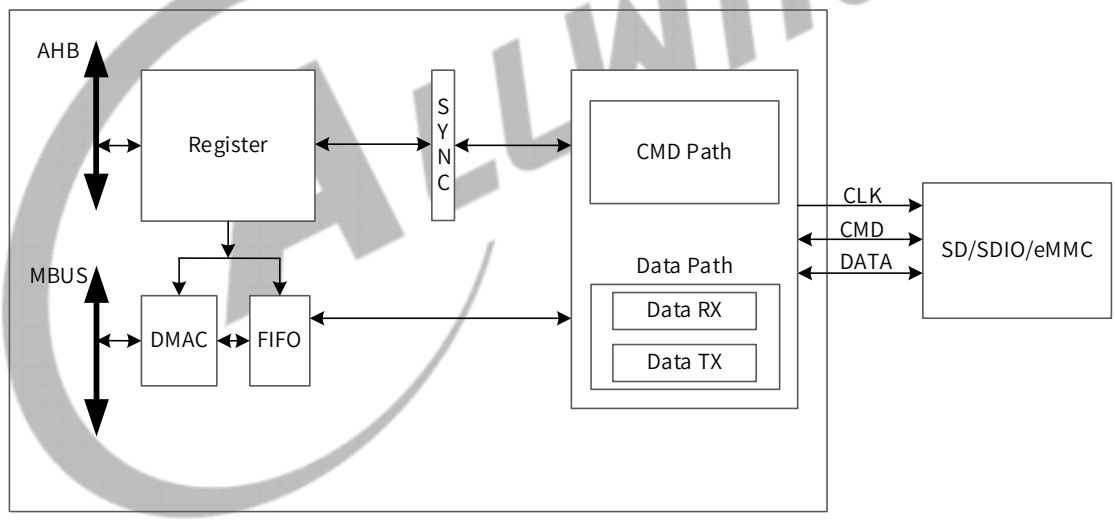


Figure 11-2 SMHC 3 Block Diagram



SMHC contains the following sub-blocks:

Table 11-1 SMHC Sub-blocks

Sub-block	Description
Register	It is used to configure the control signal for reading or writing the SD/SDIO/eMMC.
DMAC	The DMA controller that controls the data transfer between the memory and SMHC.
FIFO	A buffer for the data stream between the memory and the SMHC asynchronous clock domain.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Sub-block	Description
SYNC	It synchronizes the signals from the AHB clock domain to the SMHC clock domain.
CMD Path	It sends commands to or receives commands from the SD/SDIO/eMMC.
Data Path	It consists of Data TX and Data RX sub-modules. The Data TX sends data blocks and the CRC codes to the SD/SDIO/eMMC. The Data RX receives data blocks and the CRC codes from the SD/SDIO/eMMC.

11.3.3 Clock Sources

The following table describes the clock sources of SMHC. For clock setting, configurations, and gating information, refer to the section Clock Controller Unit (CCU).

Module	Clock Signal	Description
SMHC0/1	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.
	PERI0_400M	Its frequency is 400 MHz by default.
	PERI0_300M	Its frequency is 300 MHz by default.
	PERI1_400M	Its frequency is 400 MHz by default.
	PERI1_300M	Its frequency is 300 MHz by default.
SMHC2/3	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.
	PERI0_800M	Its frequency is 800 MHz by default.
	PERI0_600M	Its frequency is 600 MHz by default.
	PERI1_800M	Its frequency is 800 MHz by default.
	PERI1_600M	Its frequency is 600 MHz by default.

11.3.4 External Signals

The following table describes the external signals of SMHC.

Table 11-2 SMHC External Signals

Signal	Description	Type
SDC0-CLK	Clock for SD Card	O
SDC0-CMD	Command Signal for SD Card	I/O, OD
SDC0-D[3:0]	Data Input and Output for SD Card	I/O
SDC1-CLK	Clock for SDIO WIFI	O
SDC1-CMD	Command Signal for SDIO WIFI	I/O, OD
SDC1-D[3:0]	Data Input and Output for SD Card	I/O
SDC2-DS	Data Strobe for eMMC	I
SDC2-RST	Reset for eMMC	O
SDC2-CLK	Clock for eMMC	O

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Signal	Description	Type
SDC2-CMD	Command Signal for eMMC	I/O, OD
SDC2-D[7:0]	Data Input and Output for SD Card	I/O
SDC3-DS	Data Strobe for eMMC	I
SDC3-RST	Reset for eMMC	O
SDC3-CLK	Clock for eMMC	O
SDC3-CMD	Command Signal for eMMC	I/O, OD
SDC3-D[7:0]	Data Input and Output for SD Card	I/O

11.3.5 Functional Description

11.3.5.1 Data Path

The SMHC and SD/SDIO/eMMC contains the following interface buses: CLK, CMD, and DATA 1/4. During one clock cycle, the SMHC can transmit 1-bit command with one or two bits data in 1-ch DATA mode, or four or eight bits data in 4-ch DATA mode. The CMD is a bidirectional channel for initializing the SD/SDIO/eMMC and transmitting commands, and it can work in the open-drain mode and push-pull mode. The DATA is also a bidirectional channel, and it works in the push-pull mode.

- Reading Data from the SD/SDIO/eMMC

The register configures the signals for the read operation, and synchronizes the signals to the SMHC clock domain. Then the Data RX reads data from the SD/SDIO/eMMC via the CLK/CMD/DATA interface buses and writes the data in the FIFO. After that, the DMAC transfers the data from the FIFO to the memory.

- Writing Data to the SD/SDIO/eMMC

The register configures the signals for the write operation, and synchronize the signals to the SMHC clock domain. Then the DMAC reads data from the memory and writes the data to the FIFO. After that, the Data TX reads the data from the FIFO and writes the data to the SD/SDIO/eMMC via the CLK/CMD/DATA interface buses.

11.3.5.2 Package Format

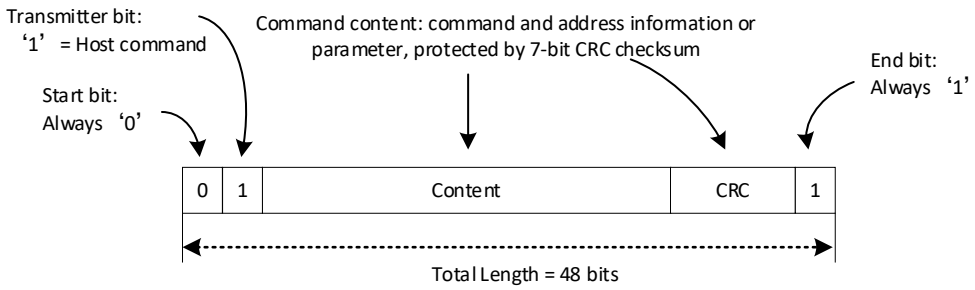
Data transfer over the SD/eMMC bus is based on command and data bit streams that are initiated by a start bit and terminated by a stop bit. There are three types of SD/eMMC packets: command token, response token, and data packet.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Command Tokens

The command token starts an operation. A command is sent from the host to a device. It is transferred serially on the CMD line. Command tokens have the following coding scheme:

Figure 11-3 Command Token Format



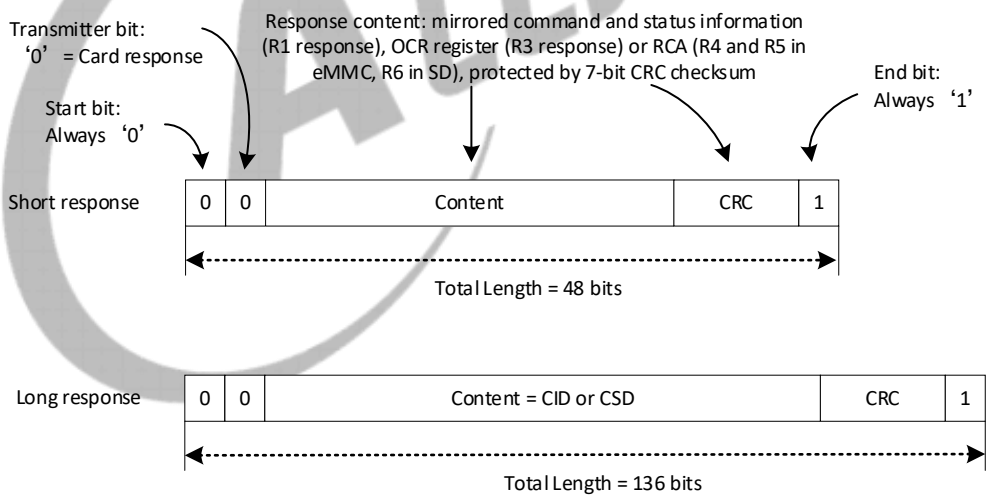
Each command token has 48 bits, preceded by a start bit (0) and succeeded by an end bit ('1'). To detect transmission errors, each token is protected by CRC bits.

Response Tokens

After receiving a command, the card returns a 48-bit or 136-bit response based on the command type.

A response token is sent from the device to the host as an answer to a previously received command. It is transferred serially on the CMD line.

Figure 11-4 Response Token Format

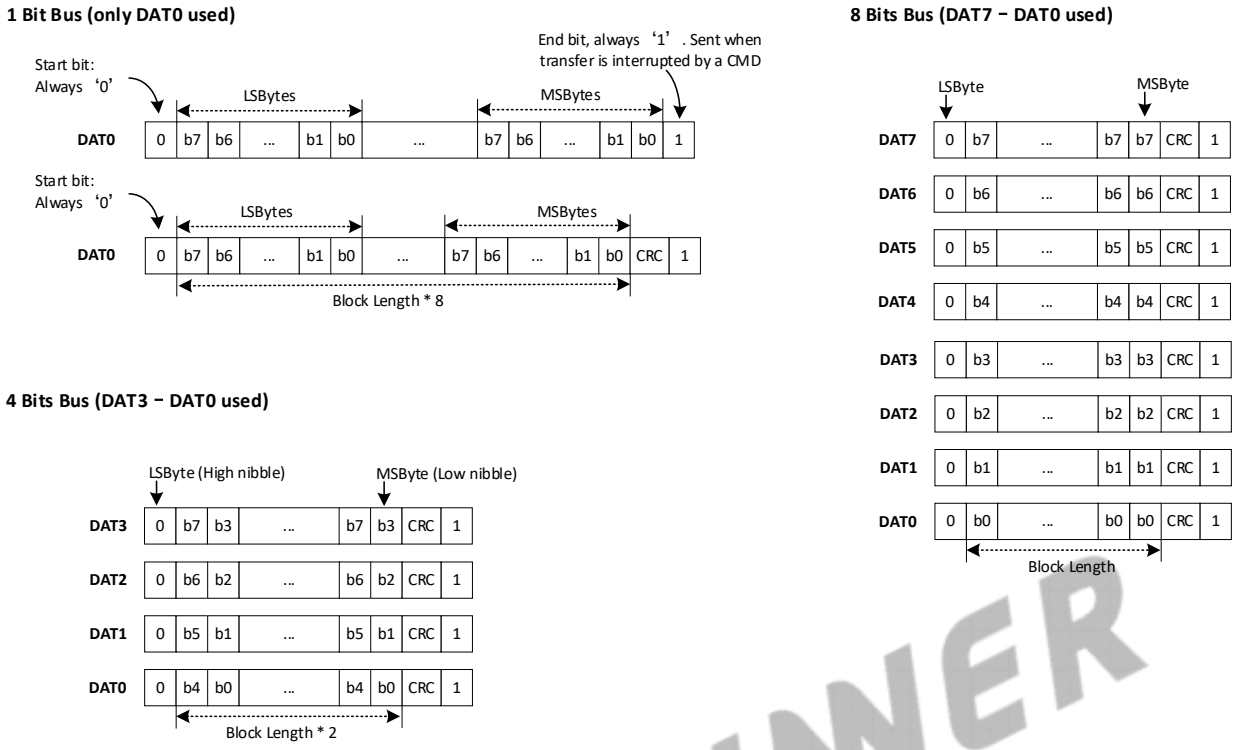


Data Packet

Data can be transferred from the device to the host or vice versa. Data are transferred via the data lines.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

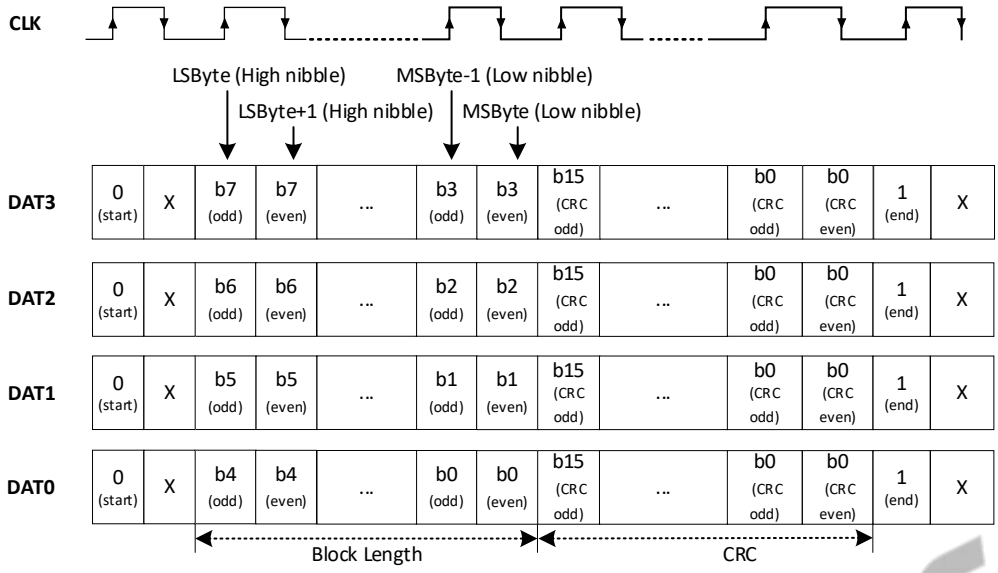
Figure 11-5 Data Packet Format for SDR



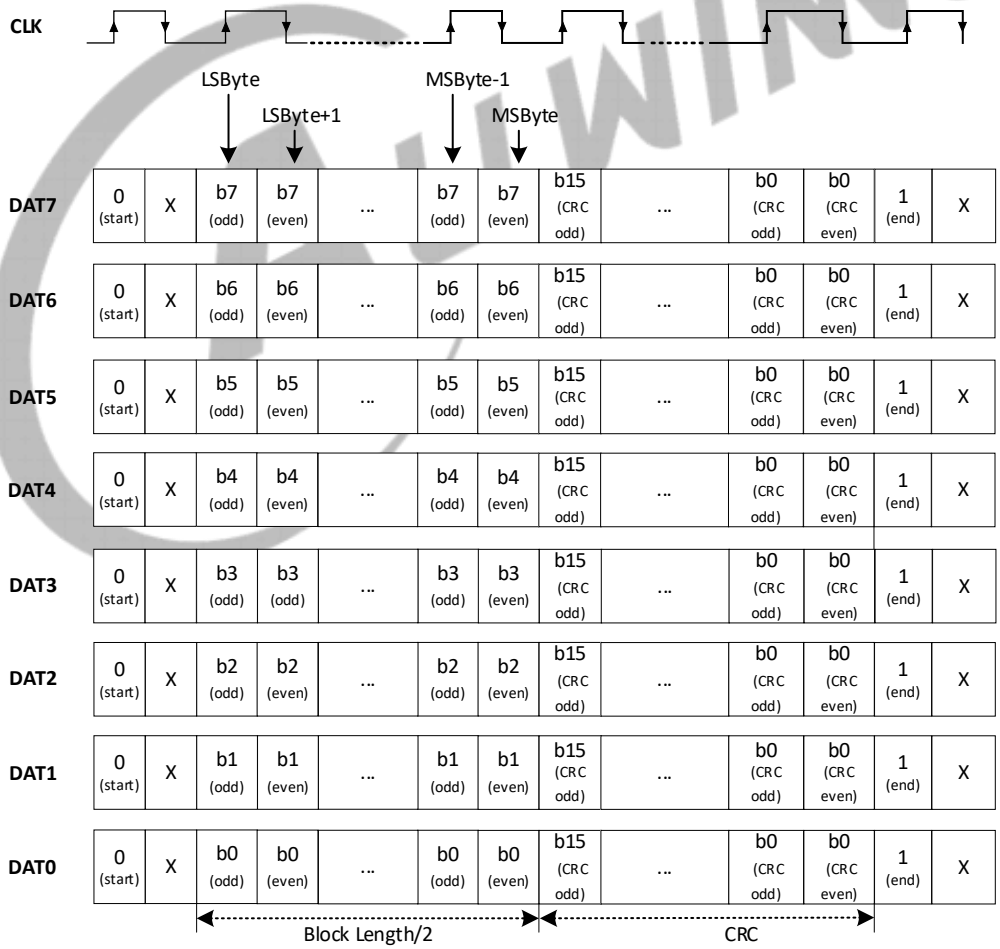
Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 11-6 Data Packet Format for DDR

4 Bits Bus DDR (DAT3 – DAT0 used)



8 Bits Bus DDR (DAT7 – DAT0 used)



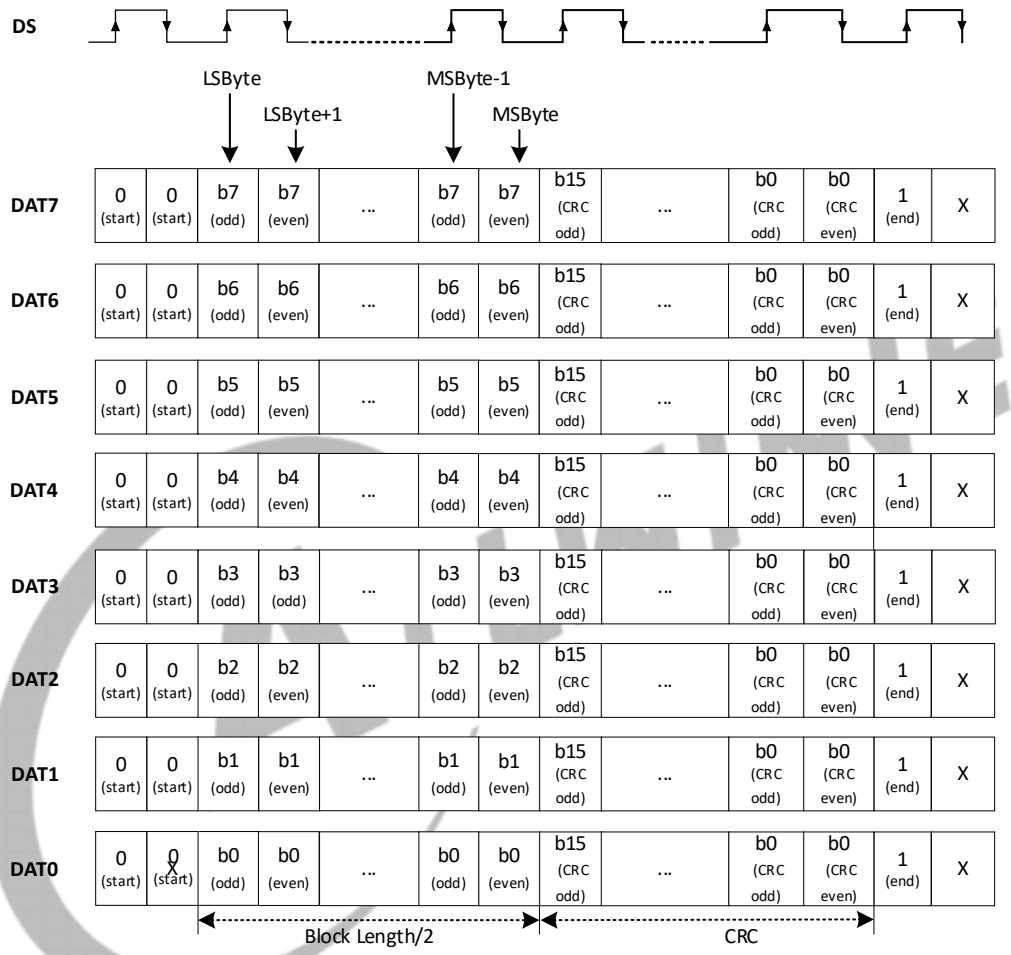
Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

NOTE

- Bytes data are not interleaved but CRCs are interleaved.
- Start and end bits are only valid on the rising edge (X indicates undefined).

Figure 11-7 Data Packet Format for DDR in HS400 Mode

8 Bits Bus DDR for HS400 Output (DAT7 – DAT0 used)



NOTE

- Bytes data are not interleaved while CRCs are interleaved.
- Start bits are valid when Data Strobe is High and Low.
- End bits are only valid when Data Strobe is High (X indicates undefined).

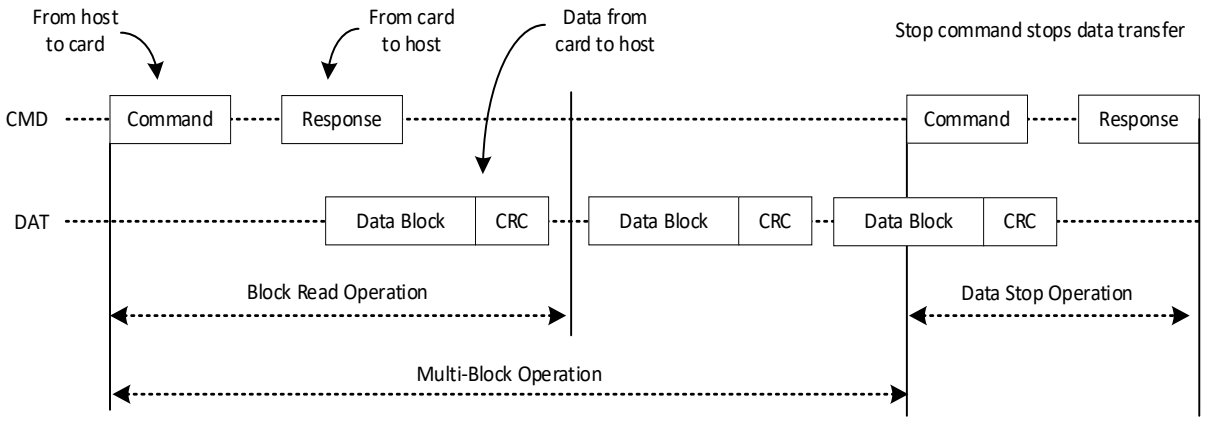
11.3.5.3 Data Transfer

Data transfers to or from the SD/eMMC card are done in blocks. Single and multiple block operations are widely used during data transfer.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

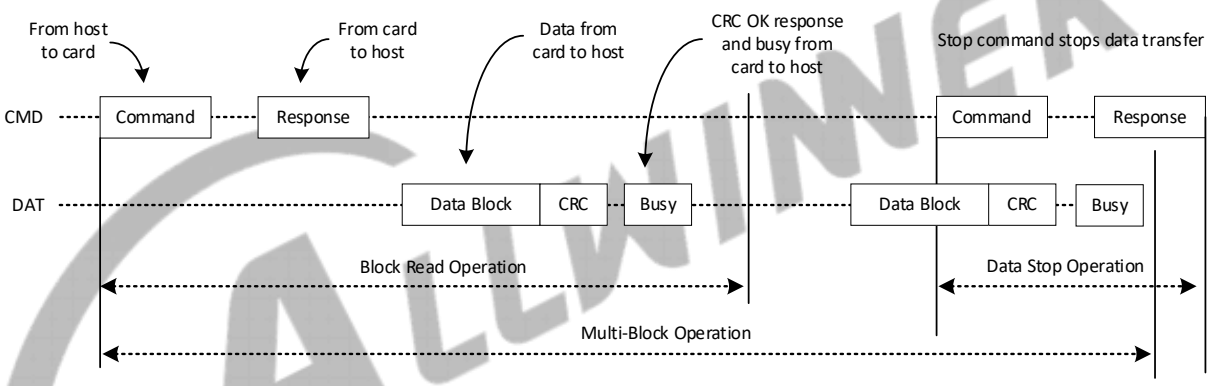
The following figure shows the single-block and multi-block read operation.

Figure 11-8 Single-Block and Multi-Block Read Operation



The following figure shows the single-block and multi-block write operation.

Figure 11-9 Single-Block and Multi-Block Write Operation



11.3.5.4 Internal DMA Controller

The SMHC has an internal DMA controller (IDMAC) to transfer data between the host memory and SMHC port. With a descriptor, the IDMAC can efficiently move data from the source to destination by automatically loading the next DMA transfer arguments, which needs less CPU intervention. Before transferring data in the IDMAC, the host driver should construct a descriptor list, configure arguments of every DMA transfer, and then launch the descriptor and start the DMA.

The IDMAC has an interrupt controller. When enabled, it generates an interrupt to the HOST CPU in situations such as data transmission is completed or some error happens.

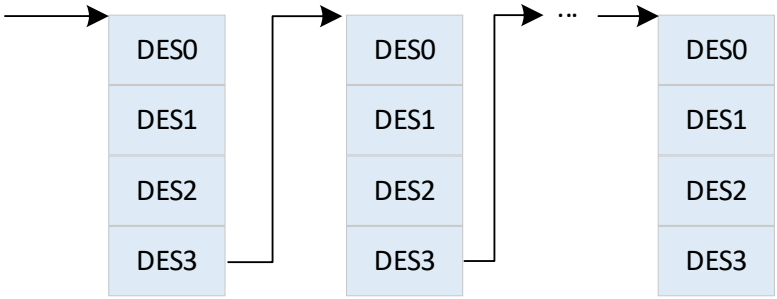
IDMAC Descriptor Structure

The IDMAC uses a descriptor with a chain structure, and each descriptor points to a unique buffer and the next descriptor.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

The following figure shows the internal formats of a descriptor.

Figure 11-10 IDMAC Descriptor Structure Diagram



This figure illustrates the internal formats of a descriptor. The descriptor address must be aligned to the bus width used for 32-bit buses. Each descriptor contains 16 bytes of control and status information.

DES0 corresponds to the [31:0] bits, DES1 corresponds to the [63:32] bits, DES2 corresponds to the [95:64] bits, and DES3 corresponds the [127:96] bits in a descriptor.

The following tables show the bit definition of DES0.

Table 11-3 SMHC 0-2 DES0 Definition

Bits	Name	Description
31	HOLD	DES_OWN_FLAG When set, this bit indicates that the descriptor is owned by the IDMAC. When this bit is reset, it indicates that the descriptor is owned by the host. This bit is cleared when transfer is over. Note: After this bit is cleared to 0, the Host CPU will be able to read the transferred data or initiate next transfer by launching a new descriptor.
30	ERROR	ERR_FLAG When some error happened in transfer, this bit will be set.
29:6	/	/
5	/	Not used
4	Chain Flag	CHAIM_MOD When set, this bit indicates that the second address in descriptor is the next descriptor address. Must be set 1.
3	First DES Flag	FIRST_FLAG When set, this bit indicates that this descriptor contains the first buffer of data. Must be set to 1 in first DES.
2	Last DES Flag	LAST_FLAG When set, this bit indicates that the buffers pointed to by this descriptor are the last data buffer
1	Disable Interrupt on completion	CUR_TXRX_OVER_INT_DIS When set, this bit will prevent the setting of the TX/RX interrupt bit of the IDMAC status register for data that ends in the buffer pointed to by this descriptor

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bits	Name	Description
0	/	/

Table 11-4 SMHC 3 DES0 Definition

Bits	Name	Description
31	HOLD	DES_OWN_FLAG When set, this bit indicates that the descriptor is owned by the IDMAC. When this bit is reset, it indicates that the descriptor is owned by the host. This bit is cleared when transfer is over. Note: After this bit is cleared to 0, the Host CPU will be able to read the transferred data or initiate next transfer by launching a new descriptor.
30:14	/	/
13:12	Buffer address pointer	BUFF_ADDR_HIGH_2BIT These bits indicate the physical address of data buffer highest 2bit, is a word(4byte) address
11:10	/	/
9 :8	Next descriptor address	NEXT_DESP_ADDR_HIGH_2BIT These bits indicate the pointer to the physical memory highest 2 bits where the next descriptor is present, is a word (4 byte) address
7:4	/	/
3	First DES Flag	FIRST_FLAG When set, this bit indicates that this descriptor contains the first buffer of data. Must be set to 1 in first DES.
2	Last DES Flag	LAST_FLAG When set, this bit indicates that the buffers pointed to by this descriptor are the last data buffer
1:0	/	/

The following table shows the bit definition of DES1.

Table 11-5 SMHC0-2 DES1 Definition

Bits	Name	Description
31:13	/	/
12:0	Buffer size	BUFF_SIZE The bits indicate the data buffer byte size, which must be a multiple of 4 bytes. If this field is 0, the DMA ignores this buffer and proceeds to the next descriptor.

Table 11-6 SMHC3 DES1 Definition

Bits	Name	Description
31:12	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bits	Name	Description
11:0	Buffer size	BUFF_SIZE These bits indicate the data buffer byte size, which must be a multiple of 4 bytes. If this filed is 0, the DMA ignores this buffer and proceeds to the next descriptor.

The following table shows the bit definition of DES2.

Table 11-7 SMHC0-3 DES2 Definition

Bits	Name	Descriptor
31:0	Buffer address pointer	BUFF_ADDR The bits indicate the physical address of the data buffer. It is a word (4byte) address.

The following table shows the bit definition of DES3.

Table 11-8 SMHC0-3 DES3 Definition

Bits	Name	Descriptor
31:0	Next descriptor address	NEXT_DESP_ADDR The bits indicate the pointer to the physical memory where the next descriptor is present. It is a word (4byte) address.

11.3.5.5 Timing Specifications

Refer to the following relative specifications:

- Physical Layer Specification Ver3.00 Final
- SDIO Specification Ver2.00
- Multimedia Cards (MMC (b)version 4.2)
- JEDEC Standard (b)JESD84-44, Embedded Multimedia Card (eMMC) Card Product Standard
- JEDEC Standard (b)JESD84-B45, Embedded Multimedia Card (eMMC) Electrical Standard (4.5 Device)
- JEDEC Standard (b)JESD84-B50, Embedded Multimedia Card (eMMC) Electrical Standard (5.0)

11.3.5.6 Phase Offset of the Command and Data

To obtain the command phase or data phase in output timing, follow the steps blow:

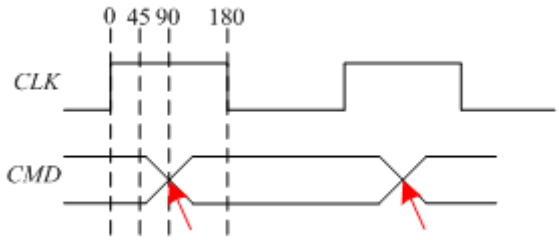
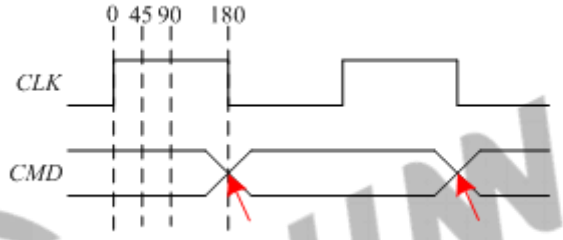
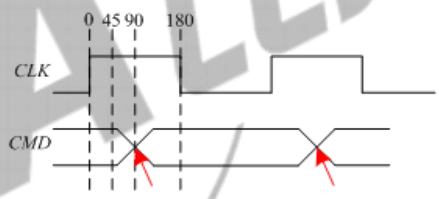
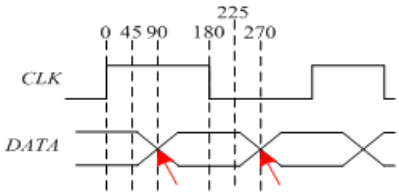
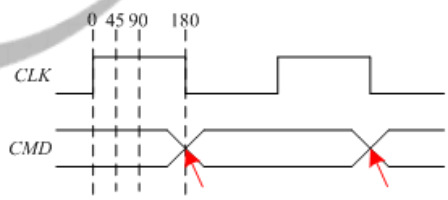
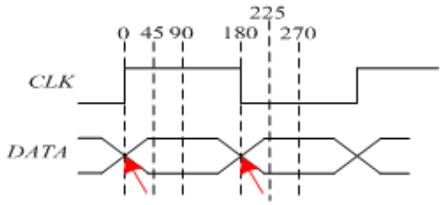
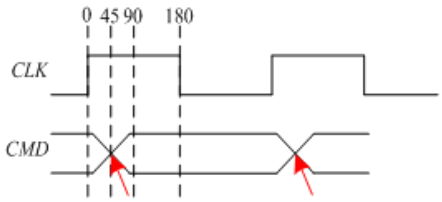
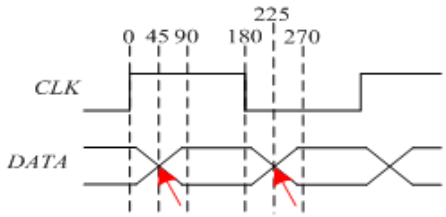
Step 1 Configure the MODE_SEL (bit [31]) and HS400_NEW_SAM_EN (bit [0]) of SMHC_NTSR (offset: 0x005C) to choose the timing mode.

Step 2 Configure the DAT_DRV_PH_SEL (bit [17]) to select data drive phase offset and configure CMD_DRV_PH_SEL (bit [16]) to select command drive phase offset in SMHC_DRV_DL (offset: 0x0140)

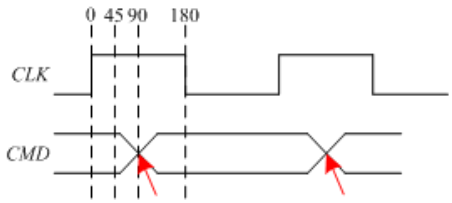
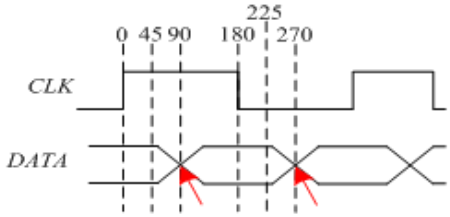
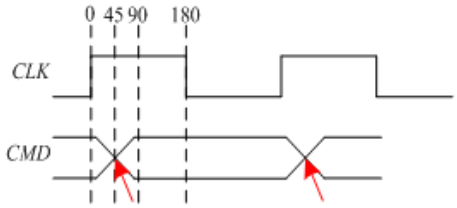
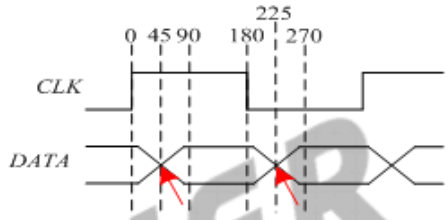
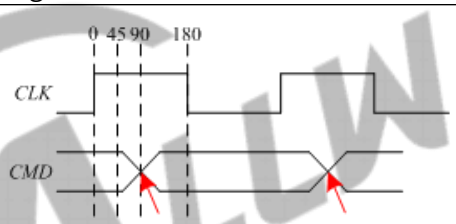
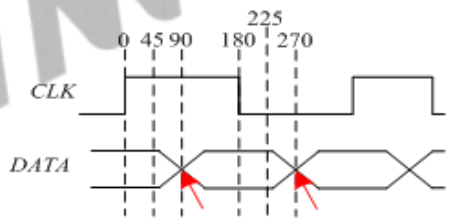
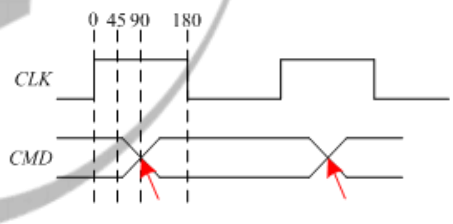
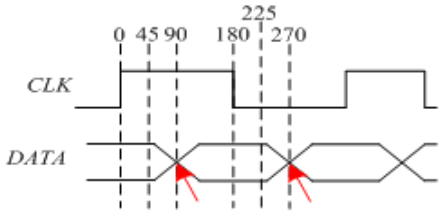
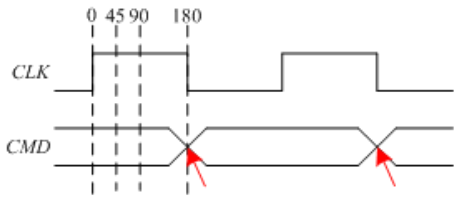
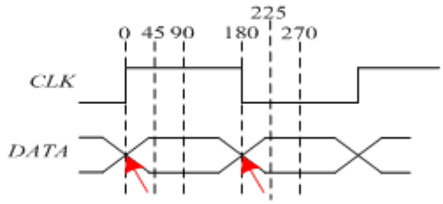
Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

The following table shows the specific configuration of command and data location.

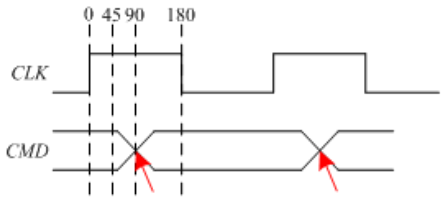
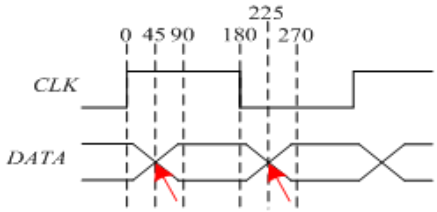
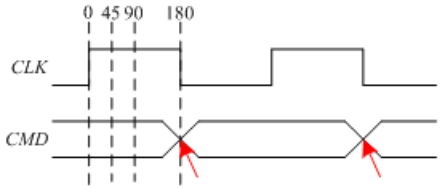
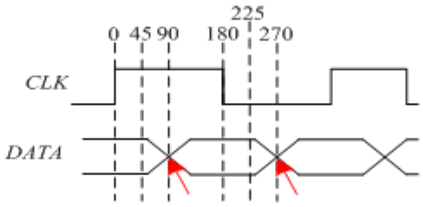
Table 11-9 Command and Data Location

Timing Mode	DRV	Command Drive Phase offset	Data Drive Phase offset
SDR	0		
		The Command updates at 90 degrees.	The data update at 90 degrees.
	1		
		The Command updates at 180 degrees.	The data updates at 180 degrees.
DDR4 (1x mode: 0x5c[31]=0)	0		
		The Command updates at 90 degrees.	The data update at 90 degrees.
	1		
		The Command updates at 180 degrees.	The data update at 0 or 180 degrees.
DDR4 (2x mode: 0x5c[31]=1)	0		

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Timing Mode	DRV	Command Drive Phase offset	Data Drive Phase offset
		The Command updates at 45 degrees.	The data update at 45 degrees.
	1		
		The Command updates at 45 degrees.	The data update at 90 degrees.
DDR8	0		
		The Command updates at 45 degrees.	The data update at 45 degrees.
	1		
		The Command updates at 90 degrees.	The data update at 90 degrees.
HS400 (1x mode: 0x5c[0] =0)	0		
		The Command updates at 90 degrees.	The data update at 90 degrees.
	1		
		The Command updates at 180 degrees.	The data update at 0 or 180 degrees.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Timing Mode	DRV	Command Drive Phase offset	Data Drive Phase offset
HS400 (2x mode: 0x5c[0] =1)	0		
		The Command updates at 90 degrees.	The data update at 45 degrees.
	1		
		The Command updates at 180 degrees.	The data update at 90 degrees.

11.3.6 Programming Guidelines

11.3.6.1 Initialization

Before data and commands are exchanged between a card and the SMHC, the SMHC needs to be initialized. The following takes SMHC0-2 as an example to initialize the SMHC:

Step 1 Configure the corresponding GPIO register as an SMHC in the section GPIO to reset clock by writing 1 to SMHCx_BGR_REG [SMHCx_RST](x=0, 1, 2, 3), and open clock gating by writing 1 to SMHCx_BGR_REG[SMHCx_GATING] (x=0, 1, 2, 3); select clock sources and set the division factor by configuring the SMHCx_CLK_REG (x=0, 1, 2, 3) register.

Step 2 Configure SMHC_CTRL to reset the FIFO and controller, and enable the global interrupt; configure SMHC_INTMASK to 0xFFCE to enable the common interrupts and the interrupts caused by error/anomaly, and then register the interrupt function.

Step 3 Configure SMHC_CLKDIV to open clock for devices. Configure SMHC_CMD as the change clock command (for example 0x80202000). Send the update clock command to deliver clock to devices.

Step 4 Configure SMHC_CMD as a normal command. Configure SMHC_CMDARG to set command parameters. Configure SMHC_CMD to set parameters like the command sequence, the response receive, the response type, the response length, the response types to send the commands. According to the initialization process in the protocol, you can finish SMHC initialization by sending the corresponding command one by one.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.3.6.2 Single-block Write

To write a single block of data, follow the steps below:

Step 1 Write 0x1 to SMHC_CTRL[DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_IDMAC to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

Step 2 Configure SMHC_FIFOTH to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA to determine the start address of the DMA descriptor.

Step 3 To write one block data to sector1, configure SMHC_BYTCNT[BYTE_CNT] to 0x200 and configure the descriptor according to the data size; set the data sector address of CMD24 (Single Data Block Write) to 0x1, write 0x80002758 to SMHC_CMD, and send CMD24 command to write data to the device.

Step 4 Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

Step 5 Check whether SMHC_IDST[TX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

Step 6 Check whether SMHC_RINTSTS[DTC] is 1. If yes, the data transfer and CMD24 writing operations are completed. Otherwise, anomaly occurs. Read SMHC_RINTSTS and SMHC_STATUS to query the existing anomaly.

Step 7 Send CMD13 command to query whether the device writing operation is completed and returns to the idle status. For example, device RCA is 0x1234, first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD, go to step4 to ensure command transfer is completed, and then check whether the highest bit of SMHC_RESP0 (CMD13 response) is 1. If yes, the device is in the idle status, and the next command can be sent. Otherwise, the device is in the busy status. Continue to send CMD13 to wait for the device to enter the idle status until timeout.

11.3.6.3 Single-block Read

To read a single block of data, follow the steps below:

Step 1 Write 0x1 to SMHC_CTRL[DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_IDMAC to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 2 Configure SMHC_FIFOTH to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA to determine the start address of the DMA descriptor.

Step 3 To read one block data from sector1, configure SMHC_BYTCNT[BYTE_CNT] to 0x200 and configure the descriptor according to the data size; set the data sector address of CMD17 command (Single Data Block Read) to 0x1, write 0x80002351 to SMHC_CMD, and send CMD17 command to read data from the device to DRAM/SRAM.

Step 4 Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

Step 5 Check whether SMHC_IDST[RX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

Step 6 Check whether SMHC_RINTSTS[DTC] is 1. If yes, data transfer and CMD17 reading operation are completed. Otherwise, anomaly occurs. Read SMHC_RINTSTS and SMHC_STATUS to query the existing abnormity.

11.3.6.4 Open-ended Multiple-Block Write

To write open-ended multiple data blocks, follow the steps below:

Step 1 Write 0x1 to SMHC_CTRL[DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_IDMAC to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

Step 2 Configure SMHC_FIFOTH to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA to determine the start address of the DMA descriptor.

Step 3 To write three blocks of data to sectors begin with sector0, configure SMHC_BYTCNT[BYTE_CNT] to 0x600 and configure the descriptor according to the data size; set the data sector address of CMD25 command (Multiple Data Blocks Write) to 0x0, write 0x80003759 to SMHC_CMD, and send CMD25 command to read data from the device to DRAM/SRAM.

Step 4 Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 5 Check whether SMHC_IDST[TX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

Step 6 Check whether SMHC_RINTSTS[ACD] and SMHC_RINTSTS[DTC] are both 1. If yes, the data transfer, CMD12 transfer, and CMD25 writing operations are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS and SMHC_STATUS to query the existing abnormity.

Step 7 Send CMD13 command to query whether the device writing operation is completed and returns to the idle status. For example, device RCA is 0x1234, first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD, go to step4 to ensure command transfer completed, and then check whether the highest bit of SMHC_RESP0 (CMD13 response) is 1. If yes, the device is in the idle status, and the next command can be sent. Otherwise, the device is in the busy status. Continue to send CMD13 to wait for the device to enter the idle status until timeout.

11.3.6.5 Open-ended Multiple-block Read

To read open-ended multiple data blocks, follow the steps below:

Step 1 Write 0x1 to SMHC_CTRL[DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_IDMAC to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

Step 2 Configure SMHC_FIFOTH to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA to determine the start address of the DMA descriptor.

Step 3 To read three blocks of data from sectors begin with sector0, configure SMHC_BYTCNT[BYTE_CNT] to 0x600 and configure the descriptor according to the data size; set the data sector address of CMD18 command (Multiple Data Blocks Read) to 0x0, write 0x80003352 to SMHC_CMD, and send CMD18 command to read data to the device. When the data transfer is completed, CMD12 will be sent automatically.

Step 4 Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

Step 5 Check whether SMHC_IDST[RX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 6 Check whether SMHC_RINTSTS[ACD] and SMHC_RINTSTS[DTC] are both 1. If yes, data transfer, CMD12 transfer, and CMD18 reading operation are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS and SMHC_STATUS to query the existing abnormity.

11.3.6.6 Pre-Defined Multiple-Block Write

To write pre-defined multiple data blocks, follow the steps below:

Step 1 Write 0x1 to SMHC_CTRL[DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_IDMAC to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

Step 2 Configure SMHC_FIFOTH to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA to determine the start address of the DMA descriptor.

Step 3 To write three blocks of data, configure SMHC_CMDARG to 0x3 to specify the number of data blocks as three. Then write 0x80000157 to SMHC_CMD to send the CMD23 command. Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successful; otherwise, continue to wait until timeout, and then exit the process.

Step 4 Configure SMHC_BYTCNT[BYTE_CNT] to 0x600 and configure the descriptor according to the data size; set the data sector address of CMD25 command (Multiple Data Blocks Write) to 0x0, write 0x80002759 to SMHC_CMD, and send CMD25 command to write data to the device.

Step 5 Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successful; otherwise, continue to wait until timeout, and then exit the process.

Step 6 Check whether SMHC_IDST[TX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

Step 7 Check whether SMHC_RINTSTS[DTC] is 1. If yes, the data transfer and CMD25 writing operations are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS and SMHC_STATUS to query the existing abnormity.

Step 8 Send CMD13 command to query whether the device writing operation is completed and returns to the idle status. For example, device RCA is 0x1234, first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD, go to step5 to ensure command transfer completed, and then check whether the highest bit of SMHC_RESP0 (CMD13 response) is 1. If yes, the device is in the idle status, and the next command can be sent. Otherwise,

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

the device is in the busy status. Continue to send CMD13 to wait for the device to enter the idle status until timeout

11.3.6.7 Pre-Defined Multiple-Block Read

To read pre-defined multiple data blocks, follow the steps below:

Step 1 Write 0x1 to SMHC_CTRL[DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_IDMAC to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

Step 2 Configure SMHC_FIFOTH to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA to determine the start address of the DMA descriptor.

Step 3 To read three blocks of data, configure SMHC_CMDARG to 0x3 to specify the number of data blocks as three. Then write 0x80000157 to SMHC_CMD to send the CMD23 command. Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successful; otherwise, continue to wait until timeout, and then exit the process.

Step 4 Configure SMHC_BYTCNT[BYTE_CNT] to 0x600 and configure the descriptor according to the data size; set the data sector address of CMD18 (Multiple Data Blocks Read) to 0x0, write 0x80002352 to SMHC_CMD, and send CMD18 command to read data from device to DRAM/SRAM.

Step 5 Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successful; otherwise, continue to wait until timeout, and then exit the process.

Step 6 Check whether SMHC_IDST[RX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

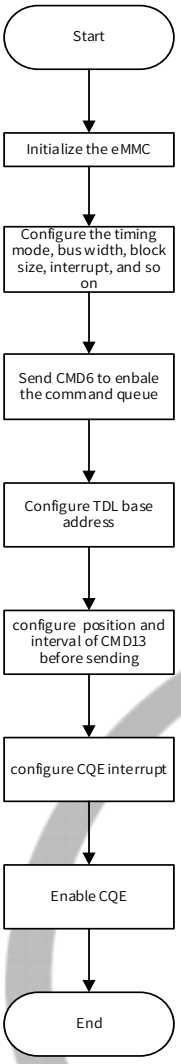
Step 7 Check whether SMHC_RINTSTS[DTC] is 1. If yes, the data transfer and CMD18 writing operations are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS and SMHC_STATUS to query the existing abnormity.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.3.6.8 eMMC Command Queue

The following figure describes the initialization process of command queue.

Figure 11-11 Command Queue Initialization



Follow the steps below to initialize the command queue:

Step 1 Initialize the eMMC. For detailed initialization steps, refer to section 11.3.6.1 Initialization.

Step 2 Send CMD6 to configure the timing mode and bus width. Send CMD16 to configure the block size as 512 B.

NOTE

The block size must be set to 512 B. After the command queue is enabled, the block size will not be able to modified.

Step 3 Send CMD6 to enable the command queue of the eMMC device.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 4 Configure CQTDLBA register and CQTDLBAU register to set the base address of the task descriptor list.

Step 5 Configure CQSSC1 register to set how to query the status of the device's task queue.

Step 6 Configure CQIC register to enable/disable interrupt, set interrupt count and timer protection.

Step 7 Configure CQRMEM register to set which errors may trigger a RED interrupt.

Step 8 Configure CQCFG register to enable CQE activity.

eMMC CMDQ supports multiple operation modes, which could be selected by configuring the CMDQ_MODE bit (bit [5:4]) of CQCFG register.

11.3.6.9 CMDP Mode

NOTE

a. SMHC1 doesn t support CMDP mode.

To enable the CMDP mode, write 1 to the CQE_EN bit (bit [0]) and configure the field value of CMDQ_MODE bit (bit [5:4]) as 2 b00 in CQCFG register.

The CMDP mode only supports block data transfers for the following transfer modes and commands:

- Data transfer- single data block reading: CMD17
- Data transfer- single data block writing: CMD24
- Data transfer- pre-defined multiple data blocks reading: CMD23 --> CMD18
- Data transfer- pre-defined multiple data blocks writing: CMD23 --> CMD25
- Data transfer - open-ended multiple data blocks reading: CMD18 --> CMD12
- Data transfer - open-ended multiple data blocks writing: CMD25 --> CMD12

In CMDP mode, the transfer descriptor and DCMD descriptor are the same as these in CMDQ mode. The differences of task descriptor between CMDP mode and CMDQ mode are as follows.

Table 11-10 Differences of Task Descriptor Between CMDP Mode and CMDQ Mode

Field Name	Bit Loc.	Description	Encoded in CMDQ	Encoded in CMDP
Valid	0	1 = The descriptor is effective and should be processed by hardware 0 = The descriptor line should not be used	Valid	Valid
End	1	Should always be set to 1. Every Task Descriptor is standalone.	End	End

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Field Name	Bit Loc.	Description	Encoded in CMDQ	Encoded in CMDP
Int	2	Indicates the interrupt generation policy required for this task. 1 = Hardware shall generate an interrupt upon the task's completion 0 = Hardware shall count task's completion for interrupt coalescing	Int	Int
Act	5:3	Shall be set to b101, to indicate this is a Task Descriptor	Act	Act
Forced Programming	6	If 1, FP is enabled. Data shall be forcefully programmed to nonvolatile storage instead of volatile cache while cache is turned ON	CMD44	CMD23[24]
Context ID	10:7	/	CMD44	CMD23[28:25]
Tag Request	11	/	CMD44	CMD23[29]
Data Direction	12	Indicates the direction of data transfer 1 = Device to Host (Read) / 0 = Host to Device (Write)	CMD44	1: Read 0: Write
Priority	13	1 = high / 0= simple	CMD44	Multiple Block 1: Multiple block transfers 0: Single block transfer
Queue Barrier (QBR)	14	/	/	Transfer Mode 1: Pre-defined transfer 0: Open-ending transfer
Reliable Write	15	To avoid data in an unknown state	CMD44	CMD23[31]
Block Count	31:16	Number of blocks to be read/written	CMD44	CMD23[15:0]
Block Address	63:32	Data block address	CMD45	CMD17/18/24/25

11.3.7 Register List

Module Name	Base Address	Comments
SMHC0	0x04020000	
SMHC1	0x04021000	SMHC1 registers are the same with those of SMHC0
SMHC2	0x04022000	SMHC2 registers are the same with those of SMHC0
SMHC3	0x04023000	

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.3.7.1 SMHC0-2 Register List

Register Name	Offset	Description
SMHC_CTRL	0x0000	SMHC Global Control Register
SMHC_CLKDIV	0x0004	SMHC Clock Control Register
SMHC_TMOUT	0x0008	SMHC Timeout Register
SMHC_CTYPE	0x000C	SMHC Bus Width Register
SMHC_BLKSIZ	0x0010	SMHC Block Size Register
SMHC_BYTCNT	0x0014	SMHC Byte Count Register
SMHC_CMD	0x0018	SMHC Command Register
SMHC_CMDARG	0x001C	SMHC Command Argument Register
SMHC_RESP0	0x0020	SMHC Response 0 Register
SMHC_RESP1	0x0024	SMHC Response 1 Register
SMHC_RESP2	0x0028	SMHC Response 2 Register
SMHC_RESP3	0x002C	SMHC Response 3 Register
SMHC_INTMASK	0x0030	SMHC Interrupt Mask Register
SMHC_MINTSTS	0x0034	SMHC Masked Interrupt Status Register
SMHC_RINTSTS	0x0038	SMHC Raw Interrupt Status Register
SMHC_STATUS	0x003C	SMHC Status Register
SMHC_FIFOTH	0x0040	SMHC FIFO Water Level Register
SMHC_FUNS	0x0044	SMHC FIFO Function Select Register
SMHC_TBC0	0x0048	SMHC Transferred Byte Count Register 0
SMHC_TBC1	0x004C	SMHC Transferred Byte Count Register 1
SMHC_CSDC	0x0054	SMHC CRC Status Detect Control Register
SMHC_A12A	0x0058	SMHC Auto Command 12 Argument Register
SMHC_NTSR	0x005C	SMHC New Timing Set Register
SMHC_HWRST	0x0078	SMHC Hardware Reset Register
SMHC_DMAC	0x0080	SMHC DMAC Control Register
SMHC_DLBA	0x0084	SMHC Descriptor List Base Address Register
SMHC_IDST	0x0088	SMHC DMAC Status Register
SMHC_IDIE	0x008C	SMHC DMAC Interrupt Enable Register
SMHC_THLD	0x0100	SMHC Card Threshold Control Register
SMHC_SFC	0x0104	SMHC Sample FIFO Control Register
SMHC_A23A	0x0108	SMHC Auto Command 23 Argument Register
EMMC_DDR_SBIT_DET	0x010C	SMHC eMMC4.5 DDR Start Bit Detection Control Register
SMHC_RESP_CRC	0x0110	SMHC Response CRC Register
SMHC_EXT_CMD	0x0138	SMHC Extended Command Register
SMHC_EXT_RESP	0x013C	SMHC Extended Response Register
SMHC_DRV_DL	0x0140	SMHC Drive Delay Control Register
SMHC_SAMP_DL	0x0144	SMHC Sample Delay Control Register
SMHC_DS_DL	0x0148	SMHC Data Strobe Delay Control Register
SMHC_CIU_CNT	0x0154	SMHC Card interface counter Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
SMHC_WR_BUSY_TMOUT	0x015C	SMHC Write Busy Timeout Register
SMHC_CQE_CTRL	0x01A0	SMHC CQE control Register
SMHC_FIFO	0x0200	SMHC FIFO Register
CQCFG	0x0408	Command Queuing Configuration Register
CQCTL	0x040C	Command Queuing Control Register
CQIS	0x0410	Command Queuing Interrupt Status Register
CQISTE	0x0414	Command Queuing Interrupt Status Enable Register
CQISGE	0x0418	Command Queuing Interrupt Signal Enable Register
CQIC	0x041C	Command Queuing Interrupt Coalescing Register
CQTDLBA	0x0420	Command Queuing Task Descriptor List Base Address Register
CQTDLBAU	0x0424	Command Queuing Task Descriptor List Base Address Upper 32 bits Register
CQTDBR	0x0428	Command Queuing Task Doorbell Register
CQTCN	0x042C	Command Queuing Task Completion Notification Register
CQDQS	0x0430	Command Queuing Device Queue Status Register
CQDPT	0x0434	Command Queuing Device Pending Tasks Register
CQTCLR	0x0438	Command Queuing Task Clear Register
CQSSC1	0x0440	Command Queuing Send Status Configuration 1 Register
CQSSC2	0x0444	Command Queuing Send Status Configuration 2 Register
CQCRDCT	0x0448	Command Queuing Command Response for Direct-Command Task Register
CQRMEM	0x0450	Command Queuing Response Mode Error Mask Register
CQTERRI	0x0454	Command Queuing Task Error Information Register
CQCRI	0x0458	Command Queuing Command Response Index Register
CQCRA	0x045C	Command Queuing Command Response Argument Register
CQFUNCCTL	0x0460	Command Queuing Function Control Register
CQDTD	0x0480	Command Queuing Descriptor Transfer Done Register
CQTCT	0x0484	Command Queuing Task Complete Total Register
CQSTATUS	0x0488	Command Queuing Controller Status Register

11.3.7.2 SMHC3 Register List

Register Name	Offset	Description
SMHC_CTRL	0x0000	SMHC Global Control Register
SMHC_CLKDIV	0x0004	SMHC Clock Control Register
SMHC_TMOUT	0x0008	SMHC Timeout Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
SMHC_CTYPE	0x000C	SMHC Bus Width Register
SMHC_BLKSIZ	0x0010	SMHC Block Size Register
SMHC_BYTCNT	0x0014	SMHC Byte Count Register
SMHC_CMD	0x0018	SMHC Command Register
SMHC_CMDARG	0x001C	SMHC Command Argument Register
SMHC_RESP0	0x0020	SMHC Response 0 Register
SMHC_RESP1	0x0024	SMHC Response 1 Register
SMHC_RESP2	0x0028	SMHC Response 2 Register
SMHC_RESP3	0x002C	SMHC Response 3 Register
SMHC_INTMASK	0x0030	SMHC Interrupt Mask Register
SMHC_MINTSTS	0x0034	SMHC Masked Interrupt Status Register
SMHC_RINTSTS	0x0038	SMHC Raw Interrupt Status Register
SMHC_STATUS	0x003C	SMHC Status Register
SMHC_FIFOTH	0x0040	SMHC FIFO Water Level Register
SMHC_FUNS	0x0044	SMHC FIFO Function Select Register
SMHC_TBC0	0x0048	SMHC Transferred Byte Count Register 0
SMHC_TBC1	0x004C	SMHC Transferred Byte Count Register 1
SMHC_CSDC	0x0054	SMHC CRC Status Detect Control Register
SMHC_A12A	0x0058	SMHC Auto Command 12 Argument Register
SMHC_NTSR	0x005C	SMHC New Timing Set Register
SMHC_HWRST	0x0078	SMHC Hardware Reset Register
SMHC_NDMA_MODE_CTL	0x007C	SMHC Normal DMA mode control Register
SMHC_DMAC	0x0080	SMHC DMAC Control Register
SMHC_DLBA	0x0084	SMHC Descriptor List Base Address Register
SMHC_IDST	0x0088	SMHC DMAC Status Register
SMHC_IDIE	0x008C	SMHC DMAC Interrupt Enable Register
SMHC_THLD	0x0100	SMHC Card Threshold Control Register
SMHC_SFC	0x0104	SMHC Sample FIFO Control Register
SMHC_A23A	0x0108	SMHC Auto Command 23 Argument Register
EMMC_DDR_SBIT_DET	0x010C	SMHC eMMC4.5 DDR Start Bit Detection Control Register
SMHC_RESP_CRC	0x0110	SMHC Response CRC Register
SMHC_EXT_CMD	0x0138	SMHC Extended Command Register
SMHC_EXT_RESP	0x013C	SMHC Extended Response Register
SMHC_DRV_DL	0x0140	SMHC Drive Delay Control Register
SMHC_SAMP_DL	0x0144	SMHC Sample Delay Control Register
SMHC_DS_DL	0x0148	SMHC Data Strobe Delay Control Register
SMHC_CIU_CNT	0x0154	SMHC Card interface counter Register
SMHC_WR_BUSY_TMOUT	0x015C	SMHC Write Busy Timeout Register
SMHC_CQE_CTRL	0x01a0	SMHC CQE Control Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
SMHC_FIFO	0x0200	SMHC FIFO Register
CQCFG	0x0408	Command Queuing Configuration Register
CQCTL	0x040C	Command Queuing Control Register
CQIS	0x0410	Command Queuing Interrupt Status Register
CQISTE	0x0414	Command Queuing Interrupt Status Enable Register
CQISGE	0x0418	Command Queuing Interrupt Signal Enable Register
CQIC	0x041C	Command Queuing Interrupt Coalescing Register
CQTDLBA	0x0420	Command Queuing Task Descriptor List Base Address Register
CQTDLBAU	0x0424	Command Queuing Task Descriptor List Base Address Upper 32 bits Register
CQTDBR	0x0428	Command Queuing Task Doorbell Register
CQTCN	0x042C	Command Queuing Task Completion Notification Register
CQDQS	0x0430	Command Queuing Device Queue Status Register
CQDPT	0x0434	Command Queuing Device Pending Tasks Register
CQTCLR	0x0438	Command Queuing Task Clear Register
CQSSC1	0x0440	Command Queuing Send Status Configuration 1 Register
CQSSC2	0x0444	Command Queuing Send Status Configuration 2 Register
CQCRDCT	0x0448	Command Queuing Command Response for Direct-Command Task Register
CQRMEM	0x0450	Command Queuing Response Mode Error Mask Register
CQTERRI	0x0454	Command Queuing Task Error Information Register
CQCRI	0x0458	Command Queuing Command Response Index Register
CQFUNCCTL	0x0460	Command Queuing Function Control Register
CQCRA	0x045C	Command Queuing Command Response Argument Register
CQDTD	0x0480	Command Queuing Descriptor Transfer Done Register
CQTCT	0x0484	Command Queuing Task Complete Total Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
CQSTATUS	0x0488	Command Queuing Controller Status Register

11.3.8 SMHC0-2 Register Description

11.3.8.1 0x0000 SMHC Global Control Register (Default Value: 0x0000_0100)

Offset: 0x0000			Register Name: SMHC_CTRL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	FIFO_AC_MOD FIFO Access Mode 1: AHB bus 0: DMA bus
30:21	/	/	/
20	R/W	0x0	DDR_16G_OFFSET Access DDR 16 G space offset 0: Hold 1: Offset When the bit is 0,normal access is available. When the bit is 1, AHB bus sends a 16G-17G address space, while the actual access is the DDR15G-16G address space.
19:18	/	/	/
17:16	R/W	0x0	SRAM_BIST_SEL SRAM BIST Select 00: for SMHC 4K SRAM(1024x32) BIST 01: for CQE SRAM(32x56) BIST 10: for EMCE SRAM BIST 11: Reserved
15:13	/	/	/
12	R/W	0x0	TIME_UNIT_CMD Time unit for command line Time unit used to calculate command line time out value defined in RTO_LMT. 0: 1 card clock period 1: 256 card clock period
11	R/W	0x0	TIME_UNIT_DAT Time unit for data line Time unit used to calculate data line time out value defined in DTO_LMT. 0: 1 card clock period 1: 256 card clock period

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: SMHC_CTRL
Bit	Read/Write	Default/Hex	Description
10	R/W	0x0	DDR_MOD_SEL DDR Mode Select Although eMMC s HS400 speed mode is 8-bit DDR, this filed should be cleared when HS400_MD_EN is set. 0: SDR mode 1: DDR mode
9	/	/	/
8	R/W	0x1	CD_DBC_ENB Card Detect (Data[3] status) De-bounce Enable 0: Disable de-bounce 1: Enable de-bounce
7:6	/	/	/
5	R/W	0x0	DMA_ENB DMA Global Enable 0: Disable DMA to transfer data, using AHB bus 1: Enable DMA to transfer data
4	R/W	0x0	INT_ENB Global Interrupt Enable 0: Disable interrupts 1: Enable interrupts
3	/	/	/
2	R/W	0x0	DMA_RST DMA Reset
1	R/W	0x0	FIFO_RST FIFO Reset 0: No change 1: Reset FIFO This bit is auto-cleared after completion of reset operation.
0	R/W	0x0	SOFT_RST Software Reset 0: No change 1: Reset SD/MMC controller This bit is auto-cleared after completion of reset operation.

11.3.8.2 0x0004 SMHC Clock Control Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: SMHC_CLKDIV
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: SMHC_CLKDIV
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MASK_DAT0 Mask Data0 0: Do not mask data0 when update clock ; 1: Mask data0 when update clock;
30:18	/	/	/
17	R/W	0x0	CCLK_CTRL Card Clock Output Control 0: Card clock always on 1: Turn off card clock when FSM in IDLE state
16	R/W	0x0	CCLK_ENB Card Clock Enable 0: Card Clock off 1: Card Clock on
15:8	/	/	/
7:0	R/W	0x0	CCLK_DIV Card clock divider n: Source clock is divided by 2*n.(n=0~255) when HS400_MD_EN is set, this field must be cleared.

11.3.8.3 0x0008 SMHC Timeout Register (Default Value:0xFFFF_FF40)

Offset: 0x0008			Register Name: SMHC_TMOUT
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: SMHC_TMOUT
Bit	Read/Write	Default/Hex	Description
31:8	R/W	0xffffff	DTO_LMT Data Timeout Limit This field can set time of the Host wait for the data from the Device. Ensure to communicate with the Device,this field must be set to maximum that greater than the time N_{AC}. About the N_{AC}, the explanation is as follows: When Host read data, data transmission from the Device starts after the access time delay N_{AC} beginning from the end bit of the read command(ACMD51,CMD8,CMD17,CMD18). When Host read multiple block(CMD18),the next block s data transmission from the Device starts after the access time delay N_{AC} beginning from the end bit of the previous block. When Host write data, this value is no effect. Note: Under the following 3 conditions, the timeout limit is half of the set time. 1> DDR8 mode 2> DDR4 and SMHC_NTSR[MODE_SELEC](0x5C[31]) high 3> HS400 and SMHC_NTSR[HS400_NEW_SAMPLE_EN](0x5C[0]) high
7:0	R/W	0x40	RTO_LMT Response Timeout Limit

11.3.8.4 0x000C SMHC Bus Width Register (Default Value:0x0000_0000)

Offset: 0x000C			Register Name: SMHC_CTYPE
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	CARD_WID Card width 00: 1-bit width 01: 4-bit width 1x: 8-bit width

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.3.8.5 0x0010 SMHC Block Size Register (Default Value:0x0000_0200)

Offset: 0x0010			Register Name: SMHC_BLKSIZ
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x200	BLK_SZ Block size

11.3.8.6 0x0014 SMHC Byte Count Register (Default Value:0x0000_0200)

Offset: 0x0014			Register Name: SMHC_BYTCNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x200	BYTE_CNT Byte counter Number of bytes to be transferred. It must be integer multiple of Block Size(BLK_SZ) for block transfers.

11.3.8.7 0x0018 SMHC Command Register (Default Value:0x0000_0000)

Offset: 0x0018			Register Name: SMHC_CMD
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CMD_LOAD Start Command. This bit is auto cleared when current command is sent. If there is no any response error happened, a command complete interrupt bit will be set in SMHC_RINTSTS register. You should not write any other command before this bit is cleared.
30:29	/	/	/
28	R/W	0x0	VOL_SW Voltage Switch 0: Normal command 1: Voltage switch command, set for CMD11 only
27	R/W	0x0	BOOT_ABT Boot Abort Setting this bit will terminate the boot operation.
26	R/W	0x0	EXP_BOOT_ACK Expect Boot Acknowledge. When Software sets this bit along in mandatory boot operation, controller expects a boot acknowledge start pattern of 0-1-0 from the selected card.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0018			Register Name: SMHC_CMD
Bit	Read/Write	Default/Hex	Description
25:24	R/W	0x0	BOOT_MOD Boot Mode 00: Normal command 01: Mandatory Boot operation 10: Alternate Boot operation 11: Reserved
23:22	/	/	/
21	R/W	0x0	PRG_CLK Change Clock 0: Normal command 1: Change Card Clock; When this bit is set, controller will change clock domain and clock output. No command will be sent.
20:18	/	/	/
17	R/W	0x0	R1B_BUSY_HW_DETECT R1b busy hardware detect enable 0: Disable hardware detect r1b busy 1: Enable hardware detect r1b busy
16	R/W	0x0	R1B_RESP R1b response 0: The response type isn t r1b for current command 1: The response type is r1b for current command Note: if STOP_CMD_FLAG set, R1B_RESP will be set by controller when send CMD12, and will be clear by controller when send next command.
15	R/W	0x0	SEND_INIT_SEQ Send Initialization 0: Normal command sending 1: Send initialization sequence before sending this command.
14	R/W	0x0	STOP_ABT_CMD Stop Abort Command 0: Normal command sending 1: Send Stop or abort command to stop current data transfer in progress.(CMD12, CMD52 for writing I/O Abort in SDIO CCCR)

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0018			Register Name: SMHC_CMD
Bit	Read/Write	Default/Hex	Description
13	R/W	0x0	WAIT_PRE_OVER Wait Data Transfer Over 0: Send command at once, do not care of data transferring 1: Wait for data transfer completion before sending current command
12	R/W	0x0	STOP_CMD_FLAG Send Stop CMD Automatically (CMD12) 0: Do not send stop command at end of data transfer 1: Send stop command automatically at end of data transfer If set, the SMHC_RESP1 will record the response of auto CMD12.
11	R/W	0x0	TRANS_MODE Transfer Mode 0: Block data transfer command 1: Stream data transfer command
10	R/W	0x0	TRANS_DIR Transfer Direction 0: Read operation 1: Write operation
9	R/W	0x0	DATA_TRANS Data Transfer 0: without data transfer 1: with data transfer
8	R/W	0x0	CHK_RESP_CRC Check Response CRC 0: Do not check response CRC 1: Check response CRC
7	R/W	0x0	LONG_RESP Response Type 0:Short Response (48 bits) 1:Long Response (136 bits)
6	R/W	0x0	RESP_RCV Response Receive 0: Command without Response 1: Command with Response
5:0	R/W	0x0	CMD_IDX CMD Index Command index value

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.3.8.8 0x001C SMHC Command Argument Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SMHC_CMDARG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CMD_ARG Command argument

11.3.8.9 0x0020 SMHC Response 0 Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SMHC_RESP0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CMD_RESP0 Response 0 Bit[31:0] of response

11.3.8.10 0x0024 SMHC Response 1 Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: SMHC_RESP1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CMD_RESP1 Response 1 Bit[63:32] of response

11.3.8.11 0x0028 SMHC Response 2 Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: SMHC_RESP2
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CMD_RESP2 Response 2 Bit[95:64] of response

11.3.8.12 0x002C SMHC Response 3 Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: SMHC_RESP3
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CMD_RESP3 Response 3 Bit[127:96] of response

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.3.8.13 0x0030 SMHC Interrupt Mask Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SMHC_INTMASK
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CARD_REMOVAL_INT_EN Card Removed Interrupt Enable
30	R/W	0x0	CARD_INSERT_INT_EN Card Inserted Interrupt Enable
29:19	/	/	/
18	R/W	0x0	DATA_WR_BUSY_TO_INT_EN Data write busy timeout interrupt enable
17	R/W	0x0	R1B_BUSY_CLR_INT_EN
16	R/W	0x0	SDIO_INT_EN SDIO Interrupt Enable
15	R/W	0x0	DEE_INT_EN Data End-bit Error Interrupt Enable
14	R/W	0x0	ACD_INT_EN Auto Command Done Interrupt Enable
13	R/W	0x0	DSE_BC_INT_EN Data Start Error Interrupt Enable
12	R/W	0x0	CB_IW_INT_EN Command Busy and Illegal Write Interrupt Enable
11	R/W	0x0	FU_FO_INT_EN FIFO Underrun/Overflow Interrupt Enable
10	R/W	0x0	DSTO_VSD_INT_EN Data Starvation Timeout/V1.8 Switch Done Interrupt Enable
9	R/W	0x0	DTO_BDS_INT_EN Data Timeout/Boot Data Start Interrupt Enable
8	R/W	0x0	RTO_BACK_INT_EN Response Timeout/Boot ACK Received Interrupt Enable
7	R/W	0x0	DCE_INT_EN Data CRC Error Interrupt Enable
6	R/W	0x0	RCE_INT_EN Response CRC Error Interrupt Enable
5	R/W	0x0	DRR_INT_EN Data Receive Request Interrupt Enable
4	R/W	0x0	DTR_INT_EN Data Transmit Request Interrupt Enable
3	R/W	0x0	DTC_INT_EN Data Transfer Complete Interrupt Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0030			Register Name: SMHC_INTMASK
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	CC_INT_EN Command Complete Interrupt Enable
1	R/W	0x0	RE_INT_EN Response Error Interrupt Enable
0	/	/	/

11.3.8.14 0x0034 SMHC Masked Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: SMHC_MINTSTS
Bit	Read/Write	Default/Hex	Description
31	R	0x0	M_CARD_REMOVAL_INT Card Removed
30	R	0x0	M_CARD_INSERT Card Inserted
29:19	/	/	/
18	R	0x0	DATA_WR_BUSY_TO_INT Data write busy timeout interrupt
17	R	0x0	R1B_BUSY_CLR_INT
16	R	0x0	M_SDIO_INT SDIO Interrupt
15	R	0x0	M_DEE_INT Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit. When set during transmitting data, it means that host controller does not receive CRC status token.
14	R	0x0	M_ACD_INT Auto Command Done When set, it means auto stop command(CMD12) completed.
13	R	0x0	M_DSE_BC_INT Data Start Error/busy clear When set during receiving data, it means that host controller found a error start bit. When set during transmitting data, it means that busy signal is cleared after the last block.
12	R	0x0	M_CB_IW_INT Command Busy and Illegal Write
11	R	0x0	M_FU_FO_INT FIFO Underrun/Overflow

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0034			Register Name: SMHC_MINTSTS
Bit	Read/Write	Default/Hex	Description
10	R	0x0	M_DSTO_VSD_INT Data Starvation Timeout/V1.8 Switch Done
9	R	0x0	M_DTO_BDS_INT Data Timeout/Boot Data Start
8	R	0x0	M_RTO_BACK_INT Response Timeout/Boot ACK Received
7	R	0x0	M_DCE_INT Data CRC Error When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status token is negative.
6	R	0x0	M_RCE_INT Response CRC Error
5	R	0x0	M_DRR_INT Data Receive Request When set, it means that there are enough data in FIFO during receiving data.
4	R	0x0	M_DTR_INT Data Transmit Request When set, it means that there are enough space in FIFO during transmitting data.
3	R	0x0	M_DTC_INT Data Transfer Complete
2	R	0x0	M_CC_INT Command Complete
1	R	0x0	M_RE_INT Response Error When set, Transmit Bit error or End Bit error or CMD Index error may occurs.
0	/	/	/

11.3.8.15 0x0038 SMHC Raw Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	CARD_REMOVAL Card Removed This is write-1-to-clear bits.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	Read/Write	Default/Hex	Description
30	R/W1C	0x0	CARD_INSERT Card Inserted This is write-1-to-clear bits.
29:19	/	/	/
18	R/W1C	0x0	DATA_WR_BUSY_TO_INT Data write busy timeout interrupt This is write-1-to-clear bits
17	R/W1C	0x0	R1B_BUSY_CLR R1b busy clear When set, it means that the r1b busy has finished or not set.
16	R/W1C	0x0	SDIOI_INT SDIO Interrupt This is write-1-to-clear bits.
15	R/W1C	0x0	DEE Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit. When set during transmitting data, it means that host controller does not receive CRC status token. This is write-1-to-clear bits.
14	R/W1C	0x0	ACD Auto Command Done When set, it means auto stop command(CMD12) completed. This is write-1-to-clear bits.
13	R/W1C	0x0	DSE_BC Data Start Error/busy clear When set during receiving data, it means that host controller found a error start bit. It is valid at 4-bit or 8-bit bus mode, When it set, host found start bit at data0, but not find start bit at some or all of the other data lines. When set during transmitting data, it means that busy signal is cleared after the last block. This is write-1-to-clear bits.
12	R/W1C	0x0	CB_IW Command Busy and Illegal Write This is write-1-to-clear bits.
11	R/W1C	0x0	FU_FO FIFO Underrun/Overflow This is write-1-to-clear bits.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	Read/Write	Default/Hex	Description
10	R/W1C	0x0	DSTO_VSD Data Starvation Timeout/V1.8 Switch Done This is write-1-to-clear bits.
9	R/W1C	0x0	DTO_BDS Data Timeout/Boot Data Start When set during receiving data, it means host did not find start bit on data0(1-bit bus) or data0~data3(4-bit bus) or data0~data7(8-bit bus). This is write-1-to-clear bits.
8	R/W1C	0x0	RTO_BACK Response Timeout/Boot ACK Received This is write-1-to-clear bits.
7	R/W1C	0x0	DCE Data CRC Error When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status token is negative. This is write-1-to-clear bits.
6	R/W1C	0x0	RCE Response CRC Error This is write-1-to-clear bits.
5	R/W1C	0x0	DRR Data Receive Request When set, it means that there are enough data in FIFO during receiving data. This is write-1-to-clear bits.
4	R/W1C	0x0	DTR Data Transmit Request When set, it means that there are enough space in FIFO during transmitting data. This is write-1-to-clear bits.
3	R/W1C	0x0	DTC Data Transfer Complete This is write-1-to-clear bits.
2	R/W1C	0x0	CC Command Complete When set, it means that current command completes even through error occurs. This is write-1-to-clear bits.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	Read/Write	Default/Hex	Description
1	R/W1C	0x0	RE Response Error When set, Transmit Bit error or End Bit error or CMD Index error may occurs. This is write-1-to-clear bits.
0	/	/	/

11.3.8.16 0x003C SMHC Status Register (Default Value: 0x0000_0006)

Offset: 0x003C			Register Name: SMHC_STATUS
Bit	Read/Write	Default/Hex	Description
31	R	0x0	DMA_REQ DMA Request DMA request signal state
30:28	/	/	/
27:17	R	0x0	FIFO_LEVEL FIFO Level Number of filled locations in FIFO
16:11	R	0x0	RESP_IDX Response Index Index of previous response, including any auto-stop sent by controller
10	R	0x0	FSM_BUSY Data FSM Busy Data transmit or receive state-machine is busy 0: Card FSM is idle 1: Card FSM is busy
9	R	0x0	CARD_BUSY Card data busy Inverted version of DATA[0] 0: Card data not busy 1: Card data busy
8	R	0x0	CARD_PRESENT Data[3] status level of DATA[3]; checks whether card is present 0: Card not present 1: Card present

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x003C			Register Name: SMHC_STATUS
Bit	Read/Write	Default/Hex	Description
7:4	R	0x0	FSM_STA Command FSM states: 0000: Idle 0001: Send init sequence 0010: TX CMD start bit 0011: TX CMD TX bit 0100: TX CMD index + argument 0101: TX CMD CRC7 0110: TX CMD end bit 0111: RX response start bit 1000: RX response IRQ response 1001: RX response TX bit 1010: RX response CMD index 1011: RX response data 1100: RX response CRC7 1101: RX response end bit 1110: CMD path wait NCC 1111: Wait; CMD-to-response turnaround
3	R	0x0	FIFO_FULL FIFO full 1: FIFO full 0: FIFO not full
2	R	0x1	FIFO_EMPTY FIFO Empty 1: FIFO Empty 0: FIFO not Empty
1	R	0x1	FIFO_TX_LEVEL FIFO TX Water Level flag 0: FIFO didn t reach transmit trigger level 1: FIFO reached transmit trigger level
0	R	0x0	FIFO_RX_LEVEL FIFO TX Water Level flag 0: FIFO didn t reach receive trigger level 1: FIFO reached receive trigger level

11.3.8.17 0x0040 SMHC FIFO Water Level Register (Default Value: 0x000F_0000)

Offset: 0x0040			Register Name: SMHC_FIFOTH
Bit	Read/Write	Default/Hex	Description
31	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0040			Register Name: SMHC_FIFOTH
Bit	Read/Write	Default/Hex	Description
30:28	R/W	0x0	BSIZE_OF_TRANS Burst size of multiple transaction 000: 1 transfers 001: 4 010: 8 011: 16 Others: Reserved Should be programmed same as DMA controller multiple transaction size. The units for transfers are the DWORD(4Byte). A single transfer would be signaled based on this value. Value should be sub-multiple of (RX_TL + 1) and (FIFO_DEPTH - TX_TL) Recommended: BSIZE_OF_TRANS = 3,MSize = 16, TX_TL = 240, RX_TL = 15 FIFO_DEPTH = 256 FIFO_SIZE = 256 * 32 = 1K
27	/	/	/
26:16	R/W	0xF	RX_TL RX Trigger Level When BLOCK2K_EXIST is 1 b1: 0x0~0x3FE: RX Trigger Level is 0~1022(Unit is equal to the FIFO_WIDTH); 0x3FF reserved When BLOCK2K_EXIST is 1 b0: 0x0~0xFE: RX Trigger Level is 0~254 (Unit is equal to the FIFO_WIDTH); 0xFF reserved FIFO threshold when FIFO request host to receive data from FIFO. When FIFO data level is greater than this value, DMA is request is raised if DMA enabled, or RX interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. 15 (means greater than 15)
15:11	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0040			Register Name: SMHC_FIFOTH
Bit	Read/Write	Default/Hex	Description
10:0	R/W	0x0	TX_TL TX Trigger Level When BLOCK2K_EXIST is 1 b1: 0x1~0x3FF: TX Trigger Level is 1~1023 (Unit is equal to the FIFO_WIDTH); 0x0: no trigger When BLOCK2K_EXIST is 1 b0: 0x1~0xFF: TX Trigger Level is 1~255 (Unit is equal to the FIFO_WIDTH); 0x0: no trigger FIFO threshold when FIFO requests host to transmit data to FIFO. When FIFO data level is less than or equal to this value, DMA TX request is raised if DMA enabled, or TX request interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. Recommended: 240(means less than or equal to 240)

11.3.8.18 0x0044 SMHC FIFO Function Select Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: SMHC_FUNS
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	ABT_RDATA Abort Read Data 0: Ignored 1: After suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets bit to reset data state-machine, which is waiting for next block of data. Used in SDIO card suspends sequence. This bit is auto-cleared once controller reset to idle state.
1	R/W	0x0	READ_WAIT Read Wait 0: Clear SDIO read wait 1: Assert SDIO read wait

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0044			Register Name: SMHC_FUNS
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	HOST_SEND_MMC_IRQRESQ Host Send MMC IRQ Response 0: Ignored 1: Send auto IRQ response When host is waiting MMC card interrupt response, setting this bit will make controller cancel wait state and return to idle state, at which time, controller will receive IRQ response sent by itself. This bit is auto-cleared after response is sent.

11.3.8.19 0x0048 SMHC Transferred Byte Count Register 0 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: SMHC_TBC0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	TBC0 Transferred Count 0 Number of bytes transferred between card and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

11.3.8.20 0x004C SMHC Transferred Byte Count Register 1 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: SMHC_TBC1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	TBC1 Transferred Count 1 Number of bytes transferred between Host/DMA memory and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

11.3.8.21 0x0054 SMHC CRC Status Detect Control Register (Default Value: 0x0000_0003)

Offset: 0x0054			Register Name: SMHC_CSDC
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

3:0	R/W	0x3	CRC_DET_PARA CRC Detect Para 110: HS400 speed mode 011: Other speed mode Others: Reserved

11.3.8.22 0x0058 SMHC Auto Command 12 Argument Register (Default Value: 0x0000_FFFF)

Offset: 0x0058			Register Name: SMHC_A12A
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0xFFFF	A12A Auto CMD12 Argument The argument of command 12 automatically send by controller with this field.

11.3.8.23 0x005C SMHC New Timing Set Register (Default Value: 0x8171_0000)

Offset: 0x005C			Register Name: SMHC_NTSR
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	MODE_SEL Mode Select 0: Old mode of Sample/Output Timing 1: New mode of Sample/Output Timing Default value : 1
30:26	/	/	/
25	R/W	0x0	BOOT_DAT_RX_PHASE_CLR After boot ack, before receive boot data, clear data lines input phase. 0: Disable 1: Enable
24	R/W	0x1	CMD_DAT_RX_PHASE_CLR During update clock operation, clear command line s and data lines input phase. 0: Disable 1: Enable
23	/	/	/
22	R/W	0x1	DAT_CRC_STATUS_RX_PHASE_CLR Before receive CRC status, clear data lines input phase. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

21	R/W	0x1	DAT_TRANS_RX_PHASE_CLR Before transfer data, clear data lines input phase. 0: Disable 1: Enable
20	R/W	0x1	DAT_RECV_RX_PHASE_CLR Before receive data, clear data lines input phase clear 0: Disable 1: Enable
19:17	/	/	/
16	R/W	0x1	CMD_SEND_RX_PHASE_CLR Before send command, command rx phase clear 0: Disable 1: Enable
15:10	/	/	/
9:8	R/W	0x0	DAT_SAM_TIM_PHS Data Sample Timing Phase 00: Sample timing phase offset 90^0 01: Sample timing phase offset 180^0 10: Sample timing phase offset 270^0 11: Sample timing phase offset 0^0（only for SD2 hs400 mode） Default value: 00
7:6	/	/	/
5:4	R/W	0x0	CMD_SAM_TIM_PHS Command Sample Timing Phase 00: Sample timing phase offset 90^0 01: Sample timing phase offset 180^0 10: Sample timing phase offset 270^0 11: Ignore Default value: 00
3:1	/	/	/
0	R/W	0x0	HS400_NEW_SAM_EN HS400 New Sample Enable 1: Enable hs400 new sample method 0: Disable hs400 new sample method

11.3.8.24 0x0078 SMHC Hardware Reset Register (Default Value: 0x0000_0001)

Offset: 0x0078			Register Name: SMHC_HWRST
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

0	R/W	0x1	HW_RST Hardware Reset 1: Active mode 0: Reset These bits cause the cards to enter pre-idle state, which requires them to be re-initialized.

11.3.8.25 0x0080 SMHC DMAC Control Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: SMHC_DMAC
Bit	Read/Write	Default/Hex	Description
31	W	0x0	DES_LOAD_CTRL When DMAC fetches a descriptor, if the valid bit of a descriptor is not set, DMAC FSM will go to the suspend state. Setting this bit will make DMAC re-fetch descriptor again and do the transfer normally.
30:8	/	/	/
7	R/W	0x0	IDMAC_ENB IDMAC Enable. When set, the IDMAC is enabled. DE is read/write.
6:2	/	/	/
1	R/W	0x0	FIX_BUST_CTRL Fixed Burst. Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations.
0	R/W	0x0	IDMAC_RST DMA Reset. When set, the DMA Controller resets all its internal registers. SWR is read/write. It is automatically cleared after 1 clock cycle.

11.3.8.26 0x0084 SMHC Descriptor List Base Address Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: SMHC_DLBA
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	DES_BASE_ADDR Start of Descriptor List. Contains the base address of the First Descriptor, is a word(4byte) address

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.3.8.27 0x0088 SMHC DMAC Status Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: SMHC_IDST
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:10	R	0x0	DMAC_ERR_STA Error Bits. Indicates the type of error that caused a Bus Error. Valid only with Fatal Bus Error bit (SMHC_ IDST[2]) set. This field does not generate an interrupt. 001: Host Abort received during transmission 010: Host Abort received during reception Others: Reserved This bit is read-only.
9	R/W1C	0x0	AIS Abnormal Interrupt Summary. Logical OR of the following: SMHC_IDST[2]: Fatal Bus Interrupt SMHC_IDST[4]: Descriptor unavailable bit Interrupt SMHC_IDST[5]: Card Error Summary Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes AIS to be set is cleared. Writing a 1 clears this bit.
8	R/W1C	0x0	NIS Normal Interrupt Summary. Logical OR of the following: SMHC_IDST[0]: Transmit Interrupt SMHC_IDST[1]: Receive Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes NIS to be set is cleared. Writing a 1 clears this bit.
7:6	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

5	R/W1C	0x0	ERR_FLAG_SUM Card Error Summary. Indicates the status of the transaction to/from the card; also present in RINTSTS. Indicates the logical OR of the following bits: EBE: End Bit Error RTO: Response Timeout RCRC: Response CRC SBE: Start Bit Error DRTO: Data Read Timeout DCRC: Data CRC for Receive RE: Response Error Writing a 1 clears this bit.
4	R/W1C	0x0	DES_UNAVL_INT Descriptor Unavailable Interrupt. This bit is set when the descriptor is unavailable due to OWN bit = 0 (DES0[31] =0). Writing a 1 clears this bit.
3	/	/	/
2	R/W1C	0x0	FATAL_BERR_INT Fatal Bus Error Interrupt. Indicates that a Bus Error occurred (SMHC_IDST [12:10]). When this bit is set, the DMA disables all its bus accesses. Writing a 1 clears this bit.
1	R/W1C	0x0	RX_INT Receive Interrupt. Indicates the completion of data reception for a descriptor. Writing a 1 clears this bit.
0	R/W1C	0x0	TX_INT Transmit Interrupt. Indicates that data transmission is finished for a descriptor. Writing a 1 clears this bit.

11.3.8.28 0x008C SMHC DMAC Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: SMHC_IDIE
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	ERR_SUM_INT_ENB Card Error summary Interrupt Enable. When set, it enables the Card Interrupt summary.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

4	R/W	0x0	DES_UNAVL_INT_ENB Descriptor Unavailable Interrupt. When set along with Abnormal Interrupt Summary Enable, the Descriptor Unavailable interrupt is enabled.
3	/	/	/
2	R/W	0x0	FERR_INT_ENB Fatal Bus Error Enable. When set with Abnormal Interrupt Summary Enable, the Fatal Bus Error Interrupt is enabled. When reset, Fatal Bus Error Enable Interrupt is disabled.
1	R/W	0x0	RX_INT_ENB Receive Interrupt Enable. When set , Normal Interrupt Summary Enable, Receive Interrupt is enabled. When reset, Receive Interrupt is disabled.
0	R/W	0x0	TX_INT_ENB Transmit Interrupt Enable. When set , Normal Interrupt Summary Enable, Transmit Interrupt is enabled. When reset, Transmit Interrupt is disabled.

11.3.8.29 0x0100 SMHC Card Threshold Control Register (Default Value: 0x0000_0005)

Offset: 0x0100			Register Name: SMHC_THLD
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	CARD_WR_THLD Card Read/write Threshold Size (Unit: byte)
15:3	/	/	/
2	R/W	0x1	CARD_WR_THLD_ENB Card Write Threshold Enable 0: Card write threshold disable 1: Card write threshold enabled Host controller initiates write transfer only if card threshold amount of data is available in transmit FIFO
1	R/W	0x0	BCIG Busy Clear Interrupt Generation 0: Busy Clear Interrupt disabled 1: Busy Clear Interrupt Enabled The application can disable this feature if it does not want to wait for a Busy Clear Interrupt.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

0	R/W	0x1	CARD_RD_THLD_ENB Card Read Threshold Enable 0: Card Read Threshold Disable 1: Card Read Threshold Enable Host controller initiates Read Transfer only if CARD_RD_THLD amount of space is available in receive FIFO

11.3.8.30 0x0104 SMHC Sample FIFO Control Register (Default Value: 0x0000_0006)

Offset: 0x0104			Register Name: SMHC_SFC
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4:1	R/W	0x3	STOP_CLK_CTRL Stop Clock Control When receiving data, if CARD_RD_THLD_ENB is set and CARD_RD_THLD is set same with BLK_SZ, the device clock may stop at block gap during data receiving. This field is used to control the position of stopping clock. The value can be change between 0x0 and 0xF,but actually the available value and the position of stopping clock must be decided by the actual situation. The value increase one in this field is linked to one cycle(two cycle in DDR mode) that the position of stopping clock moved up.
0	R/W	0x0	BYPASS_EN Bypass enable When set, sample FIFO will be bypassed.

11.3.8.31 0x0108 SMHC Auto Command 23 Argument Register (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: SMHC_A23A
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	A23A Auto CMD23 Argument The argument of command 23 is automatically sent by controller with this field.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.3.8.32 0x010C SMHC eMMC4.5 DDR Start Bit Detection Control Register (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: EMMC_DDR_SBIT_DET
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HS400_MD_EN HS400 Mode Enable 0: Disable 1: Enable It is required to set this bit to '1' before initiating any data transfer CMD in HS400 mode.
30:1	/	/	/
0	R/W	0x0	HALF_START_BIT Control for start bit detection mechanism inside host controller based on duration of start bit. For eMMC 4.5, start bit can be: 0: Full cycle 1: Less than one full cycle Set HALF_START_BIT=1 for eMMC 4.5 and above; set to 0 for SD applications.

11.3.8.33 0x0110 SMHC Response CRC Register (Default Value:0x0000_0000)

Offset: 0x0110			Register Name: SMHC_RESP_CRC
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:0	R	0x0	RESP_CRC Response CRC Response CRC from device

11.3.8.34 0x0138 SMHC Extended Command Register (Default Value: 0x0000_0000)

Offset: 0x0138			Register Name: SMHC_EXT_CMD
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	AUTO_CMD23_EN Send CMD23 Automatically When set this bit, send CMD23 automatically before send command specified in SMHC_CMD register. When SOFT_RST set, this field will be cleared.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.3.8.35 0x013C SMHC Extended Response Register (Default Value: 0x0000_0000)

Offset: 0x013C			Register Name: SMHC_EXT_RESP
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	SMHC_EXT_RESP When AUTO_CMD23_EN is set, this register stores the response of CMD23.

11.3.8.36 0x0140 SMHC Drive Delay Control Register (Default Value: 0x0001_0000)

Offset: 0x0140			Register Name: SMHC_DRV_DL
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	DAT_DRV_PH_SEL Data Drive Phase Select 0: Data drive phase offset is: 90^0 at SDR mode, 45^0 at DDR8 mode, 90^0 at DDR4 mode when 0x5C[31] is low, 45^0 at DDR4 mode when 0x5C[31] is high, 90^0 at HS400 mode when 0x5C[0] is low, 45^0 at HS400 mode when 0x5C[0] is high. 1: Data drive phase offset is: 180^0 at SDR mode, 90^0 at DDR8 mode, 180^0 at DDR4 mode when 0x5C[31] is low, 90^0 at DDR4 mode when 0x5C[31] is high, 180^0 at HS400 mode when 0x5C[0] is low, 90^0 at HS400 mode when 0x5C[0] is high.
16	R/W	0x1	CMD_DRV_PH_SEL Command Drive Phase Select 0: Command drive phase offset is: 90^0 at SDR mode, 45^0 at DDR8 mode, 90^0 at DDR4 mode when 0x5C[31] is low, 45^0 at DDR4 mode when 0x5C[31] is high, 90^0 at HS400 mode 1: Command drive phase offset is: 180^0 at SDR mode, 90^0 at DDR8 mode, 180^0 at DDR4 mode when 0x5C[31] is low, 90^0 at DDR4 mode when 0x5C[31] is high, 180^0 at HS400 mode.
15:0	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.3.8.37 0x0144 SMHC Sample Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0144			Register Name: SMHC_SAMP_DL
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:8	R	0x20	Reserved
7	R/W	0x0	SAMP_DL_SW_EN Sample Delay Software Enable When set, enable sample delay specified at SAMP_DL_SW
6	/	/	/
5:0	R/W	0x0	SAMP_DL_SW Sample Delay Software The relative delay between clock line and command line, data lines. It can be determined according to the value of SAMP_DL, the cycle of card clock and device s input timing requirement.

11.3.8.38 0x0148 SMHC Data Strobe Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0148			Register Name: SMHC_DS_DL
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:8	R	0x20	Reserved
7	R/W	0x0	DS_DL_SW_EN Sample Delay Software Enable
6	/	/	/
5:0	R/W	0x0	DS_DL_SW Data Strobe Delay Software

11.3.8.39 0x0154 SMHC Card interface counter Register (Default Value:0x0)

Offset: 0x0154			Register Name: SMHC_CIU_CNT
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0154			Register Name: SMHC_CIU_CNT
Bit	Read/Write	Default/Hex	Description
31:6	R	0x0	DATA_PATH_CNT Data Path Counter This field indicates the count value of counters for each stage when host read or write data. When Host read data, this field is one of the following values: 1. The time of wait data start bit
5:0	/	/	/

11.3.8.40 0x015C SMHC Write Busy Timeout Register (Default Value:0x00FF_FFFF)

Offset: 0x015C			Register Name: SMHC_WR_BUSY_TMOUT
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:0	R/W	0xffffff	WR_BUSY_TO_LMT Data write busy timeout Limit Actually, timeout limit is WR_BUSY_TO_LMT+1.

11.3.8.41 0x01A0 SMHC CQE Control Register (Default Value: 0x0000_0003)

Offset: 0x01A0			Register Name: SMHC_CQE_CTRL
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
8	R/W	0x0	DS_SAMP_RESP_EN datastrobe sample response enable It should be set when CQE work at HS400 enhance strobe mode
7:2	/	/	/
1	R/W	0x1	CQE_CLR_DTC_EN 0: cqe clear data transfer complete(DTC) status disable 1: cqe clear data transfer complete(DTC) status enable
0	R/W	0x1	CQE_CLR_CC_EN 0: cqe clear command complete(CC) status disable 1: cqe clear command complete(CC) status enable

11.3.8.42 0x0200 SMHC FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0200	Register Name: SMHC_FIFO

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TX/RX_FIFO Data FIFO

11.3.8.43 0x0408 Command Queuing Configuration Register (Default Value: 0x0200_0000)

This register controls CQE behavior affecting the general operation of command queuing module or operation of multiple tasks in the same time.

Offset: 0x0408			Register Name: CQCFG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x200	CQE_BLOCK_SIZE CQE Block Size Configuration It must be 0x200 when CMDQ_MODE is cmdq or cmdq_half or cmdq_almost.
15:13	/	/	/
12	R/W	0x0	CQE_DCMD_EN Direct Command (DCMD) Enable This bit indicates to the hardware whether the Task Descriptor in slot #31 of the TDL is a Data Transfer Task Descriptor, or a Direct Command Task Descriptor. CQE uses this bit when a task is issued in slot #31, to determine how to decode the Task Descriptor. Bit Value Description 1 = Task descriptor in slot #31 is a DCMD Task Descriptor 0 = Task descriptor in slot #31 is a Data Transfer Task Descriptor
11:9	/	/	/
8	R/W	0x0	CQE_TASK_DESC_SIZE Task Descriptor Size This bit indicates whether the task descriptor size is 128 bits or 64 bits as detailed in Data Structures section. This bit can only be configured when Command Queuing Enable bit is 0 (command queuing is disabled) Bit Value Description 1: Task descriptor size is 128 bits. 0: Task descriptor size is 64 bits.
7:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0408			Register Name: CQCFG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	CQE_EN Command Queuing Enable Software shall write 1 this bit when in order to enable command queuing mode (i.e., enable CQE). When this bit is 0, CQE is disabled and software controls the eMMC bus using the legacy eMMC host controller. Before software writes 1 to this bit, software shall verify that the eMMC host controller is in idle state and there are no commands or data transfers ongoing. When software wants to exit command queuing mode, it shall clear all previous tasks if such exist before setting this bit to 0.

11.3.8.44 0x040C Command Queuing Control Register (Default Value: 0x0000_0000)

This register controls CQE behavior affecting the general operation of command queuing module or operation of multiple tasks in the same time.

Offset: 0x040C			Register Name: CQCTL
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/WAC	0x0	CQE_TCL_ALL CQE Task Cleared All Software shall write 1 this bit when it wants to clear all the tasks sent to the device. This bit can only be written when CQE is in halt state (i.e., Halt bit is 1). When software writes 1, the value of the register is updated to 1 , and CQE shall reset CQTDBR register and all other context information for all unfinished tasks. Then CQE will clear this bit. Software should poll on this bit until it is set to back 0 and may then resume normal operation, by clearing the Halt bit. CQE does not communicate to the device that the tasks were cleared. It is software s responsibility to order the device to discard the tasks in its queue using CMDQ_TASK_MGMT command. Writing 0 to this register shall have no effect.
7:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x040C			Register Name: CQCTL
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	CQE_HALT Host software shall write 1 to the bit when it wants to acquire software control over the eMMC bus and disable CQE from issuing commands on the bus. For example, issuing a Discard Task command (CMDQ_TASK_MGMT) When software writes 1 , CQE shall complete the ongoing task if such a task is in progress. Once the task is completed and CQE is in idle state, CQE shall not issue new commands and shall indicate so to software by setting this bit to 1. Software may poll on this bit until it is set to 1, and may only then send commands on the eMMC bus. In order to exit halt state (i.e., resume CQE activity), software shall clear this bit (write 0). Writing 0 when the value is already 0 shall have no effect.

11.3.8.45 0x0410 Command Queuing Interrupt Status Register (Default Value: 0x0000_0000)

This register indicates pending interrupts that require service. Each bit in this registers is asserted in response a specific event, only if the respective bit is set in CQISTE register.

Offset: 0x0410			Register Name: CQIS
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W1C	0x0	CQIS_TCL Task Cleared This status bit is asserted (if CQISTE.TCL=1) when a task clear operation is completed by CQE. The completed task clear operation is either an individual task clear (CQTCLR) or clearing of all tasks (CQCTL).
2	R/W1C	0x0	CQIS_RED Response Error Detected Interrupt This status bit is asserted (if CQISTE.RED=1) when a response is received with an error bit set in the device status field. The contents of the device status field are listed in 6.13. Software uses CQRMEM register to configure which device status bit fields may trigger an interrupt, and which are masked.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0410			Register Name: CQIS
Bit	Read/Write	Default/Hex	Description
1	R/W1C	0x0	CQIS_TCC Task Complete Interrupt This status bit is asserted (if CQISTE.TCC=1) when at least one of the following two conditions are met: A task is completed and the INT bit is set in its Task Descriptor Interrupt caused by Interrupt Coalescing logic (see 0)
0	R/W1C	0x0	CQIS_HAC Halt Complete Interrupt This status bit is asserted (if CQISTE.HAC=1) when halt bit in CQCTL register transitions from 0 to 1 indicating that host controller has completed its current ongoing task and has entered halt state.

11.3.8.46 0x0414 Command Queuing Interrupt Status Enable Register (Default Value: 0x0000_0000)

This register enables and disables the reporting of the corresponding interrupt to host software in CQIS register. When a bit is set ('1') and the corresponding interrupt condition is active, then the bit is CQIS is asserted. Interrupt sources that are disabled ('0') are not indicated in the CQIS register. This register is bit-index matched to CQIS register.

Offset: 0x0414			Register Name: CQISTE
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	CQISTE_TCL Task Cleared Status Enable 1 = CQIS.TCL will be set when its interrupt condition is active 0 = CQIS.TCL is disabled
2	R/W	0x0	CQISTE_RED Response Error Detected Status Enable 1 = CQIS.RED will be set when its interrupt condition is active 0 = CQIS.RED is disabled
1	R/W	0x0	CQISTE_TCC Task Complete Status Enable 1 = CQIS.TCC will be set when its interrupt condition is active 0 = CQIS.TCC is disabled

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0414			Register Name: CQISTE
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	CQISTE_HAC Halt Complete Status Enable 1 = CQIS.HAC will be set when its interrupt condition is active 0 = CQIS.HAC is disabled

11.3.8.47 0x0418 Command Queuing Interrupt Signal Enable Register (Default Value: 0x0000_0000)

This register enables and disables the generation of interrupts to host software. When a bit is set ('1') and the corresponding bit in CQIS is set, then an interrupt is generated. Interrupt sources that are disabled ('0') are still indicated in the CQIS register. This register is bit-index matched to CQIS register.

Offset: 0x0418			Register Name: CQISGE
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	CQISGE_TCL Task Cleared Signal Enable When set and CQIS.TCL is asserted, the CQE shall generate an interrupt
2	R/W	0x0	CQISGE_RED Response Error Detected Signal Enable When set and CQIS.RED is asserted, the CQE shall generate an interrupt
1	R/W	0x0	CQISGE_TCC Task Complete Signal Enable When set and CQIS.TCC is asserted, the CQE shall generate an interrupt
0	R/W	0x0	CQISGE_HAC Halt Complete Signal Enable When set and CQIS.HAC is asserted, the CQE shall generate an interrupt

11.3.8.48 0x041C Command Queuing Interrupt Coalescing Register (Default Value: 0x0000_0000)

This register controls the interrupt coalescing feature.

Offset: 0x041C			Register Name: CQIC
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x041C			Register Name: CQIC
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CQIC_EN Interrupt Coalescing Enable/Disable When set to 0 by software, command responses are neither counted nor timed. Interrupts are still triggered by completion of tasks with INT=1 in the Task Descriptor. When set to 1 , the interrupt coalescing mechanism is enabled and coalesced interrupts are generated
30:21	/	/	/
20	R	0x0	CQIC_SB Interrupt Coalescing Status Bit This bit indicates to software whether any tasks (with INT=0) have completed and counted towards interrupt coalescing (i.e., ICSB is set if and only if IC counter > 0). Bit Value Description 1: At least one task completion has been counted (IC counter >0) 0: No task completions have occurred since last counter reset (IC counter =0)
19:17	/	/	/
16	W	0x0	CQIC_CTR Counter and Timer Reset When host driver writes 1 , the interrupt coalescing timer and counter are reset
15	W	0x0	CQIC_CTH_WEN Interrupt Coalescing Counter Threshold Write Enable When software writes 1 , the value ICCTH is updated with the contents written at the same cycle. When software writes 0 , the value in ICCTH is not updated. NOTE: Write operations to ICCTH are only allowed when the task queue is empty.
14:13	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x041C			Register Name: CQIC
Bit	Read/Write	Default/Hex	Description
12:8	R/W	0x0	CQIC_CTH Interrupt Coalescing Counter Threshold Software uses this field to configure the number of task completions (only tasks with INT=0 in the Task Descriptor) which are required in order to generate an interrupt. Counter Operation: As data transfer tasks with INT=0 complete, they are counted by CQE. The counter is reset by software during the interrupt service routine. The counter stops counting when it reaches the value configured in ICCTH. The maximum allowed value is 31 NOTE 1：When ICCTH is 0, task completions are not counted, and counting-based interrupts are not generated. NOTE 2：When ICCTH is 1, interrupt is actually not coalesced, and CQIC_SB will not be set. In order to write to this field, the ICCTHWEN bit must be set at the same write operation.
7	W	0x0	CQIC_TOVAL_WEN Interrupt Coalescing Timeout Value Write Enable When software writes 1 , the value ICTOVAL is updated with the contents written at the same cycle. When software writes 0 , the value in ICTOVAL is not updated. NOTE: Write operations to ICTOVAL are only allowed when the task queue is empty.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x041C			Register Name: CQIC
Bit	Read/Write	Default/Hex	Description
6:0	R/W	0x0	CQIC_TOVAL Interrupt Coalescing Timeout Value Software uses this field to configure the maximum time allowed between the completion of a task on the bus and the generation of an interrupt. Timer Operation: The timer is reset by software during the interrupt service routine. It starts running when a data transfer task with INT=0 is completed, after the timer was reset. When the timer reaches the value configured in ICTOVAL field it generates an interrupt and stops. The timer s unit is equal to 1024 clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field CQCAP register. The minimum value is 01h (1024 clock periods) and the maximum value is 7Fh (127*1024 clock periods). For example, a CQCAP field value of 0 indicates a 19.2 MHz clock frequency (period = 52.08 ns). If the setting in ICTOVAL is 10h, the calculated polling period is 16*1024*52.08 ns= 853.33 us NOTE: When ICTOVAL is 0, the timer is not running, and timer-based interrupts are not generated. In order to write to this field, the ICTOVALWEN bit must be set at the same write operation.

11.3.8.49 0x0420 Command Queuing Task Descriptor List Base Address Register (Default Value: 0x0000_0000)

This register is used for configuring the lower 32 bits of the byte address of the head of the Task Descriptor List in the host memory.

Offset: 0x0420			Register Name: CQTDLBA
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0420			Register Name: CQTDLBA
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CQE_TDLBA Task Descriptor List Base Address This register stores the LSB bits (bits 31:0) of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is 32 * (Task Descriptor size + Transfer Descriptor size) as configured by Host driver. This address shall be set on 1 KByte boundary: The lower 10 bits of this register shall be set to 0 by software and shall be ignored by CQE.

11.3.8.50 0x0424 Command Queuing Task Descriptor List Base Address Upper 32 Bits Register (Default Value: 0x0000_0000)

This register is used for configuring the upper 32 bits of the byte address of the head of the Task Descriptor List in the host memory.

Offset: 0x0424			Register Name: CQTDLBAU
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CQE_TDLBAU Task Descriptor List Base Address Upper This register stores the MSB bits (bits 63:32) of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is 32 * (Task Descriptor size + Transfer Descriptor size) as configured by Host driver. This register is reserved when using 32-bit addressing mode.

11.3.8.51 0x0428 Command Queuing Task Doorbell Register (Default Value: 0x0000_0000)

Using this register, software triggers CQE to process a new task.

Offset: 0x0428			Register Name: CQTDBR
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0428			Register Name: CQTDBR
Bit	Read/Write	Default/Hex	Description
31:0	R/W1S	0x0	CQE_TDBR Command Queuing Task Doorbell Software shall configure TDLBA and TDLBAU, and enable CQE in CQCFG before using this register. Writing 1 to bit n of this register triggers CQE to start processing the task encoded in slot n of the TDL. CQE always processes tasks in-order according to the order submitted to the list by CQTDBR write transactions. CQE processes Data Transfer tasks by reading the Task Descriptor and sending QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) commands to the device. CQE processes DCMD tasks (in slot #31, when enabled) by reading the Task Descriptor, and generating the command encoded by its index and argument. The corresponding bit is cleared to 0 by CQE in one of the following events: When a task execution is completed (with success or error) The task is cleared using CQTCLR register All tasks are cleared using CQCTL register CQE is disabled using CQCFG register Software may initiate multiple tasks at the same time (batch submission) by writing 1 to multiple bits of this register in the same transaction. In the case of batch submission: CQE shall process the tasks in order of the task index, starting with the lowest index. If one or more tasks in the batch are marked with QBR, the ordering of execution will be based on said processing order. Writing 0 by software shall have no impact on the hardware, and will not change the value of the register bit.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.3.8.52 0x042C Command Queuing Task Completion Notification Register (Default Value: 0x0000_0000)

This register is used by CQE to notify software about completed tasks.

Offset: 0x042C			Register Name: CQTCN
Bit	Read/Write	Default/Hex	Description
31:0	R/W1C	0x0	CQE_TCN Task Complete Notification CQE shall set bit *n* of this register (at the same time it clears bit *n* of CQTDBR) when a task execution is completed (with success or error). When receiving interrupt for task completion, software may read this register to know which tasks have finished. After reading this register, software may clear the relevant bit fields by writing 1 to the corresponding bits.

11.3.8.53 0x0430 Command Queuing Device Queue Status Register (Default Value: 0x0000_0000)

This register stores the most recent value of the device's queue status.

Offset: 0x0430			Register Name: CQDQS
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CQE_DQS Device Queue Status Every time the Host controller receives a queue status register (QSR) from the device, it updates this register with the response of status command, i.e., the device s queue status.

11.3.8.54 0x0434 Command Queuing Device Pending Tasks Register (Default Value: 0x0000_0000)

This register indicates to software which tasks are queued in the device, awaiting execution.

Offset: 0x0434			Register Name: CQDPT
Bit	Read/Write	Default/He	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0434			Register Name: CQDPT
Bit	Read/Write	Default/He	Description
31:0	R	0x0	CQE_DPT Device Pending Tasks Bit *n* of this register is set if and only if QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) were sent for this specific task and if this task hasn t been executed yet. CQE shall set this bit after receiving a successful response for CMD45. CQE shall clear this bit after the task has completed execution. Software needs to read this register in the task-discard procedure, when the controller is halted, to determine if the task is queued in the device. If the task is queued, the driver sends a CMDQ_TASK_MGMT (CMD48) to the device ordering it to discard the task. Then software clears the task in the CQE. Only then the software orders CQE to resume its operation using CQCTL register.

11.3.8.55 0x0438 Command Queuing Task Clear Register (Default Value: 0x0000_0000)

This register is used for removing an outstanding task in the CQE. The register should be used only when CQE is in Halt state.

Offset: 0x0438			Register Name: CQTCLR
Bit	Read/Write	Default/He	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0438			Register Name: CQTCLR
Bit	Read/Write	Default/He	Description
31:0	R/W	0x0	CQE_TASK_CLR Command Queuing Task Clear Writing 1 to bit *n* of this register orders CQE to clear a task which software has previously issued. This bit can only be written when CQE is in Halt state as indicated in CQCTL register Halt bit. When software writes 1 to a bit in this register, CQE updates the value to 1 , and starts clearing the data structures related to the task. CQE clears the bit fields (sets a value of 0) in CQTCLR and in CQTDBR once clear operation is complete. Software should poll on the CQTCLR until it is cleared to verify clear operation was complete. Writing to this register only clears the task in the CQE and does not have impact on the device. In order to discard the task in the device, host software shall send CMDQ_TASK _MGMT while CQE is still in Halt state. Host driver is not allowed to use this register to clear multiple tasks at the same time. Clearing multiple tasks can be done using CQCTL register. Writing 0 to a register bit shall have no impact.

11.3.8.56 0x0440 Command Queuing Send Status Configuration 1 Register (Default Value: 0x0000_1000)

The register controls the when SEND_QUEUE_STATUS commands are sent.

Offset: 0x0440			Register Name: CQSSC1
Bit	Read/Write	Default/He	Description
31:16	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0440			Register Name: CQSSC1
Bit	Read/Write	Default/He	Description
15:0	R/W	0x1000	CQE_SSC_CIT Send Status Command Idle Timer This field indicates to CQE the polling period to use when using periodic SEND_QUEUE_STATUS (CMD13) polling. Periodic polling is used when tasks are pending in the device, but no data transfer is in progress. When a SEND_QUEUE_STATUS response indicating that no task is ready for execution, CQE counts the configured time until it issues the next SEND_QUEUE_STATUS. Timer units are clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field CQCAP register. The minimum value is 0001h (1 clock period) and the maximum value is FFFFh (65535 clock periods). Default interval is: 4096 clock periods. For example, a CQCAP field value of 0 indicates a 19.2 MHz clock frequency (period = 52.08 ns). If the setting in CQSSC1.CIT is 1000h, the calculated polling period is 4096*52.08 ns= 213.33 us

11.3.8.57 0x0444 Command Queuing Send Status Configuration 2 Register (Default Value: 0x0000_0000)

This register is used for configuring RCA field in SEND_QUEUE_STATUS command argument.

Offset: 0x0444			Register Name: CQSSC2
Bit	Read/Write	Default/He	Description
31:16	/	/	/
15:0	R/W	0x0	CQE_SSC_RCA Send Queue Status RCA This field provides CQE with the contents of the 16-bit RCA field in SEND_QUEUE_ STATUS (CMD13) command argument. CQE shall copy this field to bits 31:16 of the argument when transmitting SEND_ QUEUE_STATUS (CMD13) command.

11.3.8.58 0x0448 Command Queuing Command Response for Direct-Command Task Register (Default Value: 0x0000_0000)

This register is used for passing the response of a DCMD task to software.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0448			Register Name: CQCRDCT
Bit	Read/Write	Default/He	Description
31:0	R	0x0	CQE_DCMD_LAST_RESP Direct Command Last Response This register contains the response of the command generated by the last direct- command (DCMD) task which was sent. CQE shall update this register when it receives the response for a DCMD task. This register is considered valid only after bit 31 of CQTDBR register is cleared by CQE.

11.3.8.59 0x0450 Command Queuing Response Mode Error Mask Register (Default Value: 0xFDF9_A080)

This register controls the generation of Response Error Detection (RED) interrupt.

Offset: 0x0450			Register Name: CQRMEM
Bit	Read/Write	Default/He	Description
31:0	R/W	0xFDF9A080	CQE_RMEM Response Mode Error Mask This bit is used as in interrupt mask on the device status filed which is received in R1/R1b responses. Bit Value Description (for any bit i): 1: When a R1/R1b response is received, with bit *i* in the device status set, a RED interrupt is generated 0: When a R1/R1b response is received, bit *i* in the device status is ignored The reset value of this register is set to trigger an interrupt on all Error type bits in the device status, as defined in 6.13. NOTE: Responses to CMD13 (SQS) encode the QSR, so they are ignored by this logic.

11.3.8.60 0x0454 Command Queuing Task Error Information Register (Default Value: 0x0000_0000)

This register is updated by CQE when an error occurs on data or command related to a task activity.

When such error is detected by CQE or indicated by the *e*•MMC controller CQE stores in CQTERRI the task IDs and the command indices of the commands which were executed on the command line and data lines when the error occurred.

Software is expected to use this information in the error recovery procedure. See B.2.8 for more details.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0454			Register Name: CQERRI
Bit	Read/Write	Default/He	Description
31	R	0x0	CQE_DTE_VLD Data Transfer Error fields Valid This bit is updated when an error is detected by CQE, or indicated by eMMC controller. If a data transfer is in progress when the error is detected/indicated, the bit is set to 1. If a no data transfer is in progress when the error is detected/indicated, the bit is cleared to 0.
30:29	/	/	/
28:24	R	0x0	CQE_DTE_TASK_ID Data Transfer Error Task ID This field indicates the ID of the task which was executed on the data lines when an error occurred. The field is updated if a data transfer is in progress when an error is detected by CQE, or indicated by eMMC controller.
23:22	/	/	/
21:16	R	0x0	CQE_DTE_CMD_IDX Data Transfer Error Command Index This field indicates the index of the command which was executed on the data lines when an error occurred. The index shall be set to EXECUTE_READ_TASK (CMD46) or EXECUTE_WRITE_TASK (CMD47) according to the data direction. The field is updated if a data transfer is in progress when an error is detected by CQE, or indicated by eMMC controller.
15	R	0x0	CQE_RME_VLD Response Mode Error fields Valid This bit is updated when an error is detected by CQE, or indicated by eMMC controller. If a command transaction is in progress when the error is detected/indicated, the bit is set to 1. If a no command transaction is in progress when the error is detected/indicated, the bit is cleared to 0.
14:13	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0454			Register Name: CQERRI
Bit	Read/Write	Default/He	Description
12:8	R	0x0	CQE_RME_TASK_ID Response Mode Error Task ID This field indicates the ID of the task which was executed on the command line when an error occurred. The field is updated if a command transaction is in progress when an error is detected by CQE, or indicated by eMMC controller.
7:6	/	/	/
5:0	R	0x0	CQE_RME_CMD_IDX Response Mode Error Command Index This field indicates the index of the command which was executed on the command line when an error occurred. The field is updated if a command transaction is in progress when an error is detected by CQE, or indicated by eMMC controller.

11.3.8.61 0x0458 Command Queuing Command Response Index Register (Default Value: 0x0000_0000)

This register stores the index of the last received command response.

Offset: 0x0458			Register Name: CQCRI
Bit	Read/Write	Default/He	Description
31:6	/	/	/
5:0	R	0x0	CQE_LAST_RESP_IDX Last Command Response index This field stores the index of the last received command response. CQE shall update the value every time a command response is received.

11.3.8.62 0x045C Command Queuing Command Response Argument Register (Default Value: 0x0000_0000)

This register stores the argument of the last received command response.

Offset: 0x045C			Register Name: CQCRA
Bit	Read/Write	Default/He	Description
31:0	R	0x0	CQE_LAST_RESP_ARG Last Command Response Argument This field stores the argument of the last received command. CQE shall update the value every time a command response is received.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.3.8.63 0x0460 Command Queuing Function Control Register (Default Value: 0x0000_0000)

This register is used to enable or disable some CQE functions.

Offset: 0x0460			Register Name: CQFUNCCTL
Bit	Read/Write	Default/He	Description
31:16	/	/	/
15:8	R/W	0x0	CQE_SMHC_ERR_MASK This field is used to mask errors that CQE does not need to consider. bit7 for Data End-bit error mask bit6 for Data Start-bit error mask bit5 for Data Starvation error mask bit4 for Data timeout mask bit3 for Response timeout mask bit2 for Data CRC error mask bit1 for Response CRC error mask bit0 for Response error mask For any bit: 0: CQE will consider this SMHC error 1: CQE will not consider this SMHC error
7:1	/	/	/
0	R/W	0x0	CQE_CLR_REG_EN This field is used to control whether to clear register when disable CQE 0: Not clear register when disable CQE 1: Clear register to reset value when disable CQE

11.3.8.64 0x0480 Command Queuing Descriptor Transfer Done Register (Default Value: 0x0000_0000)

This register is used to indicate that the descriptor has been transferred from the system memory to cqe.

Offset: 0x0480			Register Name: CQDTD
Bit	Read/Write	Default/He	Description
31:0	R	0x0	CQE_DTD Descriptor Transfer Done Bit Value Description (for any bit i): 1: The descriptor of task-i has been transferred from the system memory to cqe. 0: The descriptor of task-i not transferred from the system memory to cqe.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.3.8.65 0x0484 Command Queuing Task Complete Total Register (Default Value: 0x0000_0000)

This register is used to indicate that the total number of task that has been completed by cqe.

Offset: 0x0484			Register Name: CQTCT
Bit	Read/Write	Default/He	Description
31:0	R	0x0	CQE_TCT Task Complete Total This resgister will be add 1 when a task execution is completed (with success or error) by cqe.

11.3.8.66 0x0488 Command Queuing Controller Status Register (Default Value: 0x0000_0000)

This register is used to indicate the cqe controller status.

Offset: 0x0488			Register Name: CQSTATUS
Bit	Read/Write	Default/He	Description
31:24	/	/	/
23:0	R	0x0	CQE_FSM_STATUS cqe_cnl FSM status, the format is: {2 b0, fsm_task_exe, 3 b0, fsm_task_chk, 2 b0, fsm_task_send}

11.3.9 SMHC3 Register Description

11.3.9.1 0x0000 SMHC Global Control Register (Default Value: 0x0000_0100)

Offset: 0x0000			Register Name: SMHC_CTRL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	FIFO_AC_MOD FIFO Access Mode 1: AHB bus 0: DMA bus
30:18	/	/	/
17:16	R/W	0x0	SRAM_BIST_SEL SRAM BIST Select 00: for SMHC 4K SRAM(1024x32) BIST 01: for CQE SRAM(32x56) BIST 10: for EMCE SRAM BIST 11: Reserved
15:13	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: SMHC_CTRL
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	TIME_UNIT_CMD Time unit for command line Time unit used to calculate command line time out value defined in RTO_LMT. 0: 1 card clock period 1: 256 card clock period
11	R/W	0x0	TIME_UNIT_DAT Time unit for data line Time unit used to calculate data line time out value defined in DTO_LMT. 0: 1 card clock period 1: 256 card clock period
10	R/W	0x0	DDR_MOD_SEL DDR Mode Select Although eMMC s HS400 speed mode is 8-bit DDR, this filed should be cleared when HS400_MD_EN is set. 0: SDR mode 1: DDR mode
9	/	/	/
8	R/W	0x1	CD_DBC_ENB Card Detect (Data[3] status) De-bounce Enable 0: Disable de-bounce 1: Enable de-bounce
7:6	/	/	/
5	R/W	0x0	DMA_ENB DMA Global Enable 0: Disable DMA to transfer data, using AHB bus 1: Enable DMA to transfer data
4	R/W	0x0	INT_ENB Global Interrupt Enable 0: Disable interrupts 1: Enable interrupts
3	/	/	/
2	R/W	0x0	DMA_RST DMA Reset
1	R/W	0x0	FIFO_RST FIFO Reset 0: No change 1: Reset FIFO This bit is auto-cleared after completion of reset operation.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: SMHC_CTRL
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	SOFT_RST Software Reset 0: No change 1: Reset SD/MMC controller This bit is auto-cleared after completion of reset operation.

11.3.9.2 0x0004 SMHC Clock Control Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: SMHC_CLKDIV
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MASK_DAT0 Mask Data0 0: Do not mask data0 when update clock ; 1: Mask data0 when update clock;
30:18	/	/	/
17	R/W	0x0	CCLK_CTRL Card Clock Output Control 0: Card clock always on 1: Turn off card clock when FSM in IDLE state
16	R/W	0x0	CCLK_ENB Card Clock Enable 0: Card Clock off 1: Card Clock on
15:8	/	/	/
7:0	R/W	0x0	CCLK_DIV Card clock divider n: Source clock is divided by 2*n.(n=0~255) when HS400_MD_EN is set, this field must be cleared.

11.3.9.3 0x0008 SMHC Timeout Register (Default Value:0xFFFF_FF40)

Offset: 0x0008			Register Name: SMHC_TMOUT
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: SMHC_TMOUT
Bit	Read/Write	Default/Hex	Description
31:8	R/W	0xffffff	DTO_LMT Data Timeout Limit This field can set time of the Host wait for the data from the Device. Ensure to communicate with the Device,this field must be set to maximum that greater than the time N_{AC}. About the N_{AC}, the explanation is as follows: When Host read data, data transmission from the Device starts after the access time delay N_{AC} beginning from the end bit of the read command(ACMD51,CMD8,CMD17,CMD18). When Host read multiple block(CMD18),the next block s data transmission from the Device starts after the access time delay N_{AC} beginning from the end bit of the previous block. When Host write data, this value is no effect. Note: Under the following 3 conditions, the timeout limit is half of the set time. 1> DDR8 mode 2> DDR4 and SMHC_NTSR[MODE_SELEC](0x5C[31]) high 3> HS400 and SMHC_NTSR[HS400_NEW_SAMPLE_EN](0x5C[0]) high
7:0	R/W	0x40	RTO_LMT Response Timeout Limit

11.3.9.4 0x000C SMHC Bus Width Register (Default Value:0x0000_0000)

Offset: 0x000C			Register Name: SMHC_CTYPE
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	CARD_WID Card width 00: 1-bit width 01: 4-bit width 1x: 8-bit width

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.3.9.5 0x0010 SMHC Block Size Register (Default Value:0x0000_0200)

Offset: 0x0010			Register Name: SMHC_BLKSIZ
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x200	BLK_SZ Block size

11.3.9.6 0x0014 SMHC Byte Count Register (Default Value:0x0000_0200)

Offset: 0x0014			Register Name: SMHC_BYTCNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x200	BYTE_CNT Byte counter Number of bytes to be transferred. It must be integer multiple of Block Size(BLK_SZ) for block transfers.

11.3.9.7 0x0018 SMHC Command Register (Default Value:0x0000_0000)

Offset: 0x0018			Register Name: SMHC_CMD
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CMD_LOAD Start Command. This bit is auto cleared when current command is sent. If there is no any response error happened, a command complete interrupt bit will be set in SMHC_RINTSTS register. You should not write any other command before this bit is cleared.
30:29	/	/	/
28	R/W	0x0	VOL_SW Voltage Switch 0: Normal command 1: Voltage switch command, set for CMD11 only
27	R/W	0x0	BOOT_ABT Boot Abort Setting this bit will terminate the boot operation.
26	R/W	0x0	EXP_BOOT_ACK Expect Boot Acknowledge. When Software sets this bit along in mandatory boot operation, controller expects a boot acknowledge start pattern of 0-1-0 from the selected card.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0018			Register Name: SMHC_CMD
Bit	Read/Write	Default/Hex	Description
25:24	R/W	0x0	BOOT_MOD Boot Mode 00: Normal command 01: Mandatory Boot operation 10: Alternate Boot operation 11: Reserved
23:22	/	/	/
21	R/W	0x0	PRG_CLK Change Clock 0: Normal command 1: Change Card Clock; When this bit is set, controller will change clock domain and clock output. No command will be sent.
20:18	/	/	/
17	R/W	0x0	R1B_BUSY_HW_DETECT R1b busy hardware detect enable 0: Disable hardware detect r1b busy 1: Enable hardware detect r1b busy
16	R/W	0x0	R1B_RESP R1b response 0: The response type isn t r1b for current command 1: The response type is r1b for current command Note: if STOP_CMD_FLAG set, R1B_RESP will be set by controller when send CMD12, and will be clear by controller when send next command.
15	R/W	0x0	SEND_INIT_SEQ Send Initialization 0: Normal command sending 1: Send initialization sequence before sending this command.
14	R/W	0x0	STOP_ABT_CMD Stop Abort Command 0: Normal command sending 1: send Stop or abort command to stop current data transfer in progress.(CMD12, CMD52 for writing I/O Abort in SDIO CCCR)

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0018			Register Name: SMHC_CMD
Bit	Read/Write	Default/Hex	Description
13	R/W	0x0	WAIT_PRE_OVER Wait Data Transfer Over 0: Send command at once, do not care of data transferring 1: Wait for data transfer completion before sending current command
12	R/W	0x0	STOP_CMD_FLAG Send Stop CMD Automatically (CMD12) 0: Do not send stop command at end of data transfer 1: Send stop command automatically at end of data transfer If set, the SMHC_RESP1 will record the response of auto CMD12.
11	R/W	0x0	TRANS_MODE Transfer Mode 0: Block data transfer command 1: Stream data transfer command
10	R/W	0x0	TRANS_DIR Transfer Direction 0: Read operation 1: Write operation
9	R/W	0x0	DATA_TRANS Data Transfer 0: without data transfer 1: with data transfer
8	R/W	0x0	CHK_RESP_CRC Check Response CRC 0: Do not check response CRC 1: Check response CRC
7	R/W	0x0	LONG_RESP Response Type 0:Short Response (48 bits) 1:Long Response (136 bits)
6	R/W	0x0	RESP_RCV Response Receive 0: Command without Response 1: Command with Response
5:0	R/W	0x0	CMD_IDX CMD Index Command index value

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.3.9.8 0x001C SMHC Command Argument Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SMHC_CMDARG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CMD_ARG Command argument

11.3.9.9 0x0020 SMHC Response 0 Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SMHC_RESP0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CMD_RESP0 Response 0 Bit[31:0] of response

11.3.9.10 0x0024 SMHC Response 1 Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: SMHC_RESP1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CMD_RESP1 Response 1 Bit[63:32] of response

11.3.9.11 0x0028 SMHC Response 2 Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: SMHC_RESP2
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CMD_RESP2 Response 2 Bit[95:64] of response

11.3.9.12 0x002C SMHC Response 3 Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: SMHC_RESP3
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CMD_RESP3 Response 3 Bit[127:96] of response

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.3.9.13 0x0030 SMHC Interrupt Mask Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SMHC_INTMASK
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CARD_REMOVAL_INT_EN Card Removed Interrupt Enable
30	R/W	0x0	CARD_INSERT_INT_EN Card Inserted Interrupt Enable
29:19	/	/	/
18	R/W	0x0	DATA_WR_BUSY_TO_INT_EN Data write busy timeout interrupt enable
17	R/W	0x0	R1B_BUSY_CLR_INT_EN
16	R/W	0x0	SDIO_INT_EN SDIO Interrupt Enable
15	R/W	0x0	DEE_INT_EN Data End-bit Error Interrupt Enable
14	R/W	0x0	ACD_INT_EN Auto Command Done Interrupt Enable
13	R/W	0x0	DSE_BC_INT_EN Data Start Error Interrupt Enable
12	R/W	0x0	CB_IW_INT_EN Command Busy and Illegal Write Interrupt Enable
11	R/W	0x0	FU_FO_INT_EN FIFO Underrun/Overflow Interrupt Enable
10	R/W	0x0	DSTO_VSD_INT_EN Data Starvation Timeout/V1.8 Switch Done Interrupt Enable
9	R/W	0x0	DTO_BDS_INT_EN Data Timeout/Boot Data Start Interrupt Enable
8	R/W	0x0	RTO_BACK_INT_EN Response Timeout/Boot ACK Received Interrupt Enable
7	R/W	0x0	DCE_INT_EN Data CRC Error Interrupt Enable
6	R/W	0x0	RCE_INT_EN Response CRC Error Interrupt Enable
5	R/W	0x0	DRR_INT_EN Data Receive Request Interrupt Enable
4	R/W	0x0	DTR_INT_EN Data Transmit Request Interrupt Enable
3	R/W	0x0	DTC_INT_EN Data Transfer Complete Interrupt Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0030			Register Name: SMHC_INTMASK
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	CC_INT_EN Command Complete Interrupt Enable
1	R/W	0x0	RE_INT_EN Response Error Interrupt Enable
0	/	/	/

11.3.9.14 0x0034 SMHC Masked Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: SMHC_MINTSTS
Bit	Read/Write	Default/Hex	Description
31	R	0x0	M_CARD_REMOVAL_INT Card Removed
30	R	0x0	M_CARD_INSERT Card Inserted
29:19	/	/	/
18	R	0x0	DATA_WR_BUSY_TO_INT Data write busy timeout interrupt
17	R	0x0	R1B_BUSY_CLR_INT
16	R	0x0	M_SDIO_INT SDIO Interrupt
15	R	0x0	M_DEE_INT Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit. When set during transmitting data, it means that host controller does not receive CRC status token.
14	R	0x0	M_ACD_INT Auto Command Done When set, it means auto stop command(CMD12) completed.
13	R	0x0	M_DSE_BC_INT Data Start Error/busy clear When set during receiving data, it means that host controller found a error start bit. When set during transmitting data, it means that busy signal is cleared after the last block.
12	R	0x0	M_CB_IW_INT Command Busy and Illegal Write
11	R	0x0	M_FU_FO_INT FIFO Underrun/Overflow

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0034			Register Name: SMHC_MINTSTS
Bit	Read/Write	Default/Hex	Description
10	R	0x0	M_DSTO_VSD_INT Data Starvation Timeout/V1.8 Switch Done
9	R	0x0	M_DTO_BDS_INT Data Timeout/Boot Data Start
8	R	0x0	M_RTO_BACK_INT Response Timeout/Boot ACK Received
7	R	0x0	M_DCE_INT Data CRC Error When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status token is negative.
6	R	0x0	M_RCE_INT Response CRC Error
5	R	0x0	M_DRR_INT Data Receive Request When set, it means that there are enough data in FIFO during receiving data.
4	R	0x0	M_DTR_INT Data Transmit Request When set, it means that there are enough space in FIFO during transmitting data.
3	R	0x0	M_DTC_INT Data Transfer Complete
2	R	0x0	M_CC_INT Command Complete
1	R	0x0	M_RE_INT Response Error When set, Transmit Bit error or End Bit error or CMD Index error may occurs.
0	/	/	/

11.3.9.15 0x0038 SMHC Raw Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	CARD_REMOVAL Card Removed This is write-1-to-clear bits.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	Read/Write	Default/Hex	Description
30	R/W1C	0x0	CARD_INSERT Card Inserted This is write-1-to-clear bits.
29:19	/	/	/
18	R/W1C	0x0	DATA_WR_BUSY_TO_INT Data write busy timeout interrupt This is write-1-to-clear bits
17	R/W1C	0x0	R1B_BUSY_CLR R1b busy clear When set, it means that the r1b busy has finished or not set.
16	R/W1C	0x0	SDIOI_INT SDIO Interrupt This is write-1-to-clear bits.
15	R/W1C	0x0	DEE Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit. When set during transmitting data, it means that host controller does not receive CRC status token. This is write-1-to-clear bits.
14	R/W1C	0x0	ACD Auto Command Done When set, it means auto stop command(CMD12) completed. This is write-1-to-clear bits.
13	R/W1C	0x0	DSE_BC Data Start Error/busy clear When set during receiving data, it means that host controller found a error start bit. It is valid at 4-bit or 8-bit bus mode, When it set, host found start bit at data0, but not find start bit at some or all of the other data lines. When set during transmitting data, it means that busy signal is cleared after the last block. This is write-1-to-clear bits.
12	R/W1C	0x0	CB_IW Command Busy and Illegal Write This is write-1-to-clear bits.
11	R/W1C	0x0	FU_FO FIFO Underrun/Overflow This is write-1-to-clear bits.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	Read/Write	Default/Hex	Description
10	R/W1C	0x0	DSTO_VSD Data Starvation Timeout/V1.8 Switch Done This is write-1-to-clear bits.
9	R/W1C	0x0	DTO_BDS Data Timeout/Boot Data Start When set during receiving data, it means host did not find start bit on data0(1-bit bus) or data0~data3(4-bit bus) or data0~data7(8-bit bus). This is write-1-to-clear bits.
8	R/W1C	0x0	RTO_BACK Response Timeout/Boot ACK Received This is write-1-to-clear bits.
7	R/W1C	0x0	DCE Data CRC Error When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status token is negative. This is write-1-to-clear bits.
6	R/W1C	0x0	RCE Response CRC Error This is write-1-to-clear bits.
5	R/W1C	0x0	DRR Data Receive Request When set, it means that there are enough data in FIFO during receiving data. This is write-1-to-clear bits.
4	R/W1C	0x0	DTR Data Transmit Request When set, it means that there are enough space in FIFO during transmitting data. This is write-1-to-clear bits.
3	R/W1C	0x0	DTC Data Transfer Complete This is write-1-to-clear bits.
2	R/W1C	0x0	CC Command Complete When set, it means that current command completes even through error occurs. This is write-1-to-clear bits.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	Read/Write	Default/Hex	Description
1	R/W1C	0x0	RE Response Error When set, Transmit Bit error or End Bit error or CMD Index error may occurs. This is write-1-to-clear bits.
0	/	/	/

11.3.9.16 0x003C SMHC Status Register (Default Value: 0x0000_0006)

Offset: 0x003C			Register Name: SMHC_STATUS
Bit	Read/Write	Default/Hex	Description
31	R	0x0	DMA_REQ DMA Request DMA request signal state
30:28	/	/	/
27:17	R	0x0	FIFO_LEVEL FIFO Level Number of filled locations in FIFO
16:11	R	0x0	RESP_IDX Response Index Index of previous response, including any auto-stop sent by controller
10	R	0x0	FSM_BUSY Data FSM Busy Data transmit or receive state-machine is busy 0: Card FSM is idle 1: Card FSM is busy
9	R	0x0	CARD_BUSY Card data busy Inverted version of DATA[0] 0: Card data not busy 1: Card data busy
8	R	0x0	CARD_PRESENT Data[3] status level of DATA[3]; checks whether card is present 0: Card not present 1: Card present

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x003C			Register Name: SMHC_STATUS
Bit	Read/Write	Default/Hex	Description
7:4	R	0x0	FSM_STA Command FSM states: 0000: Idle 0001: Send init sequence 0010: TX CMD start bit 0011: TX CMD TX bit 0100: TX CMD index + argument 0101: TX CMD CRC7 0110: TX CMD end bit 0111: RX response start bit 1000: RX response IRQ response 1001: RX response TX bit 1010: RX response CMD index 1011: RX response data 1100: RX response CRC7 1101: RX response end bit 1110: CMD path wait NCC 1111: Wait; CMD-to-response turnaround
3	R	0x0	FIFO_FULL FIFO full 1: FIFO full 0: FIFO not full
2	R	0x1	FIFO_EMPTY FIFO Empty 1: FIFO Empty 0: FIFO not Empty
1	R	0x1	FIFO_TX_LEVEL FIFO TX Water Level flag 0: FIFO didn t reach transmit trigger level 1: FIFO reached transmit trigger level
0	R	0x0	FIFO_RX_LEVEL FIFO TX Water Level flag 0: FIFO didn t reach receive trigger level 1: FIFO reached receive trigger level

11.3.9.17 0x0040 SMHC FIFO Water Level Register (Default Value: 0x300F_0000)

Offset: 0x0040			Register Name: SMHC_FIFOTH
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0040			Register Name: SMHC_FIFOTH
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x3	MBUS_OT_NUM Mbus outstanding num 0000: OT=1 0001: OT=2 ..... 1111:OT=16 Mbus can send max mbus req numbers, mbus req include descriptor read, descriptor write, dma read, dma write, dma read, Recommended: Mbus_OT_Num = 3, when transfer bolck count = 512B, also, can set this value bigger.
27	/	/	/
26:16	R/W	0xF	RX_TL RX Trigger Level When BLOCK2K_EXIST is 1 b1: 0x0~0x3FE: RX Trigger Level is 0~1022(Unit is equal to the FIFO_WIDTH); 0x3FF reserved When BLOCK2K_EXIST is 1 b0: 0x0~0xFE: RX Trigger Level is 0~254 (Unit is equal to the FIFO_WIDTH); 0xFF reserved FIFO threshold when FIFO request host to receive data from FIFO. When FIFO data level is greater than this value, DMA is request is raised if DMA enabled, or RX interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. 15 (means greater than 15)
15:11	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0040			Register Name: SMHC_FIFOTH
Bit	Read/Write	Default/Hex	Description
10:0	R/W	0x0	TX_TL TX Trigger Level When BLOCK2K_EXIST is 1 b1: 0x1~0x3FF: TX Trigger Level is 1~1023 (Unit is equal to the FIFO_WIDTH); 0x0: no trigger When BLOCK2K_EXIST is 1 b0: 0x1~0xFF: TX Trigger Level is 1~255 (Unit is equal to the FIFO_WIDTH); 0x0: no trigger FIFO threshold when FIFO requests host to transmit data to FIFO. When FIFO data level is less than or equal to this value, DMA TX request is raised if DMA enabled, or TX request interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. Recommended: 240(means less than or equal to 240)

Note: The trigger levels of RX_TL and TX_TL are set as general-purpose DMA DRQ signals, and matches with the DRQ data of DMA.

11.3.9.18 0x0044 SMHC FIFO Function Select Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: SMHC_FUNS
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	ABT_RDATA Abort Read Data 0: Ignored 1: After suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets bit to reset data state-machine, which is waiting for next block of data. Used in SDIO card suspends sequence. This bit is auto-cleared once controller reset to idle state.
1	R/W	0x0	READ_WAIT Read Wait 0: Clear SDIO read wait 1: Assert SDIO read wait

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0044			Register Name: SMHC_FUNS
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	HOST_SEND_MMC_IRQRESQ Host Send MMC IRQ Response 0: Ignored 1: Send auto IRQ response When host is waiting MMC card interrupt response, setting this bit will make controller cancel wait state and return to idle state, at which time, controller will receive IRQ response sent by itself. This bit is auto-cleared after response is sent.

11.3.9.19 0x0048 SMHC Transferred Byte Count Register 0 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: SMHC_TBC0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	TBC0 Transferred Count 0 Number of bytes transferred between card and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

11.3.9.20 0x004C SMHC Transferred Byte Count Register 1 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: SMHC_TBC1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	TBC1 Transferred Count 1 Number of bytes transferred between Host/DMA memory and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

11.3.9.21 0x0054 SMHC CRC Status Detect Control Register (Default Value: 0x0000_0003)

Offset: 0x0054			Register Name: SMHC_CSDC
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0054			Register Name: SMHC_CSDC
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x3	CRC_DET_PARA CRC Detect Para 110: HS400 speed mode 011: Other speed mode Others: Reserved

11.3.9.22 0x0058 SMHC Auto Command 12 Argument Register (Default Value: 0x0000_FFFF)

Offset: 0x0058			Register Name: SMHC_A12A
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0xFFFF	A12A Auto CMD12 Argument The argument of command 12 automatically send by controller with this field.

11.3.9.23 0x005C SMHC New Timing Set Register (Default Value: 0x8171_0000)

Offset: 0x005C			Register Name: SMHC_NTSR
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	MODE_SEL Mode Select 0: Old mode of Sample/Output Timing 1: New mode of Sample/Output Timing Default value : 1
30:26	/	/	/
25	R/W	0x0	BOOT_DAT_RX_PHASE_CLR After boot ack, before receive boot data, clear data lines input phase. 0: Disable 1: Enable
24	R/W	0x1	CMD_DAT_RX_PHASE_CLR During update clock operation, clear command line s and data lines input phase. 0: Disable 1: Enable
23	/	/	/
22	R/W	0x1	DAT_CRC_STATUS_RX_PHASE_CLR Before receive CRC status, clear data lines input phase. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x005C			Register Name: SMHC_NTSR
Bit	Read/Write	Default/Hex	Description
21	R/W	0x1	DAT_TRANS_RX_PHASE_CLR Before transfer data, clear data lines input phase. 0: Disable 1: Enable
20	R/W	0x1	DAT_RECV_RX_PHASE_CLR Before receive data, clear data lines input phase clear 0: Disable 1: Enable
19:17	/	/	/
16	R/W	0x1	CMD_SEND_RX_PHASE_CLR Before send command, command rx phase clear 0: Disable 1: Enable
15:10	/	/	/
9:8	R/W	0x0	DAT_SAM_TIM_PHS Data Sample Timing Phase 00: Sample timing phase offset 90^0 01: Sample timing phase offset 180^0 10: Sample timing phase offset 270^0 11: Sample timing phase offset 0^0（only for SD2 hs400 mode） Default value: 00
7:6	/	/	/
5:4	R/W	0x0	CMD_SAM_TIM_PHS Command Sample Timing Phase 00: Sample timing phase offset 90^0 01: Sample timing phase offset 180^0 10: Sample timing phase offset 270^0 11: Ignore Default value: 00
3:1	/	/	/
0	R/W	0x0	HS400_NEW_SAM_EN HS400 New Sample Enable 1: Enable hs400 new sample method 0: Disable hs400 new sample method

11.3.9.24 0x0078 SMHC Hardware Reset Register (Default Value: 0x0000_0001)

Offset: 0x0078	Register Name: SMHC_HWRST

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	HW_RST Hardware Reset 1: Active mode 0: Reset These bits cause the cards to enter pre-idle state, which requires them to be re-initialized.

11.3.9.25 0x007C SMHC Normal DMA mode control Register (Default Value: 0x0000_0000)

Offset: 0x007C			Register Name: SMHC_NDMA_MODE_CTL
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	HANDSHAKE_CONFIG Handshake configuration 0xA5: DMA wait cycle mode 0xE5: DMA handshake mode [20:16] indicates digital synchrounous beat number, which can be theoretically modified. [23:21] is used to distinguish between handshake mode and waiting mode. When it is waiting mode, DRQ signals are transmitted. When it is handshake mode, the ack signals after a few clock cycles will be synchronized.
15:2	/	/	/
1	R/W	0x0	DMA_RX_EN DMA RX req enable
0	R/W	0x0	DMA_TX_EN DMA tx req enable

11.3.9.26 0x0080 SMHC DMAC Control Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: SMHC_DMAC
Bit	Read/Write	Default/Hex	Description
31	W	0x0	DES_LOAD_CTRL When DMAC fetches a descriptor, if the valid bit of a descriptor is not set, DMAC FSM will go to the suspend state. Setting this bit will make DMAC re-fetch descriptor again and do the transfer normally.
30:8	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0080			Register Name: SMHC_DMAC
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	IDMAC_ENB IDMAC Enable. When set, the IDMAC is enabled. DE is read/write.
6:1	/	/	/
0	R/W	0x0	IDMAC_RST DMA Reset. When set, the DMA Controller resets all its internal registers. SWR is read/write. It is automatically cleared after 1 clock cycle.

11.3.9.27 0x0084 SMHC Descriptor List Base Address Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: SMHC_DLBA
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	DES_BASE_ADDR Start of Descriptor List. Contains the base address of the First Descriptor, is a word(4byte) address

11.3.9.28 0x0088 SMHC DMAC Status Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: SMHC_IDST
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W1C	0x0	NIS Normal Interrupt Summary. Logical OR of the following: SMHC_IDST[0]: Transmit Interrupt SMHC_IDST[1]: Receive Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes NIS to be set is cleared. Writing a 1 clears this bit.
7:6	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0088			Register Name: SMHC_IDST
Bit	Read/Write	Default/Hex	Description
5	R/W1C	0x0	ERR_FLAG_SUM Card Error Summary. Indicates the status of the transaction to/from the card; also present in RINTSTS. Indicates the logical OR of the following bits: EBE: End Bit Error RTO: Response Timeout RCRC: Response CRC SBE: Start Bit Error DRTO: Data Read Timeout DCRC: Data CRC for Receive RE: Response Error Writing a 1 clears this bit.
4	R/W1C	0x0	DES_UNAVL_INT Descriptor Unavailable Interrupt. This bit is set when the descriptor is unavailable due to OWN bit = 0 (DES0[31] =0). Writing a 1 clears this bit.
3:2	/	/	/
1	R/W1C	0x0	RX_INT Receive Interrupt. Indicates the completion of data reception for a descriptor. Writing a 1 clears this bit.
0	R/W1C	0x0	TX_INT Transmit Interrupt. Indicates that data transmission is finished for a descriptor. Writing a 1 clears this bit.

11.3.9.29 0x008C SMHC DMAC Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: SMHC_IDIE
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	ERR_SUM_INT_ENB Card Error summary Interrupt Enable. When set, it enables the Card Interrupt summary.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x008C			Register Name: SMHC_IDIE
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	DES_UNAVL_INT_ENB Descriptor Unavailable Interrupt. When set along with Abnormal Interrupt Summary Enable, the Descriptor Unavailable interrupt is enabled.
3	/	/	/
2	R/W	0x0	FERR_INT_ENB Fatal Bus Error Enable. When set with Abnormal Interrupt Summary Enable, the Fatal Bus Error Interrupt is enabled. When reset, Fatal Bus Error Enable Interrupt is disabled.
1	R/W	0x0	RX_INT_ENB Receive Interrupt Enable. When set , Normal Interrupt Summary Enable, Receive Interrupt is enabled. When reset, Receive Interrupt is disabled.
0	R/W	0x0	TX_INT_ENB Transmit Interrupt Enable. When set , Normal Interrupt Summary Enable, Transmit Interrupt is enabled. When reset, Transmit Interrupt is disabled.

11.3.9.30 0x0100 SMHC Card Threshold Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: SMHC_THLD
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	CARD_WR_THLD Card Read/write Threshold Size (Unit: byte)
15:3	/	/	/
2	R/W	0x1	CARD_WR_THLD_ENB Card Write Threshold Enable 0: Card write threshold disable 1: Card write threshold enabled Host controller initiates write transfer only if card threshold amount of data is available in transmit FIFO

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0100			Register Name: SMHC_THLD
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	BCIG Busy Clear Interrupt Generation 0: Busy Clear Interrupt disabled 1: Busy Clear Interrupt Enabled The application can disable this feature if it does not want to wait for a Busy Clear Interrupt.
0	R/W	0x1	CARD_RD_THLD_ENB Card Read Threshold Enable 0: Card Read Threshold Disable 1: Card Read Threshold Enable Host controller initiates Read Transfer only if CARD_RD_THLD amount of space is available in receive FIFO

11.3.9.31 0x0104 SMHC Sample FIFO Control Register (Default Value: 0x0000_0006)

Offset: 0x0104			Register Name: SMHC_SFC
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4:1	R/W	0x3	STOP_CLK_CTRL Stop Clock Control When receiving data, if CARD_RD_THLD_ENB is set and CARD_RD_THLD is set same with BLK_SZ, the device clock may stop at block gap during data receiving. This field is used to control the position of stopping clock. The value can be change between 0x0 and 0xF,but actually the available value and the position of stopping clock must be decided by the actual situation. The value increase one in this field is linked to one cycle(two cycle in DDR mode) that the position of stopping clock moved up.
0	R/W	0x0	BYPASS_EN Bypass enable When set, sample FIFO will be bypassed.

11.3.9.32 0x0108 SMHC Auto Command 23 Argument Register (Default Value: 0x0000_0000)

Offset: 0x0108	Register Name: SMHC_A23A

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	A23A Auto CMD23 Argument The argument of command 23 is automatically sent by controller with this field.

11.3.9.33 0x010C SMHC eMMC4.5 DDR Start Bit Detection Control Register (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: EMMC_DDR_SBIT_DET
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HS400_MD_EN HS400 Mode Enable 0: Disable 1: Enable It is required to set this bit to '1' before initiating any data transfer CMD in HS400 mode.
30:1	/	/	/
0	R/W	0x0	HALF_START_BIT Control for start bit detection mechanism inside host controller based on duration of start bit. For eMMC 4.5, start bit can be: 0: Full cycle 1: Less than one full cycle Set HALF_START_BIT=1 for eMMC 4.5 and above; set to 0 for SD applications.

11.3.9.34 0x0110 SMHC Response CRC Register (Default Value:0x0000_0000)

Offset: 0x0110			Register Name: SMHC_RESP_CRC
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:0	R	0x0	RESP_CRC Response CRC Response CRC from device

11.3.9.35 0x0138 SMHC Extended Command Register (Default Value: 0x0000_0000)

Offset: 0x0138			Register Name: SMHC_EXT_CMD
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0138			Register Name: SMHC_EXT_CMD
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	AUTO_CMD23_EN Send CMD23 Automatically When set this bit, send CMD23 automatically before send command specified in SMHC_CMD register. When SOFT_RST set, this field will be cleared.

11.3.9.36 0x013C SMHC Extended Response Register (Default Value: 0x0000_0000)

Offset: 0x013C			Register Name: SMHC_EXT_RESP
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	SMHC_EXT_RESP When AUTO_CMD23_EN is set, this register stores the response of CMD23.

11.3.9.37 0x0140 SMHC Drive Delay Control Register (Default Value: 0x0001_0000)

Offset: 0x0140			Register Name: SMHC_DRV_DL
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	DAT_DRV_PH_SEL Data Drive Phase Select 0: Data drive phase offset is: 90^0 at SDR mode, 45^0 at DDR8 mode, 90^0 at DDR4 mode when 0x5C[31] is low, 45^0 at DDR4 mode when 0x5C[31] is high, 90^0 at HS400 mode when 0x5C[0] is low, 45^0 at HS400 mode when 0x5C[0] is high. 1: Data drive phase offset is: 180^0 at SDR mode, 90^0 at DDR8 mode, 180^0 at DDR4 mode when 0x5C[31] is low, 90^0 at DDR4 mode when 0x5C[31] is high, 180^0 at HS400 mode when 0x5C[0] is low, 90^0 at HS400 mode when 0x5C[0] is high.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0140			Register Name: SMHC_DRV_DL
Bit	Read/Write	Default/Hex	Description
16	R/W	0x1	CMD_DRV_PH_SEL Command Drive Phase Select 0: Command drive phase offset is: 90^0 at SDR mode, 45^0 at DDR8 mode, 90^0 at DDR4 mode when 0x5C[31] is low, 45^0 at DDR4 mode when 0x5C[31] is high, 90^0 at HS400 mode 1: Command drive phase offset is: 180^0 at SDR mode, 90^0 at DDR8 mode, 180^0 at DDR4 mode when 0x5C[31] is low, 90^0 at DDR4 mode when 0x5C[31] is high, 180^0 at HS400 mode.
15:0	/	/	/

11.3.9.38 0x0144 SMHC Sample Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0144			Register Name: SMHC_SAMP_DL
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:8	R	0x20	Reserved
7	R/W	0x0	SAMP_DL_SW_EN Sample Delay Software Enable When set, enable sample delay specified at SAMP_DL_SW
6	/	/	/
5:0	R/W	0x0	SAMP_DL_SW Sample Delay Software The relative delay between clock line and command line, data lines. It can be determined according to the value of SAMP_DL, the cycle of card clock and device s input timing requirement.

11.3.9.39 0x0148 SMHC Data Strobe Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0148			Register Name: SMHC_DS_DL
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0148			Register Name: SMHC_DS_DL
Bit	Read/Write	Default/Hex	Description
13:8	R	0x20	Reserved
7	R/W	0x0	DS_DL_SW_EN Sample Delay Software Enable
6	/	/	/
5:0	R/W	0x0	DS_DL_SW Data Strobe Delay Software

11.3.9.40 0x0154 SMHC Card interface counter Register (Default Value:0x0)

Offset: 0x0154			Register Name: SMHC_CIU_CNT
Bit	Read/Write	Default/Hex	Description
31:6	R	0x0	DATA_PATH_CNT Data Path Counter This field indicates the count value of counters for each stage when host read or write data. When Host read data, this field is one of the following values: 1. The time of wait data start bit
5:0	/	/	/

11.3.9.41 0x015C SMHC Write Busy Timeout Register (Default Value:0x00FF_FFFF)

Offset: 0x015C			Register Name: SMHC_WR_BUSY_TMOUT
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:0	R/W	0xffffff	WR_BUSY_TO_LMT Data write busy timeout Limit The actual written busy timeout value is WR_BUSY_TO_LMT + 1.

11.3.9.42 0x01A0 SMHC CQE Control Register (Default Value: 0x0000_0003)

Offset: 0x01A0			Register Name: SMHC_CQE_CTRL
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
8	R/W	0x0	DS_SAMP_RESP_EN datastrobe sample response enable It should be set when CQE work at HS400 enhance strobe mode

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x01A0			Register Name: SMHC_CQE_CTRL
Bit	Read/Write	Default/Hex	Description
7:2	/	/	/
1	R/W	0x1	CQE_CLR_DTC_EN 0: cqe clear data transfer complete(DTC) status disable 1: cqe clear data transfer complete(DTC) status enable
0	R/W	0x1	CQE_CLR_CC_EN 0: cqe clear command complete(CC) status disable 1: cqe clear command complete(CC) status enable

11.3.9.43 0x0200 SMHC FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: SMHC_FIFO
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TX/RX_FIFO Data FIFO

11.3.9.44 0x0408 Command Queuing Configuration Register (Default Value: 0x0200_0000)

This register controls CQE behavior affecting the general operation of command queuing module or operation of multiple tasks in the same time.

Offset: 0x0408			Register Name: CQCFG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x200	CQE_BLOCK_SIZE CQE Block Size Configuration It must be 0x200 when CMDQ_MODE is cmdq or cmdq_half or cmdq_almost.
15:13	/	/	/
12	R/W	0x0	CQE_DCMD_EN Direct Command (DCMD) Enable This bit indicates to the hardware whether the Task Descriptor in slot #31 of the TDL is a Data Transfer Task Descriptor, or a Direct Command Task Descriptor. CQE uses this bit when a task is issued in slot #31, to determine how to decode the Task Descriptor. Bit Value Description 1: Task descriptor in slot #31 is a DCMD Task Descriptor 0: Task descriptor in slot #31 is a Data Transfer Task Descriptor
11:9	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0408			Register Name: CQCFG
Bit	Read/Write	Default/Hex	Description
8	R/W	0x0	CQE_TASK_DESC_SIZE Task Descriptor Size This bit indicates whether the task descriptor size is 128 bits or 64 bits as detailed in Data Structures section. This bit can only be configured when Command Queuing Enable bit is 0 (command queuing is disabled) Bit Value Description 1: Task descriptor size is 128 bits 0: Task descriptor size is 64 bits
7:1	/	/	/
0	R/W	0x0	CQE_EN Command Queuing Enable Software shall write 1 this bit when in order to enable command queuing mode (i.e., enable CQE). When this bit is 0, CQE is disabled and software controls the eMMC bus using the legacy eMMC host controller. Before software writes 1 to this bit, software shall verify that the eMMC host controller is in idle state and there are no commands or data transfers ongoing. When software wants to exit command queuing mode, it shall clear all previous tasks if such exist before setting this bit to 0.

11.3.9.45 0x040C Command Queuing Control Register (Default Value: 0x0000_0000)

This register controls CQE behavior affecting the general operation of command queuing module or operation of multiple tasks in the same time.

Offset: 0x040C			Register Name: CQCTL
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x040C			Register Name: CQCTL
Bit	Read/Write	Default/Hex	Description
8	R/WAC	0x0	CQE_TCL_ALL CQE Task Cleared All Software shall write 1 this bit when it wants to clear all the tasks sent to the device. This bit can only be written when CQE is in halt state (i.e., Halt bit is 1). When software writes 1, the value of the register is updated to 1 , and CQE shall reset CQTDBR register and all other context information for all unfinished tasks. Then CQE will clear this bit. Software should poll on this bit until it is set to back 0 and may then resume normal operation, by clearing the Halt bit. CQE does not communicate to the device that the tasks were cleared. It is software s responsibility to order the device to discard the tasks in its queue using CMDQ_TASK_MGMT command. Writing 0 to this register shall have no effect.
7:1	/	/	/
0	R/W	0x0	CQE_HALT Host software shall write 1 to the bit when it wants to acquire software control over the eMMC bus and disable CQE from issuing commands on the bus. For example, issuing a Discard Task command (CMDQ_TASK_MGMT) When software writes 1 , CQE shall complete the ongoing task if such a task is in progress. Once the task is completed and CQE is in idle state, CQE shall not issue new commands and shall indicate so to software by setting this bit to 1. Software may poll on this bit until it is set to 1, and may only then send commands on the eMMC bus. In order to exit halt state (i.e., resume CQE activity), software shall clear this bit (write 0). Writing 0 when the value is already 0 shall have no effect.

11.3.9.46 0x0410 Command Queuing Interrupt Status Register (Default Value: 0x0000_0000)

This register indicates pending interrupts that require service. Each bit in this registers is asserted in response a specific event, only if the respective bit is set in CQISTE register.

Offset: 0x0410			Register Name: CQIS
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0410			Register Name: CQIS
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W1C	0x0	CQIS_TCL Task Cleared This status bit is asserted (if CQISTE.TCL=1) when a task clear operation is completed by CQE. The completed task clear operation is either an individual task clear (CQTCLR) or clearing of all tasks (CQCTL).
2	R/W1C	0x0	CQIS_RED Response Error Detected Interrupt This status bit is asserted (if CQISTE.RED=1) when a response is received with an error bit set in the device status field. The contents of the device status field are listed in 6.13. Software uses CQRMEM register to configure which device status bit fields may trigger an interrupt, and which are masked.
1	R/W1C	0x0	CQIS_TCC Task Complete Interrupt This status bit is asserted (if CQISTE.TCC=1) when at least one of the following two conditions are met: A task is completed and the INT bit is set in its Task Descriptor Interrupt caused by Interrupt Coalescing logic (see 0)
0	R/W1C	0x0	CQIS_HAC Halt Complete Interrupt This status bit is asserted (if CQISTE.HAC=1) when halt bit in CQCTL register transitions from 0 to 1 indicating that host controller has completed its current ongoing task and has entered halt state.

11.3.9.47 0x0414 Command Queuing Interrupt Status Enable Register (Default Value: 0x0000_0000)

This register enables and disables the reporting of the corresponding interrupt to host software in CQIS register. When a bit is set ('1') and the corresponding interrupt condition is active, then the bit is CQIS is asserted. Interrupt sources that are disabled ('0') are not indicated in the CQIS register. This register is bit-index matched to CQIS register.

Offset: 0x0414			Register Name: CQISTE
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0414			Register Name: CQISTE
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	CQISTE_TCL Task Cleared Status Enable 1: CQIS.TCL will be set when its interrupt condition is active 0: CQIS.TCL is disabled
2	R/W	0x0	CQISTE_RED Response Error Detected Status Enable 1: CQIS.RED will be set when its interrupt condition is active 0: CQIS.RED is disabled
1	R/W	0x0	CQISTE_TCC Task Complete Status Enable 1: CQIS.TCC will be set when its interrupt condition is active 0: CQIS.TCC is disabled
0	R/W	0x0	CQISTE_HAC Halt Complete Status Enable 1: CQIS.HAC will be set when its interrupt condition is active 0: CQIS.HAC is disabled

11.3.9.48 0x0418 Command Queuing Interrupt Signal Enable Register (Default Value: 0x0000_0000)

This register enables and disables the generation of interrupts to host software. When a bit is set ('1') and the corresponding bit in CQIS is set, then an interrupt is generated. Interrupt sources that are disabled ('0') are still indicated in the CQIS register. This register is bit-index matched to CQIS register.

Offset: 0x0418			Register Name: CQISGE
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	CQISGE_TCL Task Cleared Signal Enable When set and CQIS.TCL is asserted, the CQE shall generate an interrupt
2	R/W	0x0	CQISGE_RED Response Error Detected Signal Enable When set and CQIS.RED is asserted, the CQE shall generate an interrupt

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0418			Register Name: CQISGE
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	CQISGE_TCC Task Complete Signal Enable When set and CQIS.TCC is asserted, the CQE shall generate an interrupt
0	R/W	0x0	CQISGE_HAC Halt Complete Signal Enable When set and CQIS.HAC is asserted, the CQE shall generate an interrupt

11.3.9.49 0x041C Command Queuing Interrupt Coalescing Register (Default Value: 0x0000_0000)

This register controls the interrupt coalescing feature.

Offset: 0x041C			Register Name: CQIC
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CQIC_EN Interrupt Coalescing Enable/Disable When set to 0 by software, command responses are neither counted nor timed. Interrupts are still triggered by completion of tasks with INT=1 in the Task Descriptor. When set to 1 , the interrupt coalescing mechanism is enabled and coalesced interrupts are generated
30:21	/	/	/
20	R	0x0	CQIC_SB Interrupt Coalescing Status Bit This bit indicates to software whether any tasks (with INT=0) have completed and counted towards interrupt coalescing (i.e., ICSB is set if and only if IC counter > 0). Bit Value Description 1 = At least one task completion has been counted (IC counter >0) 0 = No task completions have occurred since last counter reset (IC counter =0)
19:17	/	/	/
16	W	0x0	CQIC_CTR Counter and Timer Reset When host driver writes 1 , the interrupt coalescing timer and counter are reset

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x041C			Register Name: CQIC
Bit	Read/Write	Default/Hex	Description
15	W	0x0	CQIC_CTH_WEN Interrupt Coalescing Counter Threshold Write Enable When software writes 1 , the value ICCTH is updated with the contents written at the same cycle. When software writes 0 , the value in ICCTH is not updated. NOTE Write operations to ICCTH are only allowed when the task queue is empty.
14:13	/	/	/
12:8	R/W	0x0	CQIC_CTH Interrupt Coalescing Counter Threshold Software uses this field to configure the number of task completions (only tasks with INT=0 in the Task Descriptor) which are required in order to generate an interrupt. Counter Operation: As data transfer tasks with INT=0 complete, they are counted by CQE. The counter is reset by software during the interrupt service routine. The counter stops counting when it reaches the value configured in ICCTH. The maximum allowed value is 31 NOTE 1: When ICCTH is 0, task completions are not counted, and counting-based interrupts are not generated. NOTE 2: When ICCTH is 1, interrupt is actually not coalesced, and CQIC_SB will not be set. In order to write to this field, the ICCTHWEN bit must be set at the same write operation.
7	W	0x0	CQIC_TOVAL_WEN Interrupt Coalescing Timeout Value Write Enable When software writes 1 , the value ICTOVAL is updated with the contents written at the same cycle. When software writes 0 , the value in ICTOVAL is not updated. NOTE Write operations to ICTOVAL are only allowed when the task queue is empty.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x041C			Register Name: CQIC
Bit	Read/Write	Default/Hex	Description
6:0	R/W	0x0	CQIC_TOVAL Interrupt Coalescing Timeout Value Software uses this field to configure the maximum time allowed between the completion of a task on the bus and the generation of an interrupt. Timer Operation: The timer is reset by software during the interrupt service routine. It starts running when a data transfer task with INT=0 is completed, after the timer was reset. When the timer reaches the value configured in ICTOVAL field it generates an interrupt and stops. The timer s unit is equal to 1024 clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field CQCAP register. The minimum value is 01h (1024 clock periods) and the maximum value is 7Fh (127*1024 clock periods). For example, a CQCAP field value of 0 indicates a 19.2 MHz clock frequency (period = 52.08 ns). If the setting in ICTOVAL is 10h, the calculated polling period is 16*1024*52.08 ns= 853.33 us NOTE: When ICTOVAL is 0, the timer is not running, and timer-based interrupts are not generated. In order to write to this field, the ICTOVALWEN bit must be set at the same write operation.

11.3.9.50 0x0420 Command Queuing Task Descriptor List Base Address Register (Default Value: 0x0000_0000)

This register is used for configuring the lower 32 bits of the byte address of the head of the Task Descriptor List in the host memory.

Offset: 0x0420			Register Name: CQTDLBA
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0420			Register Name: CQTDLBA
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CQE_TDLBA Task Descriptor List Base Address This register stores the LSB bits (bits 31:0) of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is 32 * (Task Descriptor size + Transfer Descriptor size) as configured by Host driver. This address shall be set on 1 KByte boundary: The lower 10 bits of this register shall be set to 0 by software and shall be ignored by CQE.

11.3.9.51 0x0424 Command Queuing Task Descriptor List Base Address Upper 32 Bits Register (Default Value: 0x0000_0000)

This register is used for configuring the upper 32 bits of the byte address of the head of the Task Descriptor List in the host memory.

Offset: 0x0424			Register Name: CQTDLBAU
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CQE_TDLBAU Task Descriptor List Base Address Upper This register stores the MSB bits (bits 63:32) of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is 32 * (Task Descriptor size + Transfer Descriptor size) as configured by Host driver. This register is reserved when using 32-bit addressing mode.

11.3.9.52 0x0428 Command Queuing Task Doorbell Register (Default Value: 0x0000_0000)

Using this register, software triggers CQE to process a new task.

Offset: 0x0428			Register Name: CQTDBR
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0428			Register Name: CQTDBR
Bit	Read/Write	Default/Hex	Description
31:0	R/W1S	0x0	CQE_TDBR Command Queuing Task Doorbell Software shall configure TDLBA and TDLBAU, and enable CQE in CQCFG before using this register. Writing 1 to bit n of this register triggers CQE to start processing the task encoded in slot n of the TDL. CQE always processes tasks in-order according to the order submitted to the list by CQTDBR write transactions. CQE processes Data Transfer tasks by reading the Task Descriptor and sending QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) commands to the device. CQE processes DCMD tasks (in slot #31, when enabled) by reading the Task Descriptor, and generating the command encoded by its index and argument. The corresponding bit is cleared to 0 by CQE in one of the following events: When a task execution is completed (with success or error) The task is cleared using CQTCLR register All tasks are cleared using CQCTL register CQE is disabled using CQCFG register Software may initiate multiple tasks at the same time (batch submission) by writing 1 to multiple bits of this register in the same transaction. In the case of batch submission: CQE shall process the tasks in order of the task index, starting with the lowest index. If one or more tasks in the batch are marked with QBR, the ordering of execution will be based on said processing order. Writing 0 by software shall have no impact on the hardware, and will not change the value of the register bit.

11.3.9.53 0x042C Command Queuing Task Completion Notification Register (Default Value: 0x0000_0000)

This register is used by CQE to notify software about completed tasks.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x042C			Register Name: CQTCN
Bit	Read/Write	Default/Hex	Description
31:0	R/W1C	0x0	CQE_TCN Task Complete Notification CQE shall set bit *n* of this register (at the same time it clears bit *n* of CQTDBR) when a task execution is completed (with success or error). When receiving interrupt for task completion, software may read this register to know which tasks have finished. After reading this register, software may clear the relevant bit fields by writing 1 to the corresponding bits.

11.3.9.54 0x0430 Command Queuing Device Queue Status Register (Default Value: 0x0000_0000)

This register stores the most recent value of the device's queue status.

Offset: 0x0430			Register Name: CQDQS
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CQE_DQS Device Queue Status Every time the Host controller receives a queue status register (QSR) from the device, it updates this register with the response of status command, i.e., the device s queue status.

11.3.9.55 0x0434 Command Queuing Device Pending Tasks Register (Default Value: 0x0000_0000)

This register indicates to software which tasks are queued in the device, awaiting execution.

Offset: 0x0434			Register Name: CQDPT
Bit	Read/Write	Default/He	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0434			Register Name: CQDPT
Bit	Read/Write	Default/He	Description
31:0	R	0x0	CQE_DPT Device Pending Tasks Bit *n* of this register is set if and only if QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) were sent for this specific task and if this task hasn t been executed yet. CQE shall set this bit after receiving a successful response for CMD45. CQE shall clear this bit after the task has completed execution. Software needs to read this register in the task-discard procedure, when the controller is halted, to determine if the task is queued in the device. If the task is queued, the driver sends a CMDQ_TASK_MGMT (CMD48) to the device ordering it to discard the task. Then software clears the task in the CQE. Only then the software orders CQE to resume its operation using CQCTL register.

11.3.9.56 0x0438 Command Queuing Task Clear Register (Default Value: 0x0000_0000)

This register is used for removing an outstanding task in the CQE. The register should be used only when CQE is in Halt state.

Offset: 0x0438			Register Name: CQTCLR
Bit	Read/Write	Default/He	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0438			Register Name: CQTCLR
Bit	Read/Write	Default/He	Description
31:0	R/W	0x0	CQE_TASK_CLR Command Queuing Task Clear Writing 1 to bit *n* of this register orders CQE to clear a task which software has previously issued. This bit can only be written when CQE is in Halt state as indicated in CQCTL register Halt bit. When software writes 1 to a bit in this register, CQE updates the value to 1 , and starts clearing the data structures related to the task. CQE clears the bit fields (sets a value of 0) in CQTCLR and in CQTDBR once clear operation is complete. Software should poll on the CQTCLR until it is cleared to verify clear operation was complete. Writing to this register only clears the task in the CQE and does not have impact on the device. In order to discard the task in the device, host software shall send CMDQ_TASK _MGMT while CQE is still in Halt state. Host driver is not allowed to use this register to clear multiple tasks at the same time. Clearing multiple tasks can be done using CQCTL register. Writing 0 to a register bit shall have no impact.

11.3.9.57 0x0440 Command Queuing Send Status Configuration 1 Register (Default Value: 0x0000_1000)

The register controls the when SEND_QUEUE_STATUS commands are sent.

Offset: 0x0440			Register Name: CQSSC1
Bit	Read/Write	Default/He	Description
31:16	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0440			Register Name: CQSSC1
Bit	Read/Write	Default/He	Description
15:0	R/W	0x1000	CQE_SSC_CIT Send Status Command Idle Timer This field indicates to CQE the polling period to use when using periodic SEND_QUEUE_STATUS (CMD13) polling. Periodic polling is used when tasks are pending in the device, but no data transfer is in progress. When a SEND_QUEUE_STATUS response indicating that no task is ready for execution, CQE counts the configured time until it issues the next SEND_QUEUE_STATUS. Timer units are clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field CQCAP register. The minimum value is 0001h (1 clock period) and the maximum value is FFFFh (65535 clock periods). Default interval is: 4096 clock periods. For example, a CQCAP field value of 0 indicates a 19.2 MHz clock frequency (period = 52.08 ns). If the setting in CQSSC1.CIT is 1000h, the calculated polling period is 4096*52.08 ns= 213.33 us

11.3.9.58 0x0444 Command Queuing Send Status Configuration 2 Register (Default Value: 0x0000_0000)

This register is used for configuring RCA field in SEND_QUEUE_STATUS command argument.

Offset: 0x0444			Register Name: CQSSC2
Bit	Read/Write	Default/He	Description
31:16	/	/	/
15:0	R/W	0x0	CQE_SSC_RCA Send Queue Status RCA This field provides CQE with the contents of the 16-bit RCA field in SEND_QUEUE_ STATUS (CMD13) command argument. CQE shall copy this field to bits 31:16 of the argument when transmitting SEND_ QUEUE_STATUS (CMD13) command.

11.3.9.59 0x0448 Command Queuing Command Response for Direct-Command Task Register (Default Value: 0x0000_0000)

This register is used for passing the response of a DCMD task to software.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0448			Register Name: CQCRDCT
Bit	Read/Write	Default/He	Description
31:0	R	0x0	CQE_DCMD_LAST_RESP Direct Command Last Response This register contains the response of the command generated by the last direct- command (DCMD) task which was sent. CQE shall update this register when it receives the response for a DCMD task. This register is considered valid only after bit 31 of CQTDBR register is cleared by CQE.

11.3.9.60 0x0450 Command Queuing Response Mode Error Mask Register (Default Value: 0xFDF9_A080)

This register controls the generation of Response Error Detection (RED) interrupt.

Offset: 0x0450			Register Name: CQRMEM
Bit	Read/Write	Default/He	Description
31:0	R/W	0xFDF9A080	CQE_RMEM Response Mode Error Mask This bit is used as in interrupt mask on the device status filed which is received in R1/R1b responses. Bit Value Description (for any bit i): 1 = When a R1/R1b response is received, with bit *i* in the device status set, a RED interrupt is generated 0 = When a R1/R1b response is received, bit *i* in the device status is ignored The reset value of this register is set to trigger an interrupt on all Error type bits in the device status, as defined in 6.13. NOTE: Responses to CMD13 (SQS) encode the QSR, so they are ignored by this logic.

11.3.9.61 0x0454 Command Queuing Task Error Information Register (Default Value: 0x0000_0000)

This register is updated by CQE when an error occurs on data or command related to a task activity.

When such error is detected by CQE or indicated by the *e*•MMC controller CQE stores in CQTERRI the task IDs and the command indices of the commands which were executed on the command line and data lines when the error occurred.

Software is expected to use this information in the error recovery procedure. See B.2.8 for more details.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0454			Register Name: CQERRI
Bit	Read/Write	Default/He	Description
31	R	0x0	CQE_DTE_VLD Data Transfer Error fields Valid This bit is updated when an error is detected by CQE, or indicated by eMMC controller. If a data transfer is in progress when the error is detected/indicated, the bit is set to 1. If a no data transfer is in progress when the error is detected/indicated, the bit is cleared to 0.
30:29	/	/	/
28:24	R	0x0	CQE_DTE_TASK_ID Data Transfer Error Task ID This field indicates the ID of the task which was executed on the data lines when an error occurred. The field is updated if a data transfer is in progress when an error is detected by CQE, or indicated by eMMC controller.
23:22	/	/	/
21:16	R	0x0	CQE_DTE_CMD_IDX Data Transfer Error Command Index This field indicates the index of the command which was executed on the data lines when an error occurred. The index shall be set to EXECUTE_READ_TASK (CMD46) or EXECUTE_WRITE_TASK (CMD47) according to the data direction. The field is updated if a data transfer is in progress when an error is detected by CQE, or indicated by eMMC controller.
15	R	0x0	CQE_RME_VLD Response Mode Error fields Valid This bit is updated when an error is detected by CQE, or indicated by eMMC controller. If a command transaction is in progress when the error is detected/indicated, the bit is set to 1. If a no command transaction is in progress when the error is detected/indicated, the bit is cleared to 0.
14:13	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0454			Register Name: CQERRI
Bit	Read/Write	Default/He	Description
12:8	R	0x0	CQE_RME_TASK_ID Response Mode Error Task ID This field indicates the ID of the task which was executed on the command line when an error occurred. The field is updated if a command transaction is in progress when an error is detected by CQE, or indicated by eMMC controller.
7:6	/	/	/
5:0	R	0x0	CQE_RME_CMD_IDX Response Mode Error Command Index This field indicates the index of the command which was executed on the command line when an error occurred. The field is updated if a command transaction is in progress when an error is detected by CQE, or indicated by eMMC controller.

11.3.9.62 0x0458 Command Queuing Command Response Index Register (Default Value: 0x0000_0000)

This register stores the index of the last received command response.

Offset: 0x0458			Register Name: CQCRI
Bit	Read/Write	Default/He	Description
31:6	/	/	/
5:0	R	0x0	CQE_LAST_RESP_IDX Last Command Response index This field stores the index of the last received command response. CQE shall update the value every time a command response is received.

11.3.9.63 0x045C Command Queuing Command Response Argument Register (Default Value: 0x0000_0000)

This register stores the argument of the last received command response.

Offset: 0x045C			Register Name: CQCRA
Bit	Read/Write	Default/He	Description
31:0	R	0x0	CQE_LAST_RESP_ARG Last Command Response Argument This field stores the argument of the last received command. CQE shall update the value every time a command response is received.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.3.9.64 0x0460 Command Queuing Function Control Register (Default Value: 0x0000_0000)

This register is used to enable or disable some CQE functions.

Offset: 0x0460			Register Name: CQFUNCCTL
Bit	Read/Write	Default/He	Description
31:16	/	/	/
15:8	R/W	0x0	CQE_SMHC_ERR_MASK This field is used to mask errors that CQE does not need to consider. bit7 for Data End-bit error mask bit6 for Data Start-bit error mask bit5 for Data Starvation error mask bit4 for Data timeout mask bit3 for Response timeout mask bit2 for Data CRC error mask bit1 for Response CRC error mask bit0 for Response error mask For any bit: 0: CQE will consider this SMHC error 1: CQE will not consider this SMHC error
7:1	/	/	/
0	R/W	0x0	CQE_CLR_REG_EN This field is used to control whether to clear register when disable CQE 0: Not clear register when disable CQE 1: Clear register to reset value when disable CQE

11.3.9.65 0x0480 Command Queuing Descriptor Transfer Done Register (Default Value: 0x0000_0000)

This register is used to indicate that the descriptor has been transferred from the system memory to cqe.

Offset: 0x0480			Register Name: CQDTD
Bit	Read/Write	Default/He	Description
31:0	R	0x0	CQE_DTD Descriptor Transfer Done Bit Value Description (for any bit i): 1: The descriptor of task-i has been transferred from the system memory to cqe. 0: The descriptor of task-i not transferred from the system memory to cqe.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.3.9.66 0x0484 Command Queuing Task Complete Total Register (Default Value: 0x0000_0000)

This register is used to indicate that the total number of task that has been completed by cqe.

Offset: 0x0484			Register Name: CQTCT
Bit	Read/Write	Default/He	Description
31:0	R	0x0	CQE_TCT Task Complete Total This resgister will be add 1 when a task execution is completed (with success or error) by cqe.

11.3.9.67 0x0488 Command Queuing Controller Status Register (Default Value: 0x0000_0000)

This register is used to indicate the cqe controller status.

Offset: 0x0488			Register Name: CQSTATUS
Bit	Read/Write	Default/He	Description
31:24	/	/	/
23:0	R	0x0	CQE_FSM_STATUS cqe_cnl FSM status, the format is: {2 b0, fsm_task_exe, 3 b0, fsm_task_chk, 2 b0, fsm_task_send}

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.4 NAND Flash Controller (NDFC)

The NDFC is the NAND Flash Controller which supports all NAND flash memory available in the market. New type flash can be supported by software re-configuration.

The On-the-fly error correction code (ECC) is built-in NDFC for enhancing reliability. BCH is implemented and it can detect and correct up to 80 bits error per 1024 bytes data. The on-chip ECC and parity checking circuitry of NDFC frees CPU for other tasks. The ECC function can be disabled by software.

The data can be transferred by DMA or by CPU memory-mapped IO method. The NDFC provides automatic timing control for reading or writing external Flash. The NDFC maintains the proper relativity for CLE, CE# and ALE control signal lines. There are three different kinds of modes for serial read access, mode0 is for conventional serial access, mode1 is for EDO type and the mode2 is for extension EDO type. NDFC can monitor the status of R/B# signal line. Block management and wear leveling management are implemented in software.

The NDFC has the following features:

- Supports all SLC/MLC flash and EF-NAND memory available in the market
- Software configure seed for randomize engine
- Software configure method for adaptability to a variety of system and memory types
- Supports 2CE/2RB
- Supports 8-bit Data Bus Width
- Supports 1024, 2048, 4096, 8192, 16384, 32768 bytes size per page
- Supports Conventional and EDO serial access method for serial reading Flash
- On-the-fly BCH error correction code which correcting up to 80 bits per 1024 bytes
- Corrected Error bits number information report
- ECC automatic disable function for all 0xff data
- NDFC status information is reported by its registers and interrupt is supported
- One Command FIFO
- Supports internal DMA controller based on chain-structured descriptor list
- Two 256x32-bit RAM for Pipeline Procession
- Supports SDR, ONFI DDR1.0, Toggle DDR1.0, ONFI DDR2.0 and Toggle DDR2.0 RAW NAND FLASH
- Supports the Maximum IO Rate of Mass Production 50MHz in SDR mode, the Mass Production 100MHz in DDR1.0 mode, and the Mass Production 150MHz in DDR2.0 mode
- Supports self (b)debug for NDFC debug

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.5 SPI Flash Controller (SPIF)

11.5.1 Overview

The SPI is a synchronous, serial communication interface which allows rapid data communication with fewer software interrupts. Different from SPI, this SPIF is typically designed for higher speed Flash devices and it only works at Master mode.

The SPI_Flash has the following features:

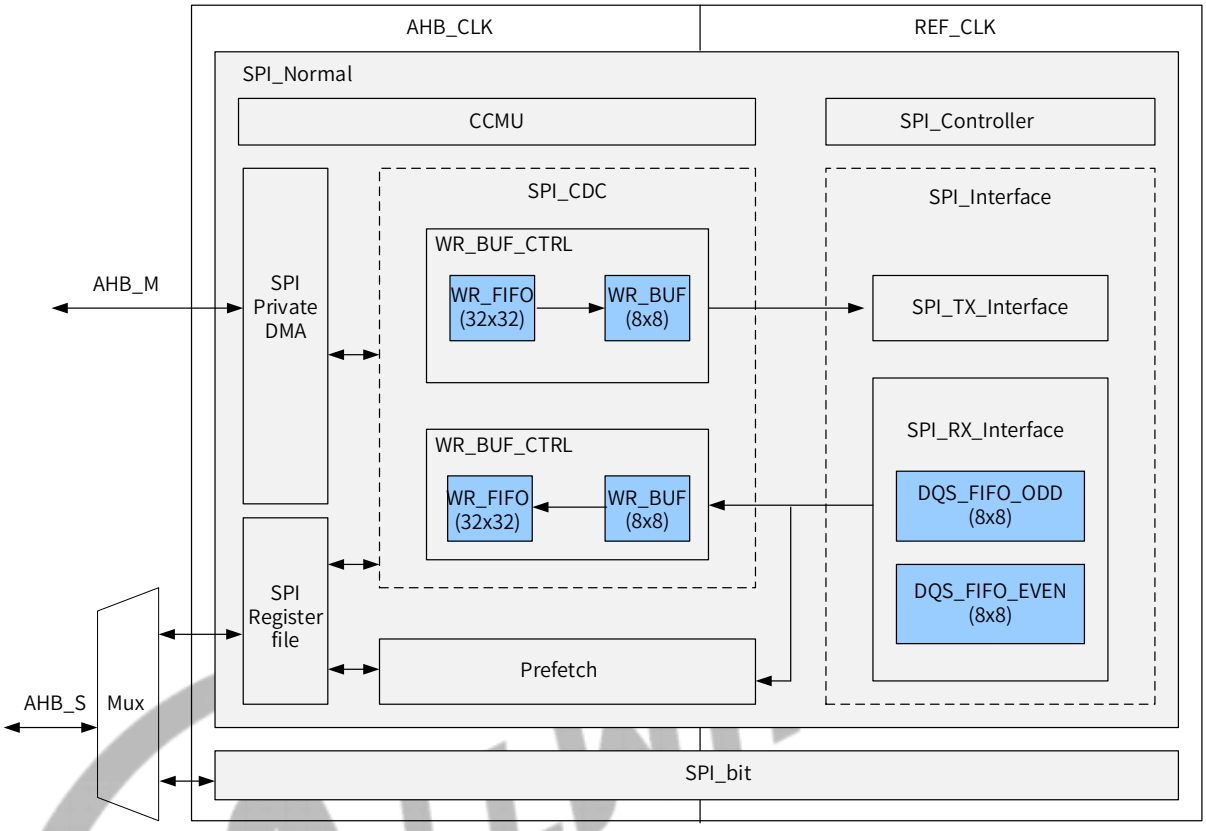
- Supports multiple SPI mode
  - Standard SPI (3-Wire/4-Wire SPI)
  - Dual-Output/Dual-Input SPI and Dual I/O SPI
  - Quad-Output/Quad-Input SPI, Quad I/O SPI, and QPI
  - Octal-Input/Octal-Output SPI, Octal I/O SPI, and OPI
  - Programmable serial data frame length: 1 bit to 32 bits
- Supports Prefetch mode of operation for executing code from FLASH memory, which significantly reduces read time
- Supports Single Transfer Rate (STR) mode and Dual Transfer Rate (DTR) mode, and DTR mode supports DQS signal
- High Speed Clock Frequency
  - 150MHz for STR Mode
  - 100MHz for DTR Mode
- Software Write Protection
  - Write protection for all/portion of memory via software
  - Top/Bottom Block protection
- Programmable delay between transactions
- Supports Mode0, Mode1, Mode2 and Mode3
- Supports control signal configuration
  - Up to one chip select to support multiple peripherals
  - Polarity and phase of the Chip Select (SPIF_CS) and SPI Clock (SPIF_CLK) are configurable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.5.2 Block Diagram

The following figure shows a block diagram of the SPI_Flash.

Figure 11-12 SPI_Flash Block Diagram



SPI_Flash contains the following sub-blocks:

Table 11-11 SPI_Flash Sub-blocks

Sub-block	Description
SPI_Register_File	It is responsible for registers configuration and CPU prefetching data through AHB1 bus.
SPI_Private_DMA	It is the private DMA for SPI, which contains AHB master and supports TXFIFO(WR_FIFO) and RXFIFO(RD_FIFO).
CCU	It is responsible for generating internal clock o_spi_clk (divided by i_spi_ref_clk) and communication clock sckt/sckr (sourcing from spi_clk). In addition, it Implements sckr delay, clock sources selection, clock gating, and scan.
SPI_CDC	SPI clock-domain-cross module, in which bit width transition finishes. (TX: 32bit->8bit; RX: 8bit->32bit) WR_BUF: Cache the write SPI data of AHB, and write them to WR_FIFO. RD_BUF: Cache the read SPI data of RD_FIFO to AHB. WR_FIFO: SPI write data FIFO (SRAM 32x32) RD_FIFO: SPI read data FIFO (SRAM 32x32) in the normal mode.
Prefetch	When prefetching instructions, the CPU can directly access SPI through this module.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Sub-block	Description
SPI_Controller	SPI controlling center. It generates TX/RX controlling signal in the course of SPI communication.
SPI_Interface	Standard SPI interface. It is responsible for receiving and transmitting data with Devices.
SPI_bit	the processing module in SPI 3-wire mode.

11.5.3 Clock Sources

The following table describes the clock sources of SPIF. For clock setting, configurations, and gating information, refer to the section Clock Controller Unit (CCU).

Module	Clock Signal	Description
SPIF	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.
	PERI0_400M	Its frequency is 400 MHz by default.
	PERI0_300M	Its frequency is 300 MHz by default.
	PERI1_400M	Its frequency is 400 MHz by default.
	PERI1_300M	Its frequency is 300 MHz by default.
	PERI0_160M	Its frequency is 160 MHz by default.
	PERI1_160M	Its frequency is 160 MHz by default.
	DCXO	The external high-frequency crystal oscillator. Its frequency is 26 MHz.

11.5.4 External Signals

The following table describes the external signals of SPI_Flash. When using SPI_Flash, the corresponding PADs are selected as SPI_Flash function via section GPIO.

Table 11-12 SPI_Flash External Signals

Signal Name	Description	Type
SPIF0-MOSI	SPI Master Data Out, Slave Data In	I/O
SPIF0-CS0	SPI Peripheral Chip Select Signal, Low Active	O
SPIF0-MISO	SPI Master Data In, Slave Data Out	I/O
SPIF0-DQS	Data Strobe Signal	I
SPIF0-D[7:4]	SPI Master Mode Data Input in octal mode. In single/dual/quad mode, this port should stay low.	I/O
SPIF0-CLK	SPI Master Mode Clock Output	O
SPIF0-WP/SPIF0-D2	SPI Write Protect, Low Active	I/O
SPIF0-HOLD/SPIF0-D3	SPI Hold Signal	I/O

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

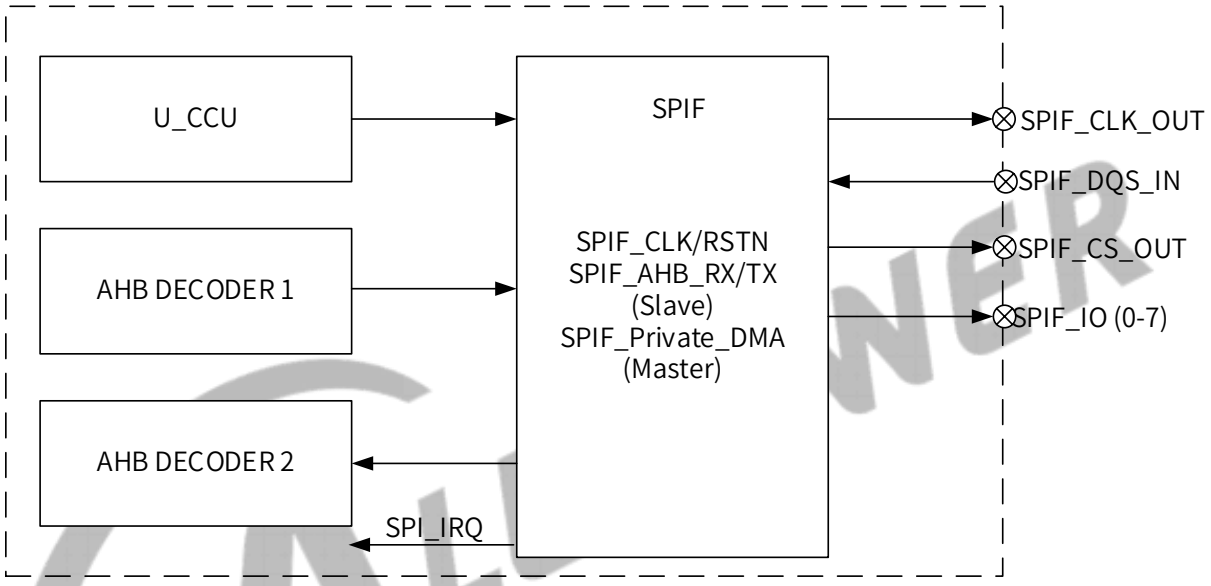
11.5.5 Functional Description

11.5.5.1 Typical Application

The SPI controller running in Master device. SPIF_CLK is generated and transmitted to external device, and data from the TX FIFO is transmitted on the MOSI pin, the data from slave is received on the MISO pin and sent to RX FIFO. Chip Select(SPIF_CS) is active low signal. SPIF_CS must be set low before data are transmitted or received.

The circuit connection between the SPI Device must flow the following figure.

Figure 11-13 Typical Application



11.5.5.2 SPI_Flash Support List

Table 11-13 SPI_Flash Support List

SPI mode		Specification Items					
		STR	DTR	DTR-RX-DQS	SCK_MODE	Address Size	Remark
Bit Mode	3-wire 4-wire	⋮	×	×	mode0	×	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

SPI mode		Specification Items					
		STR	DTR	DTR-RX-DQS	SCK_MODE	Address Size	Remark
Standard SPI	1-1-1-1	¦	¦	¦	• mode 0/1/2/3 (STR) • mode0 (DTR)	24bit/32 bit	• 1-1-1-1: cmd-addr-mode-data. • mode is optional and can be turned off.
Dual SPI	1-1-1-2	¦	¦	¦			/
	1-1-2-2						
	1-2-2-2						
	2-2-2-2						
Quad SPI	1-1-1-4	¦	¦	¦			/
	1-1-4-4						
	1-4-4-4						
	4-4-4-4						
Octal SPI	1-1-1-8	¦	¦	¦			8-wire DTR only supports the following: ADDR-24+MODE ADDR-32
	1-1-8-8						
	1-8-8-8						
	8-8-8-8						

11.5.5.3 SPI Clock

The SPI includes two clock domains: ahb_clk and spi_clk.

- ahb_clk supports parameter analysis (ahb_register) and DMA.
- spi_clk supports the communication between cross-domain clock, main control unit, and SPI-TX/RX and external devices.

The SPI_CMU divides the external SPI reference clock to get the SPI internal clock, which will be handled to get the sckt/sckr in accordance with the clock properties configured by the CPU. Then, the sckt/sckr will be used by the SPI_TX_INTERFACE/SPI_RX_INTERFACE.

The clock properties include:

- SPI Clock Mode
- DQS EN
- STR or DTR

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

SPI Clock Mode

The SPI Flash supports 4 different modes for data transfer. Software can select one of the four modes in which the SPI works by setting the bit5(SPI_CPOL) and bit4(SPI_CPHA) of SPI Global Control Register[0x0004].

The SPI_CPOL defines the signal polarity when SPIF_CLK is in the idle state. The SPIF_CLK is high level when POL is '1 'and it is low level when POL is '0'. The SPI_CPHA decides whether the leading edge of SPIF_CLK is used for setup or sample data. The leading edge is used for setup data when PHA is '1' and for sample data when PHA is '0'. The four kind of modes are listed Table:

Table 11-14 SPI Flash Modes with Clock Polarity and Phase

SPI Mode	POL	PHA	Leading Edge	Trailing Edge
0	0	0	Rising, Sample	Falling, Setup
1	0	1	Rising, Setup	Falling, Sample
2	1	0	Falling, Sample	Rising, Setup
3	1	1	Failing, Setup	Rising, Sample

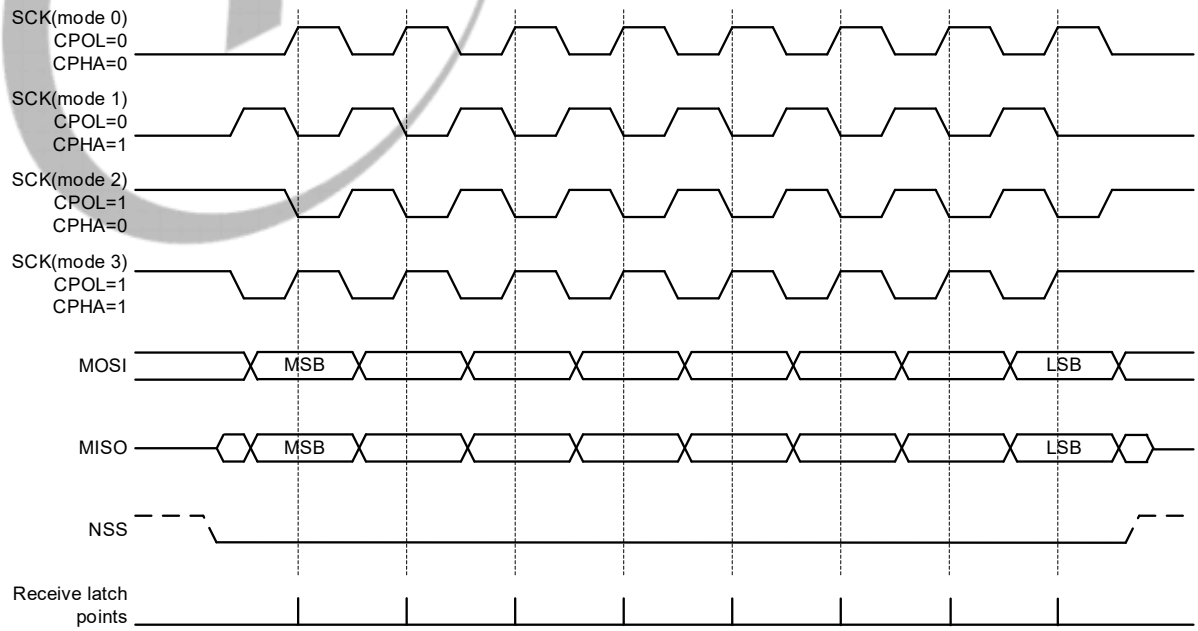
During Phase 0, Polarity 0 and Phase 1, Polarity 1 operations, output data changes on the falling edge and input data is shifted in on the rising edge.

During Phase 1, Polarity 0 and Phase 0, Polarity 1 operations, output data changes on the rising edges and is shifted in on falling edges.

The Bit Mode only supports Phase 0, Polarity 0 operation; the most significant bit (MSB) of data is transmitted first which is not configurable.

The following figure describe four waveforms for SPIF_CLK.

Figure 11-14 SPI Transfer Mode



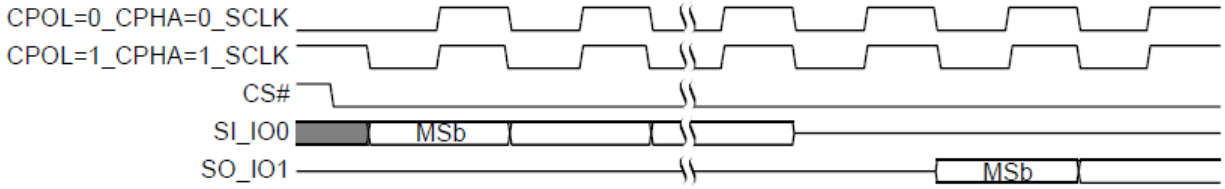
For MSB first

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

STR & DTR

In the SPI mode 0 and mode 3, the input data of devices will be latched at the rising edge of SCK, and the output data can be used at the falling edge of SCK.

Figure 11-15 SPI STR Transfer



As with the STR command, the instruction bit is latched at the rising edge of the clock in the DTR command. However, after that, the address and input data are latched at the dual edge. After the instruction bit is latched at the falling edge of SCK, the first address bit will be latched at the next rising edge of SCK. The first output data bit will be sent at the falling edge of the last access latency period.

As with the STR command, the SCK period is obtained by measuring the cycle between two adjacent SCK falling edges. In the mode 0, the SCK is already at a low level when some command starts to be executed, thus the first SCK period during the command execution indicates the cycle from the falling edge of CS# to the first falling edge of SCK.

Figure 11-16 SPI DTR Transfer Example, 1-4-4

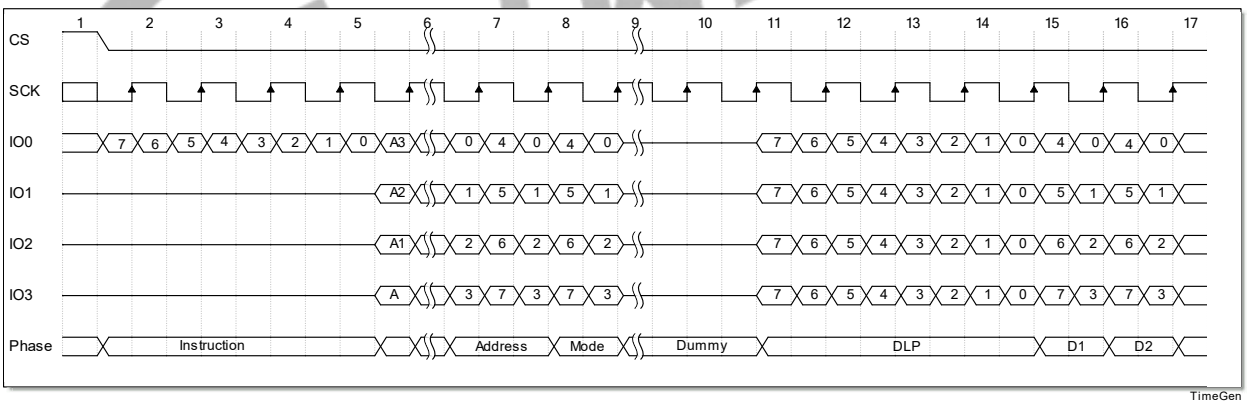
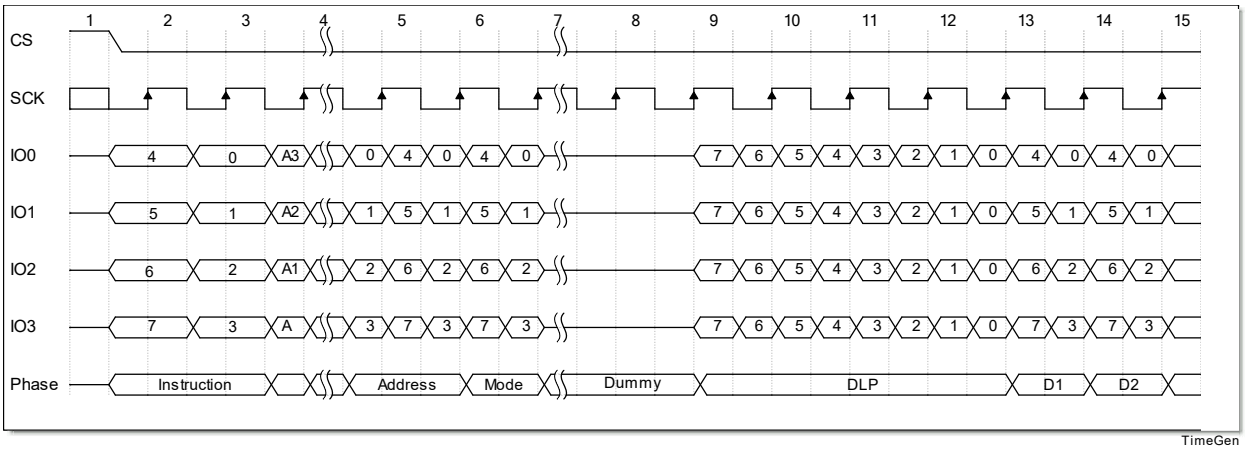


Figure 11-17 SPI DTR Transfer Example, 4-4-4

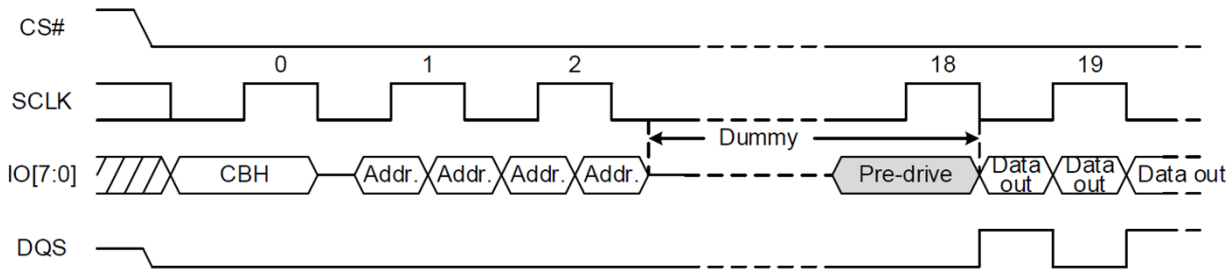


Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

DQS

DQS signal indicates input/output data valid for DTR modes and is required to support high-speed data. When data strobe function is enabled, DQS signal will be driven to ground once CS# goes LOW till the device is driving output data, in which case DQS toggles to synchronize data output. When data strobe function is not enabled, DQS signal will not be driven.

Figure 11-18 SPI DTR Transfer with DQS Input Clock Signal



11.5.5.4 SPI Chip Select Signal

The SPIF supports one chip select signal, which can be activated by the SPI_CS_SEL (bit[7:6]) of SPI_GLOBAL_CTRL. The polarities of CS signals can be configured by the SPI_CS_POL (bit[5]) of SPI_GLOBAL_CTRL.

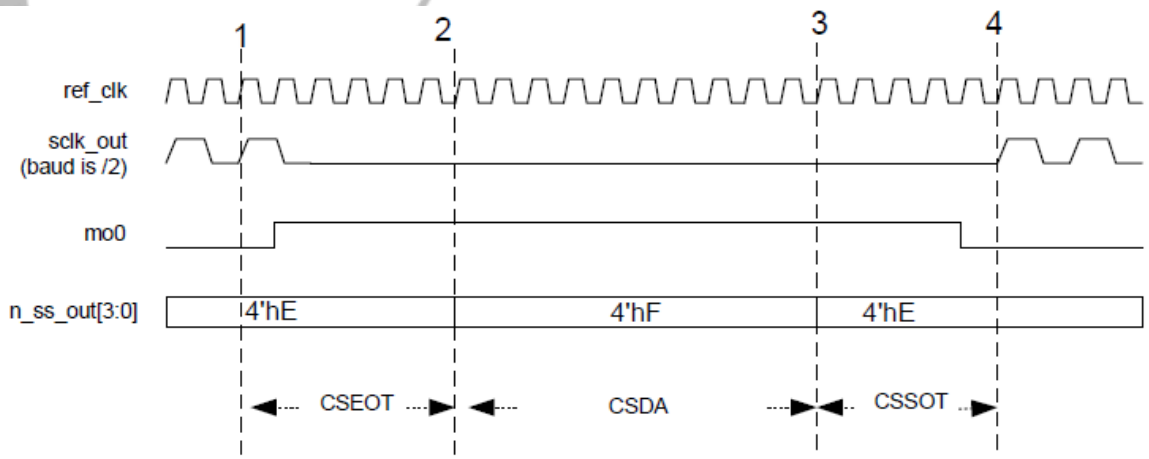
The various intervals of CS signals can be configured by SPI_CS_DELAY. The specific configuration steps are as follows.

Step 1 Delay CSSOT and output the effective data after CS is enabled.

Step 2 Delay CSEOT at the rising edge of last valid data, and disable CS.

Step 3 After the CS is disabled, the interval between enabling CS and disabling CS is CSDA.

Figure 11-19 SPI CS Select Timing Relation



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.5.5.5 SPI Transfer Mode

SPI supports multiple transfer modes such as SPI Bit Mode, SPI Standard Mode, SPI Dual Mode, SPI Quad Mode, and SPI Octal Mode. Their main differences lie in the number of wires. Even in the same transfer mode, the subdivision modes will be further derived based on the number of wires used to data transfer. The number of data lines used by Command-Address-Data is specified on the subdivision pattern heading in the manner of X-X-X. For example, one Data line for Commend, two for Address, and two for data, are identified as (1-2-2).

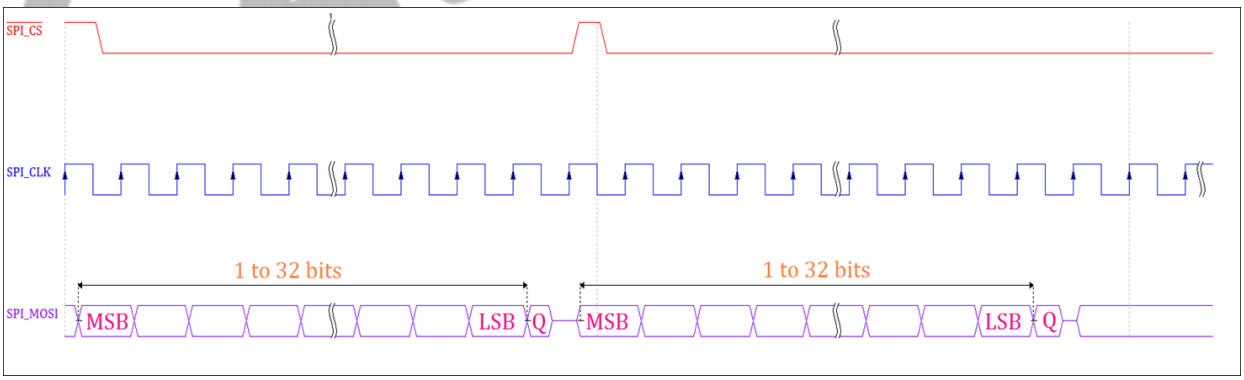
SPI Bit Mode (3-Wire/4-Wire)

For some specific scenarios, the devices such as the sensor take the SPI interfaces as the communication protocol. Generally, their data volume is relatively small, and some devices support three wires, so the SPI Bit Mode is added, and 3-wire mode and 4-wire mode are subdivided, which includes SPIF_CS, SPIF_CLK, and 1/2 data line. The transmission length ranges from 1-32bit.

The 4-Wire Mode is selected when the Work Mode Select(bit[1:0]) is equal to 0x3 in the SPI Bit-Aligned Transfer Configure Register. In SPI 4-Wire Mode, the input data and output data use the independent two data lines. The MISO is used for inputting data, and the MOSI is used for outputting data.

The SPI 3-Wire Mode is only valid when the SPI controller works as Master Device, and selected when the Work Mode Select(bit[1:0]) is equal to 0x2 in the SPI Bit-Aligned Transfer Configure Register. In the 3-Wire mode, the input data and the output data use the same single data line. The following figure describe this mode.

Figure 11-20 SPI 3-Wire Mode



SPI Standard Mode (4-Wire)

Signal Wire: CS#, SCK, IO0, and IO1.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 11-21 SPI CMD with Single IO

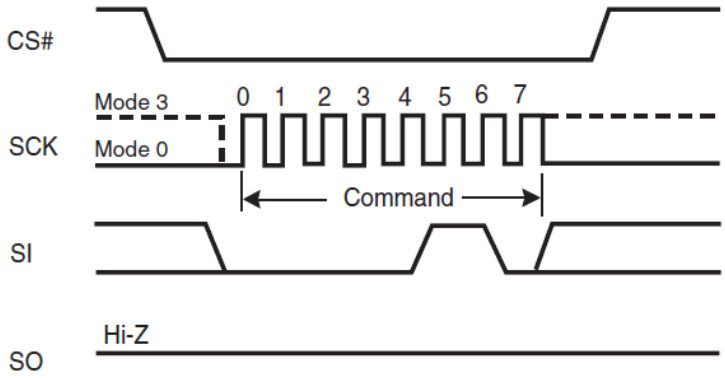


Figure 11-22 SPI Write CMD and DATA with One Wire

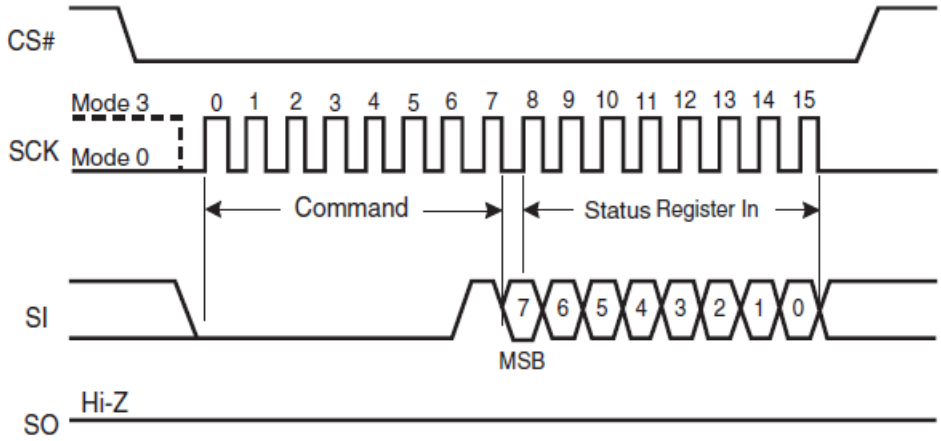
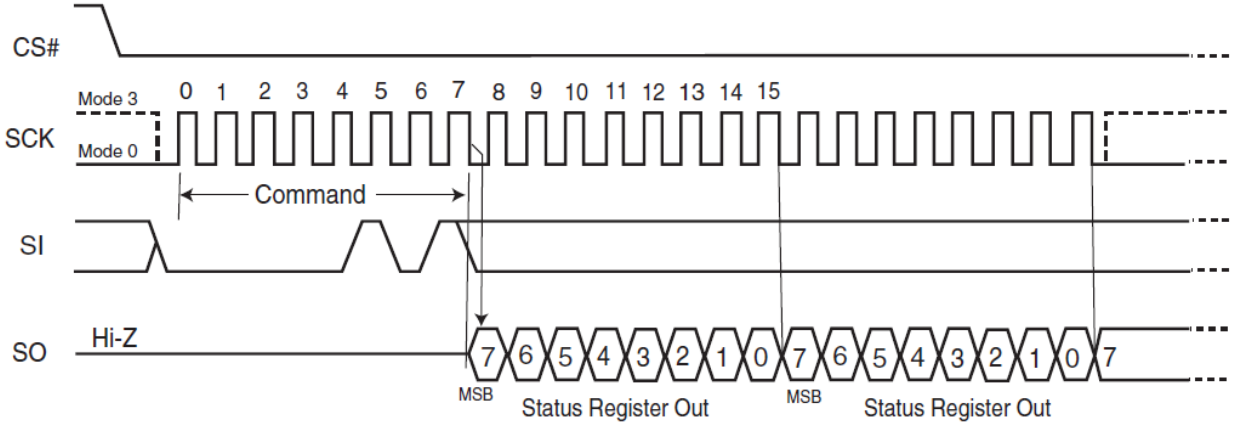
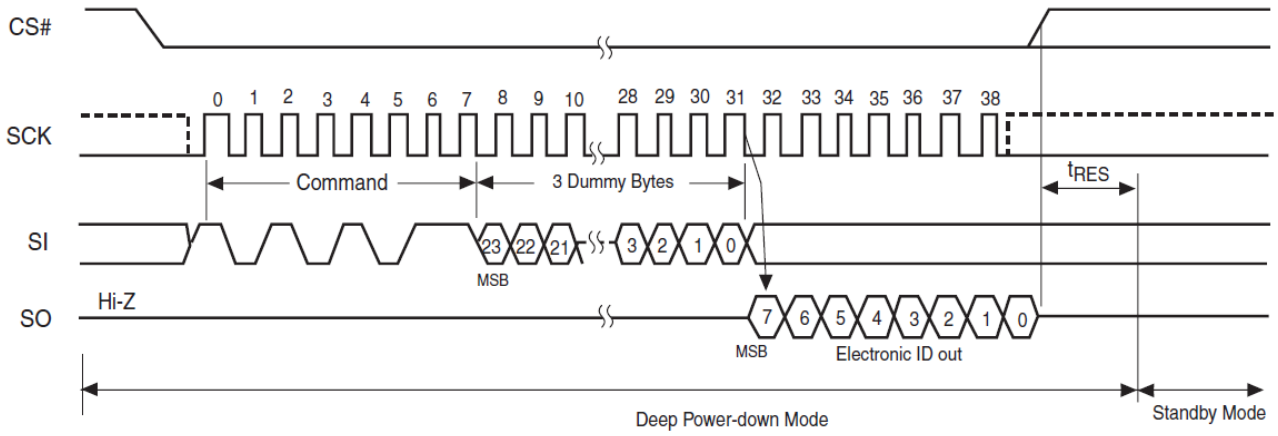


Figure 11-23 SPI Write CMD and Read DATA with One Wire (No Dummy)



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 11-24 SPI Write CMD and Read DATA with One Wire (with Dummy)



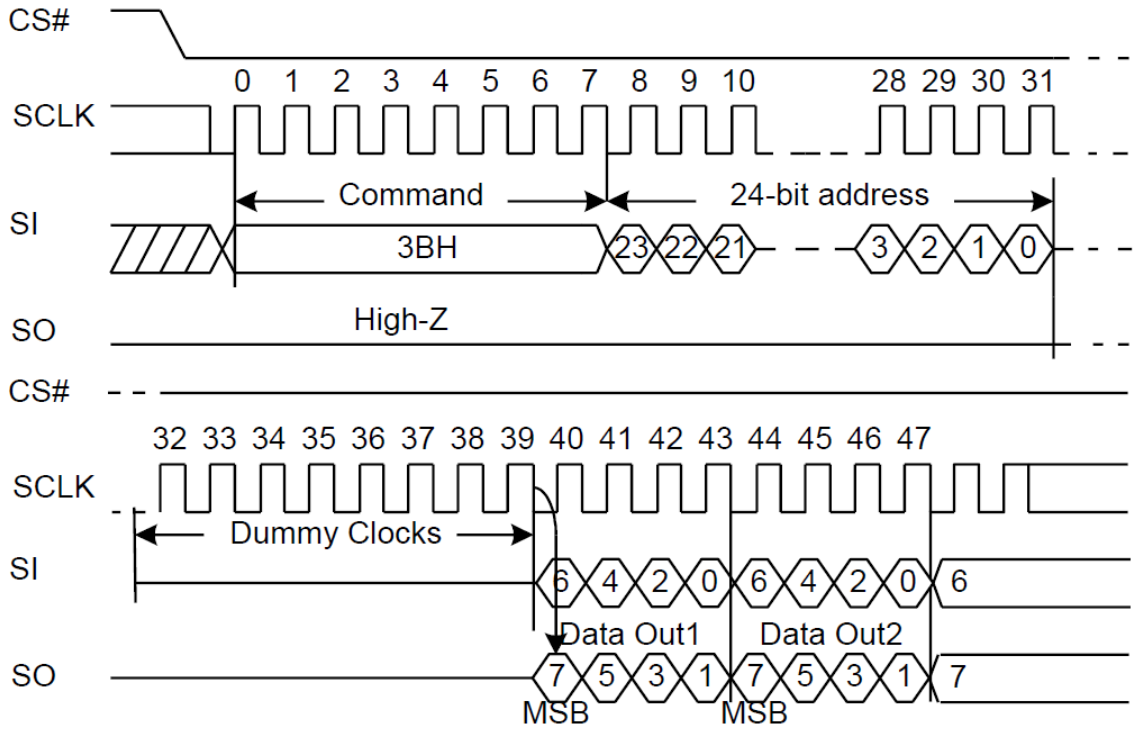
SPI Dual Mode

Using the dual mode allows data to be transferred to or from the device at two times the rate of standard single mode SPI devices. Data can be read at a faster speed using two data bits (MOSI and MISO) at a time. The following describe the Dual Input/Dual Output SPI (1-1-2), the Dual IO SPI (1-2-2), and the (2-2-2) SPI Mode.

- SPI Dual Input/dual Output Mode (1-1-2)

In the dual Input/dual Output SPI, the command, address, and the dummy bytes are output in the unit of a single bit in serial mode through SPIF_MOSI line. Only the data bytes are output (write) and input (read) in unit of dual bits through the SPIF_MOSI and SPIF_MISO.

Figure 11-25 SPI Dual Input/Dual Output Mode 1-1-2

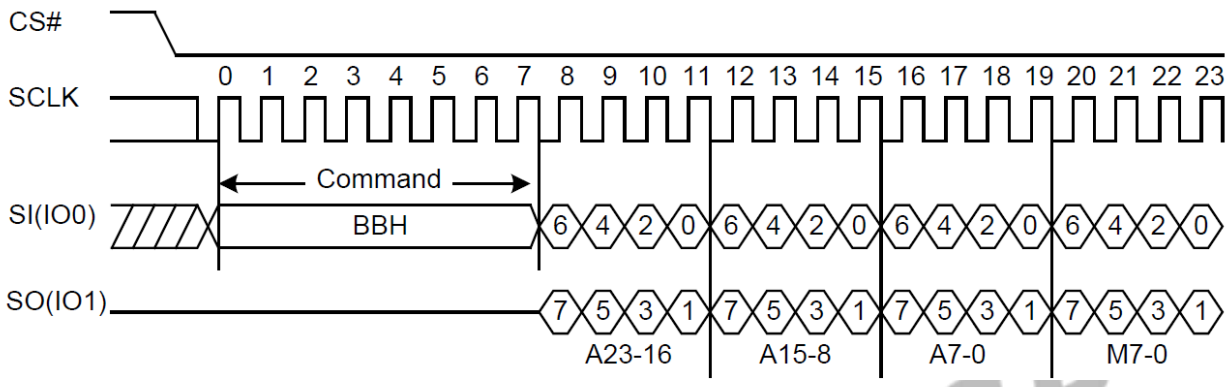


Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- SPI Dual IO Mode (1-2-2)

In the Dual IO SPI, only the command bytes are output in the unit of a single bit in serial mode through SPIF_MOSI line. The address bytes and the dummy bytes are output in the unit of dual bits through the SPIF_MOSI and SPIF_MISO. And the data bytes are output (write) and input (read) in the unit of dual bits through the SPIF_MOSI and SPIF_MISO.

Figure 11-26 SPI Dual Input/Dual Output Mode (1-2-2)



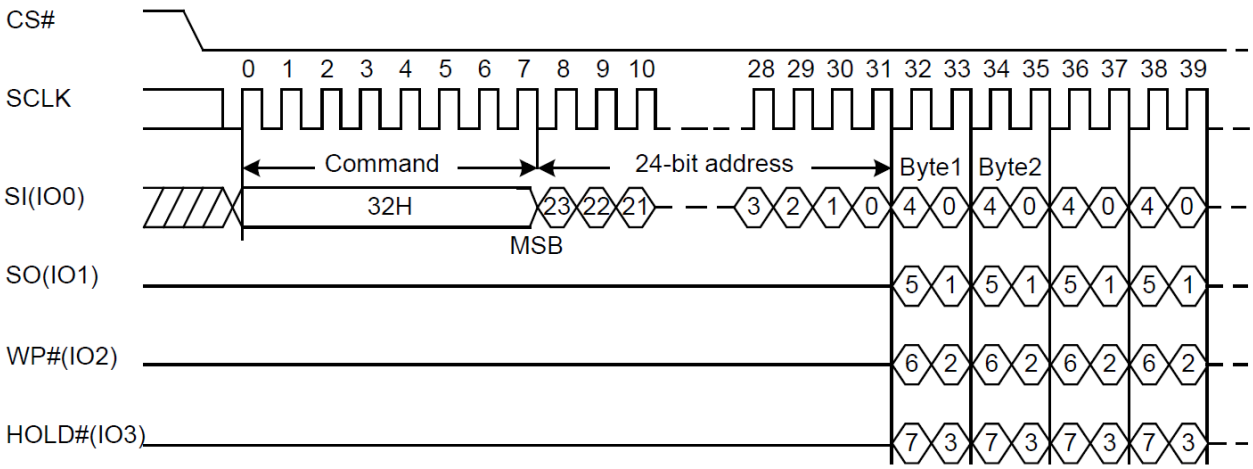
SPI Quad Mode

Using the quad mode allows data to be transferred to or from the device at 4 times the rate of standard single mode SPI devices, data can be read at fast speed using four data bits (MOSI, MISO, IO2(WP#) and IO3(HOLD#)) at the same time. The following describe the Quad Input/Quad Output SPI (1-1-4), 1-4-4 mode, and 4-4-4 mode.

- Quad Input/Quad Output SPI (1-1-4)

In the Quad Input/Quad Output SPI, the command, address, and the dummy bytes are output in unit of a single bit in serial mode through SPIF_MOSI line. Only the data bytes are output (write) and input(read) in unit of quad bits through the SPIF_MOSI, SPIF_MISO, SPIF_WP# and SPIF_HOLD#.

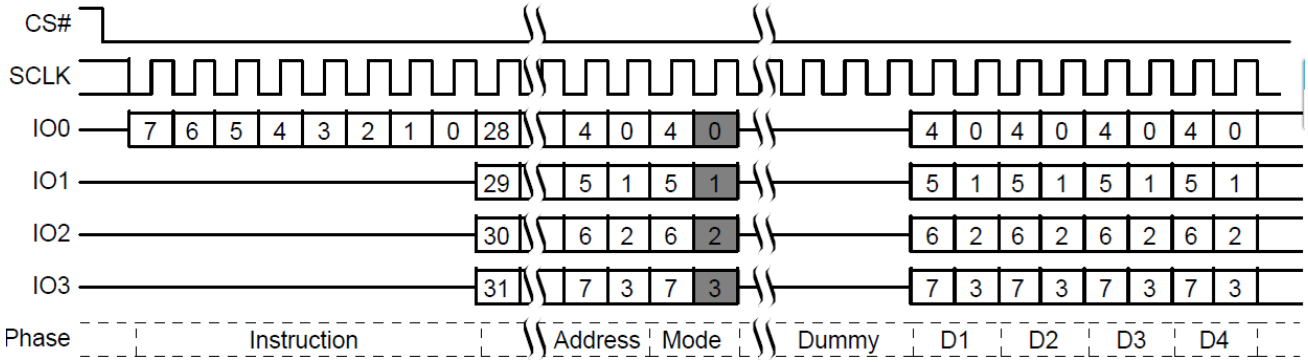
Figure 11-27 SPI Quad Input/Quad Output Mode (1-1-4)



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

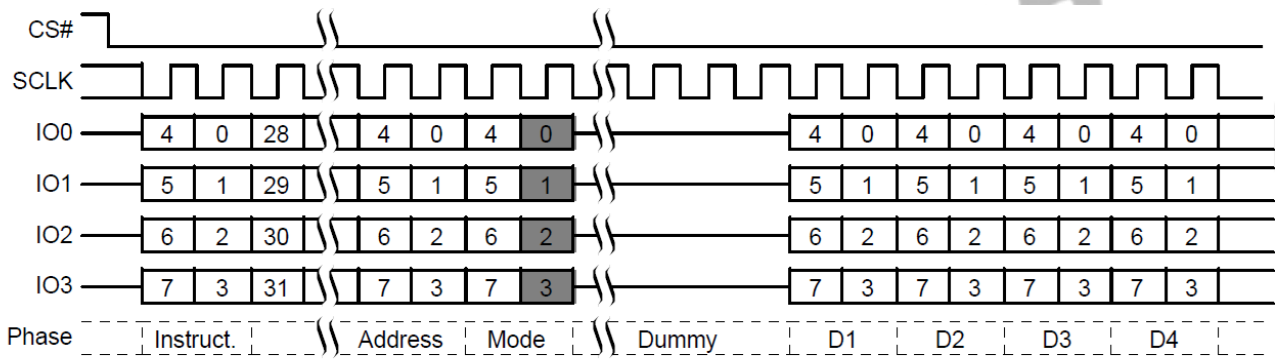
- 1-4-4 Mode

Figure 11-28 SPI Quad Input/Quad Output Mode (1-4-4)



- 4-4-4 Mode

Figure 11-29 SPI Quad Input/Quad Output Mode (4-4-4)

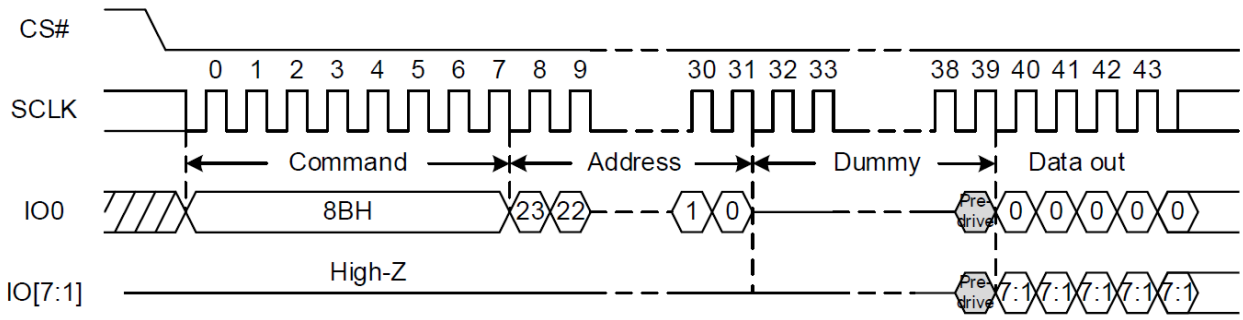


SPI Octal Mode

The Octal SPI Mode allow data to be transferred to or from the device at eight times the rate of the standard SPI. When using the Octal SPI, there are 8 data wires.

- SPI Octal 1-1-8

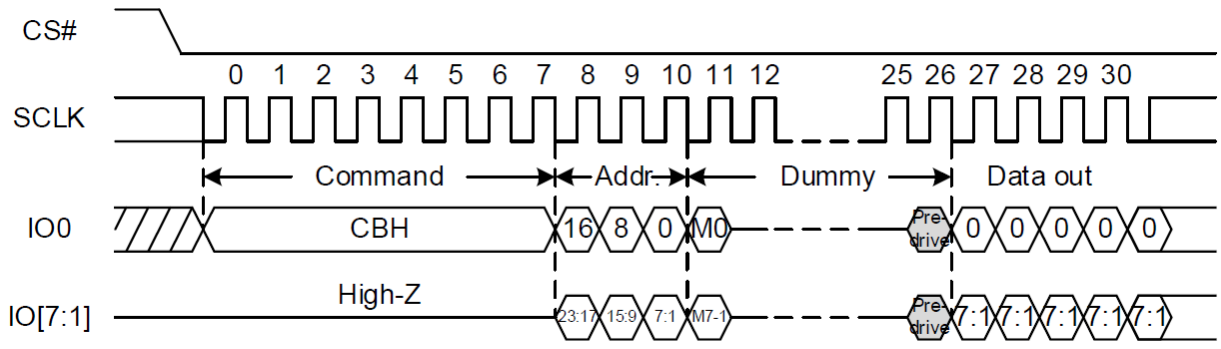
Figure 11-30 SPI Octal Input/Octal Output Mode (1-1-8)



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

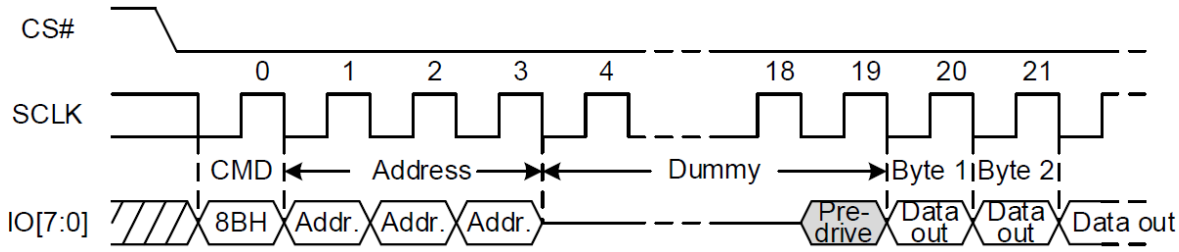
- SPI Octal 1-8-8

Figure 11-31 SPI Octal Input/Octal Output Mode (1-8-8)



- SPI Octal 8-8-8

Figure 11-32 SPI Octal Input/Octal Output Mode (8-8-8)



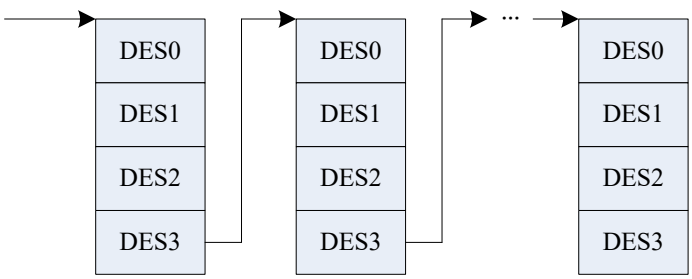
11.5.5.6 Prefetch Mode

If the CPU wants to directly access Flash, the prefetch mode is needed to improve efficiency. In the prefetch mode, the CPU continues fetching instructions from flash and cache them (The maximum cache size is 128 Bytes.). Then HREADY_I should be controlled by handshake to send back the instructions to CPU through AHB.

11.5.5.7 SPI Flash Private DMA

The private DMA adopts the chained descriptor structure. The address and size of the first descriptor are configured by registers. After getting the first descriptor, the hardware will obtain the data from the address recorded in the descriptors. When the current transfer finishes, the hardware will continue to obtain descriptors based on the address of the next descriptor given by the previous descriptor until the terminal character is found. Then, a DMA transfer ends.

Figure 11-33 Descriptor Structure Diagram



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

The private DMA also supports SPI parameter configuration. The SPI transfer can be configured by the parameters of the descriptors 4-7.

Descriptor0 Definition

Bits	Descriptor
31:7	Reserved
6:4	HBURST_TYPE indicate hburst len 000: SINGLE, hburst_len = 1 011: INCR4, hburst_len = 4 101: INCR8, hburst_len = 8 111: INCR16, hburst_len = 16
3:2	/
1	DMA_DIR DMA Write Process or Read Process 0: Read 1: Write
0	DMA_FINISH_FLAG DMA Finish Flag

Descriptor1 Definition

Bits	Descriptor
31:24	DMA_BLK_LEN DMA Block Len Mode 0: 8Byte 1: 16Byte 2: 32Byte 3: 64Byte Recommended Configuration: The data volume of DMA_BLK_LEN is greater than or equal to that of HBURST_TYPE.
23:17	/
16:0	DMA_DATA_LEN Indicate the data byte number of current DMA operation.

Descriptor2 Definition

Bits	Descriptor
31:0	DMA_Buffer_ SADDR The real address is as below The word address is needed. Namely, the byte address abandons the low 2 bits.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Descriptor3 Definition

Bits	Descriptor
31:0	NEXT_DESCRIPTOR_ADDR These bits indicate the pointer to the physical memory where the next descriptor is present, which are word (4byte) address. Namely, the byte address abandons the low 2 bits.

Descriptor4 Definition

Bit	Description
31:30	/
29	CMD_DTR CMD DTR Control 1: CMD DTR 0: CMD not DTR CAUTION: When CMD DTR, DTR must be on and CMD2 is required.
28	COMMAND_TRANS_EN Set to 1 if command data need trans to device SPI Controller FSM Phase Enable 1: Enable 0: Disable
27:25	/
24	ADDRESS_TRANS_EN Set to 1 if address need trans to device SPI Controller FSM Phase Enable 1: Enable 0: Disable
23:21	/
20	MODE_BIT_TRANS_EN Set to 1 if Mode bit need trans after address SPI Controller FSM Phase Enable 1: Enable 0: Disable
19:17	/
16	DUMMY_BIT_TRANS_EN Dummy Bit State Enable SPI Controller FSM Phase Enable 1: Enable 0: Disable
15:13	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Description
12	TX_DATA_EN Set to 1 if Data Need Trans SPI Controller FSM Phase Enable 1: Enable 0: Disable
11:9	/
8	RX_DATA_EN Set to 1 if Data Need Receive SPI Controller FSM Phase Enable 1: Enable 0: Disable
7:0	/

Descriptor5 Definition

Bit	Description
31:0	ADDR_OPCODE Address Content Trans Through SPI

Descriptor6 Definition

This register should be setup while the controller is idle.

Bit	Description
31:24	CMD_OPCODE Command Content Trans Through SPI
23:16	MODE_OPCODE Mode Content Trans Through SPI
15:8	CMD_OPCODE2 Command2 Content Trans Through SPI
7:6	CMD_TRANS_TYPE Command Transfer Type 00: Command can be Shifted to the device on DQ0 01: Command can be Shifted to the device on DQ0 and DQ1 10: Command can be Shifted to the device on DQ0- DQ3 11: Command can be Shifted to the device on DQ0-DQ7
5:4	ADDR_TRANS_TYPE Address Transfer Type 00: Address can be Shifted to the device on DQ0 01: Address can be Shifted to the device on DQ0 and DQ1 10: Address can be Shifted to the device on DQ0- DQ3 11: Address can be Shifted to the device on DQ0-DQ7

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Description
3:2	MODE_BIT_TRANS_TYPE Mode Bit Transfer Type 00: Mode Bit can be Shifted to the device on DQ0 01: Mode Bit can be Shifted to the device on DQ0 and DQ1 10: Mode Bit can be Shifted to the device on DQ0- DQ3 11: Mode Bit can be Shifted to the device on DQ0-DQ7
1:0	DATA_TRANS_TYPE Data Transfer Type 00: Opcode can be Shifted to the device on DQ0 only 01: Opcode can be Shifted to the device on DQ0 and DQ1 only 10: Opcode can be Shifted to the device on DQ0- DQ3 11: Opcode can be Shifted to the device on DQ0-DQ7

Descriptor7 Definition

Bit	Description
31	DATA_TRANS_NUM[16]
30:29	/
28	SPI_NORMAL_EN if dma config spi, this bit start SPI FSM.
27	/
26	CMD_LEN 0: 1byte 1: 2byte
25:24	ADDR_SIZE_MODE Address Size Mode 00: Address Size 8 bit. 01: Address Size 16 bit. 10: Address Size 24 bit. 11: Address Size 32 bit.
23:16	DUMMY_TRANS_NUM Number of Dummy Cycles A value of 0 = 1 Cycle A value of 1 = 1 Cycle ... A value of N = N Cycle

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Description
15:0	DATA_TRANS_NUM Num of Data Trans Through SPI(Byte) 0: Non-Write. 1: Write 1 Byte. 2: Write 2 Bytes. 3: Write 3 Bytes. ..... 65535: Write 65535 Bytes. *Note: These Bits indicate the number of data bytes in a CHIP SELECT period. Notice the difference between DATA_TRANS_NUM here and DMA_DATA_LEN in Descriptor1.*

11.5.6 Programming Guidelines

11.5.6.1 DMA Transfer

The software operation of the SPI DMA transfer is divided into 5 steps as follows.

a) System Setup

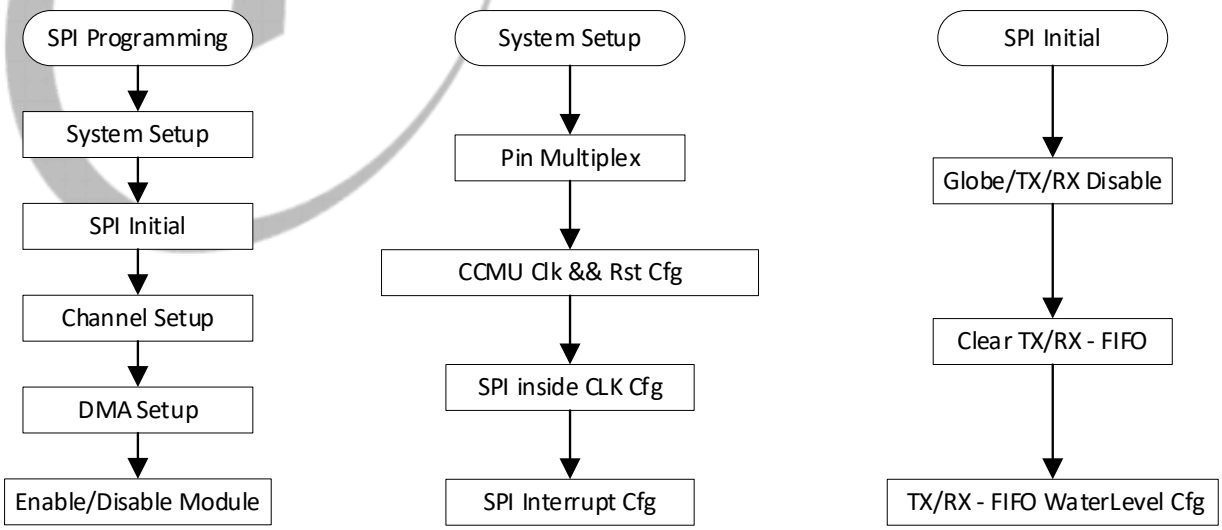
b) SPI Initialization

c) Channel Setup

d) DMA Setup

e) Enable SPI

Figure 11-34 SPI Programming Flow



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

System Setup

Configure SPI Pin

Program the GPIO to configure the SPI PIN.

Configure SPI Clock and Reset

Configure SPI ref clock, AHB Clock, De-assert SPI ref Reset, and AHB reset in the section CCU.

Configure SPI Internal Clock

Step 1 Configure clock source (SPI_TIMING_CFG[0x000C])

- STR Mode

  Write 0 to the CLK_SPI_SRC_SEL bit (bit [24]), the CLK_SCK_SRC_SEL bit (bit [25]) bit, and the CLK_SCKOUT_SRC_SEL bit (bit [26]) bit.

- DTR Mode

  Write 0 to the CLK_SPI_SRC_SEL bit (bit [24]) and the CLK_SCK_SRC_SEL bit (bit [25]) bit.

  Write 1 to the CLK_SCKOUT_SRC_SEL bit (bit [26]) bit.

NOTE

When the value of the CLK_SCKOUT_SRC_SEL (bit [26]) bit is 1, the real output clock frequency of SPIF-CLK signal is the SPIFC clock frequency divided by 2.

Step 2 Generate the sckr of SPI data receiving

- Configure SCKR delay mode (SPI_TIMING_CFG[0x000C]).

  SCKR_DLY_MODE_SEL (bit [20]): Select delay mode. Writing 0 is the digital delay, and writing 1 is the digital and analog delay.

- Configure the digital delay of SCKR

  SPI_TIMING_CFG[0x000C], DIGITAL_SCKR_DELAY_CFG (bit[18:16]): digital delay volume. The step length is 0.5 clock.

- Configure the analog delay of SCKR

  SPI_TIMING_CFG[0x000C], ANALOG_SAMP_DL_SW_VALUE (bit[5:0])

Step 3 Generate SPI output clock

- Select SPI working mode (SPI_MODE). Refer to the section SPI Clock Mode for more details.

- Configure SPI_GLOBAL_CTRL[0x0004]:

  SPI_CPOL (bit [5]): Clock Polarity

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

SPI_CPHA (bit [4]): Clock Phase

- DTR switch SPI_GLOBAL_CTRL[0x0004]

  DTR_EN (bit [16]): It is closed by default. When it is closed, the output clock frequency is same to that of SCKR and SCKT; when it is open, the output clock frequency is half that of SCKR and SCKT.

Configure SPI Interrupt

Set the SPI_INT_EN (0x0014[31:0]) as 0.

SPI Initialization

Step 1 Disable the SPI_GLOBAL_CTRL by writing 0 to SPI_NMODE_EN(bit [2]), SPI_PMODE_EN(bit[3]), SPI_CPU_MODE_EN(bit[20]), and SPI_AUTO_READ_STATUS_MODE_EN(bit[21]).

Step 2 Reset TX/RX FIFO (SPI_GLOBAL_CTRL_ADD[0x0008])

Reset the CDC-BUF/FIFO of TX channel: Write 1 to CDC_WF_SRST to reset the WR_BUFF and WR_FIFO in SPI_WR_BUF_CTRL and the SWF in SPI_TX_INTERFACE.

Reset the CDC-BUF/FIFO of RX channel: Write 1 to CDC_RF_SRST.

Step 3 Configure the water level of FIFO in SPI_CDC_FIFO_TRIG_LEVEL.

Channel Setup

Select SPI Channel Parameter Resource

- SPI channel parameter resources:
  - CPU is configured by AHB.
  - The private DMA fetches descriptors and parses the descriptors 4-7.
- Configure SPI channel parameter sources: SPI_GLOBAL_CTRL[0x0004] and SPI_CFG_MODE(bit[0])
  - 0: Source from CPU
  - 1: Source from DMA descriptor

NOTE

If the parameters source from CPU, finish the configuration in reference to all the guidelines in the section Channel Setup. If the parameters source from DMA, skip the steps after CS Delay Configuration in this section to initiate the DMA. For the descriptions of DMA descriptors, refer to the section SPI Flash Private DMA.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

SPI Interface Public Configuration

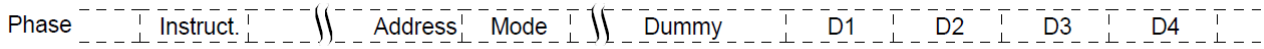
Step 1 CS Delay Configuration: SPI_CS_DELAY[0x001C]

- CSDA (bit [23:16]): The intervals of two adjacent CS enable is recommended to be no less than 6sclk. The actual value is CSDA+1.
- CSEOT (bit [15:8]): After the SCLK_OUT is invalid, the CS signal will be de-asserted after CSEOT SCLK. The minimum interval is 1sclk. The actual value is CSEOT+1.
- CSSOT (bit [7:0]): After the SCLK_OUT is valid, the CS signal will be asserted after CSSOT SCLK. The minimum interval is 1sclk. The actual value is CSSOT+1.

Step 2 Activate SPI Trans Phase SPI_TRANS_PHA_CFG.

- In a transmission of the SPI interface, the transferring content of I/O line is as follows. Enable the corresponding Trans Phase based on the content to be transferred by writing 1 to the COMMAND_TRANS_EN (bit [28]), ADDRESS_TRANS_EN (bit [24]), MODE_BIT_TRANS_EN (bit [20]), DUMMY_BIT_TRANS_EN (bit [16]), TX_DATA_EN (bit [12]), and RX_DATA_EN (bit [8]).

Figure 11-35 SPI Transfer Phase Flow Diagram



NOTE

RX_DATA_EN and TX_DATA_EN cannot be activated at the same time.

Step 3 Configure the number of I/O used by TransPhase by setting the CMD_TRANS_TYPE (bit [13:12]), ADDR_TRANS_TYPE (bit [9:8]), MODE_BIT_TRANS_TYPE (bit [5:4]), and DATA_BIT_TRANS_TYPE (bit [1:0]) in the (SPI_TRANS_CFG2.

Step 4 Configure the transferring volume of TransPhase in the SPI_TRANS_NUM[0x002C].

SPI Interface Normal Read and Write

Configure the contents of all TransPhase by setting the following bits.

Step 1 ADDR: SPI_TRANS_CFG1[0x0024], ADDR_OPCODE (bit [31:0])

Step 2 CMD: SPI_TRANS_CFG2[0x0028], CMD_OPCODE (bit[31:24])

Step 3 CMD2: SPI_TRANS_CFG2[0x0028], CMD_OPCODE2 (bit[15:8])

Step 4 MODE: SPI_TRANS_CFG2[0x0028], CMD_OPCODE (bit[23:16])

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

SPI Interface Prefetch Mode

Step 1 Configure whether to use address mapping mode by setting the PREFETCH_ADDR_MAP_MODE (bit[1]) in the SPI_GLOBAL_CTRL.

Step 2 Configure the contents of all TransPhase by setting the following bits.

- CMD: SPI_TRANS_CFG2[0x0028], CMD_OPCODE (bit[31:24])
- MODE: SPI_TRANS_CFG2[0x0028], CMD_OPCODE (bit[23:16])

Step 3 Configure the effective range of Prefetch by setting the PREFETCH_START_ADDR and the PREFETCH_END_ADDR.

SPI Interface BIT Mode

Refer to the functions of SPI Bit Mode (3-Wire/4-Wire).

DMA Setup

Step 1 Configure the length and starting address of the first descriptor in the SPI_DMA_CTRL and SPI_DESCRIPTOR_SADDR to initiate DMA.

Step 2 Configure the length and the starting address of storage location for the first descriptor. Then, finish the following operations to complete DMA Configuration.

- Descriptor0
  - AHB Master Burst Type Configuration

    HBURST_TYPE (bit [6:4]): Supports SINGLE/INCR4/INCR8/INCR16 mode.
  - DMA Transfer Direction Configuration

    DMA_DIR (bit [1]): DMA read or DMA write.
  - DMA Finish Flag

    DMA_FINISH_FLAG (bit [0]): Currently the memory space allocated by the CPU to DMA may be a part of the total data volume to be transferred. For instance, the 256 Byte memory space is allocated to transfer 1 MB data. In this situation, a DMA descriptor merely points to the allocated 256 Byte data location, and it will also point to the next descriptor to fetch data. When the data of the last descriptor is fetched, the stop bit should be pulled up to terminate a DMA handling.
- Descriptor1
  - DMA_BLK_LEN ([31:16])

    DMA BLK length. It indicates the size of each DMA packet, with multiples of 8 Byte aligned to achieve the optimized rate when accessing storage.
  - DMA_DATA_LEN (bit [15:0])

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

It indicates the data volume indicated by the current descriptor of DMA.

- Descriptor2

  It indicates the data storage location of current descriptor.

- Descriptor3

  It indicates the storage location of the next descriptor.

- Descriptor4-7

  The SPI configuration parameters. In the course of setting parameters with DMA for SPI, the content of descriptors is configured to SPI.

Enable SPI

Write 1 to the SPI_NMODE_EN in the SPI_GLOBAL_CTRL, then it will be auto pulled down.

11.5.6.2 CPU Transfer

The software operation of CPU transfer is almost the same as DMA transfer. However, there are still two main differences.

One difference is that when the CPU transfers, channel parameter cannot come from DMA descriptors. SPI_GLOBAL_CTRL[0x0004], SPI_CFG_MODE(bit[0]) must be set to 0. All parameters should come from REGISTER FILE. SPI_GLOBAL_CTRL[0x0004], SPI_CPU_MODE_EN(bit[20]) is used to start CPU transfer (Different from descriptor and SPI_GLOBAL_CTRL[0x0004], SPI_NMODE_EN(bit[2])).

The other difference is that when reading data from Register [0x0210], it is recommended to read SPI_CDC_FIFO_STA[0x0050], RF_CNT([bit5-0]), especially when total read number is not integer multiple of trigger level. When writing data to Register [0x0220], it is always ready as long as trigger level is not reached.

NOTE

Register [0x0040] and [0x0044] are not used in CPU transfer.

11.5.6.3 Auto Status Reading

The software operation of status reading is almost the same as CPU transfer. CMD_TRANS_EN and RX_DATA_EN must be set high because RX data path is used for status reading. MODE_BIT_TRANS_EN and DUMMY_BIT_TRANS_EN should be set accordingly. But STATUS OPCODE will not go through READ_FIFO and READ_BUFFER. Meanwhile, I/O Pins used should be set accordingly. SPI_STATUS_READ[0x0068] and SPI_STATUS_READ_2[0x006C] are used for STATUS READING. And to avoid endless reading and dead lock, the CPU should tell the maximum reading times. Then, to start STATUS READING, SPI_READ_STATUS_MODE_EN should be set. In this mode, DATA_TRANS_NUM (002C, [15:0]) is suggested to be 1 and DTR_EN [0x0004, bit 16] is suggested to be 0.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.5.6.4 Prefetch

The software operation of PREFETCH is almost the same as CPU transfer.

The System Setup part, SPI Initialization part and Channel Setup part is the same as DMA transfer.

After the basic initialization and setup, enable SPI_GLOBAL_CTRL[0x0004], SPI_PMODE_EN(bit 3) to enter PREFETCH mode. Then directly read in prefetch area to get data; for details, see the section Memory Map.

CAUTION

a) DQS function is not supported in the prefetch mode. As in this mode, if the DQS of external devices goes wrong, it may lead to hang.

b) LSB first operation is supported in the prefetch mode.

11.5.7 Register List

Module Name	Base Address
SPIF	0x047F0000

Register Name	Offset	Description
SPI_GLOBAL_CTRL	0x0004	SPI Global Control Register
SPI_GLOBAL_CTRL_ADD	0x0008	SPI Global Control Additional Register
SPI_TIMING_CFG	0x000C	SPI Timing Configure Register
SPI_TIMING_DLY_STA	0x0010	SPI Timing Delay State Register
SPI_INT_EN	0x0014	SPI Interrupt Enable Register
SPI_INT_STA	0x0018	SPI Interrupt Status Register
SPI_CS_DELAY	0x001C	SPI Chipselect Delay Register
SPI_TRANS_PHA_CFG	0x0020	SPI Trans Phase Configure Register
SPI_TRANS_CFG1	0x0024	SPI Trans Configure1 Register
SPI_TRANS_CFG2	0x0028	SPI Trans Configure2 Register
SPI_TRANS_NUM	0x002C	SPI Trans Number Register
SPI_PREFETCH_STA	0x0030	SPI Prefetch State Register
SPI_PREFETCH_START_ADDR	0x0034	SPI Prefetch Start Address Register
SPI_PREFETCH_END_ADDR	0x0038	SPI Prefetch End Address Register
SPI_PREFETCH_MAP_ADDR	0x003C	SPI Prefetch Map Address Register
SPI_DMA_CTRL	0x0040	SPI DMA Control Register
SPI_DESCRIPTOR_SADDR	0x0044	SPI DMA Descriptor Start Address Register
SPI_CDC_FIFO_TRIG_LEVEL	0x004C	SPI CDC FIFO Trigger Level Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
SPI_CDC_FIFO_STA	0x0050	SPI CDC FIFO Status Register
SPI_BATC	0x0054	SPI Bit-Aligned Transfer Configure Register
SPI_BA_CCR	0x0058	SPI Bit-Aligned CLOCK Configuration Register
SPI_TBR	0x005C	SPI TX Bit Register
SPI_RBR	0x0060	SPI RX Bit Register
SPI_STATUS	0x0064	SPI Status Register
SPI_STATUS_READ	0x0068	SPI READ Status Register
SPI_STATUS_READ2	0x006C	SPI READ Status Register_2
SPI_PREFETCH_RX_DATA	0x0200	SPI Prefetch RX Data Register
SPI_PREFETCH_RX_DATA	0x0200	SPI Prefetch RX Data Register
SPI_RX_DATA	0x0210	SPI RX Data Register
SPI_TX_DATA	0x0220	SPI TX Data Register

11.5.8 Register Description

11.5.8.1 0x0004 SPI Global Control Register (Default Value: 0x0000_0100)

Offset: 0x0004			Register Name: SPI_GLOBAL_CTRL
Bit	Read/Write	Default/Hex	Description
31:23	/	/	/
22	R/W	0x0	START_MODE 0: old start mode 1: new start mode
21	R/WAC	0x0	SPI_READ_STATUS_MODE_EN SPI READ STATUS Mode Enable 0: Disable 1: Enable This bit is not used for data transfer. It is used for status confirm. And when this operation ends, the last returned byte value is sent to 0x0064[31:24].
20	R/WAC	0x0	SPI_CPU_MODE_EN SPI CPU Mode Enable 0: Disable 1: Enable
19	R/W	0x0	SPI_CLK_OUTPUT 0: Disable 1: Enable When the SPI_CLK_OUTPUT is enabled, the SPI_FLASH will convey the sclk from CCU to the spi_sck_out pin. This bit cannot be enabled in the process of data transmission to avoid anomaly.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: SPI_GLOBAL_CTRL
Bit	Read/Write	Default/Hex	Description
18	R/W	0x0	SPI_TX_CFG_FBS Transmit Interface First Transmit Bit Select. 0: MSB First 1: LSB First
17	R/W	0x0	SPI_RX_CFG_FBS Receive Interface First Transmit Bit Select. 0: MSB First 1: LSB First
16	R/W	0x0	DTR_EN Double Trans Rate Enable 0: Disable 1: Enable
15	R/W	0x0	SPI_WP_EN 0: Disable 1: Enable In Standard SPI or Dual SPI, SPI PIN Write Protect Function can be open In the open status, SPI_WP_IO2_OUT is enabled. The exact polarity is decided by the configuration of SPI_WP_POL. In the closed status, SPI_WP_IO2_OUT is controlled by hardware. The exact polarity is decided by the controller.
14	R/W	0x0	SPI_WP_POL SPI PIN Write Protect Polar 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle)
13	R/W	0x0	SPI_HOLD_EN 0: Disable 1: Enable In Standard SPI or Dual SPI, SPI PIN HOLD Function can be open. In the open status, SPI_HOLD_IO3_OUT is enabled. The exact polarity is decided by the configuration of SPI_HOLD_POL. In the closed status, SPI_HOLD_IO3_OUT is controlled by hardware. The exact polarity is decided by the controller.
12	R/W	0x0	SPI_HOLD_POL SPI PIN HOLD Polar 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle)

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: SPI_GLOBAL_CTRL
Bit	Read/Write	Default/Hex	Description
11	/	/	/
10	R/W	0x0	DQS_RX_EN Receive DQS Signal Enable 0: Disable 1: Enable
9	R/W	0x0	DUMMY_BIT_POL Dummy Bit Trans Value 0: Dummy bit Trans 0 1: Dummy bit Trans 1 In the dummy period, the output data of Hold and Write Protection will be controlled by the DUMMY_BIT_POPL.
8	R/W	0x1	SPI_CS_POL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = idle) 1: Active low polarity (1 = idle)
7:6	R/W	0x0	SPI_CS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPIF_CS0 will be asserted 01: SPIF_CS1 will be asserted (not used) 10: SPIF_CS2 will be asserted (not used) 11: SPIF_CS3 will be asserted (not used)
5	R/W	0x0	SPI_CPOL SPI Clock Polarity Control 0: Active High Polarity. 1: Active Low Polarity.
4	R/W	0x0	SPI_CPHA SPI Clock/Data Phase Control 0: Phase 0(Leading Edge for Sample Data) 1: Phase 1(Leading Edge For Setup Data)
3	R/W	0x0	SPI_PMODE_EN SPI Prefetch Mode Enable 0: Configuring AHB0-bus Prefetch. 1: Configure AHB0-bus Prefetch Done. Note1: When CPU Needs Configure AHB0-bus Prefetch Operation, Clear 0, then send Configuration parameters. Note2: When CPU Configure AHB0-bus Prefetch Done, Set 1. Note3: When SPI Controller detect 'Enable Prefetch =1' ,will latch the parameters.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: SPI_GLOBAL_CTRL
Bit	Read/Write	Default/Hex	Description
2	R/WAC	0x0	SPI_DMA_MODE_EN SPI DMA Mode Enable 0: Disable 1: Enable
1	R/W	0x0	PREFETCH_ADDR_MAP_MODE Prefetch Address Map Mode When the CPU accesses Flash through SPI, the address map mode can be selected by adding N to the address and then mapping the fetching address to the ADDR+N.
0	R/W	0x0	SPI_CFG_MODE SPI Parameter Config Source in normal(DMA) mode. Set to 0 When CPU Transfer. 0: From REGISTER 1: From DMA Descriptor

11.5.8.2 0x0008 SPI Global Control Additional Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: SPI_GLOBAL_CTRL_ADD
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/WAC	0x0	SPI_FLASH_DMA_END Terminate the DMA Chain after the present BLK is done. After the DMA chain terminates, set 1 to this bit to stop DMA transmission after the DMA module finishes the present BLK whether the current chain completes or the finish_flag is set to 1. DMA_END and SPI_SRST should be used together: Enable the DMA_END first, and then enable the SPI_FLASH_SRST after DMA_END is cleared.
3	R/WAC	0x0	SPI_FLASH_SRST Reset All the Logic in SPI Flash (DMA chain is not included) SPI is globally reset, and all the clock domain logic is reset
2	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: SPI_GLOBAL_CTRL_ADD
Bit	Read/Write	Default/Hex	Description
1	R/WAC	0x0	CDC_WF_SRST Transfer FIFO Software Reset, In SPI_WR_BUF_CTRL Module 0: Auto Clear to 0. 1: Reset Transfer FIFO. Writing 1 to this bit will reset the control portion of the transfer FIFO, and auto clear to 0 when completing reset operation. Writing 0 to this bit has no effect.
0	R/WAC	0x0	CDC_RF_SRST Receiver FIFO Software Reset, In SPI_RD_BUF_CTRL Module 0: Auto Clear to 0. 1: Reset Receiver FIFO. Writing 1 to this bit will reset the control portion of the receiver FIFO, and auto clear to 0 when completing reset operation, write 0 to this bit has no effect.

11.5.8.3 0x000C SPI Timing Configure Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: SPI_TIMING_CFG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26	R/W	0x0	CLK_SCKOUT_SRC_SEL SPI Output Clk Select Select the rate of SPI output clock (SCK_OUT). 0: Original Clock (i_spi_ref_clk from CCU) 1: Two-frequency Clock (i_spi_ref_clk /2)
25	R/W	0x0	CLK_SCK_SRC_SEL SPI Interface Clock Select 0: Original Clock (i_spi_ref_clk from CCU) 1: Two-frequency Clock (i_spi_ref_clk /2)
24	R/W	0x0	CLK_SPI_SRC_SEL SPI Inter Process Clock Select 0: Original Clock (i_spi_ref_clk from CCU) 1: Two-frequency (i_spi_ref_clk/2)
23:22	/	/	/
21	R/W	0x0	SCKT_DELAY_MODE_SEL SCKT Delay Mode Select 0: Select the SCKT without delay 1: Select the SCKT after the analog delay chain adjustment

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x000C			Register Name: SPI_TIMING_CFG
Bit	Read/Write	Default/Hex	Description
20	R/W	0x0	SCKR_DELAY_MODE_SEL SCKR Delay Mode Select 0: digital delay 1: digital delay + analog delay
19	/	/	/
18:16	R/W	0x0	DIGITAL_SCKR_DELAY_CFG Digital SCKR Delay Value Config, Step 0.5 spi_clk 000: delay 0 clk 001: delay 0.5 clk 010: delay 1 clk 011: delay 1.5 clk 100: delay 2 clk 101: delay 2.5 clk 110: delay 3 clk 111: delay 3.5 clk
15	R/W	0x0	ANALOG_SAMP_DL_CAL_START_TX Sample Delay Calibration Start When set, start sample delay chain calibration.
14	R/W	0x0	ANALOG_SAMP_DL_SW_EN_TX Sample Delay Software Enable When set, enable sample delay specified at SAMP_DL_SW
13:8	R/W	0x0	ANALOG_SAMP_DL_SW_VALUE_TX Sample Delay Software Value The relative delay between clock line and command line, data lines. It can be determined according to the value of SAMP_DL, the cycle of card clock and device s input timing requirement.
7	R/W	0x0	ANALOG_SAMP_DL_CAL_START_RX Sample Delay Calibration Start When set, start sample delay chain calibration.
6	R/W	0x0	ANALOG_SAMP_DL_SW_EN_RX Sample Delay Software Enable When set, enable sample delay specified at SAMP_DL_SW

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x000C			Register Name: SPI_TIMING_CFG
Bit	Read/Write	Default/Hex	Description
5:0	R/W	0x0	ANALOG_SAMP_DL_SW_VALUE_RX Sample Delay Software Value The relative delay between clock line and command line, data lines. It can be determined according to the value of SAMP_DL, the cycle of card clock and device s input timing requirement.

11.5.8.4 0x0010 SPI Timing Delay State Register (Default Value: 0x0000_2020)

Offset: 0x0010			Register Name: SPI_TIMING_DLY_STA
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R	0x0	ANALOG_SAMP_DL_CAL_DONE_TX Sample Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in SAMP_DL.
14	/	/	/
13:8	R	0x20	ANALOG_SAMP_DL_TX Sample Delay Value It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of card clock nearly. Generally, it is necessary to do drive delay calibration when card clock is changed. This bit is valid only when SAMP_DL_CAL_DONE is set.
7	R	0x0	ANALOG_SAMP_DL_CAL_DONE_RX Sample Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in SAMP_DL.
6	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0010			Register Name: SPI_TIMING_DLY_STA
Bit	Read/Write	Default/Hex	Description
5:0	R	0x20	ANALOG_SAMP_DL_RX Sample Delay Value It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of card clock nearly. Generally, it is necessary to do drive delay calibration when card clock is changed. This bit is valid only when SAMP_DL_CAL_DONE is set.

11.5.8.5 0x0014 SPI Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0014			Name: SPI_INT_EN
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R/W	0x0	READ_STATUS_DONE_INT_EN 0: Disable. 1: Enable.
27	R/W	0x0	READ_STATUS_TIME_OUT_INT_EN 0: Disable. 1: Enable.
26	R/W	0x0	SPI_TRANS_DONE_INT_EN SPI Transmit Finish Interrupt Enable 0: Disable. 1: Enable.
25	R/W	0x0	PREFETCH_READ_WORD_ACK_INT_EN Prefetch Mode Read back request word Interrupt Enable 0: Disable. 1: Enable.
24	R/W	0x0	DMA_TRANS_DONE_INT_EN DMA Chain Transmit Finish Interrupt Enable 0: Disable. 1: Enable.
23	R/W	0x0	DQS_RF_ODD_UDF_INT_EN DQS Receive FIFO Underflow Interrupt Enable 0: Disable. 1: Enable.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Name: SPI_INT_EN
Bit	Read/Write	Default/Hex	Description
22	R/W	0x0	DQS_RF_ODD_OVF_INT_EN DQS Receive FIFO Overflow Interrupt Enable 0: Disable. 1: Enable.
21	R/W	0x0	DQS_RF_EVEN_UDF_INT_EN DQS Receive FIFO Underflow Interrupt Enable 0: Disable. 1: Enable.
20	R/W	0x0	DQS_RF_EVEN_OVF_INT_EN DQS Receive FIFO Overflow Interrupt Enable 0: Disable. 1: Enable.
19:12	/	/	/
11	R/W	0x0	WF_UDF_INT_EN Write FIFO Underflow Interrupt Enable 0: Disable. 1: Enable.
10	R/W	0x0	WF_OVF_INT_EN Write FIFO Overflow Interrupt Enable 0: Disable. 1: Enable.
9	R/W	0x0	RF_UDF_INT_EN Read FIFO Underflow Interrupt Enable 0: Disable. 1: Enable.
8	R/W	0x0	RF_OVF_INT_EN Read FIFO Overflow Interrupt Enable 0: Disable. 1: Enable.
7:5	/	/	/
4	R/W	0x0	WF_RDY_INT_EN Write FIFO Ready Request Interrupt Enable 0: Disable. 1: Enable.
3:1	/	/	/
0	R/W	0x0	RF_RDY_INT_EN Read FIFO Ready Request Interrupt Enable 0: Disable. 1: Enable.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.5.8.6 0x0018 SPI Interrupt Status Register (Default Value: 0x0000_0010)

Offset: 0x0018			Name: SPI_INT_STA
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R/W1C	0x0	READ_STATUS_DONE_INT READ_STATUS MODE Done Interrupt. When set, this bit indicates that at least one wanted bit has got expected value.
27	R/W1C	0x0	READ_STATUS_TIME_OUT_INT READ_STATUS MODE TIME OUT Interrupt. When set, this bit indicates that READ_STATUS MODE ends and in the written period, no wanted bit gets expected value.
26	R/W1C	0x0	SPI_TRANS_DONE_INT SPI Transmit Finish Interrupt
25	R/W1C	0x0	PREFETCH_READ_WORD_ACK_INT Prefetch Mode Read Back Request Word Interrupt Note: When set, this bit indicates that Write FIFO has underflow. Writing “1” to this bit clears it.
24	R/W1C	0x0	DMA_TRANS_DONE_INT DMA Chain Transmit Finish Interrupt Note: When set, this bit indicates that Write FIFO has underflow. Writing 1 to this bit clears it.
23	R/W1C	0x0	DQS_RF_ODD_UDF_INT DQS Receive FIFO underflow Interrupt Flag Note: When set, this bit indicates that Write FIFO has underflow. Writing 1 to this bit clears it.
22	R/W1C	0x0	DQS_RF_ODD_OVF_INT DQS Receive FIFO Overflow Interrupt Flag Note: When set, this bit indicates that Write FIFO has overflowed. Writing 1 to this bit clears it.
21	R/W1C	0x0	DQS_RF_EVEN_UDF_INT DQS Receive FIFO Underflow Interrupt Flag Note: When set, this bit indicates that Read FIFO has underflow. Writing 1 to this bit clears it.
20	R/W1C	0x0	DQS_RF_EVEN_OVF_INT DQS Receive FIFO Overflow Interrupt Flag Note: When set, this bit indicates that Read FIFO has overflowed. Writing 1 to this bit clears it.
19:12	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0018			Name: SPI_INT_STA
Bit	Read/Write	Default/Hex	Description
11	R/W1C	0x0	WF_UDF_INT Write FIFO underflow Interrupt Flag Note: When set, this bit indicates that Write FIFO has underflow. Writing 1 to this bit clears it.
10	R/W1C	0x0	WF_OVF_INT Write FIFO Overflow Interrupt Flag Note: When set, this bit indicates that Write FIFO has overflowed. Writing 1 to this bit clears it.
9	R/W1C	0x0	RF_UDF_INT Read FIFO Underflow Interrupt Flag Note: When set, this bit indicates that Read FIFO has underflow. Writing 1 to this bit clears it.
8	R/W1C	0x0	RF_OVF_INT Read FIFO Overflow Interrupt Flag Note: When set, this bit indicates that Read FIFO has overflowed. Writing 1 to this bit clears it.
7:5	/	/	/
4	R/W1C	0x1	WF_RDY_INT Write FIFO Ready Request Interrupt Flag 0: WF_WL > WF_EMPTY_TRIG_LEVEL. 1: WF_WL <= WF_EMPTY_TRIG_LEVEL. This bit is set any time if WF_WL <= WF_EMPTY_TRIG_LEVEL. Writing 1 to this bit clears it.
3:1	/	/	/
0	R/W1C	0x0	RF_RDY_INT Read FIFO Ready Request Interrupt Flag 0: RF_WL < RX_EMPTY_TRIG_LEVEL and rest total RX data byte number is larger than RX_EMPTY_TRIG_LEVEL. 1: RF_WL >= RX_EMPTY_TRIG_LEVEL, or rest total RX data byte number is smaller than RX_EMPTY_TRIG_LEVEL meanwhile RF_WL >= 1. This bit is set any time if condition is reached. Writing 1 to this bit clears it.

11.5.8.7 0x001C SPI Chipselect Delay Register (Default Value: 0x0000_0606)

Offset: 0x001C			Register Name: SPI_CS_DELAY
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x001C			Register Name: SPI_CS_DELAY
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	DBG_SEL 0: The high 8 bits of debug signal are io*_oen, and the low 8 bits are 0. 1: The high 8 bits are WF_CNT, and the low 8 bits are RF_CNT. 2: The high 8 bits are WB_CNT, and the low 8 bits are RB_CNT. 3: The high 8 bits are DMA state machine, and the low 8 bits are SPI state machine. 4: Debug signal are read DRQ and write DRQ. 2'b0: dqs_rfifo_even water level; 4'b0: dqs_rfifo_odd water level.
23:16	R/W	0x0	CSDA Chip Select De-Assert The interval of two adjacent CS signal enable, namely, the interval of two SPI scheduling. The unit is the i_clk_spi_ref. The minimum interval A (CSDA=0) is 4 clk (used for ending SPI functions) The maximum A (CSDA=FB) is FF clk (used for ending SPI functions) When CSDA is X, the actual interval is X+A.
15:8	R/W	0x6	CSEOT Chip Select End of Transfer The interval between the rising edge of last output clock signal (SPI_CLK_OUT) and the CS signal disable. The unit is the reference clock (i_clk_spi_ref). The minimum interval B (CSEOT=0) is: DTR-TX: 3 clk DTR-RX: 5 clk STR-TX, CPOL=0: 3 clk STR-RX, CPOL=0: 4 clk STR-TX, CPOL=1: 2.5 clk STR-RX, CPOL=1: 3.5 clk When CSEOT is X, the actual interval is X+B. When using delay, the length of CSEOT should be larger than that of delay, or the data will be lost.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x001C			Register Name: SPI_CS_DELAY
Bit	Read/Write	Default/Hex	Description
7:0	R/W	0x6	CSSOT Chip Select Start of Transfer The interval between the CS signal enable and the rising edge of the first output clock signal (SPI_CLK_OUT). The unit is the reference clock (i_clk_spi_ref). The minimum interval C (CSSOT=0) is: CPOL=0: 1 clk CPOL=1: 1.5 clk When CSSOT is X, the actual interval is X+C. The minimum interval is recommended to be 6, or the anomaly will occur in some special conditions. The minimum interval should be larger than 6 in NEW_START_MODE.

11.5.8.8 0x0020 SPI Transfer Phase Configure Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SPI_TRANS_PHA_CFG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R/W	0x0	CMD_DTR CMD DTR Control 1: CMD DTR 0: CMD not DTR CAUTION: When CMD DTR, DTR_EN must be on and CMD_LEN must be 2byte.
28	R/W	0x0	COMMAND_TRANS_EN Set to 1 if command data need trans to device SPI Controller FSM Phase Enable 1: Enable 0: Disable
27:25	/	/	/
24	R/W	0x0	ADDRESS_TRANS_EN Set to 1 if address need trans to device SPI Controller FSM Phase Enable 1: Enable 0: Disable
23:21	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0020			Register Name: SPI_TRANS_PHA_CFG
Bit	Read/Write	Default/Hex	Description
20	R/W	0x0	MODE_BIT_TRANS_EN Set to 1 if Mode bit need trans after address SPI Controller FSM Phase Enable 1: Enable 0: Disable
19:17	/	/	/
16	R/W	0x0	DUMMY_BIT_TRANS_EN Dummy Bit State Enable SPI Controller FSM Phase Enable 1: Enable 0: Disable
15:13	/	/	/
12	R/W	0x0	TX_DATA_EN Set to 1 if Data Need Trans SPI Controller FSM Phase Enable 1: Enable 0: Disable The CPU channels should be configured before writing to this bit out of protection requirements.
11:9	/	/	/
8	R/W	0x0	RX_DATA_EN Set to 1 if Data Need Receive SPI Controller FSM Phase Enable 1: Enable 0: Disable The CPU channels should be configured before reading from this bit out of protection requirements.
7:0	/	/	/

11.5.8.9 0x0024 SPI Trans Configure1 Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: SPI_TRANS_CFG1
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0024			Register Name: SPI_TRANS_CFG1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	ADDR_OPCODE Address Content Trans Through SPI **When the length of ADDR is configured as 24bit.** a) If the MSB first is configured, the low 24 bits of ADDR_OPCODE is used, namely, ADDR_OPCODE [23:0]. The sending sequence is from bit23 to bit0. b) If the LSB first is configured, the high 24 bits of ADDR_OPCODE is used, namely, ADDR_OPCODE [31:8]. The sending sequence is from bit8 to bit31. **When the length of ADDR is configured as 16bit.** a) If the MSB first is configured, the low 16 bits of ADDR_OPCODE is used, namely, ADDR_OPCODE [15:0]. The sending sequence is from bit15 to bit0. b) If the LSB first is configured, the high 16 bits of ADDR_OPCODE is used, namely, ADDR_OPCODE [31:16]. The sending sequence is from bit16 to bit31. **When the length of ADDR is configured as 8bit.** a) If the MSB first is configured, the low 8 bits of ADDR_OPCODE is used, namely, ADDR_OPCODE [7:0]. The sending sequence is from bit7 to bit0. b) If the LSB first is configured, the high 8 bits of ADDR_OPCODE is used, namely, ADDR_OPCODE [31:24]. The sending sequence is from bit24 to bit31.

11.5.8.10 0x0028 SPI Trans Configure2 Register (Default Value: 0x0000_0000)

NOTE

This register should be setup while the controller is idle.

Offset: 0x0028			Register Name: SPI_TRANS_CFG2
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	CMD_OPCODE Command Content Trans Through SPI

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0028			Register Name: SPI_TRANS_CFG2
Bit	Read/Write	Default/Hex	Description
23:16	R/W	0x0	MODE_OPCODE Mode Content Trans Through SPI
15:8	R/W	0x0	CMD_OPCODE2 Command2 Content Trans Through SPI
7:6	R/W	0x0	CMD_TRANS_TYPE Command Transfer Type 00: Command can be Shifted to the device on DQ0 01: Command can be Shifted to the device on DQ0 and DQ1 10: Command can be Shifted to the device on DQ0-DQ3 11: Command can be Shifted to the device on DQ0-DQ7
5:4	R/W	0x0	ADDR_TRANS_TYPE Address Transfer Type 00: Address can be Shifted to the device on DQ0 01: Address can be Shifted to the device on DQ0 and DQ1 10: Address can be Shifted to the device on DQ0- DQ3 11: Address can be Shifted to the device on DQ0-DQ7
3:2	R/W	0x0	MODE_BIT_TRANS_TYPE Mode Bit Transfer Type 00: Mode Bit can be Shifted to the device on DQ0 01: Mode Bit can be Shifted to the device on DQ0 and DQ1 10: Mode Bit can be Shifted to the device on DQ0- DQ3 11: Mode Bit can be Shifted to the device on DQ0-DQ7
1:0	R/W	0x0	DATA_TRANS_TYPE Data Transfer Type 00: Opcode can be Shifted to the device on DQ0 only 01: Opcode can be Shifted to the device on DQ0 and DQ1 only 10: Opcode can be Shifted to the device on DQ0- DQ3 11: Opcode can be Shifted to the device on DQ0-DQ7

11.5.8.11 0x002C SPI Trans Number Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: SPI_TRANS_NUM
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DATA_TRANS_NUM[16]
30:27	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x002C			Register Name: SPI_TRANS_NUM
Bit	Read/Write	Default/Hex	Description
26	R/W	0x0	CMD_LEN 0: 1byte 1: 2byte
25:24	R/W	0x0	ADDR_SIZE_MODE Address Size Mode 00: Address Size 8bit. 01: Address Size 16bit. 10: Address Size 24bit. 11: Address Size 32bit.
23:16	R/W	0x0	DUMMY_TRANS_NUM Number of Dummy Cycles A value of 0 = 1 Cycle A value of 1 = 1 Cycle ... A value of N = N Cycle
15:0	R/W	0x0	DATA_TRANS_NUM_LOW Bit [15:0] of DATA_TRANS_NUM. Num of Data Trans Through SPI(Byte) 0: Non-Write. 1: Write 1 Byte. 2: Write 2 Bytes. 3: Write 3 Bytes. ..... 65535: Write 65535 Bytes. Note: These Bits Indicate Current Operation is Write Data To Flash.

11.5.8.12 0x0030 SPI Prefetch State Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SPI_PREFETCH_STA
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:0	R	0x0	PREFETCH_HIT_POSITION prefetch hit position

11.5.8.13 0x0034 SPI Prefetch Start Address Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: SPI_PREFETCH_START_ADDR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PREFETCH_START_ADDR Prefetch Work Start Address

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.5.8.14 0x0038 SPI Prefetch End Address Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: SPI_PREFETCH_END_ADDR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PREFETCH_END_ADDR Prefetch Work End Address

11.5.8.15 0x003C SPI Prefetch Map Address Register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: SPI_PREFETCH_MAP_ADDR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PREFETCH_MAP_ADDR Prefetch Map Address, N When the address mapping mode (0x0004,bit[1]) is activated, the actual access address is ADDR+N.

11.5.8.16 0x0040 SPI DMA Control Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: SPI_DMA_CTRL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	COMMON_MEM_SEL 0: SRAM 1: DDR For 16G DDR and SRAM support. Both DMA_BUFFER_ SADDR and NEXT_DESCRIPTOR_ADDR should be in the same zone, either DDR or SRAM.
30:12			
11:4	R/W	0x0	DMA_DESCRIPTOR_LEN DMA Descriptor Length In the initial design, there are eight DMA descriptors and the length of each descriptor is 4 Byte. In this bit, the length of descriptor is set to 32=8*4Byte.
3:1	/	/	/
0	R/WAC	0x0	CFG_DMA_START Config DMA Start Signal When all the DMA parameters are configured well, pull up a pulse of this signal to enable DMA chain.

11.5.8.17 0x0044 SPI DMA Descriptor Start Address Register (Default Value: 0x0000_0000)

Offset: 0x0044	Register Name: SPI_DESCRIPTOR_SADDR

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	FIRST_DESCRIPTOR_SADDR First Descriptor Start Address The WORD address is needed. Namely, the low 2 bit of byte address being removed.

11.5.8.18 0x004C SPI CDC FIFO Trigger Level Register (Default Value: 0x1001_1a10)

Offset: 0x004C			Name: SPI_CDC_FIFO_TRIG_LEVEL
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:24	R/W	0x10	WF_DMA_TRIG_LEVEL Write FIFO DMA Request Trigger Level (WORD) In the case of DMA transfer, this bit should be set to be less than or equal to 16 to avoid the efficiency reduction.
23:22	/	/	/
21:16	R/W	0x01	WF_CPU_TRIG_LEVEL Write FIFO CPU Request Trigger Level (WORD) In the case of DMA transfer, when WF_CNT is less than WF_CPU_TRIG_LEVEL, WF_RDY interrupts will be asserted.
15:14	/	/	/
13:8	R/W	0x1a	RF_FULL_TRIG_LEVEL Read FIFO Full Request Trigger Level (WORD) It is recommended to be less than or equal to 26 to avoid FIFO anomaly. It only determines the volume of RX_FIFO and has no effect on the RX_RDY_INT.
7:6	/	/	/
5:0	R/W	0x10	RF_RDY_TRIG_LEVEL Read FIFO RDY Request Trigger Level (WORD). In the case of CPU reading data, when the rest data volume is larger than RF_RDY_TRIG_LEVEL, and RF_CN is greater than RF_RDY_TRIG_LEVEL, or the rest data volume is less than RF_RDY_TRIG_LEVEL, and RF_CNT is larger than 1, the RF_RDY_INT will be sent out.

11.5.8.19 0x0050 SPI CDC FIFO Status Register (Default Value: 0x0000_0000)

Offset: 0x0050	Name: SPI_CDC_FIFO_STA

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:26	R	0x0	Flash Controller State Debug Reg.
25	R	0x0	WB_WR Write Buffer Could or Not Write.
24:21	R	0x0	WB_CNT Write Buffer Counter(Byte) These Bits Indicate Number of Bytes in Write Buffer.
20	R	0x0	RB_RD_RDY_STATE Read Buffer Could or Not Read
19:16	R	0x0	RB_CNT Read Buffer Counter(Byte) These Bits Indicate Number of Bytes in Read Buffer.
15:14	/	/	/
13:8	R	0x0	WF_CNT Write FIFO Counter (Level) These Bits Indicate Water Level in Write FIFO. 0: 0 level in Write FIFO. 1: 1 level in Write FIFO. (p) 32: 32 level in Write FIFO.
7:6	/	/	/
5:0	R	0x0	RF_CNT Read FIFO Counter (Level) These Bits Indicate Water Level in Read FIFO. 0: 0 level in Read FIFO. 1: 1 level in Read FIFO. (p) 32: 32 level in Read FIFO.

11.5.8.20 0x0054 SPI Bit-Aligned Transfer Configure Register (Default Value: 0x0000_00A0)

Offset: 0x0054			Register Name: SPI_BATC
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0054			Register Name: SPI_BATC
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	TCE Transfer Control Enable In master mode, it is used to start t1o transfer the serial bit s frame, it is only valid when Work Mode Select==0x10/0x11. 0: Idle 1: Initiates transfer. Writing 1 to this bit will start to transfer serial bits frame (the value comes from the SPI TX Bit Register or SPI RX Bit Register), and will auto clear after the bursts transfer completely. Write 0 to this bit has no effect.
30	R/W	0x0	MSMS Master Sample Standard 0: Standard Sample Mode 1: Delay Sample Mode In the Standard Sample Mode, SPI master samples the data at the standard rising edge of SCLK for each SPI mode. In the Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the standard rising edge of SCLK defined in respective SPI mode.
29:26	/	/	
25	R/W1C	0x0	TBC Transfer Bits Completed When set, this bit indicates that the last bit of the serial data frame in SPI TX Bit Register (or SPI RX Bit Register) has been transferred completely. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed Note: It is only valid when Work Mode Select=0x10/0x11.
24	R/W	0x0	TBC_INT_EN Transfer Bits Completed Interrupt Enable 0: Disable 1: Enable Note: It is only valid when Work Mode Select=0x10/0x11.
23:22	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0054			Register Name: SPI_BATC
Bit	Read/Write	Default/Hex	Description
21:16	R/W	0x00	RX_FEM_LEN Configure the length of serial data frame(burst) of RX 0x0: 0bit 0x1: 1bit (p) 0x20: 32bits Other values: reserved *Note: It is only valid when Work Mode Select==0x10/0x11, and can t be written when TCE=1.*
15:14	/	/	/
13:8	R/W	0x0	TX_FEM_LEN Configure the length of serial data frame(burst) of TX 0x0: 0bit 0x1: 1bit (p) 0x20: 32bits Other values: reserved *Note: It is only valid when Work Mode Select==0x10/0x11, and can t be written when TCE=1.*
7	R/W	0x1	SS_LEVEL When control SS signal manually, set this bit to 1 or 0 to control the level of SS signal. 0: set SS to low 1: set SS to high *Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can t be written when TCE=1.*
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software *Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can t be written when TCE=1.*

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0054			Register Name: SPI_BATC
Bit	Read/Write	Default/Hex	Description
5	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) *Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can t be written when TCE=1.*
4	/	/	/
3:2	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_CS0 will be asserted 01: SPI_CS1 will be asserted 10: SPI_CS2 will be asserted 11: SPI_CS3 will be asserted *Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can t be written when TCE=1.*
1:0	R/W	0x0	Work Mode Select 00: Data frame is byte aligned in Standard SPI, Dual-Output/Dual Input SPI, Dual IO SPI and Quad-Output/Quad-Input SPI. 01: Reserve 10: Data frame is bit aligned in 3-Wire SPI 11: Data frame is bit aligned in Standard SPI

11.5.8.21 0x0058 SPI Bit-Aligned CLOCK Configuration Register (Default Value: 0x0000_0000)

NOTE

This register is only valid when Work Mode Select=0x10/0x11.

Offset: 0x0058			Register Name: SPI_BA_CCR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	CDR_N Clock Divide Rate (Master Mode Only) The SPIF_CLK is determined according to the following equation: SPIF_CLK = Source_CLK / (2*(CDR_N + 1)).

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.5.8.22 0x005C SPI TX Bit Register (Default Value: 0x0000_0000)

NOTE

This register is only valid when Work Mode Select=0x10/0x11.

Offset: 0x005C			Register Name: SPI_TBR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VTB The Value of the Transmit Bits This register is used to store the value of the transmitted serial data frame. Note: In the process of transmission, the LSB is transmitted first.

11.5.8.23 0x0060 SPI RX Bit Register (Default Value: 0x0000_0000)

NOTE

This register is only valid when Work Mode Select=0x10/0x11.

Offset: 0x0060			Register Name: SPI_RBR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VRB The Value of the Receive Bits This register is used to store the value of the received serial data frame. Note: In the process of transmission, the LSB is transmitted first.

11.5.8.24 0x0064 SPI STATUS Register (Default Value: 0x0000_0885)

Offset: 0x0064			Register Name: SPI_STATUS
Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	READ_STATUS_RESULT
23:12	/	/	/
11:8	R	0x8	DQS_RF_ODD_WL Rest of space.
7: 4	R	0x8	DQS_RF_EVEN_WL Rest of space.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0064			Register Name: SPI_STATUS
Bit	Read/Write	Default/Hex	Description
3	R	0x0	WF_FULL Write FIFO Full Interrupt Flag 0: Write FIFO is Not Full. 1: Write FIFO is Full. Note: This bit is set when the Write FIFO is full.
2	R	0x1	WF_EMPTY Write FIFO Empty Request Interrupt Flag 0: Write FIFO always contains one or more bytes. 1: Write FIFO has been empty. Note: This bit is set if the Write FIFO is empty.
1	R	0x0	RF_FULL Read FIFO Full Interrupt Flag 0: Not Full. 1: Read FIFO has been Full. Note: This bit is set when Read FIFO is full.
0	R	0x1	RF_EMPTY Read FIFO Empty Interrupt Flag 0: Not Empty. 1: Read FIFO has been Empty. Note: This bit is set if the Read FIFO is empty.

11.5.8.25 0x0068 SPI STATUS READ Register (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: SPI_STATUS_READ
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	SPI_READ_STATUS_DETECTED_BIT_POSITION These 8 bits are used to distinguish the wanted bit in a STATUS BYTE. For every bit that CPU cares, put a high level in the corresponding bit position.
15:8	/	/	/
7:0	R/W	0x0	SPI_READ_STATUS_DETECTED_BIT_VALUE These 8 bits are used to distinguish the wanted bit in a STATUS BYTE. For every bit that CPU cares, put the level that CPU wants in the corresponding bit position. And when one bit is detected the same value, READ_STATUS_MODE shall stop and return a DONE interrupt. Then CPU shall check the exact result in 0x0068[31:24].

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.5.8.26 0x006C SPI STATUS READ Register_2(Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: SPI_STATUS_READ2
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x0	MAXIMUM_STATUS_READ_TIME These 14 bits are used to tell the module that when reading FLASH status, how many times it should read before it stops reading and instead return a TIME_OUT INTERRUPT to avoid dead lock. *NOTE: The suggested minimum value is 1.*
15:14	/	/	/
13:0	R/W	0x0	READ_STATUS_INTERVAL The INTERVAL is counted with 32KHz clock. These 14 bits are used to tell that when READING STATUS, after how many rising edge of the 32K clock should the module start a READ STATUS visit to the connected FLASH. *NOTE: The suggested minimum value is 1.*

11.5.8.27 0x0200 SPI Prefetch RX Data Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: SPI_PREFETCH_RX_DATA
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	SPI_PREFETCH_RX_DATA Spi prefetch data.

11.5.8.28 0x0210 SPI RX Data Register (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: SPI_RX_DATA
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	SPI_RX_DATA SPI RX Data. It cannot be read when DMA transfer.

11.5.8.29 0x0220 SPI TX Data Register (Default Value: 0x0000_0000)

Offset: 0x0220			Register Name: SPI_TX_DATA
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	SPI_TX_DATA SPI TX Data. It cannot be written when DMA transfer.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

12 Interrupts

12.1 Interrupt Controller

12.1.1 Overview

The Interrupt Control module is used to handle interrupt coalescing and provide interrupt recording in multi-core systems. This module provides an independent interrupt processing mechanism for each core to adapt to the limitations of different cores on the number of interrupts.

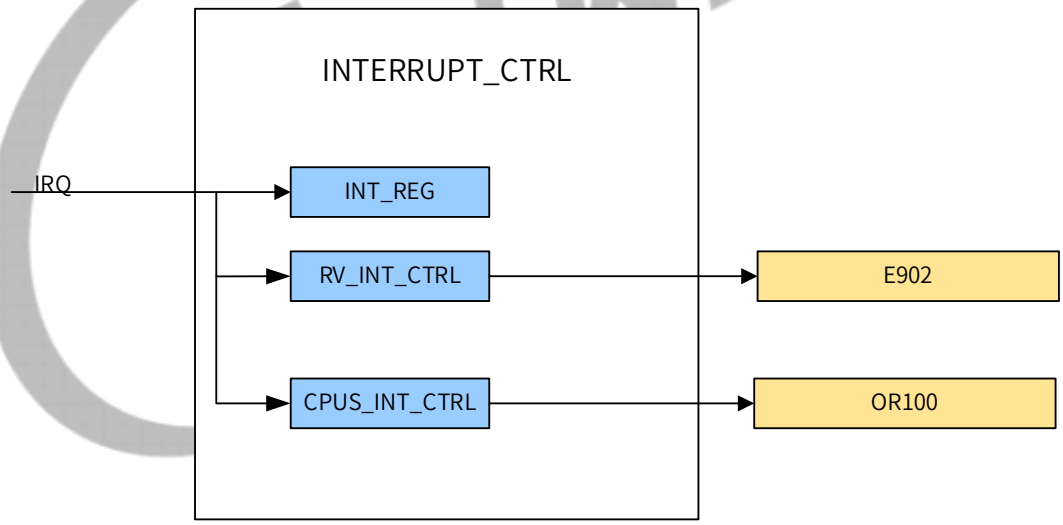
This module has the following features:

- Interrupt coalescing
- Interrupt recording

12.1.2 Block Diagram

The following figure shows the block diagram of the interrupt controller.

Figure 12-1 Interrupt Controller Block Diagram



12.1.3 Functional Description

Interrupt Coalescing

Different cores will use independent interrupt coalescing schemes and interrupt mask registers. Software can allocate interrupts according to respective scheme. After the chip is powered up, software can mask the interrupts that need responding resources and do not belong to its own core.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Interrupt Recording

When the coalesced interrupt is triggered, this module provides interrupt recording registers, namely, system interrupt state registers. Software can query the flag bit to get the interrupt number of the specific module that initiated the interrupt.

12.1.4 Register List

Module Name	Base Address
CPUS_INTERRUPT_CTRL	0x02055000
RV_INTERRUPT_CTRL	0x02056000

Register Name	Offset	Description
INTC_CONFIG_REG0	0x0010	Group Interrupt Configuration Register 0
INTC_CONFIG_REG1	0x0014	Group Interrupt Configuration Register 1
INTC_CONFIG_REG2	0x0018	Group Interrupt Configuration Register 2
INTC_CONFIG_REG3	0x001C	Group Interrupt Configuration Register 3
INTC_CONFIG_REG4	0x0020	Group Interrupt Configuration Register 4
INTC_CONFIG_REG5	0x0024	Group Interrupt Configuration Register 5
INTC_CONFIG_REG6	0x0028	Group Interrupt Configuration Register 6
INTC_CONFIG_REG7	0x002C	Group Interrupt Configuration Register 7
SYS_INT_STATE0	0x0100	System Interrput0 State Register
SYS_INT_STATE1	0x0104	System Interrput1 State Register
SYS_INT_STATE2	0x0108	System Interrput2 State Register
SYS_INT_STATE3	0x010C	System Interrput3 State Register
SYS_INT_STATE4	0x0110	System Interrput4 State Register
SYS_INT_STATE5	0x0114	System Interrput5 State Register
SYS_INT_STATE6	0x0118	System Interrput6 State Register

12.1.5 Register Description

12.1.5.1 0x0010 Group Interrupt Configuration Register 0 (Default Value:0x0000_0000)

Offset: 0x0010			Register Name: CPUS_INTC_CONFIG_REG0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CPUS_INTC_CONFIG_REG0. Group Interrupt [31:0] Config Bit. 0: Interrupt signal will not send to interrupt controller. 1: Interrupt signal will send to interrupt controller if it happens.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

12.1.5.2 0x0014 Group Interrupt Configuration Register 1 (Default Value:0x0000_0000)

Offset: 0x0014			Register Name: CPUS_INTC_CONFIG_REG1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CPUS_INTC_CONFIG_REG1. Group Interrupt [63:32] Config Bit. 0: Interrupt signal will not send to interrupt controller. 1: Interrupt signal will send to interrupt controller if it happens.

12.1.5.3 0x0018 Group Interrupt Configuration Register 2 (Default Value:0x0000_0000)

Offset: 0x0018			Register Name: INTC_CONFIG_REG2
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	INTC_CONFIG_REG2. Group Interrupt [95:64] Config Bit. 0: Interrupt signal will not send to interrupt controller. 1: Interrupt signal will send to interrupt controller if it happens.

12.1.5.4 0x001C Group Interrupt Configuration Register 3 (Default Value:0x0000_0000)

Offset: 0x001C			Register Name: INTC_CONFIG_REG3
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	INTC_CONFIG_REG3. Group Interrupt [127:96] Config Bit. 0: Interrupt signal will not send to interrupt controller. 1: Interrupt signal will send to interrupt controller if it happens.

12.1.5.5 0x0020 Group Interrupt Configuration Register 4 (Default Value:0x0000_0000)

Offset: 0x0020			Register Name: INTC_CONFIG_REG4
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	INTC_CONFIG_REG4. Group Interrupt [159:128] Config Bit. 0: Interrupt signal will not send to interrupt controller. 1: Interrupt signal will send to interrupt controller if it happens.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

12.1.5.6 0x0024 Group Interrupt Configuration Register 5 (Default Value:0x0000_0000)

Offset: 0x0024			Register Name: INTC_CONFIG_REG5
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	INTC_CONFIG_REG5. Group Interrupt [191:160] Config Bit. 0: Interrupt signal will not send to interrupt controller. 1: Interrupt signal will send to interrupt controller if it happens.

12.1.5.7 0x0028 Group Interrupt Configuration Register 6 (Default Value:0x0000_0000)

Offset: 0x0028			Register Name: INTC_CONFIG_REG6
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	INTC_CONFIG_REG6 Group Interrupt[223:192] Config Bit. 0: Interrupt signal will not send to interrupt controller. 1: Interrupt signal will send to interrupt controller if it happens.

12.1.5.8 0x002C Group Interrupt Configuration Register 7 (Default Value:0x0000_0000)

Offset: 0x002C			Register Name: INTC_CONFIG_REG7
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	INTC_CONFIG_REG7 Group Interrupt [255:224] Config Bit. 0: Interrupt signal will not send to interrupt controller. 1: Interrupt signal will send to interrupt controller if it happens.

12.1.5.9 0x0100 System Interrput0 State Register (Default Value: 0x0000_0000)

For the module name corresponding to each interrupt number, see Section GIC.

Offset: 0x0100			Register Name: SYS_INT_STATE0
Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	SYSTEM_INTERRPUT_STATE3 GIC Interrupt Number3: 57~64
23:16	R	0x0	SYSTEM_INTERRPUT_STATE2 GIC Interrupt Number2: 49~56
15:8	R	0x0	SYSTEM_INTERRPUT_STATE1 GIC Interrupt Number1: 40-48

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0100			Register Name: SYS_INT_STATE0
Bit	Read/Write	Default/Hex	Description
7:0	R	0x0	SYSTEM_INTERRPUT_STATE0 GIC Interrupt Number0 :32-39

12.1.5.10 0x0104 System Interrput1 State Register (Default Value: 0x0000_0000)

For the module name corresponding to each interrupt number, see Section GIC.

Offset: 0x0104			Register Name: SYS_INT_STATE1
Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	SYSTEM_INTERRPUT_STATE3 GIC Interrupt Number3: 89~96
23:16	R	0x0	SYSTEM_INTERRPUT_STATE2 GIC Interrupt Number2: 81~88
15:8	R	0x0	SYSTEM_INTERRPUT_STATE1 GIC Interrupt Number1: 73~80
7:0	R	0x0	SYSTEM_INTERRPUT_STATE0 GIC Interrupt Number0: 65~72

12.1.5.11 0x0108 System Interrput2 State Register (Default Value: 0x0000_0000)

For the module name corresponding to each interrupt number, see Section GIC.

Offset: 0x0108			Register Name: SYS_INT_STATE2
Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	SYSTEM_INTERRPUT_STATE3 GIC Interrupt Number3: 121~128
23:16	R	0x0	SYSTEM_INTERRPUT_STATE2 GIC Interrupt Number2: 113~120
15:8	R	0x0	SYSTEM_INTERRPUT_STATE1 GIC Interrupt Number1: 105~112
7:0	R	0x0	SYSTEM_INTERRPUT_STATE0 GIC Interrupt Number0: 97~104

12.1.5.12 0x010C System Interrput3 State Register (Default Value: 0x0000_0000)

For the module name corresponding to each interrupt number, see Section GIC.

Offset: 0x010C			Register Name: SYS_INT_STATE3
Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	SYSTEM_INTERRPUT_STATE3 GIC Interrupt Number3: 153~160

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x010C			Register Name: SYS_INT_STATE3
Bit	Read/Write	Default/Hex	Description
23:16	R	0x0	SYSTEM_INTERRPUT_STATE2 GIC Interrupt Number2: 145~152
15:8	R	0x0	SYSTEM_INTERRPUT_STATE1 GIC Interrupt Number1: 137~144
7:0	R	0x0	SYSTEM_INTERRPUT_STATE0 GIC Interrupt Number0: 129~136

12.1.5.13 0x0110 System Interrput4 State Register (Default Value: 0x0000_0000)

For the module name corresponding to each interrupt number, see Section GIC.

Offset: 0x0110			Register Name: SYS_INT_STATE4
Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	SYSTEM_INTERRPUT_STATE3 GIC Interrupt Number3: 185~192
23:16	R	0x0	SYSTEM_INTERRPUT_STATE2 GIC Interrupt Number2: 177~184
15:8	R	0x0	SYSTEM_INTERRPUT_STATE1 GIC Interrupt Number1: 169~176
7:0	R	0x0	SYSTEM_INTERRPUT_STATE0 GIC Interrupt Number0: 161~168

12.1.5.14 0x0114 System Interrput5 State Register (Default Value: 0x0000_0000)

For the module name corresponding to each interrupt number, see Section GIC

Offset: 0x0114			Register Name: SYS_INT_STATE5
Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	SYSTEM_INTERRPUT_STATE3 GIC Interrupt Number3: 225~232
23:16	R	0x0	SYSTEM_INTERRPUT_STATE2 GIC Interrupt Number2: 216~224
15:8	R	0x0	SYSTEM_INTERRPUT_STATE1 GIC Interrupt Number1: 201~208
7:0	R	0x0	SYSTEM_INTERRPUT_STATE0 GIC Interrupt Number0: 193~200

12.1.5.15 0x0118 System Interrput6 State Register (Default Value: 0x0000_0000)

For the module name corresponding to each interrupt number, see Section GIC.

Offset: 0x0118	Register Name: SYS_INT_STATE6

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	SYSTEM_INTERRPUT_STATE3 GIC Interrupt Number3: 257~264
23:16	R	0x0	SYSTEM_INTERRPUT_STATE2 GIC Interrupt Number2: 249~256
15:8	R	0x0	SYSTEM_INTERRPUT_STATE1 GIC Interrupt Number1: 241~248
7:0	R	0x0	SYSTEM_INTERRPUT_STATE0 GIC Interrupt Number0: 233~240

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

12.2 Generic Interrupt Controller (GIC)

12.2.1 Overview

The GIC is a generic interrupt controller that handles the interrupts from peripherals to the cores and between cores. The GIC supports a distributed microarchitecture containing several individual blocks that are used to provide a flexible GIC implementation.

All the GIC blocks communicate through fully credited AXI4-Stream interface channels. This means that the interface exerts transient backpressure only on their ic<xy>tready signals, enabling packets to be routed over any free-flowing interconnect. Channels can be routed over dedicated AXI4-Stream buses, or over any available free-flowing transport layer in the system. A channel is described as free-flowing if all transactions on that channel complete without a non-transient dependency on any other transaction.

The GIC includes build scripts that can create appropriate levels of hierarchy for any particular configuration. In small configurations, the distribution can be hidden and internally optimized.

the GIC has the following features:

- Interrupt services and masking:
  - Supports the following interrupt types:
    - Up to 56000 LPIs. A peripheral generates these interrupts by writing to a memory-mapped register in the GIC-600.
    - Up to 960 SPIs in groups of 32.
    - Up to 16 PPIs that are independent for each core and can be programmed to support either edge triggered or level-sensitive interrupts.
    - Up to 16 SGIs that are generated through the GIC CPU interface of a core.
  - Up to 16 ITS modules that provide device isolation and ID translation for message-based interrupts and enable virtual machines to program devices directly.
  - Interrupt masking and prioritization with 32 priority levels, five bits per interrupt.
- Registers and programming
  - Flexible affinity routing, using the Multiprocessor Identification Register (MPIDR) addresses, including support for all four affinity levels.
  - Single ACE-Lite slave port on each chip for programming of all GIC Distributor (GICD) registers, GIC Interrupt Translation Service (GITS) registers, and GIC Redistributor (GICR) registers. Each ITS has an optional ACE-Lite slave port for programming the GITS_TRANSLATER register.
  - Coherent view of SPI register data across multiple chips.
- Security
  - A global Disable Security (DS) bit. This bit enables support for systems without security.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- The following interrupt groups allow interrupts to target different exception levels:
  - Group 0.
  - Non-secure Group 1.
  - Secure Group 1.

- Performance Monitoring Unit (PMU) counters with snapshot functionality.
- Error correction: ARMv8.2 Reliability Accessibility Serviceability (RAS) architecture-compliant error reporting for the following:
  - Software access errors
  - ITS command and translation errors
  - Error Correcting Code (ECC) errors

12.2.2 Clock Sources

The following table describes the clock sources of GIC. For clock setting, configurations, and gating information, refer to the section CCU.

Module	Clock Sources	Description
GIC	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.
	RTC_32K	Its frequency is 32.768 KHz by default.
	PERI0_600M	Its frequency is 600 MHz by default.
	PERI0_480M	Its frequency is 480 MHz by default.
	PERI0_400M	Its frequency is 400 MHz by default.

12.2.3 Functional Description

12.2.3.1 CPUX Interrupt Source

The following table describes the details of interrupt sources:

Table 12-1 Interrupt Sources in CPU Subsystem

Interrupt Number	Interrupt Source	Interrupt Vector	Description
0	SGI0	0x0000	SGI 0 interrupt
1	SGI1	0x0004	SGI 1 interrupt
2	SGI2	0x0008	SGI 2 interrupt
3	SGI3	0x000C	SGI 3 interrupt
4	SGI4	0x0010	SGI 4 interrupt
5	SGI5	0x0014	SGI 5 interrupt
6	SGI6	0x0018	SGI 6 interrupt
7	SGI7	0x001C	SGI 7 interrupt

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Interrupt Number	Interrupt Source	Interrupt Vector	Description
8	SGI8	0x0020	SGI 8 interrupt
9	SGI9	0x0024	SGI 9 interrupt
10	SGI10	0x0028	SGI 10 interrupt
11	SGI11	0x002C	SGI 11 interrupt
12	SGI12	0x0030	SGI 12 interrupt
13	SGI13	0x0034	SGI 13 interrupt
14	SGI14	0x0038	SGI 14 interrupt
15	SGI15	0x003C	SGI 15 interrupt
16	PPI0	0x0040	Reserved
17	PPI1	0x0044	Reserved
18	PPI2	0x0048	Reserved
19	PPI3	0x004C	Reserved
20	PPI4	0x0050	Reserved
21	PPI5	0x0054	Reserved
22	PPI6	0x0058	Interrupt-driven debug communications operation
23	PPI7	0x005C	PMU interrupt request
24	PPI8	0x0060	CTI interrupt
25	PPI9	0x0064	Virtual CPU interface maintenance interrupt
26	PPI10	0x0068	Hypervisor physical timer event
27	PPI11	0x006C	Virtual timer event
28	PPI12	0x0070	Hypervisor virtual timer event
29	PPI13	0x0074	Secure physical timer event
30	PPI14	0x0078	Nonsecure physical timer event
31	PPI15	0x007C	Reserve
32	CPUX_MBOX_R	0x0080	CPUX MSGBOX READ IRQ FOR CPUX
33		0x0084	
34	UART0	0x0088	
35	UART1	0x008C	
36	UART2	0x0090	

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Interrupt Number	Interrupt Source	Interrupt Vector	Description
37	UART3	0x0094	
38	UART4	0x0098	
39	UART5	0x009C	
40	UART6	0x00A0	
41		0x00A4	
42		0x00A8	
43	TWI0	0x00AC	
44	TWI1	0x00B0	
45	TWI2	0x00B4	
46	TWI3	0x00B8	
47	TWI4	0x00BC	
48	TWI5	0x00C0	
49	TWI6	0x00C4	
50	TWI7	0x00C8	
51	TWI8	0x00CC	
52	TWI9	0x00D0	
53	TWI10	0x00D4	
54	TWI11	0x00D8	
55	TWI12	0x00DC	
56	SPI0	0x00E0	
57	SPI1	0x00E4	
58	SPI2	0x00E8	
59	SPI3	0x00EC	
60		0x00F0	
61	I2S4	0x00F4	
62	SPI_FLASH	0x00F8	
63	IS_TX	0x00FC	
64	IS_RX	0x0100	
65	LEDC	0x0104	
66	DE_CRC	0x0108	
67	PWM0	0x010C	
68	PWM1	0x0110	
69	LRADC	0x0114	
70	GPADC	0x0118	

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Interrupt Number	Interrupt Source	Interrupt Vector	Description
71	THS	0x011C	
72		0x0120	
73		0x0124	
74	I2S0	0x0128	
75	I2S1	0x012C	
76	I2S2	0x0130	
77	I2S3	0x0134	
78	OWA	0x0138	
79	DMIC	0x013C	DMIC Interrupt
80	VE_ENC	0x0140	
81	VE_DEC	0x0144	
82	DE	0x0148	
83	G2D	0x014C	
84	DI	0x0150	
85	EINK	0x0154	
86	TCON0_LCD0	0x0158	
87	TCON0_LCD1	0x015C	
88		0x0160	
89	TV0	0x0164	
90	TV1	0x0168	
91	DSI0	0x016C	
92	DSI1	0x0170	
93	HDMI	0x0174	
94	EDP	0x0178	
95	GPU	0x017C	
96	GPU_DVFS	0x0180	
97	NPU	0x0184	
98	DSC	0x0188	
99		0x018C	
100		0x0190	
101	GPIOB_NS	0x0194	
102	GPIOB_S	0x0198	
103	GPIOC_NS	0x019C	
104	GPIOC_S	0x01A0	

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Interrupt Number	Interrupt Source	Interrupt Vector	Description
105	GPIOD_NS	0x01A4	
106	GPIOD_S	0x01A8	
107	GPIOE_NS	0x01AC	
108	GPIOE_S	0x01B0	
109	GPIOF_NS	0x01B4	
110	GPIOF_S	0x01B8	
111	GPIOG_NS	0x01BC	
112	GPIOG_S	0x01C0	
113	GPIOH_NS	0x01C4	
114	GPIOH_S	0x01C8	
115		0x01CC	
116		0x01D0	
117	GPIOJ_NS	0x01D4	
118	GPIOJ_S	0x01D8	
119	GPIOK_NS	0x01DC	
120	GPIOK_S	0x01E0	
121	TIMER0	0x01E4	
122	TIMER1	0x01E8	
123	TIMER2	0x01EC	
124	TIMER3	0x01F0	
125	TIMER4	0x01F4	
126	TIMER5	0x01F8	
127	TIMER6	0x01FC	
128	TIMER7	0x0200	
129	TIMER8	0x0204	
130	TIMER9	0x0208	
131	TIMER1_0	0x020C	
132	TIMER1_1	0x0210	
133	TIMER1_2	0x0214	
134	TIMER1_3	0x0218	
135		0x021C	
136		0x0220	
137	SPINLOCK	0x0224	
138	WDT0	0x0228	

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Interrupt Number	Interrupt Source	Interrupt Vector	Description
139	CSI_DMA4	0x022C	
140	CSI_DMA5	0x0230	
141	CCU_FREQ_ERR	0x0234	
142	PLL_UNLOCK	0x0238	
143	DMA0_CPUX_NS	0x023C	
144	DMA0_ CPUX_S	0x0240	
145	DMA1_CPUX_NS	0x0244	
146	DMA1_ CPUX_S	0x0248	
147	AHB_HREADY_TIME_ OUT	0x024C	
148	NSI	0x0250	
149	CSI_DMA0	0x0254	
150	CSI_DMA1	0x0258	
151	CSI_DMA2	0x025C	
152	CSI_DMA3	0x0260	
153	CSI_VIPP0	0x0264	
154	CSI_VIPP1	0x0268	
155	CSI_VIPP2	0x026C	
156	CSI_VIPP3	0x0270	
157	CSI_PARSER0	0x0274	
158	CSI_PARSER1	0x0278	
159	CSI_PARSER2	0x027C	
160		0x0280	
161	CSI_ISP0	0x0284	
162	CSI_ISP1	0x0288	
163	CSI_ISP2	0x028C	
164	CSI_ISP3	0x0290	
165	CSI_CMB	0x0294	
166	CSI_TDM	0x0298	
167	CSI_TOP_PKT	0x029C	
168	PCIE0_EDMA0	0x02A0	
169	PCIE0_EDMA1	0x02A4	
170	PCIE0_EDMA2	0x02A8	
171	PCIE0_EDMA3	0x02AC	

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Interrupt Number	Interrupt Source	Interrupt Vector	Description
172	PCIE0_EDMA4	0x02B0	
173	PCIE0_EDMA5	0x02B4	
174	PCIE0_EDMA6	0x02B8	
175	PCIE0_EDMA7	0x02BC	
176		0x02C0	Reserved
177		0x02C4	Reserved
178		0x02C8	Reserved
179		0x02CC	Reserved
180		0x02D0	Reserved
181		0x02D4	Reserved
182		0x02D8	Reserved
183		0x02DC	Reserved
184	PCIE0_SII	0x02E0	
185	PCIE0_MSI	0x02E4	
186	COMBO0_PHY_DP	0x02E8	
187	USB2	0x02EC	
188	USB0_DEVICE	0x02F0	
189	USB0_EHCI	0x02F4	
190	USB0_OHCI	0x02F8	
191	USB1_EHCI	0x02FC	
192	USB1_OHCI	0x0300	
193	SMHC0	0x0304	
194	SMHC1	0x0308	
195	SMHC2	0x030C	
196	SMHC3	0x0310	
197	UFS	0x0314	
198	NAND	0x0318	
199	UFS_FATAL	0x031C	
200	CE_NS	0x0320	
201	CE_S	0x0324	
202	IOMMU0	0x0328	
203	IOMMU1	0x032C	
204	GMAC0_TOP	0x0330	
205	GMAC0_PERCH_TX_0	0x0334	

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Interrupt Number	Interrupt Source	Interrupt Vector	Description
206	GMAC0_PERCH_RX_0	0x0338	
207		0x033C	
208		0x0340	
209		0x0344	
210	GMAC0_PWS_CLK_CTRL	0x0348	
211		0x034C	
212	MEMC0_DERATE	0x0350	
213	MEMC0_SMC0	0x0354	
214	MEMC0_SMC1	0x0358	
215	MEMC0_DFS	0x035C	
216	DDRPHY	0x0360	
217	COMBO0_PHY_USB3	0x0364	
218	COMBO1_PHY_LN	0x0368	
219		0x036C	
220	NMI	0x0370	
221	PCK600_QCHANNEL	0x0374	
222	S_TWD	0x0378	
223	S_WDT	0x037C	
224	S_TIMER0	0x0380	
225	S_TIMER1	0x0384	
226	S_TIMER2	0x0388	
227	S_TIMER3	0x038C	
228	RTC_ALARM	0x0390	
229	GPIOL_S	0x0394	
230	GPIOL_NS	0x0398	
231	GPIOM_S	0x039C	
232	GPIOM_NS	0x03A0	
233	S_UART0	0x03A4	
234	S_UART1	0x03A8	
235	S_TWI0	0x03AC	
236	S_TWI1	0x03B0	
237	S_TWI2	0x03B4	
238	S_IRRX	0x03B8	

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Interrupt Number	Interrupt Source	Interrupt Vector	Description
239	S_PWM	0x03BC	
240	S_TZMA	0x03C0	
241	S_AHB_HREADY_TIME_OUT	0x03C4	
242	S_SPI	0x03C8	
243	CPUS_MBOX_CPUX_W	0x03CC	
244	PCK600_CPU	0x03D0	
245		0x03D4	
246		0x03D8	
247		0x03DC	
248		0x03E0	
249		0x03E4	
250		0x03E8	
251		0x03EC	
252		0x03F0	
253		0x03F4	
254		0x03F8	
255		0x03FC	
CPUX Related			
256	nERRIRQ[0]	0x0400	L3 ECC error that causes potential data corruption or loss of coherency
257	nERRIRQ[1]	0x0404	core0 ECC error that causes potential data corruption or loss of coherency
258	nERRIRQ[2]	0x0408	core1 ECC error that causes potential data corruption or loss of coherency
259	nERRIRQ[3]	0x040C	core2 ECC error that causes potential data corruption or loss of coherency
260	nERRIRQ[4]	0x0410	core3 ECC error that causes potential data corruption or loss of coherency

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Interrupt Number	Interrupt Source	Interrupt Vector	Description
261	nERRIRQ[5]	0x0414	core4 ECC error that causes potential data corruption or loss of coherency
262	nERRIRQ[6]	0x0418	core5 ECC error that causes potential data corruption or loss of coherency
263	nERRIRQ[7]	0x041C	core6 ECC error that causes potential data corruption or loss of coherency
264	nERRIRQ[8]	0x0420	core7 ECC error that causes potential data corruption or loss of coherency
265	nFAULTIRQ[0]	0x0424	L3 detected 1-bit or 2-bit ECC or Parity error in the RAMs
266	nFAULTIRQ[1]	0x0428	core0 detected 1-bit or 2-bit ECC or Parity error in the RAMs
267	nFAULTIRQ[2]	0x042C	core1 detected 1-bit or 2-bit ECC or Parity error in the RAMs
268	nFAULTIRQ[3]	0x0430	core2 detected 1-bit or 2-bit ECC or Parity error in the RAMs
269	nFAULTIRQ[4]	0x0434	core3 detected 1-bit or 2-bit ECC or Parity error in the RAMs
270	nFAULTIRQ[5]	0x0438	core4 detected 1-bit or 2-bit ECC or Parity error in the RAMs
271	nFAULTIRQ[6]	0x043C	core5 detected 1-bit or 2-bit ECC or Parity error in the RAMs
272	nFAULTIRQ[7]	0x0440	core6 detected 1-bit or 2-bit ECC or Parity error in the RAMs
273	nFAULTIRQ[8]	0x0444	core7 detected 1-bit or 2-bit ECC or Parity error in the RAMs

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Interrupt Number	Interrupt Source	Interrupt Vector	Description
274	nCLUSTERPMUIRQ	0x0448	Cluster PMU interrupt request
275	CPU_PLL_UNLOCK	0x044C	CPUPLL unlock interrupt
276	GIC_FAULT	0x0450	GIC fault handling interrupt
277	GIC_ERR	0x0454	GIC error reporting interrupt
278	GIC_PMU	0x0458	The PMU counter overflow interrupt. This interrupt can be routed internally but is provided as an external output to trigger an external agent to service the GIC

12.2.3.2 PPIs Interrupt Sources

Interrupt Index	Interrupt Source	Description
PPI-20	/	/
PPI-21	/	/
PPI-22	nCOMMIRQ[7:0]	Interrupt-driven debug communications operation
PPI-23	nPMUIRQ[7:0]	PMU interrupt request
PPI-24	CTIIRQ[7:0]	CTI interrupt
PPI-25	nVCPUMNTIRQ[7:0]	Virtual CPU interface maintenance interrupt
PPI-26	nCNTHPIRQ[7:0]	Hypervisor physical timer event
PPI-27	nCNTVIRQ[7:0]	Virtual timer event
PPI-28	nCNTHVIRQ[7:0]	Hypervisor virtual timer event
PPI-29	nCNTPSIRQ[7:0]	Secure physical timer event
PPI-30	nCNTPNSIRQ[7:0]	Nonsecure physical timer event
PPI-31	/	/

NOTE

For detailed register description, please refer to *Arm® CoreLink@ GIC-600 Generic Interrupt Controller Technical Reference Manual* and *Arm® Generic Interrupt Controller Architecture Specification GIC architecture version 3 and version 4*.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

12.3 Core-Local Interrupt Controller (CLIC)

12.3.1 Overview

The Core-Local Interrupt Controller (CLIC) is only used for sampling, priority arbitration and distribution for external interrupt sources.

- Supports RISC-V Core-Local Interrupt Controller Version 0.8 specification
- Up to 64 configurable external interrupt sources that support level interrupts and pulse interrupts; compatible with up to 16 interrupts of CLINT
- 8 levels of interrupt priority
- 4 memory-mapped control registers for each interrupt
- Supports registers like MSCRATCHCSW and MSCRATCHCSWL for the purpose of exchanging stack pointers in the interrupt handler function.

12.3.2 Functional Description

The following table describes the detail of interrupt sources.

Table 12-2 Interrupt Sources in RISC-V Subsystem

Interrupt Number	Interrupt Source	Interrupt Vector	Description
0~15	Reserved	0x0000~ 0x003C	Reserved
16	USB0_USB1_STB	0x0040	USB0_USB1_STB interrupt
17	PCK600_QCHANNEL	0x0044	STBY PCK600 Q-CHANNEL interrupt.
18	S_TWD	0x0048	STBY TWD interrupt.
19	S_WDT	0x004C	STBY WDG interrupt.
20	S_TIMER0	0x0050	STBY timer 0 interrupt.
21	S_TIMER1	0x0054	STBY timer 1 interrupt.
22	S_TIMER2	0x0058	STBY timer 2 interrupt.
23	S_TIMER3	0x005C	STBY timer 3 interrupt.
24	RTC_ALARM	0x0060	STBY RTC Alarm0 interrupt.
25	GPIOL_S	0x0064	STBY MGPIOA SECURE interrupt.
26	GPIOL_NS	0x0068	STBY MGPIOA NON-SECURE interrupt.
27	GPIOM_S	0x006C	STBY MGPIOB SECURE interrupt.
28	GPIOM_NS	0x0070	STBY MGPIOB NON-SECURE interrupt.
29	S_UART0	0x0074	STBY UART0 interrupt
30	S_UART1	0x0078	STBY UART1 interrupt
31	S_TWI0	0x007c	STBY TWI0 interrupt
32	S_TWI1	0x0080	STBY TWI1 interrupt
33	S_TWI2	0x0084	STBY TWI2 interrupt
34	S_IRRX	0x0088	STBY IRRX interrupt

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

35	S_PWM	0x008c	STBY PWM interrupt
36	S_TZMA	0x0090	STBY TZMA error interrupt
37	S_AHB_HREADY_TIME_OUT	0x0094	STBY AHBS TIMEOUT interrupt
38	S_SPI	0x0098	STBY SPI interrupt
39	CPUS_MBOX_READ_IRQ	0x009c	CPUS MSGBOX READ IRQ
40	PCK600_CPU	0x00A0	CPUIDLE interrupt
41~47	Reserved	0x00A4 ~ 0x00BC	Reserved
48	CPUX_MSGBOX_W_R	0x00C0	CPUX MSGBOX WRITE IRQ FOR CPUS/RISCV
49	SPINLOCK(CPUX)	0x00C4	SYS SPINLOCK interrupt
50	DMAC0_CPUS_NS	0x00C8	sys dmac0 CPUS non-secure interrupt
51	DMAC0_CPUS_S	0x00CC	sys dmac0 CPUS secure interrupt
52	DMAC1_CPUS_NS	0x00D0	sys dmac1 CPUS non-secure interrupt
53	DMAC1_CPUS_S	0x00D4	sys dmac1 CPUS secure interrupt
54	riscv_sys_irq_i[6]	0x00D8	Register GINTC_CONFIG_REG0[7:0] can mask gic irq [39:32]
55	riscv_sys_irq_i[7]	0x00DC	Register GINTC_CONFIG_REG0[15:8] can mask gic irq [47:40]
56	riscv_sys_irq_i[8]	0x00E0	Register GINTC_CONFIG_REG0[23:16] can mask gic irq [55:48]
57	riscv_sys_irq_i[9]	0x00E4	Register GINTC_CONFIG_REG0[31:24] can mask gic irq [63:56]
58	riscv_sys_irq_i[10]	0x00E8	Register GINTC_CONFIG_REG1[7:0] can mask gic irq [71:64]
59	riscv_sys_irq_i[11]	0x00EC	Register GINTC_CONFIG_REG1[15:8] can mask gic irq [79:72]
60	riscv_sys_irq_i[12]	0x00F0	Register GINTC_CONFIG_REG1[23:16] can mask gic irq [87:80]
61	riscv_sys_irq_i[13]	0x00F4	Register GINTC_CONFIG_REG1[31:24] can mask gic irq [95:88]
62	riscv_sys_irq_i[14]	0x00F8	Register GINTC_CONFIG_REG2[7:0] can mask gic irq [103:96]
63	riscv_sys_irq_i[15]	0x00FC	Register GINTC_CONFIG_REG2[15:8] can mask gic irq [111:104]
64	riscv_sys_irq_i[16]	0x0100	Register GINTC_CONFIG_REG2[23:16] can mask gic irq [119:112]
65	riscv_sys_irq_i[17]	0x0104	Register GINTC_CONFIG_REG2[31:24] can mask gic irq [127:120]
66	riscv_sys_irq_i[18]	0x0108	Register GINTC_CONFIG_REG3 [7:0] can mask gic irq [135:128]

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

67	riscv_sys_irq_i[19]	0x010C	Register GINTC_CONFIG_REG3[15:8] can mask gic irq [143:136]
68	riscv_sys_irq_i[20]	0x0110	Register GINTC_CONFIG_REG3[23:16] can mask gic irq [151:144]
69	riscv_sys_irq_i[21]	0x0114	Register GINTC_CONFIG_REG3[31:24] can mask gic irq [159:152]
70	riscv_sys_irq_i[22]	0x0118	Register GINTC_CONFIG_REG4[7:0] can mask gic irq [167:160]
71	riscv_sys_irq_i[23]	0x011C	Register GINTC_CONFIG_REG4[15:8] can mask gic irq [175:168]
72	riscv_sys_irq_i[24]	0x0120	Register GINTC_CONFIG_REG4[23:16] can mask gic irq [183:176]
73	riscv_sys_irq_i[25]	0x0124	Register GINTC_CONFIG_REG4[31:24] can mask gic irq [191:184]
74	riscv_sys_irq_i[26]	0x0128	Register GINTC_CONFIG_REG5[7:0] can mask gic irq [199:192]
75	riscv_sys_irq_i[27]	0x012C	Register GINTC_CONFIG_REG5[15:8] can mask gic irq [207:200]
76	riscv_sys_irq_i[28]	0x0130	Register GINTC_CONFIG_REG5[23:16] can mask gic irq [215:208]
77	riscv_sys_irq_i[29]	0x0134	Register GINTC_CONFIG_REG5[31:24] can mask gic irq [223:216]
78~79	Reserved	0x0138 ~0x013C	Reserved

12.3.3 Register List

Module Name	Base Address
RISCV CLIC	0xE080_0000

Register Name	Offset	Description
CLIC_CFG_REG	0x0000	CLIC Configuration Register
CLIC_MINTTHRESH_REG	0x0008	CLIC MINTTHRESH Register
CLIC_INT_REGn	0x1000+0x4*N(N=0~63)	CLIC Interrupt Register n

12.3.4 Register description

12.3.4.1 0x0000 CLIC Configuration Register (Default Value: 0x0000_0001)

Offset: 0x0000	Register Name: CLICCFG_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:5	R/W	0x0	NM Effective Bits in the Privilege Mode This bit is fixed to 0, as RISC-V only supports processing interrupts in machine mode. No matter what the value of CLICINTATTR MODE bit in CLIC_INT_REGn register is, it is considered to be interrupt processing in machine mode.
4:1	R/W	0x0	NL Effective Bits in the Interrupt Priority Level The number of effective bits in the interrupt priority level is fixed to 8. If the number is less than 8, you can fill with 1.
0	R/W	0x1	NV Interrupt Flag in the Hardware Vector Mode This bit is fixed to 1, indicating that the CLIC controller supports processing interrupts in the hardware vector mode. To enable hardware vector interrupt, set CLIC_INT_REGn (bit[16]) to 1. The entry address of the interrupts in the hardware vector mode can be obtained by a hardware two-level jump. Specifically, RISC-V fetches data from the address of MTVT+ interrupt ID*4 after saving the processor scene; the data is the entry address of the interrupt ID service program. RISC-V jumps to the address to execute interrupt service procedure. The entry address of interrupts in other modes is MTVEC[31:6]<<6, where the RISC-V will process interrupts.

12.3.4.2 0x0008 CLIC_MINTTHRESH_REG (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CLIC_MINTTHRESH_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	MTH Threshold in the Machine Mode
23:0	/	/	/

12.3.4.3 0x1000+0x4*N (N=0~63) Interrupt Register n (Default Value: 0x1FC0_0000)

Offset: 0x1000+0x4*N (N=0~63)	Register Name: CLIC_INT_REGn

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:29	R/W	0x0	CLICINTCTL_PRIO Interrupt Arbitration Priority Level
28:24	R	0x1f	CLICINTCTL_PRIO_LOW. The lower 5 bits of Interrupt Arbitration Priority Level is fixed at 1.
23:22	R/W	0x3	CLICINTATTR_MODE Interrupt privilege level The bit field is used to configure interrupt privilege level. As E902 merely supports responding interrupts in the machine mode, CLICINTATTR MODE is fixed as 2 b11, indicating the machine mode interrupt.
21:19	/	/	/
18:17	R/W	0x0	CLICINTATTR_TRIG Interrupt trigger Method The bit field is used to distinguish between pulse interrupt and level interrupt. CLICINTATTR_TRIG [0] = 0: Level Interrupt CLICINTATTR_TRIG [0] = 1: Pulse Interrupt CLICINTATTR_TRIG [1] =0: Triggered on Rising Edge CLICINTATTR_TRIG[1]=1: Triggered on Falling Edge
16	R/W	0x0	CLICINTATTR_SHV Hardware vector interrupt The bit indicates whether it is hardware vector interrupt.
15:9	/	/	/
8	R/W	0x0	CLICINTIE Interrupt Enable
7:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

0	R/W	0x0	CLICINTIP Interrupt Pending **Level Interrupt Mode** the CLICINTIP bit is read-only. To modify the value of this bit, you could set the external interrupt source directly: If external interrupt source is high level, IP = 1. If external interrupt source is low level, IP =0. **Pulse Interrupt Mode** the CLICINTIP bit can be read or written. **Hardware Vector mode:** The IP can be cleared automatically while RISC-V responds interrupt requests. **Non-hardware Vector mode:** While RISC-V executes a CSR command, it is suggested to perform effective reading and writing operations on MNXTI register to obtain the waiting status of interrupt and the corresponding value of IP will be cleared automatically at the same time. If the interrupt request is transmitted to the RISC-V pipeline core directly, hardware is not able to clear the value of IP when RISC-V responds this interrupt. It needs to be cleared by software.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

13 DMA

13.1 DMA Controller (DMAC)

13.1.1 Overview

The direct memory access (DMA) is a method of transferring data between peripherals and memories (including the SRAM and DRAM) without using the CPU. The data can be transferred between a peripheral and a memory, between peripherals, or between memories through DMA. It is an efficient way to offload data transfer duties from the CPU.

The DMAC has the following features:

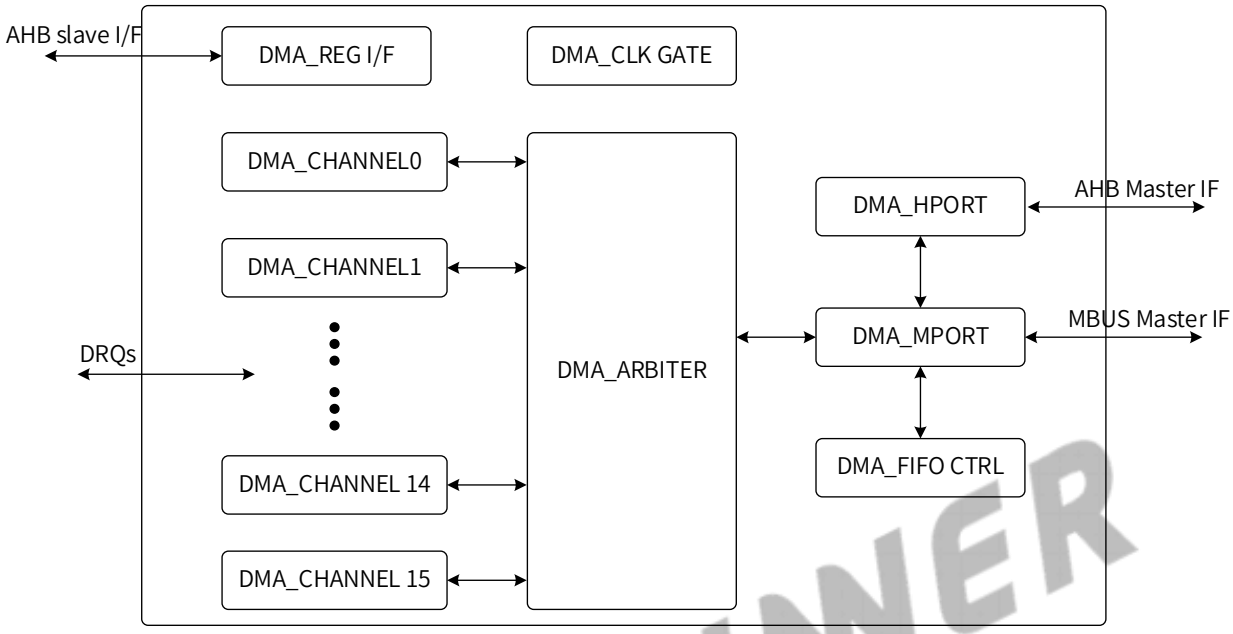
- Two 16-channel DMAs. One is in CPUX domain and the other is in CPUS domain.
- Supports DMA channel number configuration through parameters
- Supports reading or writing up to 64 peripheral DMA requests
- Supports chained transfer
- Supports programmable 8-/16-/32-/64-bit data width
- Supports programmable DMA burst length
- DRQ response includes waiting mode and handshake mode
- Supports non-aligned transfer for memory devices
- DMA channels support pausing, bmode, timeout, and IO speed mode

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

13.1.2 Block Diagram

The following figure shows a block diagram of DMAC.

Figure 13-1 DMAC Block Diagram



DMAC contains the following sub-blocks:

Table 13-1 DMAC Sub-blocks

Sub-block	Description
DMA_ARBITER	The port arbitrates the DMA read/write requests from all channels, and converts the requests to the read/write requests of ports.
DMA_CHANNELs	DMA transfer engine. Each channel is independent. The system uses the polling mechanism to decide the priorities of DMA channels. When the DMA requests from multiple peripherals are valid simultaneously, the channel with the higher priority starts data transfer first. When DMA_ARBITER is idle, channel 0 has the highest priority, whereas channel 7 has the lowest priority. When DMA_ARBITER is busy with processing the request from channel n, channel (n+1) has the highest priority.
DRQs	DMA requests. Peripherals use the DMA request signals to request a data transfer.
DMA_MPORT	The port receives the read/write requests from DMA_ARBITER, and converts them to the corresponding MBUS access requests. It is mainly used for accessing the DRAM.
DMA_HPORT	The port for accessing the AHB Master. It is mainly used for accessing the SRAM and IO devices.
DMA_FIFO CTRL	Internal FIFO cell control module.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Sub-block	Description
DMA_REG Interface	DMA_REG is the common register module that is mainly used to resolve AHB1 demands.
DMA_CLKGATE	The control module for hardware auto clock gating.

The DMAC integrates 16 independent DMA channels and each channel has an independent FIFO controller. When the DMA channel starts, the DMAC gets a DMA descriptor from the DMA_DESC_ADDR_REG and uses it as the configuration information for the data transfer of the current DMA package. Then the DMAC can transfer data between the specified devices. After transferring a DMA package, the DMAC judges whether the current channel transfer is finished via the linked address in the descriptor. If the linked address shows all the packages are transferred, the DMAC will end the chain transmission and close the channel.

13.1.3 Clock Sources

The DMAC is mounted on AHB and MBUS. Their clock frequencies influence the transfer efficiency of the DMAC.

13.1.4 Functional Description

13.1.4.1 DRQ Port Types

The following tables show the source DRQ types and destination DRQ types of different ports in CPUX domain and CPUS domain.

Table 13-2 DMA DRQ Types in CPUX domain

Source DRQ Type		Destination DRQ Type	
port0	SRAM	port0	SRAM
port1	DRAM	port1	DRAM
port2	OWA	port2	OWA
port3	I2S0_RX	port3	I2S0_TX
port4	I2S1_RX	port4	I2S1_TX
port5	I2S2_RX	port5	I2S2_TX
port6	I2S3_RX	port6	I2S3_TX
port7	I2S4_RX	port7	I2S4_TX
port8		port8	
port9	DMIC	port9	
port10	NAND	port10	NAND
port11	GPADC	port11	
port12		Port12	
port13		port13	IR_TX
port14	UART0-RX	port14	UART0-TX
port15	UART1-RX	port15	UART1-TX
port16	UART2-RX	port16	UART2-TX
port17	UART3-RX	port17	UART3-TX

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Source DRQ Type		Destination DRQ Type	
port18	UART4-RX	port18	UART4-TX
port19	UART5-RX	port19	UART5-TX
port20	UART6-RX	Port20	UART6-TX
port21		port21	
port22		port22	
port23	SPI0-RX	port23	SPI0-TX
port24	SPI1-RX	port24	SPI1-TX
port25	SPI2-RX	port25	SPI2-TX
port26	SPI3-RX	port26	SPI3-TX
port27	USB0_DEVICE_EP1	port27	USB0_DEVICE_EP1
port28	USB0_DEVICE_EP2	port28	USB0_DEVICE_EP2
port29	USB0_DEVICE_EP3	port29	USB0_DEVICE_EP3
Port30	USB0_DEVICE_EP4	Port30	USB0_DEVICE_EP4
Port31	USB0_DEVICE_EP5	Port31	USB0_DEVICE_EP5
Port32	USB0_DEVICE_EP6	Port32	USB0_DEVICE_EP6
Port33	USB0_DEVICE_EP7	Port33	USB0_DEVICE_EP7
Port34	USB0_DEVICE_EP8	Port34	USB0_DEVICE_EP8
Port35		Port35	
Port36		Port36	
Port37	TWI0	Port37	TWI0
Port38	TWI1	Port38	TWI1
Port39	TWI2	Port39	TWI2
Port40	TWI3	Port40	TWI3
Port41	TWI4	Port41	TWI4
Port42	TWI5	Port42	TWI5
Port43	TWI6	Port43	TWI6
Port44	TWI7	Port44	TWI7
Port45	TWI8	Port45	TWI8
Port46		Port46	LEDC
Port47	S_TWI0	Port47	S_TWI0
Port48	S_TWI1	Port48	S_TWI1
Port49	S_TWI2	Port49	S_TWI2
Port50	S_UART0	Port50	S_UART0
Port51	S_UART1	Port51	S_UART1
Port52		Port52	
Port53	S_SPI	Port53	S_SPI
Port54		Port54	
Port55		Port55	
Port56		Port56	
Port57		Port57	
Port58	TWI9	Port58	TWI9
Port59	TWI10	Port59	TWI10

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Source DRQ Type		Destination DRQ Type	
Port60	TWI11	Port60	TWI11
Port61	TWI12	Port61	TWI12
Port62		Port62	
Port63	SMHC3	Port63	SMHC3

13.1.4.2 DMAC Descriptor

The DMAC descriptor is the configuration information of DMA transfer and decides the DMA working mode. Each descriptor includes 6 words: Configuration, Source Address, Destination Address, Byte Counter, Parameter, and Link.

- **Configuration:** It is mainly used for configuring the following information by DMA_CFG_REG.
  - **DRQ type**: DRQ type of the source and destination devices.
  - **Address counting mode**: For both the source and destination devices, there are two address counting modes: the IO mode and linear mode. The IO mode is for IO devices whose address is fixed during the data transfer and the linear mode is for the memory whose address is increasing during the data transfer.
  - **Transferred block length**: The amount of data that non-memory peripherals can transfer in a valid DRQ. The block length supports 1 beat, 4 beats, 8 beats, and 16 beats.
  - **Transferred data width**: The data width of operating the non-memory peripherals. The data width supports 8 bits, 16 bits, 32 bits, and 64 bits.
  - **BMODE mode:** It is used in the following scenario: the source is an IO device, and the destination is a memory device. In this mode, the data amount of DMA block transmission can be limited to that when the DRQ threshold of source IO device is 1.
- **Source Address**: It configures the address of the source device.
- **Destination Address**: It configures the address of the destination device. DMA reads data from the source address and then writes data to the destination address.
- **Byte counter**: It configures the data amount of a package. The maximum value is (2^25-1) bytes. If the data amount of the package reaches the maximum value, even if DRQ is valid, the DMA will stop the current transfer.
- **Parameter**: It configures the interval of each data block and is only valid for non-memory devices. When detecting that the DRQ holds high, the DMA will start block transmission regardless of the DRQ change. When transmission ends, DMA will wait the set period and continue to the next DRQ detection.

  In addition, the Parameter is responsible for enabling and configuring TIMEOUT. In the case that the source device is an I/O device and the destination device is a memory device, the waiting time of a DRQ signal triggered by the source device can be set when TIMEOUT is enabled. When time is out, an interrupt signal of TIMEOUT will be generated by DMA. There are three sub-functions of TIMEOUT to be enabled (TIMEOUT will only generate interrupts if they are disabled): suspend the transmission of the current channel after an interrupt is

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

generated; end the transmission of the current channel after an interrupt is generated; skip to the next descriptor for transmission after an interrupt is generated. (TIMEOUT only can be enabled in BMODE.)

The Parameter also configures whether the IOspeed is enabled or not. If IOspeed is enabled, DMA will transmit the data of the I/O device from the source device or the destination device, or both of them at a faster speed. The larger block indicates a faster speed. However, when the block is 1, the speed won t change even if the IO speed is enabled.

If the address bit of the link and parameter is 0xFFFFF800, the DMAC will stop the data transfer after transferring the package; if the address bit of the link and parameter is not 0xFFFFF800, the address bit will be considered as the address of the next package configuration, which is called the chained multi-package transfer.

Figure 13-2 DMA Chained Transfer

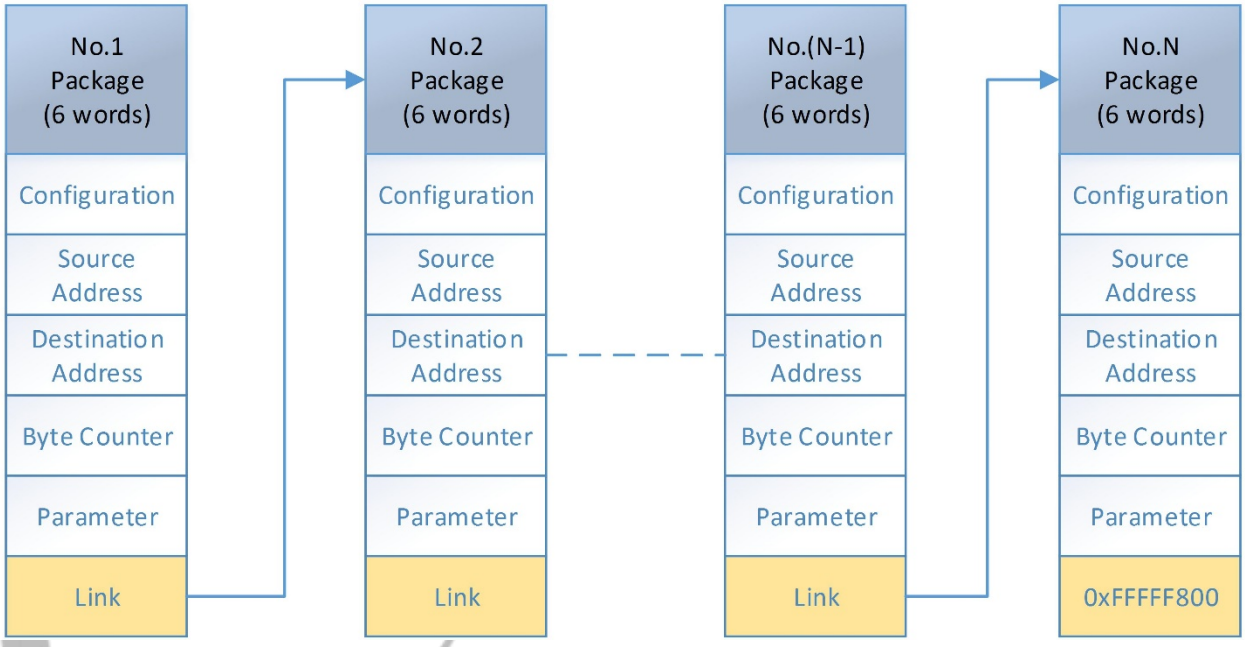


Table 13-3 DMA Address Descriptors

Descriptor Group	Bit	Description
Source Address	31:0	DMA transfers the lower 32 bits of the 34-bit source address
Destination Address	31:0	DMA transfers the lower 32 bits of the 34-bit destination address
Parameter	31:20	TIMEOUT Enable ([bit31]) When using this function, BMODE should be enabled, and IOspeed should be disabled.
		TIMEOUT Configuration ([bit30:29]) 00: Not use sub-functions 01: Generate an interrupt and suspend the transmission after timeout. 10: Generate an interrupt and end the transmission after timeout.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

		11: Generate an interrupt and skip to the next descriptor for transmission after timeout.
		TIMEOUT Configuration ([bit28:20]) Timer time of channels.
	19:18	Reserved
	17:15	The higher 3 bits of 35-bit byte destination address of DMA transfer
	14	Reserved
	13:11	The higher 3 bits of 35-bit byte source address of DMA transfer
	10	Reserved
	9	The next descriptor address of DMA. The bit33 of word address.
	8	When DMA transfers IO device data from source or destination address, DMA will improve the rate of transferring IO device data. BMODE and TIMEOUT cannot be enabled simultaneously.
	7:0	Wait Clock Cycles Set the waiting time in DRQ mode
Link	31:2	The lower 30 bits of the word address in the next group of descriptor
	1:0	The higher 2 bits of the word address in the next group of descriptor

From the above table:

True DMA source address (in byte mode) = {Parameter [13:11], Source Address [31:0]};

True DMA destination address (in byte mode) = {Parameter [17:15], Destination Address [31:0]};

True link address (in byte mode) = { Parameter [9], Link[1:0], Link[31:2],2 b00}.

13.1.4.3 Interrupts

There are four kinds of DMA interrupts: the half package interrupt, package end interrupt, queue end interrupt, and timeout interrupt.

- Half package interrupt

When enabled, the DMAC sends out a half package interrupt after transferring half of a package.

- Package end interrupt

When enabled, the DMAC sends out a package end interrupt after transferring a complete package.

- Queue end interrupt

When enabled, the DMAC sends out a queue end interrupt after transferring a complete queue.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- Timeout interrupt

If TIMEOUT is enabled, DMA will generate a timeout interrupt after timeout.

Notice that when CPU does not respond to the interrupts timely, or two DMA interrupts are generated very closely, the later interrupt may override the former one. As for CPU, the DMAC has only a system interrupt source.

13.1.4.4 Security

The DMAC supports system TrustZone and the security mode configuration of the DMA channel.

Each DMA channel is secure by default. When the TrustZone is enabled, the DMAC is secure, only the secure devices can access the DMAC.

When a DMA channel is configured to the non-secure mode, this channel can only access the non-secure area of the memory, that is, the DMAC cannot write data to the secure area of the memory, and the read-back data from the secure area of the memory is 0.

13.1.4.5 Clock Gating

The DMA_CLK_GATE module can auto control clock gating by hardware, which is mainly used for generating clocks for DMAC sub-modules and some of their circuits.

The DMA_CLK_GATE module consists of two parts: the channel clock gate and the common clock gate.

Channel Clock Gate: When the system accesses the registers of the enabled DMA channels, the channel clock gate will be automatically open. When the system finishes accessing or the DMA data transfer is completed, the channel clock gate will be automatically closed after a 16-HCLK-cycle delay; also, the related circuit clocks, such as channel control and FIFO control, will be closed.

Common Clock Gate: When all the DMA channels are closed, the clock gates of common circuits will be automatically closed. The common circuits include the common circuits of FIFO control modules, MPORT modules, and MBUS.

Whether DMA clock gating can support all the functions stated above or not is decided by software.

13.1.4.6 Transfer Mode

The peripherals initiate data transfer by transmitting DMA request signals to the DMAC. After receiving the request signal, the DMAC converts it to the internal DRQ signal and controls the DMA data transfer.

The DMAC supports two data transfer modes: the waiting mode and handshake mode.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Waiting Mode

a) When the DMAC detects a valid external request signal, the DMAC starts to operate the peripheral device. The internal DRQ always holds high before the transferred data amount reaches the transferred block length.

b) When the transferred data amount reaches the transferred block length, the internal DRQ will pull low automatically.

c) The internal DRQ holds low for certain clock cycles (WAIT_CYC), and then the DMAC restarts to detect the external requests. If the external request signal is valid, then the next transfer starts.

Handshake Mode

a) When the DMAC detects a valid external request signal, the DMAC starts to operate the peripheral device. The internal DRQ always holds high before the transferred data amount reaches the transferred block length.

b) When the transferred data amount reaches the transferred block length, the internal DRQ will be pulled down automatically. For the last data transfer of the block, the DMAC sends a DMA Last signal with the DMA commands to the peripheral device. The DMA Last signal will be packed as part of the DMA commands and transmitted on the bus. It is used to inform the peripheral device that it is the end of the data transfer for the current DRQ.

c) When the peripheral device receives the DMA Last signal, it can judge that the data transfer for the current DRQ is finished. To continue the data transfer, it sends a DMA Active signal to the DMAC.

NOTE

A DMA Active signal will be converted to one DRQ signal in the DMA module. To generate multiple DRQs, the peripheral devices need to send out multiple DMA Active signals via the bus protocol.

d) When the DMAC receives the DMA Active signal, it will send back a DMA ACK signal to the peripheral device.

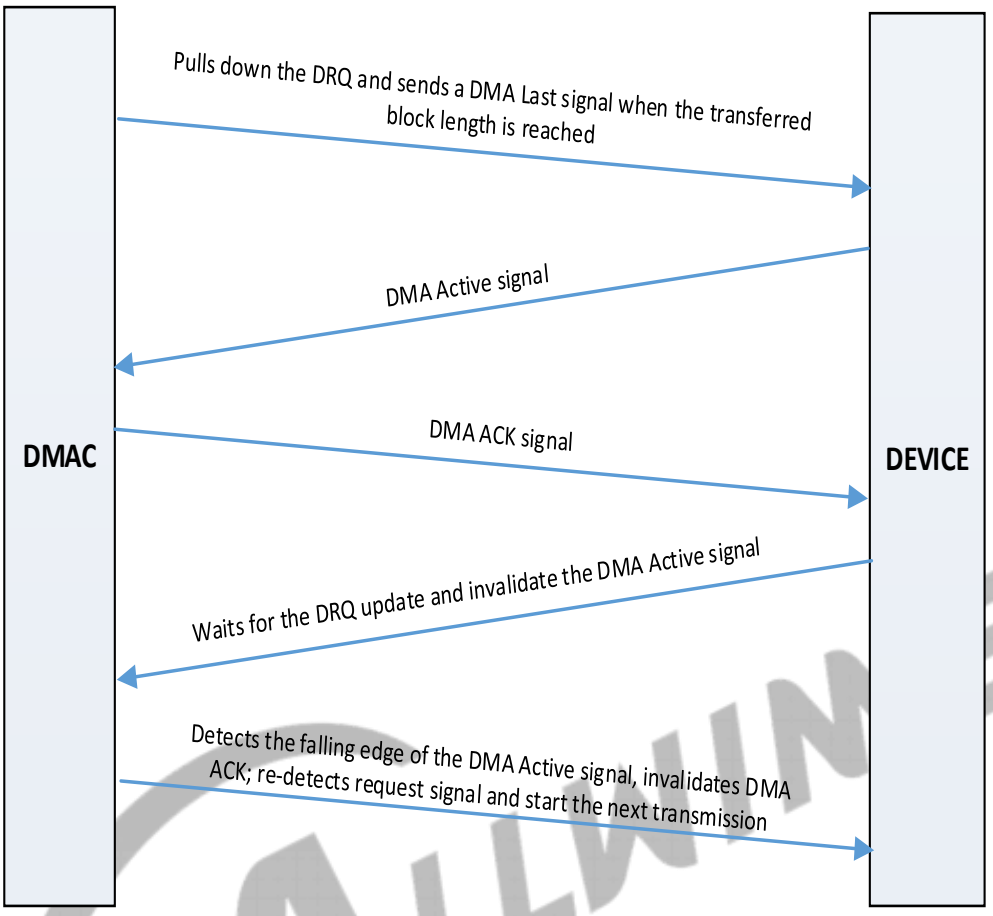
e) When the peripheral device receives the DMA ACK signal, it will wait for all the operations on the local device to be completed, and both the FIFO and DRQ status are refreshed. Then it invalidates the DMA Active signal.

f) When the DMAC detects the falling edge of the DMA Active signal, it invalidates the corresponding DMA ACK signal, and restarts to detect the external request signals. If a valid request signal is detected, the next data transfer starts.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

The following figure shows the workflow of the handshake mode.

Figure 13-3 Workflow of the DMAC Handshake Mode



13.1.4.7 Address Auto-Alignment

For the non-IO devices whose start address is not 32-byte-aligned, the DMAC will align the address to the 32-byte through the burst transfer within 32 bytes, which will improve the DRAM access efficiency.

The following example shows how the DMAC adjusts the address: when the peripheral device of a DMA channel is a non-IO device whose start address is 0x86 (not 32-byte-aligned), the DMAC firstly uses a 26-byte burst transfer to align the address to 0xA0 (32-byte-aligned), and then transfers data by 64-byte burst (the maximum transfer amount that MBUS allows).

The IO devices do not support address alignment, so the bit width of IO devices must match the address offset; otherwise, the DMAC will ignore the inconsistency and directly transmit data of the corresponding bit width to the address.

The address of the DMA descriptor does not support the address auto-alignment. Make sure the address is word-aligned; otherwise the DMAC cannot identify the descriptor.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

13.1.5 Programming Guidelines

13.1.5.1 DMAC Clock Control

a) If the DMAC clock is synchronous with the AHB clock, enable the DMAC gating bit of AHB clock before accessing the DMAC register.

b) If the reset input signal of the DMAC is asynchronous with AHB0 and is low valid by default, de-assert the reset signal of the DMAC before accessing the DMA register.

c) To avoid the indefinite state within registers, de-assert the reset signal first, and then enable the gating bit of AHB.

d) As the DMAC supports Clock Auto Gating function, it will automatically disable the DMAC clock in the idle state to reduce power consumption. The Clock Auto Gating is enabled by default.

13.1.5.2 DMAC Transfer Procedure

The DMAC transfer procedure is as follows.

Step 1 Configure DMA_IRQ_CPU_EN_REG and DMA_IRQ_CPUS_EN_REG register to select an channel interrupt to transmit to CPU field or CPUS field. If no configuration, the interrupt will transmit to both CPU field and CPUS field.

Step 2 Request DMA channel, and check if the DMA channel is idle by checking if it is enabled. A disabled channel indicates it is idle, while an enabled channel indicates it is busy.

Step 3 Write the descriptor with 6 words into the memory. The descriptor must be word-aligned. For more details, refer to the section DMA Descriptor.

Step 4 Write the start address of the descriptor to DMA_DESC_ADDR_REG and DMA_DESC_HIG_ADDR_REG.

Step 5 Enable the DMA channel, and write the corresponding channel to DMA_EN_REG.

Step 6 The DMA obtains the descriptor information.

Step 7 Start to transmit a package. When half of the package is completed, the DMA sends a Half Package Transfer Interrupt; when a total package is completed, the DMA sends a Package End Transfer Interrupt. This interrupt status can be read by DMA_IRQ_PEND_REG.

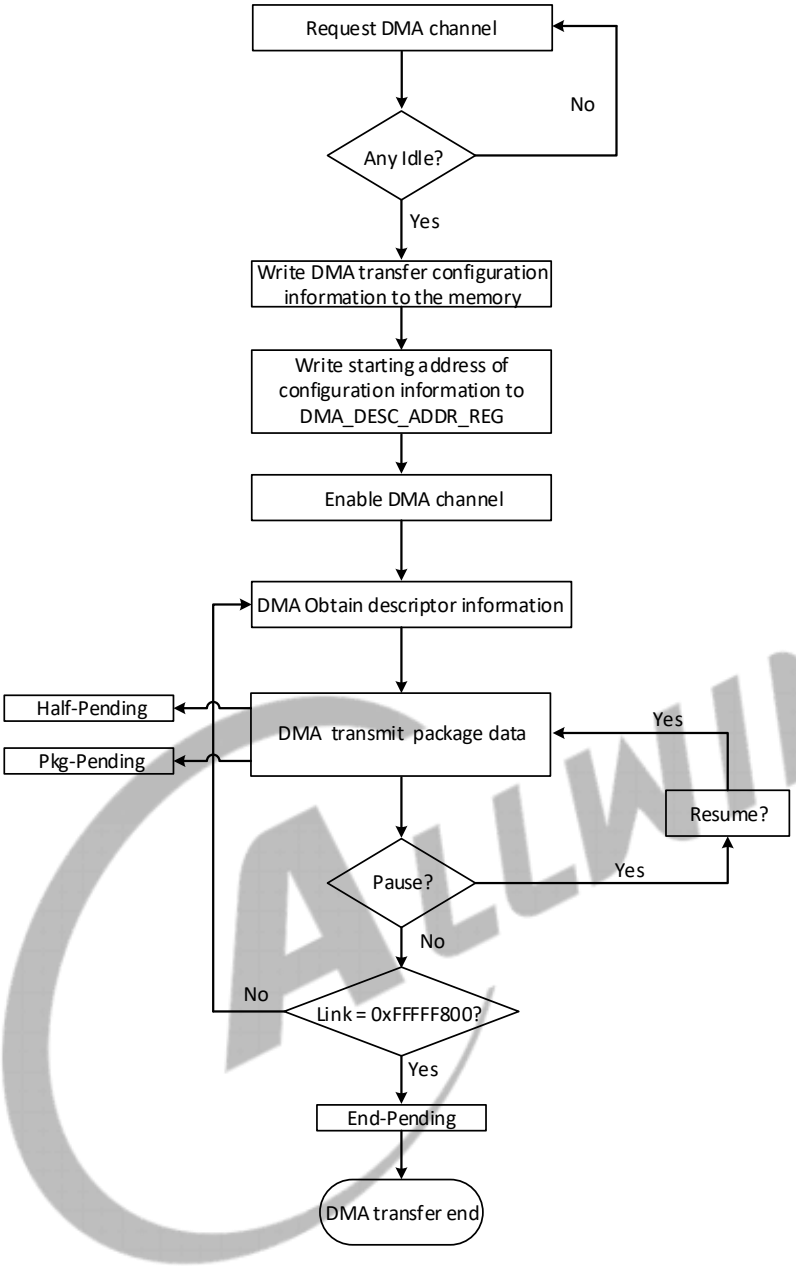
Step 8 Set DMA_PAU_REG to pause or resume the data transfer.

Step 9 After completing a total package transfer, the DMA decides to start the next package transfer or end the transfer by the link of the descriptor. If the link is 0xFFFFF800, the transfer ends; otherwise, the next package starts to transmit. When the transfer ends, the DMA sends a Queue End Transfer Interrupt.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 10 Disable the DMA channel.

Figure 13-4 DMAC Transfer Process



13.1.5.3 Interrupt Processing

Follow the steps below to process the DMAC interrupt:

Step 1 Write the corresponding interrupt enable bit of DMA_IRQ_EN_REG. The system generates an interrupt when the corresponding condition is satisfied.

Step 2 After entering the interrupt process, write to clear the interrupt pending and execute the process of waiting for the interrupt.

Step 3 Resume the interrupt and continue to execute the interrupted process.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

13.1.6 Register List

Module Name	Base Address
DMA0	0x04601000
DMA1	0x04024000

Register Name	Offset	Description
DMA_SEC_REG	0x0020	DMA Security Register
DMA_AUTO_GATE_REG	0x0028	DMA Auto Gating Register
DMA_STA_REG	0x0030	DMA Status Register
DMA_IRQ_CPU_EN_REG	0x0034	DMA IRQ Transfer to CPU Field Enable Register
DMA_IRQ_CPUS_EN_REG	0x0038	DMA IRQ Transfer to CPUS Field Enable Register
DMA_EN_REG	0x0100+0x0000+N*0x0040 (N=0~15)	DMA Channel Enable Register
DMA_PAU_REG	0x0100+0x0004+N*0x0040 (N=0~15)	DMA Channel Pause Register
DMA_DESC_ADDR_REG	0x0100+0x0008+N*0x0040 (N=0~15)	DMA Channel Descriptor Address Register
DMA_CFG_REG	0x0100+0x000C+N*0x0040 (N=0~15)	DMA Channel Configuration Register
DMA_CUR_SRC_REG	0x0100+0x0010+N*0x0040 (N=0~15)	DMA Channel Current Source Address Register
DMA_CUR_DEST_REG	0x0100+0x0014+N*0x0040 (N=0~15)	DMA Channel Current Destination Address Register
DMA_BCNT_LEFT_REG	0x0100+0x0018+N*0x0040 (N=0~15)	DMA Channel Byte Counter Left Register
DMA_PARA_REG	0x0100+0x001C+N*0x0040 (N=0~15)	DMA Channel Parameter Register
DMA_MODE_REG	0x0100+0x0028+N*0x0040 (N=0~15)	DMA Mode Register
DMA_FDESC_ADDR_REG	0x0100+0x002C+N*0x0040 (N=0~15)	DMA Former Descriptor Address Register
DMA_PKG_NUM_REG	0x0100+0x0030+N*0x0040 (N=0~15)	DMA Package Number Register
DMA_IRQ_EN_REG	0x0100+0x0034+N*0x0040 (N=0~15)	DMA IRQ Enable Register
DMA_IRQ_PEND_REG	0x0100+0x0038+N*0x0040 (N=0~15)	DMA IRQ Pending Status Register
DMA_DESC_HIG_ADDR_REG	0x0100+0x003C+N*0x0040 (N=0~15)	DMA Channel Descriptor Highest Address Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

13.1.7 Register Description

13.1.7.1 0x0020 DMA Security Register (Default Value: 0x0000_FFFF)

Offset: 0x0020			Register Name: DMA_SEC_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x1	DMA15_SEC DMA channel 15 security. 0: Secure. 1: Non-secure.
14	R/W	0x1	DMA14_SEC DMA channel 14 security. 0: Secure. 1: Non-secure.
13	R/W	0x1	DMA13_SEC DMA channel 13 security. 0: Secure. 1: Non-secure.
12	R/W	0x1	DMA12_SEC DMA channel 12 security. 0: Secure. 1: Non-secure.
11	R/W	0x1	DMA11_SEC DMA channel 11 security. 0: Secure. 1: Non-secure.
10	R/W	0x1	DMA10_SEC DMA channel 10 security. 0: Secure. 1: Non-secure.
9	R/W	0x1	DMA9_SEC DMA channel 9 security. 0: Secure. 1: Non-secure.
8	R/W	0x1	DMA8_SEC DMA channel 8 security. 0: Secure. 1: Non-secure.
7	R/W	0x1	DMA7_SEC DMA channel 7 security. 0: Secure. 1: Non-secure.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0020			Register Name: DMA_SEC_REG
Bit	Read/Write	Default/Hex	Description
6	R/W	0x1	DMA6_SEC DMA channel 6 security. 0: Secure. 1: Non-secure.
5	R/W	0x1	DMA5_SEC DMA channel 5 security. 0: Secure. 1: Non-secure.
4	R/W	0x1	DMA4_SEC DMA channel 4 security. 0: Secure. 1: Non-secure.
3	R/W	0x1	DMA3_SEC DMA channel 3 security. 0: Secure. 1: Non-secure.
2	R/W	0x1	DMA2_SEC DMA channel 2 security. 0: Secure. 1: Non-secure.
1	R/W	0x1	DMA1_SEC DMA channel 1 security. 0: Secure. 1: Non-secure.
0	R/W	0x1	DMA0_SEC DMA channel 0 security. 0: Secure. 1: Non-secure.

13.1.7.2 0x0028 DMA Auto Gating Register (Default Value: 0x00000000)

Offset: 0x0028			Register Name: DMA_AUTO_GATE_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	DMA_MCLK_CIRCUIT. DMA MCLK interface circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0028			Register Name: DMA_AUTO_GATE_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	DMA_COMMON_CIRCUIT. DMA common circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable
0	R/W	0x0	DMA_CHAN_CIRCUIT. DMA channel circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable

Note: When initializing DMA Controller, bit-2 should be set up.

13.1.7.3 0x0030 DMA Status Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: DMA_STA_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	MBUS_FIFO_STATUS MBUS FIFO Status 0: Empty 1: Not Empty
30:16	/	/	/
15	R	0x0	DMA15_STATUS DMA Channel 15 Status. 0: Idle 1: Busy
14	R	0x0	DMA14_STATUS DMA Channel 14 Status. 0: Idle 1: Busy
13	R	0x0	DMA13_STATUS DMA Channel 13 Status. 0: Idle 1: Busy
12	R	0x0	DMA12_STATUS DMA Channel 12 Status. 0: Idle 1: Busy
11	R	0x0	DMA11_STATUS DMA Channel 11 Status. 0: Idle 1: Busy

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0030			Register Name: DMA_STA_REG
Bit	Read/Write	Default/Hex	Description
10	R	0x0	DMA10_STATUS DMA Channel 10 Status. 0: Idle 1: Busy
9	R	0x0	DMA9_STATUS DMA Channel 9 Status. 0: Idle 1: Busy
8	R	0x0	DMA8_STATUS DMA Channel 8 Status. 0: Idle 1: Busy
7	R	0x0	DMA7_STATUS DMA Channel 7 Status. 0: Idle 1: Busy
6	R	0x0	DMA6_STATUS DMA Channel 6 Status. 0: Idle 1: Busy
5	R	0x0	DMA5_STATUS DMA Channel 5 Status. 0: Idle 1: Busy
4	R	0x0	DMA4_STATUS DMA Channel 4 Status. 0: Idle 1: Busy
3	R	0x0	DMA3_STATUS DMA Channel 3 Status. 0: Idle 1: Busy
2	R	0x0	DMA2_STATUS DMA Channel 2 Status. 0: Idle 1: Busy
1	R	0x0	DMA1_STATUS DMA Channel 1 Status. 0: Idle 1: Busy

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0030			Register Name: DMA_STA_REG
Bit	Read/Write	Default/Hex	Description
0	R	0x0	DMA0_STATUS DMA Channel 0 Status. 0: Idle 1: Busy

13.1.7.4 0x0034 DMA IRQ Transfer to CPU Field Enable Register (Default Value: 0x0000_FFFF)

Offset: 0x0034			Register Name: DMA_IRQ_CPU_EN_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x1	DMA15_IRQ_CPU_EN Control whether the DMA Channel 15 IRQ signal can transfer to CPU field or not. 0: cannot transfer to CPU field 1: can transfer to CPU field
14	R/W	0x1	DMA14_IRQ_CPU_EN Control whether the DMA Channel 14 IRQ signal can transfer to CPU field or not. 0: cannot transfer to CPU field 1: can transfer to CPU field
13	R/W	0x1	DMA13_IRQ_CPU_EN Control whether the DMA Channel 13 IRQ signal can transfer to CPU field or not. 0: cannot transfer to CPU field 1: can transfer to CPU field
12	R/W	0x1	DMA12_IRQ_CPU_EN Control whether the DMA Channel 12 IRQ signal can transfer to CPU field or not. 0: cannot transfer to CPU field 1: can transfer to CPU field
11	R/W	0x1	DMA11_IRQ_CPU_EN Control whether the DMA Channel 11 IRQ signal can transfer to CPU field or not. 0: cannot transfer to CPU field 1: can transfer to CPU field
10	R/W	0x1	DMA10_IRQ_CPU_EN Control whether the DMA Channel 10 IRQ signal can transfer to CPU field or not. 0: cannot transfer to CPU field 1: can transfer to CPU field

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0034			Register Name: DMA_IRQ_CPU_EN_REG
Bit	Read/Write	Default/Hex	Description
9	R/W	0x1	DMA9_IRQ_CPU_EN Control whether the DMA Channel 9 IRQ signal can transfer to CPU field or not. 0: cannot transfer to CPU field 1: can transfer to CPU field
8	R/W	0x1	DMA8_IRQ_CPU_EN Control whether the DMA Channel 8 IRQ signal can transfer to CPU field or not. 0: cannot transfer to CPU field 1: can transfer to CPU field
7	R/W	0x1	DMA7_IRQ_CPU_EN Control whether the DMA Channel 7 IRQ signal can transfer to CPU field or not. 0: cannot transfer to CPU field 1: can transfer to CPU field
6	R/W	0x1	DMA6_IRQ_CPU_EN Control whether the DMA Channel 6 IRQ signal can transfer to CPU field or not. 0: cannot transfer to CPU field 1: can transfer to CPU field
5	R/W	0x1	DMA5_IRQ_CPU_EN Control whether the DMA Channel 5 IRQ signal can transfer to CPU field or not. 0: cannot transfer to CPU field 1: can transfer to CPU field
4	R/W	0x1	DMA4_IRQ_CPU_EN Control whether the DMA Channel 4 IRQ signal can transfer to CPU field or not. 0: cannot transfer to CPU field 1: can transfer to CPU field
3	R/W	0x1	DMA3_IRQ_CPU_EN Control whether the DMA Channel 3 IRQ signal can transfer to CPU field or not. 0: cannot transfer to CPU field 1: can transfer to CPU field
2	R/W	0x1	DMA2_IRQ_CPU_EN Control whether the DMA Channel 2 IRQ signal can transfer to CPU field or not. 0: cannot transfer to CPU field 1: can transfer to CPU field

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0034			Register Name: DMA_IRQ_CPU_EN_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x1	DMA1_IRQ_CPU_EN Control whether the DMA Channel 1 IRQ signal can transfer to CPU field or not. 0: cannot transfer to CPU field 1: can transfer to CPU field
0	R/W	0x1	DMA0_IRQ_CPU_EN Control whether the DMA Channel 0 IRQ signal can transfer to CPU field or not. 0: cannot transfer to CPU field 1: can transfer to CPU field

13.1.7.5 0x0038 DMA IRQ Transfer to CPUS Field Enable Register (Default Value: 0x0000_FFFF)

Offset: 0x0038			Register Name: DMA_IRQ_CPUS_EN_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x1	DMA15_IRQ_CPUS_EN Control whether the DMA Channel 15 IRQ signal can transfer to CPUS field or not. 0: cannot transfer to CPUS field 1: can transfer to CPUS field
14	R/W	0x1	DMA14_IRQ_CPUS_EN Control whether the DMA Channel 14 IRQ signal can transfer to CPUS field or not. 0: cannot transfer to CPUS field 1: can transfer to CPUS field
13	R/W	0x1	DMA13_IRQ_CPUS_EN Control whether the DMA Channel 13 IRQ signal can transfer to CPUS field or not. 0: cannot transfer to CPUS field 1: can transfer to CPUS field
12	R/W	0x1	DMA12_IRQ_CPUS_EN Control whether the DMA Channel 12 IRQ signal can transfer to CPUS field or not. 0: cannot transfer to CPUS field 1: can transfer to CPUS field
11	R/W	0x1	DMA11_IRQ_CPUS_EN Control whether the DMA Channel 11 IRQ signal can transfer to CPUS field or not. 0: cannot transfer to CPUS field 1: can transfer to CPUS field

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0038			Register Name: DMA_IRQ_CPUS_EN_REG
Bit	Read/Write	Default/Hex	Description
10	R/W	0x1	DMA10_IRQ_CPUS_EN Control whether the DMA Channel 10 IRQ signal can transfer to CPUS field or not. 0: cannot transfer to CPUS field 1: can transfer to CPUS field
9	R/W	0x1	DMA9_IRQ_CPUS_EN Control whether the DMA Channel 9 IRQ signal can transfer to CPUS field or not. 0: cannot transfer to CPUS field 1: can transfer to CPUS field
8	R/W	0x1	DMA8_IRQ_CPUS_EN Control whether the DMA Channel 8 IRQ signal can transfer to CPUS field or not. 0: cannot transfer to CPUS field 1: can transfer to CPUS field
7	R/W	0x1	DMA7_IRQ_CPUS_EN Control whether the DMA Channel 7 IRQ signal can transfer to CPUS field or not. 0: cannot transfer to CPUS field 1: can transfer to CPUS field
6	R/W	0x1	DMA6_IRQ_CPUS_EN Control whether the DMA Channel 6 IRQ signal can transfer to CPUS field or not. 0: cannot transfer to CPUS field 1: can transfer to CPUS field
5	R/W	0x1	DMA5_IRQ_CPUS_EN Control whether the DMA Channel 5 IRQ signal can transfer to CPUS field or not. 0: cannot transfer to CPUS field 1: can transfer to CPUS field
4	R/W	0x1	DMA4_IRQ_CPUS_EN Control whether the DMA Channel 4 IRQ signal can transfer to CPUS field or not. 0: cannot transfer to CPUS field 1: can transfer to CPUS field
3	R/W	0x1	DMA3_IRQ_CPUS_EN Control whether the DMA Channel 3 IRQ signal can transfer to CPUS field or not. 0: cannot transfer to CPUS field 1: can transfer to CPUS field

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0038			Register Name: DMA_IRQ_CPUS_EN_REG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x1	DMA2_IRQ_CPUS_EN Control whether the DMA Channel 2 IRQ signal can transfer to CPUS field or not. 0: cannot transfer to CPUS field 1: can transfer to CPUS field
1	R/W	0x1	DMA1_IRQ_CPUS_EN Control whether the DMA Channel 1 IRQ signal can transfer to CPUS field or not. 0: cannot transfer to CPUS field 1: can transfer to CPUS field
0	R/W	0x1	DMA0_IRQ_CPUS_EN Control whether the DMA Channel 0 IRQ signal can transfer to CPUS field or not. 0: cannot transfer to CPUS field 1: can transfer to CPUS field

13.1.7.6 0x0100+0x0000+N*0x0040 (N=0~15) DMA Channel Enable Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0000+N*0x0040 (N=0~15)			Register Name: DMA_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	DMA_EN. DMA Channel Enable 0: Disable 1: Enable

13.1.7.7 0x0100+0x0004+N*0x0040 (N=0~15) DMA Channel Pause Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0004+N*0x0040 (N=0~15)			Register Name: DMA_PAU_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	DMA_PAUSE. Pausing DMA Channel Transfer Data. 0: Resume Transferring 1: Pause Transferring

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

13.1.7.8 0x0100+0x0008+N*0x0040 (N=0~15) DMA Channel Descriptor Address Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0008+N*0x0040 (N=0~15)			Register Name: DMA_DESC_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	DMA_DESC_LOW_ADDR DMA Channel Descriptor Word Address, Low 30bits. The Descriptor Address must be word-aligned.
1:0	R/W	0x0	DMA_DESC_HIGH_ADDR DMA Channel Descriptor High Address, High 2bits The real address is as below: DMA Channel Descriptor Address = {bit[1:0],bit[31:2],2'b00};

Note: The descriptor format is {DMA_DESC_HIG_ADDR_REG[0], DMA_DESC_HIGH_ADDR [1:0], DMA_DESC_LOW_ADDR[31:2],2 b00}

13.1.7.9 0x0100+0x000C+N*0x0040 (N=0~15) DMA Channel Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x000C+N*0x0040 (N=0~15)			Register Name: DMA_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R	0x0	BMODE_SEL Mode select 0: Normal Mode 1: BMODE
29:27	/	/	/
26:25	R	0x0	DMA_DEST_DATA_WIDTH. DMA Destination Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: 64-bit
24	R	0x0	DMA_ADDR_MODE. DMA Destination Address Mode 0: Linear Mode 1: IO Mode

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0100+0x000C+N*0x0040 (N=0~15)			Register Name: DMA_CFG_REG
Bit	Read/Write	Default/Hex	Description
23:22	R	0x0	DMA_DEST_BLOCK_SIZE. DMA Destination Block Size. 00: 1 01: 4 10: 8 11: 16
21:16	R	0x0	DMA_DEST_DRQ_TYPE. DMA Destination DRQ Type The details in DRQ Type and Port Corresponding Relation.
15:11	/	/	/
10:9	R	0x0	DMA_SRC_DATA_WIDTH. DMA Source Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: 64-bit
8	R	0x0	DMA_SRC_ADDR_MODE. DMA Source Address Mode 0: Linear Mode 1: IO Mode
7:6	R	0x0	DMA_SRC_BLOCK_SIZE. DMA Source Block Size. 00: 1 01: 4 10: 8 11: 16
5:0	R	0x0	DMA_SRC_DRQ_TYPE. DMA Source DRQ Type The details in DRQ Type and Port Corresponding Relation.

13.1.7.10 0x0100+0x0010+N*0x0040 (N=0~15) DMA Channel Current Source Address Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0010+N*0x0040 (N=0~15)			Register Name: DMA_CUR_SRC_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DMA_CUR_SRC. DMA Channel Current Source Address, read only.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

13.1.7.11 0x0100+0x0014+N*0x0040 (N=0~15) DMA Channel Current Destination Address Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0014+N*0x0040 (N=0~15)			Register Name: DMA_CUR_DEST_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DMA_CUR_DEST. DMA Channel Current Destination Address, read only.

13.1.7.12 0x0100+0x0018+N*0x0040 (N=0~15) DMA Channel Byte Counter Left Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0018+N*0x0040 (N=0~15)			Register Name: DMA_BCNT_LEFT_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:0	R	0x0	DMA_BCNT_LEFT. DMA Channel Byte Counter Left, read only.

Note: The data are not real-time. It will arrive the destination address after delaying for some time.

13.1.7.13 0x0100+0x001C+N*0x0040 (N=0~15) DMA Channel Parameter Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x001C+N*0x0040 (N=0~15)			Register Name: DMA_PARA_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	DMA_TO_EN. Timeout function Enable Bit 1: Enable 0: Disable
30:29	R	0x0	DMA_TO_FUN. Timeout function configuration: 01: Enabling pause channel transfer function after timeout 10: Enabling stop channel transfer function after timeout 11: Enabling jump next opcode function after timeout
28:20	R	0x0	DMA_TO_WAIT_CYC. The time cycle of waiting the start device to restart transferring data

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0100+0x001C+N*0x0040 (N=0~15)			Register Name: DMA_PARA_REG
Bit	Read/Write	Default/Hex	Description
19:18	/	/	/
17:15	R	0x0	DMA Channel Current Destination Address[34:32], read only.
14	/	/	/
13:11	R	0x0	DMA Channel Current Source Address[34:32], read only.
10	/	/	/
9	R	0x0	DMA next descriptor address[33](word address), read only.
8	R	0x0	DMA_IOSPEED_EN. Accelerating DMA speed when transferring the data of IO device 0: Disable 1: Enable
7:0	R	0x0	WAIT_CYC. Wait Clock Cycles

Note:

1. [28:20] time cycle formula is the required timing period*AHB clock frequency/4096. The time cycle should be integer.

2. Clock frequency is 200 MHz; clock cycle is 20.48 us; the maximum timing is 10.46 ms.

13.1.7.14 0x0100+0x0028+N*0x0040 (N=0~15) DMA Mode Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0028+N*0x0040 (N=0~15)			Register Name: DMA_MODE_REG
Bit	R/W	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	LAG_TIME_MODE In wait mode, enabling this bit, DMA will not calculate wait cycles until DMA receives or transmits data successfully. It's recommend to enable this bit before using DMA when the DMA has enable more than one channel which access IO and memory equipment. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0100+0x0028+N*0x0040 (N=0~15)			Register Name: DMA_MODE_REG
Bit	R/W	Default/Hex	Description
4	R/W	0x0	DMA_BLOCK_ZERO_EN Enable pre-read source DRQ signal when source block is configured 0. It needs to disable when opening timeout function (end mode and jump mode) and source block is configured 0. 0: enable 1: disable
3	R/W	0x0	DMA_DST_MODE. Destination communication Mode Select 0: Wait mode. 1: Handshake mode.
2	R/W	0x0	DMA_SRC_MODE. Source communication Mode Select 0: Wait mode. 1: Handshake mode.
1:0	/	/	/

13.1.7.15 0x0100+0x002C+N*0x0040 (N=0~15) DMA Former Descriptor Address Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x002C+N*0x0040 (N=0~15)			Register Name: DMA_FDESC_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DMA_FDESC_ADDR. This register is used to store the former value of DMA Channel Descriptor Address Register.

13.1.7.16 0x0100+0x0030+N*0x0040 (N=0~15) DMA Package Number Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0030+N*0x0040 (N=0~15)			Register Name: DMA_PKG_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DMA_PKG_NUM. This register will record the number of packages which has been completed in one transmission.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

13.1.7.17 0x0100+0x0034+N*0x0040 (N=0~15) DMA IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0034+N*0x0040 (N=0~15)			Register Name: DMA_IRQ_EN_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	DMA_TIMEOUT_IRQ_EN DMA Timeout Interrupt Enable. 0: Disable 1: Enable
2	R/W	0x0	DMA_QUEUE_IRQ_EN DMA Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
1	R/W	0x0	DMA_PKG_IRQ_EN DMA Package End Transfer Interrupt Enable. 0: Disable 1: Enable
0	R/W	0x0	DMA_HLAF_IRQ_EN DMA Half Package Transfer Interrupt Enable. 0: Disable 1: Enable

13.1.7.18 0x0100+0x0038+N*0x0040 (N=0~15) DMA IRQ Pending Status Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0038+N*0x0040 (N=0~15)			Register Name: DMA_IRQ_PEND_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W1C	0x0	DMA_TIMEOUT_IRQ_PEND DMA Timeout Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
2	R/W1C	0x0	DMA_QUEUE_IRQ_PEND. DMA Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0100+0x0038+N*0x0040 (N=0~15)			Register Name: DMA_IRQ_PEND_REG
Bit	Read/Write	Default/Hex	Description
1	R/W1C	0x0	DMA_PKG_IRQ_PEND DMA Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
0	R/W1C	0x0	DMA_HLAF_IRQ_PEND. DMA Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

13.1.7.19 0x0100+0x003C+N*0x0040 (N=0~15) DMA Channel Descriptor Highest Address Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x003C+N*0x0040 (N=0~15)			Register Name: DMA_DESC_HIG_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R	0x0	DMA_FDESC_ADDR_HIGHEST. This register is used to storing the former value of DMA Channel Descriptor Highest Address[34].
15:1	/	/	/
0	R/W	0x0	DMA Channel Descriptor Highest Address (descriptor[34])

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

14 Video & Graphics Engine

14.1 Video Encoder

The Video Encoding consists of the video encoding unit(VE) and JPEG encoder(JPEG). The VE supports H.264 and H.265 encoding, JPEG supports JPEG/MJPEG encoding.

14.1.1 VE

The VE is a CODEC that supports H.264 and H.265 protocol based on ASIC. It is custom-made for the IPC usage and features high compressing rate, low CPU usage, short delay and low power consumption.

The VE has the following features:

- Supports ITU-T H.264 High profile /Main profile /Baseline profile @Level 4.2 encoding, up to 4K@30fps
  - Supports the output picture format of semi-planar YCbCr4:2:0
  - Motion compensation with 1/2- or 1/4- pixel precision
  - Search Range [H:+/-128, V: +/-24]
  - Four prediction unit (PU) types of 16x16, 16x8, 8x16 and 8x8 for inter-prediction
  - Three PU types of 16x16, 8x8 and 4x4 for intra-prediction
  - Transform 4x4 and transform 8x8
  - CABAC and CAVLC entropy encoding
  - In-loop deblocking filter
  - Multi-slice encoding
  - Supports normal functions: Macro-block rate control, intra-refresh, inter-only-in-P-frame
  - Supports special functions: dynamic search window range
  - Supports region of interest(ROI) encoding with custom QP map
  - Supports three-bit rate control modes: constant bit rate(CBR), variable bit rate(VBR), and FIXEDQP.
  - Supports lossless compression for reference frame.
  - Supports OSD front-end overlaying
- Supports ITU-T H.265 Main Profile @Level 5.0 Main-Tier encoding, up to 4K@30fps
  - Supports the output picture format of semi-planar YCbCr4:2:0
  - Motion compensation with 1/2- or 1/4- pixel precision

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- Search Range [H:+/-128, V: +/-24]
- Three CU types of 32x32, 16x16 and 8x8
- Two prediction unit (PU) types of 2Nx2N, NxN
- CABAC entropy encoding
- Merge candidate list supports up to three motion vector
- In-loop deblocking filter
- Supports sample adaptive offset (SAO)
- Supports normal functions: Macro-block rate control, intra-refresh, inter-only-in-P-frame
- Supports special functions: dynamic search window range
- Supports region of interest(ROI) encoding with custom QP map
- Supports three-bit rate control modes: constant bit rate(CBR), variable bit rate(VBR), and FIXEDQP.
- Supports lossless compression for reference frame.
- Supports OSD front-end overlaying

14.1.2 JPEG

The JPEG is a high-performance JPEG encoder based on ASIC. It supports 64-megapixel snapshot or HD MJPEG encoding.

The JPEG has the following features:

- ISO/IEC 10918-1 (CCITT T.81) baseline process (DCT sequential) encoding, up to 4K@15fps
- Supports multiple input picture formats:
  - Semi-planar YCbCr4:2:0
  - YCbCr4:2:2
  - YCbCr4:4:4
- Supports configurable quantization tables for the Y component, Cb component and Cr component respectively
- Supports OSD front-end overlaying
- Supports the color-to-gray function

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

14.2 Video Decoder

The Video Decoding consists of Video Control Firmware(VCF) running on ARM processor and embedded hardware Video Engine(VE). VCF gets the bitstream from topper software, parses bitstream, invokes the Video Engine, and generates the decoding image sequence. The decoder image sequence is transmitted by the video output controller to the display device under the control of the topper software.

The Video Decoding has the following features:

- Supports ITU-T H.265 Main/Main10, level 5.2
  - Maximum video resolution: 8192x4352
  - Maximum decoding rate: 8192x4352@24fps, 10bit
- Supports VP9 Profile0/ Profile2, level 6.1
  - Maximum video resolution: 8192x8192
  - Maximum decoding rate: 8192x8192@24fps, 10bit
- Supports AVS2
  - Maximum video resolution: 8192 x 4608
  - Maximum decoding rate: 8192x4608@24fps, 10bit
- Supports ITU-T H.264 Base/Main/High Profile@Level 5.1
  - Maximum video resolution: 4096 x 2304
  - Maximum decoding rate: 4096x2304@30fps, 8bit
- Supports ITU-T H.263 Base Profile
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 1920x1080@60fps
- Supports VP8
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 1920x1080@60fps
- Supports MPEG4 Simple/ Advanced Simple Profile@Level 5
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 1920x1080@60fps
- Supports MPEG2 Main Profile, High Level
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 1920x1080@60fps
- Supports MPEG1 Main Profile, High Level
  - Maximum video resolution: 1920 x 1080

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- Maximum decoding rate: 1920x1080@60fps

- Supports XVID
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 1920x1080@60fps
- Supports Sorenson Spark
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 1920x1080@60fps
- Supports AVS/AVS+ Jizhun Profile
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 1920x1080@60fps
- Supports MJPEG
  - Maximum video resolution: 16384 x 16384
  - Maximum decoding rate: 1920x1080@60fps
- Supports WMV9/VC1 Simple/Main/Advanced Profile
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 1920x1080@30fps

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

14.3 Display Engine (DE)

The Display Engine (DE) is a hardware composer to transfer image layers from a local bus or a video buffer to the LCD interface. The DE supports many overlay windows to blend, and supports video post-processing in the video channel.

The DE has the following features:

- Supports output size up to 4096x2048.
- Supports up to 7 alpha blending channels and 2 display out.
- Supports four overlay layers in each channel, and has an independent scaler.
- Supports potter-duff compatible blending operation.
- VCH0 supports AFBD & TFBD, VCH1/UCH0~1 support TFBD, VCH2 support restricted 2K AFBD. When VCH2 AFBD is on, all PQ modules in VCH2(SNR/FCM) and DEP1(GAMMA/DRC/DITHER) except scaler are not available.
- Supports input format semi-planar of YUV422/YUV420/YUV411/P010/P210 and planar of YUV422/YUV420/ YUV411, ARGB8888/XRGB8888/RGB888/ARGB4444/ ARGB1555/RGB565.
- Supports Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data.
- Supports 10-bit processing path for HDR video.
- Supports SDR/HDR10/Hybrid-log gamma EOTF and color space conversion.
- Supports AWonder1.1 for excellent display experience.
  - Adaptive de-noising for compression noise or mosquito noise for yuv420/422 input.
  - Adaptive edge-directive scaler.
  - Adaptive local dynamic contrast enhancement.
  - Adaptive detail/edge enhancement.
  - Adaptive color enhancement (Blue-stretch, Green-stretch and fresh tone correction) and skin-tone protection.
  - 17x17x17 programmable LUT for display0.
  - Adaptive de-banding for color banding removal.
  - Hue gain, Saturation gain, and Value gain controlled.
  - Fully programmable color matrix.
  - Dynamic gamma.
  - Color temperature tuning / Auto white balance
  - Global dimming (Up to 2560x2048 for display0, 2048x2048 for display1)
- Supports write back for high efficient dual display and miracast.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- Supports output format YUV444/YUV422/YUV420/RGB444 for 10/8bit.
- Supports Register Configuration Queue for register update function.
- Supports 1/2/4 ppc (pix per cycle) output.
- Supports offline composition mode to increase bandwidth utilization.
- Supports online rotation for AFBC1.3 YUV420 format, clockwise 0/90/180/270 degress horizontal/vertical flip, up to 4K resolution.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

14.4 De-interlacer (DI)

The De-interlacer is a module which provides de-interlacing functions. It is an off-line processing module which reading input frame buffer and writing output frame buffer by memory bus. In this version of DI, it also provides Temporal Noise Reduction function to reduce the random noise. And the new-add Film Mode Detection function can detect the pull-down content from video and recover the film with maximum details. The DI has the following features:

- Supports off-line processing mode only
- Supports 8bit NV12/NV21/YV12 and planar YUV422/planar YUV422 UV-combined input data format
- Supports 8bit NV12/NV21/YV12 and planar YUV422/planar YUV422 UV-combined output data format for DIT, and YV12/planar YUV422 output data format for TNR.
- Supports video resolution from 32x32 to 2048x1280 pixel
- Supports weave/pixel-motion-adaptive de-interlace method
- Supports Field-Based Motion Detection with horizontal trailing width reduction
- Supports Temporal Noise Reduction function
- Supports Film Mode Detection with Video-On-Film Detection
- Performance:
  - Module clock 500MHz for 1080P@60Hz YUV420, 550MHz for 1080P@60Hz YUV422 with all functions enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

14.5 Graphic 2D (G2D)

The Graphic 2D (G2D) engine is hardware accelerator for 2D graphic.

The G2D has the following features:

- Supports mixer input layer size up to 7680x7680 pixels and output layer size up to 2048x2048 pixels
- Supports rotate input/output layer size up to 4096x4096 pixels
- Supports pre-multiply alpha image data
- Supports color key
- Supports two pipes Porter-Duff alpha blending
- Supports multiple video formats 4:2:0, 4:2:2, 4:1:1 and multiple pixel formats (8/16/24/32 bits graphics layer)
- Supports memory scan order option
- Supports any format convert function above
- Supports 1/16× to 32× resize ratio
- Supports 32-phase 8-tap horizontal anti-alias filter and 32-phase 4-tap vertical anti-alias filter.
- Supports window clip
- Supports FillRectangle, BitBlit, StretchBlit, and MaskBlit.
- Supports horizontal and vertical flip, clockwise 0/90/180/270 degree rotate

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

14.6 E-ink

The E-ink Engine(EE) is a hardware accelerator for E-ink LCD, It can rapidly update 64 Region LUT Pipeline.

The E-ink has the following features:

- Supports output size up to 2560x1650@106Hz.
- Supports 8/16 bits data interface.
- Supports 64 pipeline(4-bit) or 31 pipeline(5-bit) region update
- Supports dither(support Floyd-Steinberg Atkinson and Ordered dither)
- Supports auto mode selection
- Supports overlap and collision handling
- Supports dual scan display

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15 Video Output

15.1 TCON_LCD

15.1.1 Overview

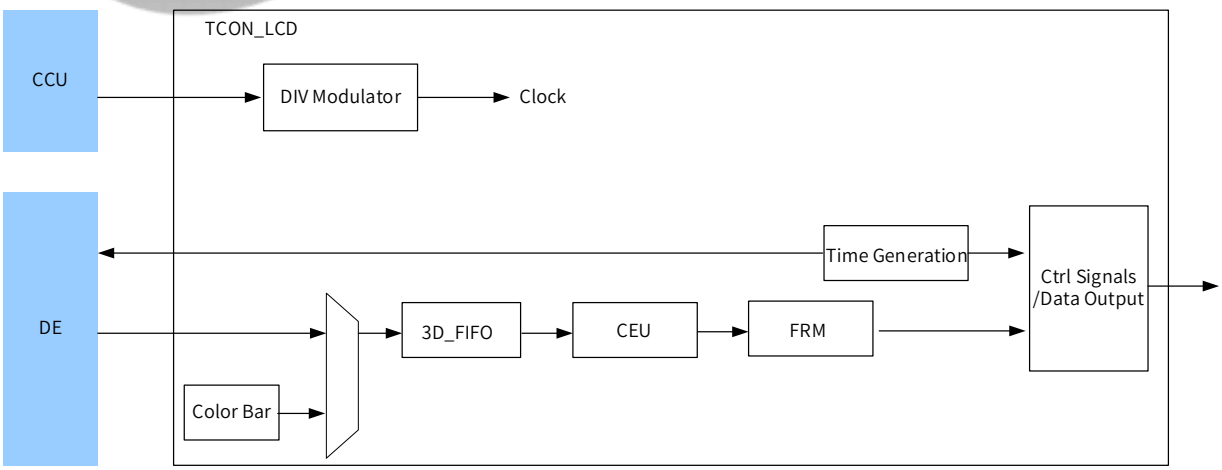
The Timing Controller_LCD (TCON_LCD) is a module that processes video signals received from system through a complicated arithmetic and then generates control signals and transmits them to the LCD panel driver IC.

The TCON_LCD includes the following features:

- Two TCON LCD controllers: TCON_LCD0 and TCON_LCD1
  - TCON_LCD0 supports 4K@45fps, and TCON_LCD1 supports 1080P@60fps
  - TCON_LCD0 controls one dual-link LVDS, one dual-link MIPI DSI, or one RGB interface
  - TCON_LCD1 controls one MIPI DSI interface
- Supports RGB interface with DE/SYNC mode, up to 1920 x 1080@60fps
- Supports serial RGB/dummy RGB interface, up to 800 x 480@60fps
- Supports LVDS interface with dual link, up to 1920 x 1080@60fps
- Supports LVDS interface with single link, up to 1366 x 768@60fps
- Supports i8080 interface, up to 800 x 480@60fps
- Supports BT.656 interface for NTSC and PAL
- Dither function for RGB888, RGB666, and RGB565 with dither function

15.1.2 Block Diagram

Figure 15-1 TCON_LCD Block Diagram



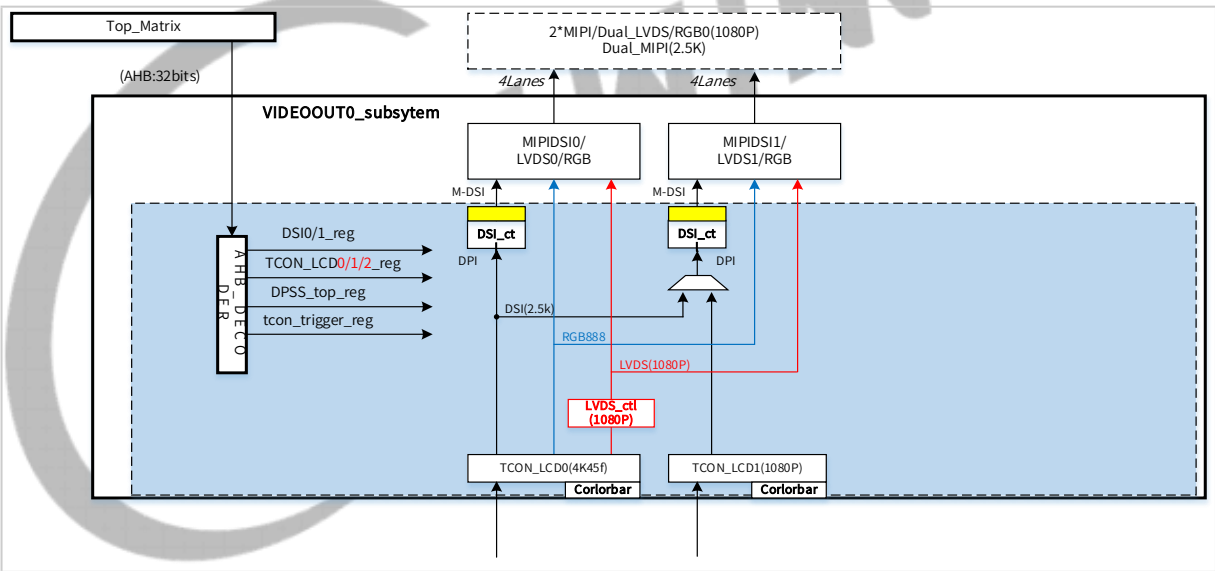
Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Table 15-1 TCON_LCD Sub-blocks

Sub-blocks	Description
ColorBar	The circuit of embedded test data source in TCON. It provides RGB colorbar pattern, grey pattern, lattice pattern, and grid pattern.
Div Modulator	It is responsible for clock division and phase adjustment.
3DFIFO	It supports sending the left and right halves of an image alternatively in the unit of pixel.
CEU	It supports strengthening or adjusting the RGB color, and convert from RGB to YUV.
FRM	It is the image processing module in the situation of outputting RGB666 or RGB565 from RGB888. It is used for making the output image to maintain the RGB888 display effect.
Timing Generation	It generates the corresponding timing based on the configured parameters and the row state machine and column state machine in the module.

15.1.3 Environment Diagram

Figure 15-2 TCON_LCD Environment Diagram



15.1.4 Clock Sources

The following table describes the clock sources of TCON_LCD. For clock setting, configurations, and gating information, refer to the section Clock Controller Unit (CCU).

Module	Clock Sources	Description
TCON_LCD0	VIDEO0PLL4X	Its frequency is 1188 MHz by default.
	VIDEO1PLL4X	Its frequency is 1188 MHz by default.
	VIDEO2PLL4X	Its frequency is 1188 MHz by default.
	PERI0PLL2X	Its frequency is 1.2 GHz by default.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.1.5 External Signals

The following table describes the external I/O signals of RGB, LVDS, and MIPI DSI.

Table 15-2 RGB, LVDS, and MIPI DSI External Signals

Signal Name	Description	Type
RGB		
LCD0-D[23:0]	LCD0 Data Input/Output	I/O
LCD0-CLK	LCD0 Clock The pixel data are synchronized by this clock	O
LCD0-DE	LCD0 Data Output Enable	O
LCD0-HSYNC	LCD0 Horizontal Sync It indicates one new scan line	O
LCD0-VSYNC	LCD0 Vertical Sync It indicates one new frame	O
TCON-FSYNC[1:0]	Frame Sync for TCON and sensor	O
LVDS		
LVDS0-D[3:0]P	LVDS0 Positive Port of Data Channel [3:0]	AO
LVDS0-D[3:0]N	LVDS0 Negative Port of Data Channel [3:0]	AO
LVDS0-CKP	LVDS0 Positive Port of Clock	AO
LVDS0-CKN	LVDS0 Negative Port of Clock	AO
LVDS1-D[3:0]P	LVDS1 Positive Port of Data Channel [3:0]	AO
LVDS1-D[3:0]N	LVDS1 Negative Port of Data Channel [3:0]	AO
LVDS1-CKP	LVDS1 Negative Port of Clock	AO
LVDS1-CKN	LVDS1 Positive Port of Clock	AO
VCC-LVDS	Power supply for LVDS	P
MIPI DSI		
DSI0-CKN	DSI0 Differential Clock Negative Signal	AO
DSI0-CKP	DSI0 Differential Clock Positive Signal	AO
DSI0-D3N	DSI0 Differential Data 3 Negative Signal	AO
DSI0-D2N	DSI0 Differential Data 2 Negative Signal	AO
DSI0-D1N	DSI0 Differential Data 1 Negative Signal	AO
DSI0-D0N	DSI0 Differential Data 0 Negative Signal	AI/O
DSI0-D3P	DSI0 Differential Data 3 Positive Signal	AO
DSI0-D2P	DSI0 Differential Data 2 Positive Signal	AO
DSI0-D1P	DSI0 Differential Data 1 Positive Signal	AO
DSI0-D0P	DSI0 Differential Data 0 Positive Signal	AI/O
DSI1-CKN	DSI1 Differential Clock Negative Signal	AO
DSI1-CKP	DSI1 Differential Clock Positive Signal	AO
DSI1-D[3:0]N	DSI1 Differential Data[3:0] Negative Signal	AO
DSI1-D[3:0]P	DSI1 Differential Data[3:0] Positive Signal	AO
DSI-TRIG-LCD-TE1	Screen Trigger Signal	AI

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

For parallel RGB, the data of LCD is high-aligned. The correspondence is as follows.

Table 15-3 The Correspondence between LCD and RGB

LCD I/O	Parallel RGB I/O		
	RGB565	RGB666	RGB888
LCD0			
LCD0-D23	R4	R5	R7
LCD0-D22	R3	R4	R6
LCD0-D21	R2	R3	R5
LCD0-D20	R1	R2	R4
LCD0-D19	R0	R1	R3
LCD0-D18	-	R0	R2
LCD0-D17	-	-	R1
LCD0-D16	-	-	R0
LCD0-D15	G5	G5	G7
LCD0-D14	G4	G4	G6
LCD0-D13	G3	G3	G5
LCD0-D12	G2	G2	G4
LCD0-D11	G1	G1	G3
LCD0-D10	G0	G0	G2
LCD0-D9	-	-	G1
LCD0-D8	-	-	G0
LCD0-D7	B4	B5	B7
LCD0-D6	B3	B4	B6
LCD0-D5	B2	B3	B5
LCD0-D4	B1	B2	B4
LCD0-D3	B0	B1	B3
LCD0-D2	-	B0	B2
LCD0-D1	-	-	B1
LCD0-D0	-	-	B0

The multiplex relationship among LCD, LVDS, and DSI is shown as follows.

Table 15-4 The Correspondence among LCD, LVDS, and DSI

LCD I/O	LVDS I/O	DSI I/O
LCD0		
LCD0-D0	/	/
LCD0-D1	/	/
LCD0-D2	LVDS0-D0P	DSI0-D0P
LCD0-D3	LVDS0-D0N	DSI0-D0N
LCD0-D4	LVDS0-D1P	DSI0-D1P
LCD0-D5	LVDS0-D1N	DSI0-D1N
LCD0-D6	LVDS0-D2P	DSI0-CKP
LCD0-D7	LVDS0-D2N	DSI0-CKN

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

LCD I/O	LVDS I/O	DSI I/O
LCD0-D8	/	/
LCD0-D9	/	/
LCD0-D10	LVDS0-CKP	DSI0-D2P
LCD0-D11	LVDS0-CKN	DSI0-D2N
LCD0-D12	LVDS0-D3P	DSI0-D3P
LCD0-D13	LVDS0-D3N	DSI0-D3N
LCD0-D14	LVDS1-D0P	DSI1-D0P
LCD0-D15	LVDS1-D0N	DSI1-D0N
LCD0-D16	/	/
LCD0-D17	/	/
LCD0-D18	LVDS1-D1P	DSI1-D1P
LCD0-D19	LVDS1-D1N	DSI1-D1N
LCD0-D20	LVDS1-D2P	DSI1-CKP
LCD0-D21	LVDS1-D2N	DSI1-CKN
LCD0-D22	LVDS1-CKP	DSI1-D2P
LCD0-D23	LVDS1-CKN	DSI1-D2N
LCD0-CLK	LVDS1-D3P	DSI1-D3P
LCD0-DE	LVDS1-D3N	DSI1-D3N
LCD0-HSYNC	/	/
LCD0-VSYNC	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.1.6 Functional Description

15.1.6.1 Control signal and data port mapping

		SYNC RGB				YUV		DC	CPU Cmd	CPU 18-bit	CPU 18bit							CPU 16bit	CPU 18bit			CPU 16bit		CPU 18bit		LVDS	DSI
External I/O	Internal pin	Para RGB	Serial RGB			BT656	BT601	YUV422		256K	256K							64K	256K			64K		256K		Single/dual link	DSI0/1
			1st	2nd	3rd						1st	2nd	3rd	1st	2nd	1st	2nd		1st	2nd	3rd	1st	2nd	1st	2nd		
LCD0_VSYNC	IO0	VSYNC					VSYN	VSYNC	CS																	Refer to Table *The Correspondence among LCD, LVDS, and DSI.*	
LCD0_HSYNC	IO1	HSYNC					HSYNC		RD																		
LCD0_CLK	IO2	DCLK				DCLK	DCLK	DCLK	WR																		
LCD0_DE	IO3	DE					DE	HSYNC	RS																		
LCD0_D23	D23	R7							D23	R5	R5	B5	G5	R5		R5	B5	R4									
LCD0_D22	D22	R6							D22	R4	R4	B4	G4	R4		R4	B4	R3									
LCD0_D21	D21	R5							D21	R3	R3	B3	G3	R3		R3	B3	R2									
LCD0_D20	D20	R4							D20	R2	R2	B2	G2	R2		R2	B2	R1									
LCD0_D19	D19	R3							D19	R1	R1	B1	G1	R1		R1	B1	R0									
LCD0_D18	D18	R2							D18	R0	R0	B0	G0	R0		R0	B0	G5									
LCD0_D17	D17	R1							D17																		
LCD0_D16	D16	R0							D16																		
LCD0_D15	D15	G7							D15	G5								G4									
LCD0_D14	D14	G6							D14	G4								G3									
LCD0_D13	D13	G5							D13	G3																	
LCD0_D12	D12	G4	D7	D7	D7	D7	D7	D7	D12	G2	G5	R5	B5	G5	B5	G5		G2	R5	G5	B5	R4	G2	R5	G2		
LCD0_D11	D11	G3	D6	D6	D6	D6	D6	D6	D11	G1	G4	R4	B4	G4	B4	G4		G1	R4	G4	B4	R3	G1	R4	G1		
LCD0_D10	D10	G2	D5	D5	D5	D5	D5	D5	D10	G0	G3	R3	B3	G3	B3	G3		G0	R3	G3	B3	R2	G0	R3	G0		
LCD0_D9	D9	G1							D9																		
LCD0_D8	D8	G0							D8																		
LCD0_D7	D7	B7	D4	D4	D4	D4	D4	D4	D7	B5	G2	R2	B2	G2	B2	G2		B4	R2	G2	B2	R1	B4	R2	B5		
LCD0_D6	D6	B6	D3	D3	D3	D3	D3	D3	D6	B4	G1	R1	B1	G1	B1	G1		B3	R1	G1	B1	R0	B3	R1	B4		
LCD0_D5	D5	B5	D2	D2	D2	D2	D2	D2	D5	B3	G0	R0	B0	G0	B0	G0		B2	R0	G0	B0	G5	B2	R0	B3		
LCD0_D4	D4	B4	D1	D1	D1	D1	D1	D1	D4	B2								B1				G4	B1	G5	B2		
LCD0_D3	D3	B3	D0	D0	D0	D0	D0	D0	D3	B1								B0				G3	B0	G4	B1		
LCD0_D2	D2	B2							D2	B0														G3	B0		
LCD0_D1	D1	B1							D1																		
LCD0_D0	D0	B0							D0																		

NOTE

- BT656 doesn't use VSYNC, HSYNC, DCLK, DE signals.
- 256K in the CPU mode indicates 2^18/1024=256K.
- In the TRIG mode of CPU, tcon_trig multiple with vsync.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.1.6.2 HV interface (Sync+DE mode)

HV I/F is also known as Sync + DE mode, which is widely used in TFT LCD module for PMP/MP4 applications.

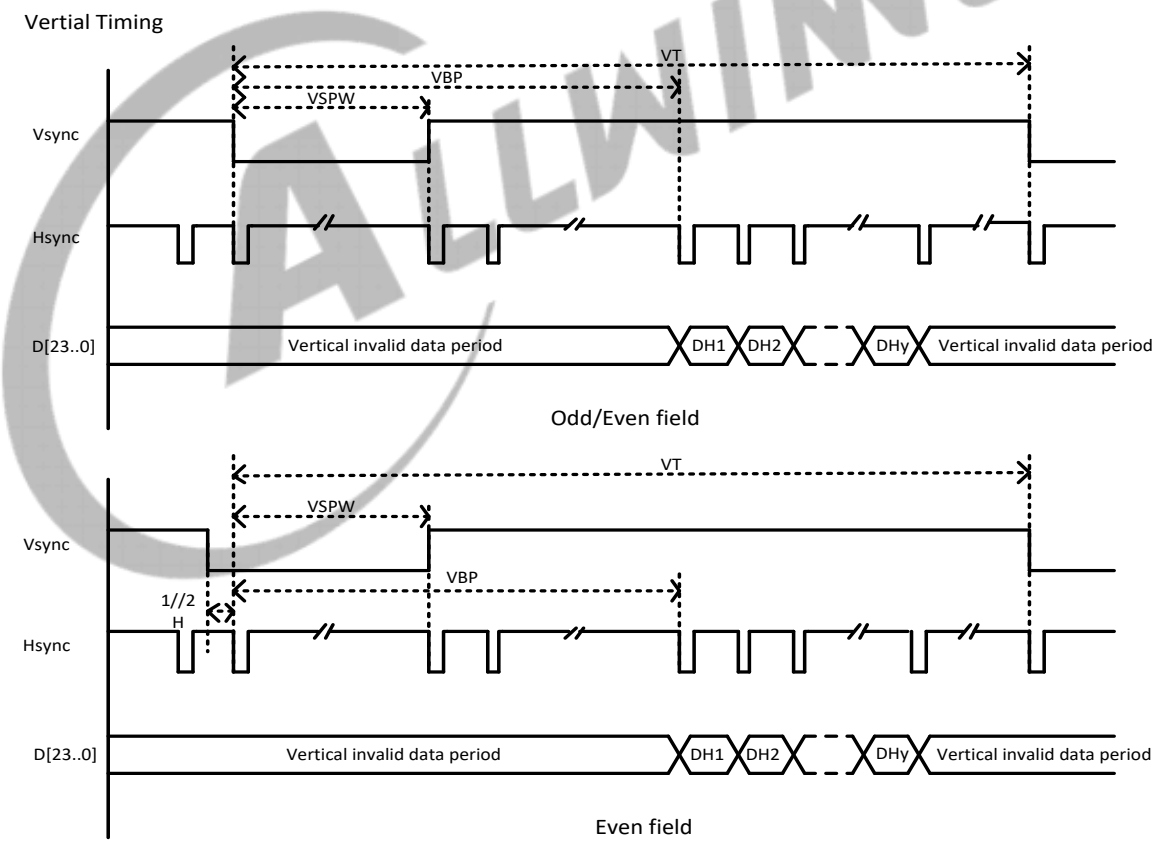
Its signals are defined as:

Table 15-5 HV Panel Signals

Signal Name	Description	Type
Vsync	Vertical sync, indicates one new frame	O
Hsync	Horizontal sync, indicates one new scan line	O
DCLK	Dot clock, pixel data are sync by this clock	O
DE	LCD data enable	O
D[23..0]	24-bit RGB output from input FIFO for panel	O

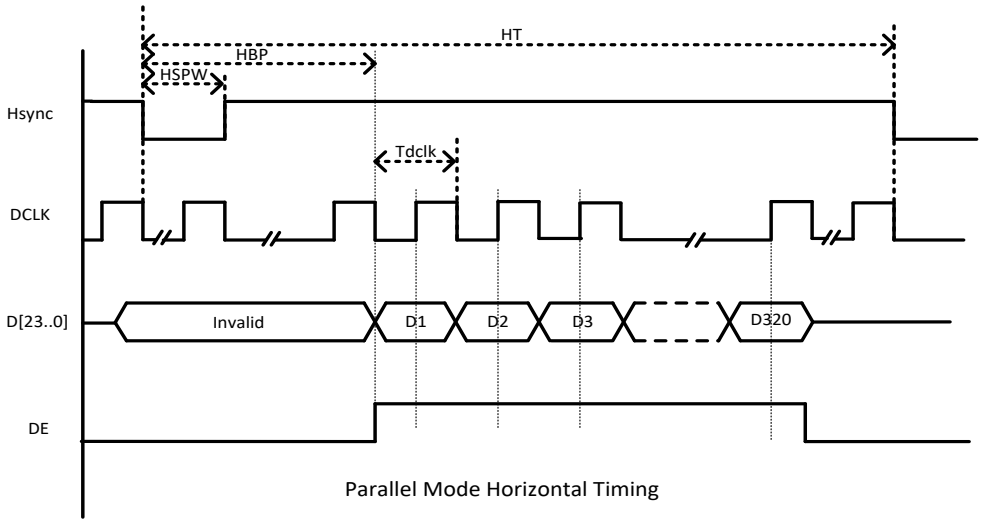
The timing diagram of HV interface is as follows.

Figure 15-3 HV Interface Vertical Timing

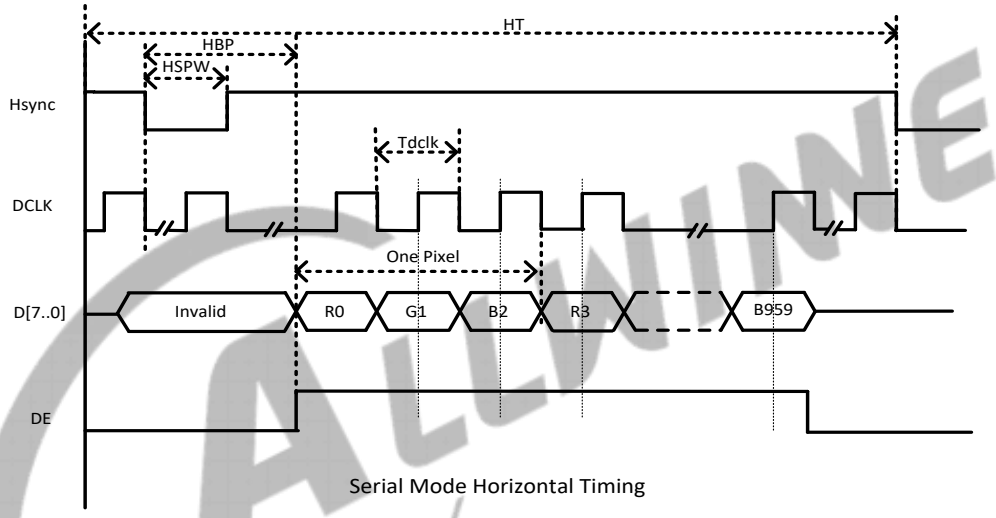


Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 15-4 HV Interface Horizontal Timing



Parallel Mode Horizontal Timing

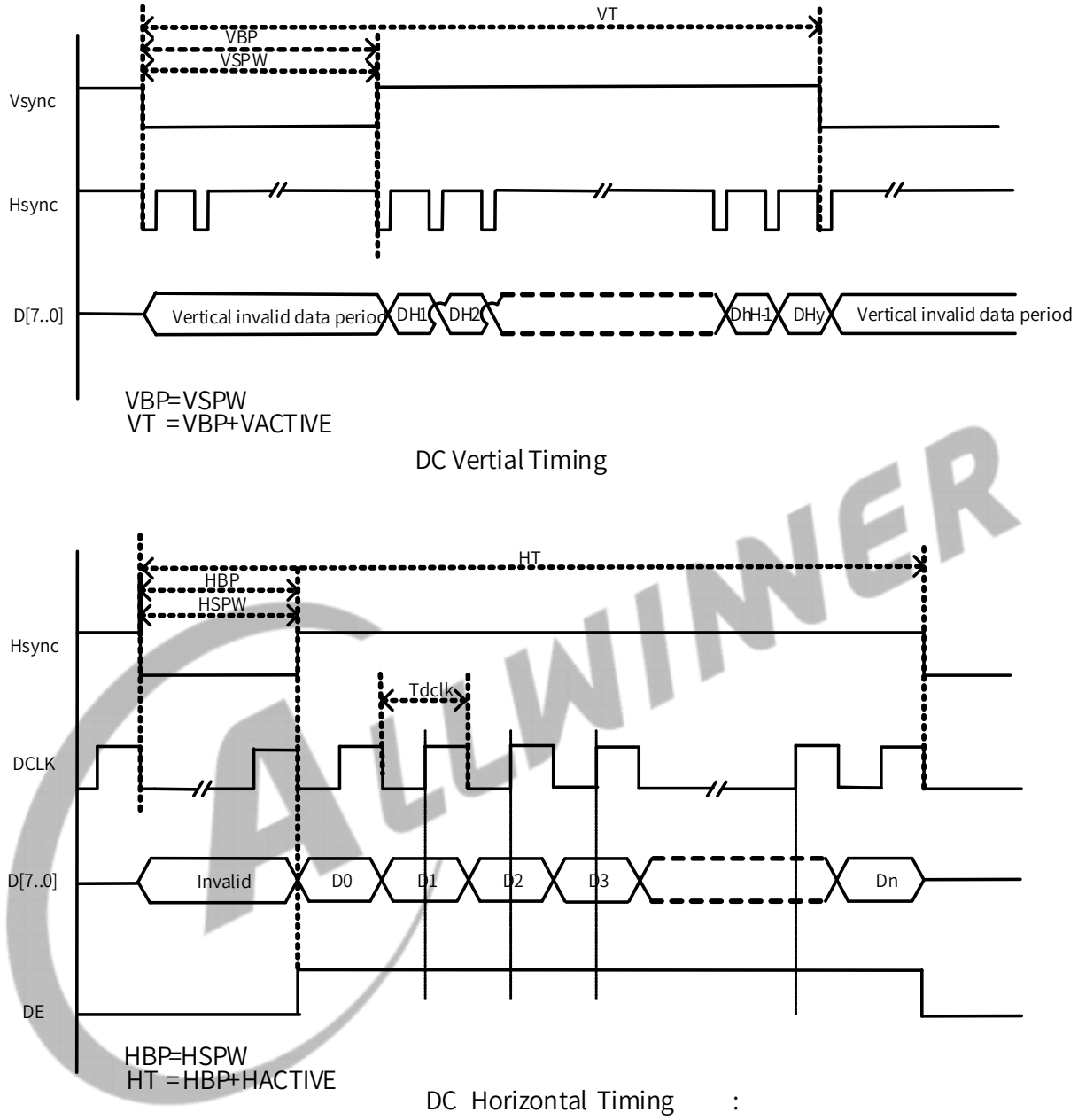


Serial Mode Horizontal Timing

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.1.6.3 DC (Digital Camera) Interface

Figure 15-5 DC Interface Timing



NOTE

In the SoC, the HSYNC signal is replaced with DE signal. Thus, it can be configured in accordance with HV interface timing in the section HV Interface (Sync+DE mode).

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.1.6.4 BT656 Interface

The BT656 transmission protocol is needed when outputting the data in YUV format in the HV interface. Compared with the standard CSI interface, BT.656 has no SYNC signals like Field, VSYN, and HSYN. Instead, it embeds the field synchronization information of image transmission in the data stream transmitted by Date Bus. The Data Bus bit width of BT.656 is 8bit. And the transmitting image data type is the interlaced YUV422. The encoding format for each row is as follows:

Row=End of Active Video (EAV) + horizontal blanking data (80H/10H) + Start of Active Video (SAV) + valid data (UYVY)

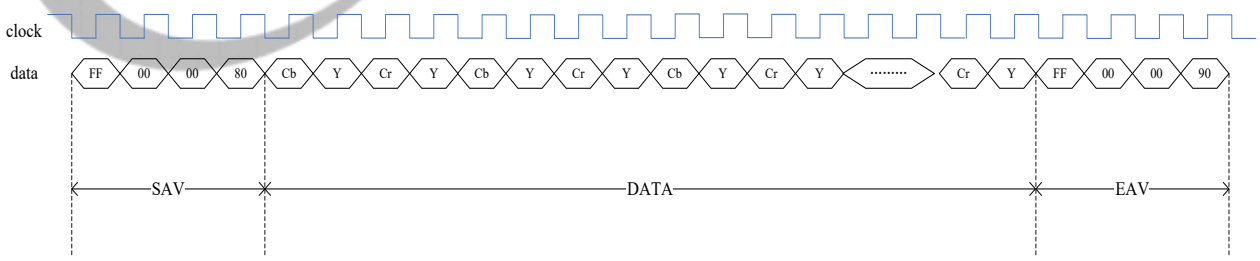
Both of the embedded EAV and SAV are four bytes in the format of FF 00 00 XY. The first three types are fixed to 8 hFF 8 h00 in hexadecimal. The last bytes XY are used as the control word. The specific image row and field synchronization information is as follows.

Table 15-6 Analysis of XY Signal

BIT	7	6	5	4	3	2	1	0
XY	1 b1	F	V	H	P3	P2	P1	P0
F	0: during field 1 1: during field 2							
V	1: during field blanking 0: field active							
H	0: in the start of active video (SAV) 1: in the end of active video (EAV)							
P3-P0	Protection Bits. Single channel: P3=V^H, P2=F^H, P1=F^V, P0=F^V^H Multi-Channel: Channel ID							

During single-channel data transmission, P3-P0 is used for calibration. The transmission timing is shown in the following figure.

Figure 15-6 Single-channel Transmission Timing

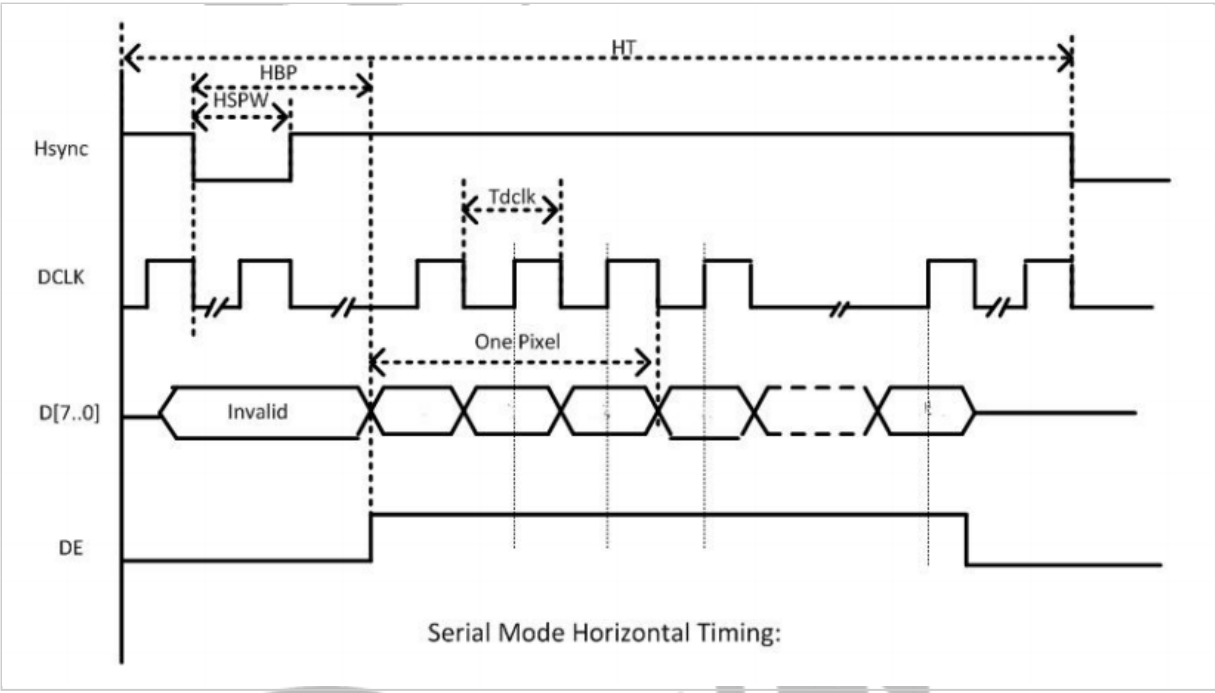


In the programming, the final output format is successfully set in the RGB2YUV. Specifically, the 8bit data output by the RGB2YUV is shown in the above figure. The ctrl_data_out module performs pin mapping for the data.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.1.6.5 BT601 Interface

Figure 15-7 BT601 Interface Timing



15.1.6.6 i8080 Interface

The i8080 I/F LCD panel is most common interfaces gee small size, low resolution LCD panels. The CPU control signals are active low.

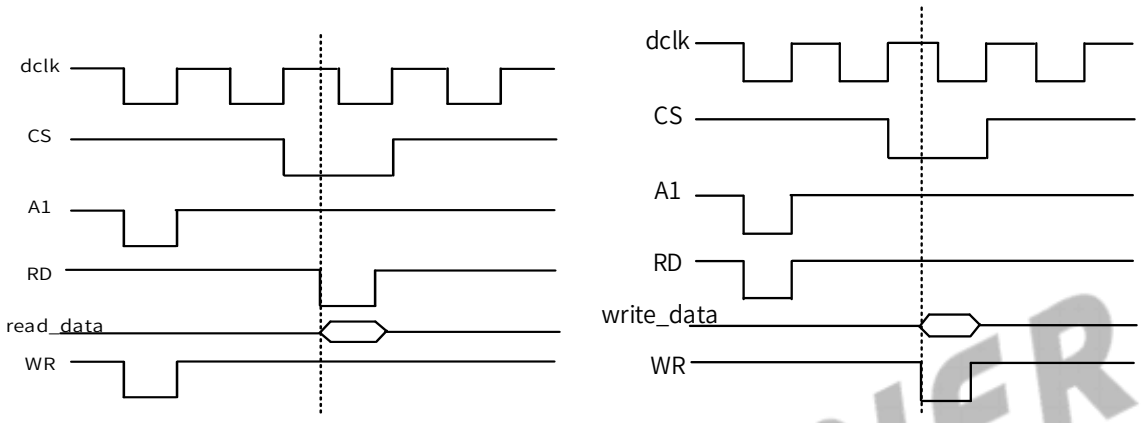
Table 15-7 CPU Panel Signals

Signal Name	Description	Type
CS	Chip select, active low	O
WR	Write strobe, active low	O
RD	Read strobe, active low	O
A1	Address bit, controlled by "LCD_CPUI/F" BIT26/25	O
D[23..0]	Digital RGB output signal	I/O

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

The following figure shows the relationship between basic timing and CPU timing. WR is fixed to 1 when reading. And it is the reverse phase of dclk1 when writing, in which it is low active and only has 1 period of low level. CS is active when pixel data is valid. RD is always set to 1 when writing. And it is the reverse phase of dclk1 when writing, in which it is low active and only has 1 period of low level. 1 is set by LCD_CPUI/F . Set to 0 or 1 when reading, and set to 1 when reading.

Figure 15-8 CPU Interface Timing (left read, right write)



When CPU I/F is in the idle state, it can generate WR/RD timing by setting LCD_CPUI/F . The CS strobe is one DCLK width, and the WR/RD strobe is half DCLK width.

There are two kinds of transmission modes for CPU interface: auto transmission and flush transmission. In the auto transmission mode, the image data is transmitted in the active area, whose transmission timing is controlled by HV timing; in the flush transmission mode, the image data is transmitted only when LCD_FIFO is non empty without taking into consideration of HV timing.

15.1.6.7 LVDS Interface

Table 15-8 LVDS Panel Signals

Signal Name	Description	Type
CKP	The positive port of clock	AO
CKN	The negative port of clock	AO
D0P	The positive port of data channel 0	AO
D0N	The negative port of data channel 0	AO
D1P	The positive port of data channel 1	AO
D1N	The negative port of data channel 1	AO
D2P	The positive port of data channel 2	AO
D2N	The negative port of data channel 2	AO
D3P	The positive port of data channel 3	AO
D3N	The negative port of data channel 3	AO

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

NOTE

The LVDS transmission protocol adopts 7:1 mode. Namely, the ratio of serial output data clock and pixel clock is 7:1.

The following figures show the timing of LVDS interface.

Figure 15-9 LVDS Single Link JEDIA Mode Interface Timing

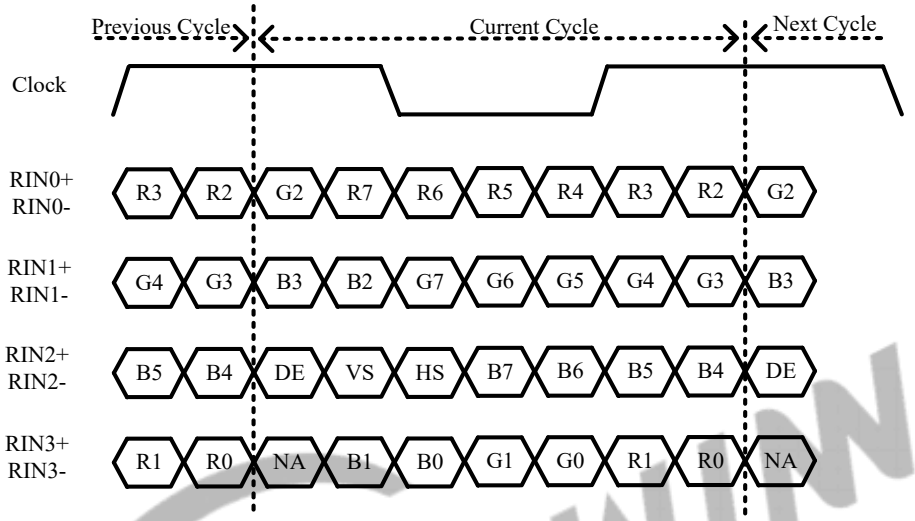
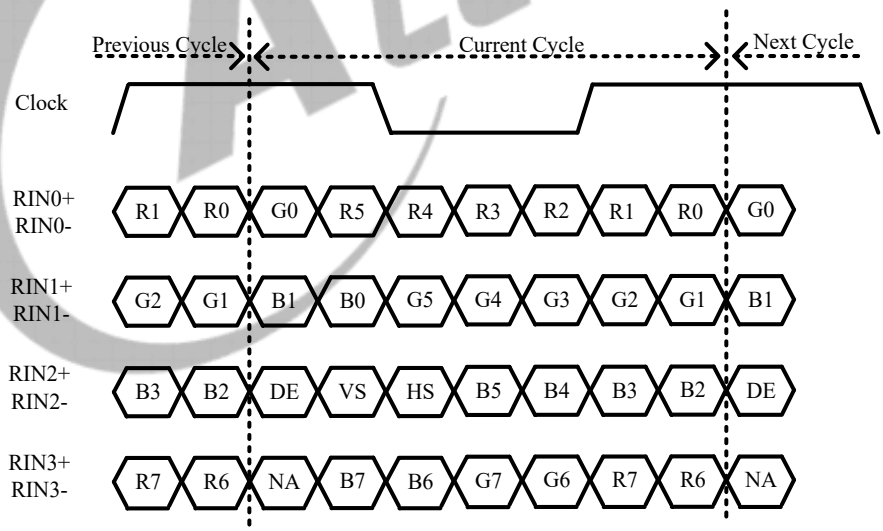


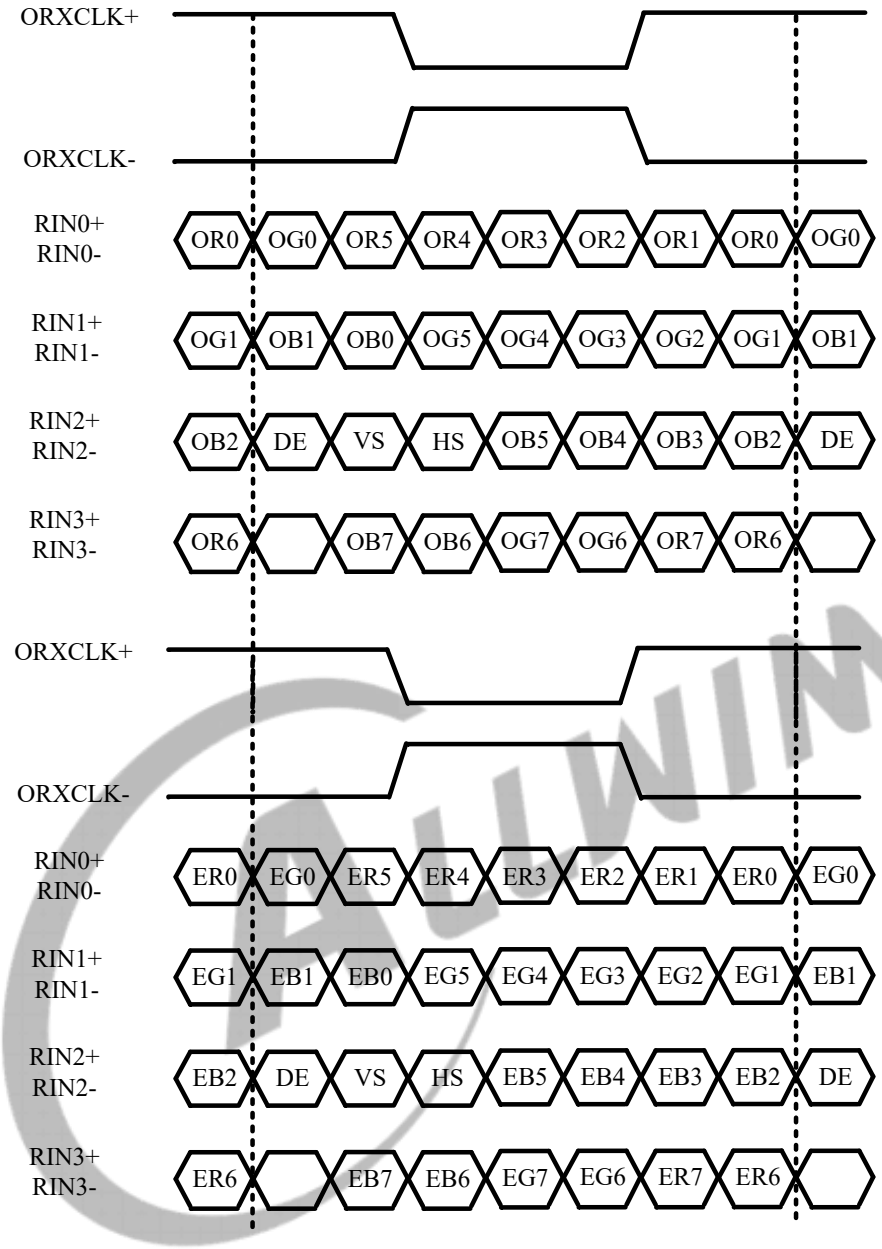
Figure 15-10 LVDS Single Link NS Mode Interface Timing



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

In the odd/even pixel mode, configure into dual-link LVDS, which is called dual-source single-screen mode.

Figure 15-11 LVDS Dual Link NS Mode Interface Timing



15.1.6.8 CEU Module

This module enhances color data from DE.

R = (((Rr*R + Rg*G + Rb*B + 8)/16) + Rc + 8)/16

G = (((Gr*R + Gg*G + Gb*B + 8)/16) + Gc + 8)/16

B = (((Br*R + Bg*G + Bb*B + 8)/16) + Bc + 8)/16

Rr, Rg, Rb, Gr, Gg, Gb, Br, Bg, Bb	s13 (-16, 16)
Rc, Gc, Bc	s19 (-16384, 16384)
R, G, B	u8 [0-255]

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

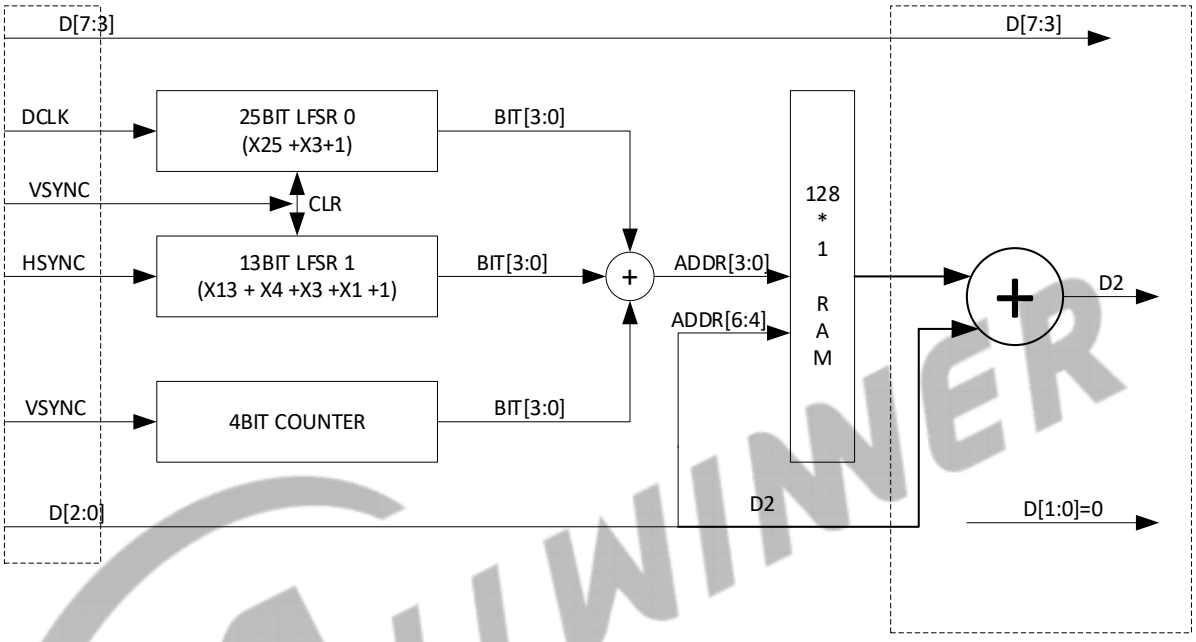
R has the range of [Rmin, Rmax]

G has the range of [Rmin, Rmax]

B has the range of [Rmin, Rmax]

15.1.6.9 FRM Module

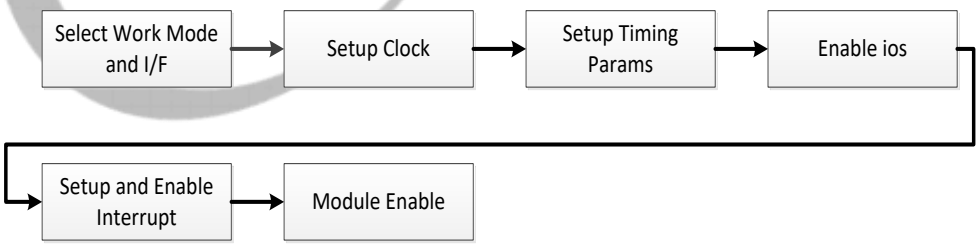
Figure 15-12 FRM Module



15.1.7 Programming Guidelines

15.1.7.1 HV Interface Configuration

Figure 15-13 HV Interface Initial Process



Parallel RGB

Step 1 Select HV interface type

Configure LCD_CTL_REG[LCD_IF] to 0 to select HV (Sync+DE) mode, and configure LCD_HV_IF_REG [HV_MODE] to 0 to select 24bit/1cycle parallel mode.

lcd_dev[sel]->lcd_ctl.lcd_if = HV(Sync+DE);

lcd_dev[sel]->lcd_ctl.src_sel = src; //src = DE/color/grayscale/...

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

lcd_dev[sel]->lcd_hv_ctl. hv_mode = 24bit/1cycle parallel mode;

Step 2 Clock configuration

NOTE

- In parallel RGB mode, the displayed pixel clock (pixel_CLK) is required to be consistent with the DCLK, the pixel_clk (pixel_clk=Ht*Vt*frame rate) is decided by external LCD.
- When using phase adjustment function, the LCD_IO_POL_REG.DCLK_SEL (reg0x88) selects dclk0(b2) of different phase, and LCD_IO_POL_REG.IO2_INV can achieve 180°phase delay.

Configure corresponding frequency by setting PLL_VIDEO0/1 register, and configure TCON LCD0 Clock register.

Configure internal frequency division of TCON_LCD. Based on clock source of TCON and DCLK clock ratio, configure LCD_DCLK_REG[LCD_DCLK_DIV]. If using phase adjustment function, LCD_DCLK_REG[LCD_DCLK_EN] needs to be set, usually is 0xf. When the dclk1 and dclk2 in LCD_DCLK_REG[LCD_DCLK_EN] are used, the value of LCD_DCLK_REG[LCD_DCLK_DIV] needs no less than 6.

lcd_dev[sel]->lcd_dclk. dclk_en = en;

lcd_dev[sel]->lcd_dclk. dclk_div = div;

Step 3 Set sequence parameters

The sequence parameters include x, ht, hbp, hspw, y, vt, vbp, vspw, and correspond to LCD_BASE_REG from reg0x48 to reg 0x54. Note that hbp includes hspw, and vbp includes vspw. And LCD_BASIC2_REG.VT needs be set to the twice of the actual value.

lcd_dev[sel]->lcd_basic0.x = x-1;

lcd_dev[sel]->lcd_basic0.y = y-1;

lcd_dev[sel]->lcd_basic1.ht = ht-1;

lcd_dev[sel]->lcd_basic1.hbp = hbp-1;

lcd_dev[sel]->lcd_basic2.vt = vt*2;

lcd_dev[sel]->lcd_basic2.vbp = vbp-1;

lcd_dev[sel]->lcd_basic3.hspw = hspw-1;

lcd_dev[sel]->lcd_basic3.vspw = vspw-1;

Step 4 Enable IO output

Set the corresponding data IO enable and control signal IO enable of LCD_IO_TRI_REG (reg0x8C) to 0 to start enable. Note that except the internal IO of TCON_LCD, the external GPIO mapping needs to be set to LCD mode.

When some control signals require polarity reversal, it can realize by setting LCD_IO_POL_REG. IO 0-3_INV.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 5 Set and open interrupt function

The LCD_GINT0_REG controls interrupt mode and flag, and the LCD_GINT1_REG sets the interrupt line position of Line interrupt mode.

V interrupt:

lcd_dev[sel]->lcd_gint0.vb_en = 1;

Line interrupt:

lcd_dev[sel]->lcd_gint1.lcd_line_int_num = line;

lcd_dev[sel]->lcd_gint0.line_en = 1;

Step 6 Turn on module enable

Enable LCD_CTL_REG[LCD_EN] and LCD_GCTL_REG[LCD_EN].

lcd_dev[sel]->lcd_ctl.lcd_en = 1;

lcd_dev[sel]->lcd_gctl.lcd_en = 1;

The following table is an example of typical parameter configuration.

Serial RGB

The serial RGB mode is consistent with parallel RGB mode, the main difference is the definition of clock and the sequence of serial data. The difference is as follows.

Step 1 Select HV interface type

Set LCD_CTL_REG [LCD_IF] to 0 to select HV(Sync+DE) mode; set LCD_HV_IF_REG [HV_MODE] to select 8bit/3cycle RGB serial mode (RGB888), 8bit/4cycle Dummy RGB mode (DRGB) or 8bit/4cycle RGB Dummy mode (RGBD).

lcd_dev[sel]->lcd_ctl.lcd_if = HV(Sync+DE);

lcd_dev[sel]->lcd_ctl.src_sel = src; //src = DE/color/grayscale/...

lcd_dev[sel]->lcd_hv_ctl. hv_mode = Serial mode;

Step 2&3 Set clock and sequence parameters

In serial RGB mode, DCLK is the transfer clock of each byte data. In the same resolution, pixel_clk of serial RGB is three times of its clock in parallel RGB, and ht, hbp, hspw own the same conversion relation. When display is split into odd field and even field, LCD_BASIC2_REG [VT] needs not to be set to the twice of the actual value.

lcd_dev[sel]->lcd_basic2.vt = vt;

Set LCD_HV_IF_REG[RGB888_ODD_ORDER/LCD_HV_IF_REG.RGB888_ODD_EVEN] to select RGB output sequence of the selected odd and even lines.

lcd_dev[lcd_sel]->lcd_hv_ctl. srgb_seq_even = seq_even;

lcd_dev[lcd_sel]->lcd_hv_ctl. srgb_seq_odd = seq_odd;

Step	Register offset	Typical Value of Simulation	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step	Register offset	Typical Value of Simulation	Description
Step1	0x058	32'h0000_0000	Parallel RGB Mode
	0x040	32'h0000_0040	Identify data sources
	/	/	Enable some functions, such as 3dfifo, frm.
Step2	0x044	32'hf000_0002	/
Step3	0x048	32'h0063_000f	Set x and y
	0x04c	32'h0095_0013	Set ht and hbp
	0x050	32'h0030_0001	Set vt and vbp
	0x054	32'h0009_0000	Set HSPW and VSPW; the actual value is HSPW+1 and VSPW+1.
Step4	0x088	32'h0000_0000	
	0x08c	32'he000_0000	1: disable 0: enable
Step5	0x008	32'h0010_0000	/
	0x004	32'h2000_0000	/
Step6	0x040	32'h8000_0040	Turn on enable
	0x000	32'h8000_0000	Enable vs and hs to start counting

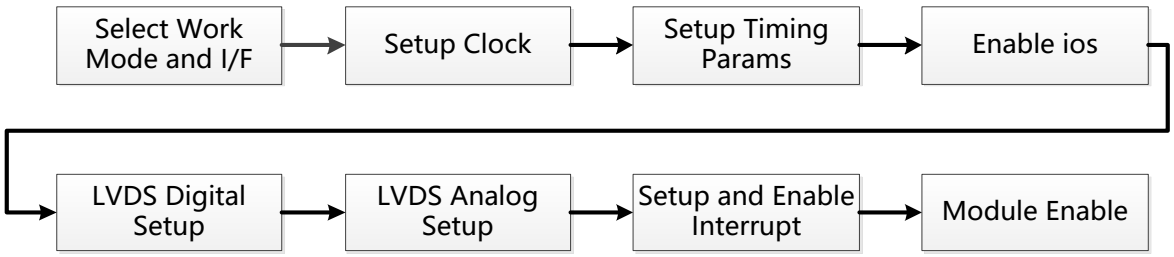
15.1.7.2 DC Interface Configuration

The DC interface configuration process is similar to the parallel mode of HV interface. Ensure that

- The configuration value of HBP and HSPW are the same.
- HT = HBP + HACTIVE
- The configuration value of VBP and VSPW are the same.
- VT = VBP + VACTIVE

15.1.7.3 LVDS Interface Configuration

Figure 15-14 LVDS interface initial sequence



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

The TCON_LCD LVDS configuration process is similar to that of HV interface except that the parallel RGB should be selected in step 1 and LVDS Digital Setup and LVDS Analog Setup are added in step 4.

LVDS Digital Setup

Configure single link or dual link, NS or JEDIA mode, LVDS clock source. When mipi PLL is selected as the clock source of LVDS, that of TCON_LCD should also be mipi PLL.

LVDS Analog Setup

Set the analog parameters of LVDS by turn on LVDS PHY power to set common mode voltage and differential voltage magnitude.

Step	Register offset	Typical Value of Simulation	Description	Configuration
1	0x0058	32'h0000_0000	Select parallel RGB mode	Configure HV_MODE as parallel mode
	0x0040	32'h0000_0020	Confirm the data source	Configure LCD_SRC_SEL, and its data sources from DE.
	/	/	Configure some function enable, such as 3dfifo and frm enable	/
2	0x0044	32'hf000_0002	/	/
3	0x0048	32'h0063_000f	Set x, y	Configure screen timing parameters
	0x004c	32'h00C7_0013	Set ht, hbp	
	0x0050	32'h0050_0001	Set vt, vbp	
	0x0054	32'h0009_0000	Set HSPW and VSPW to get the configured value. The actual value is equal to the configured value plus one.	
4	0x0084	32'hc010_0000	Digital: LVDS link mode configuration. Dual link mode and single link mode are supported.	Enable LCD_LVDS_EN and Set 0 to LCD_LVDS_LINK to enable single link.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step	Register offset	Typical Value of Simulation	Description	Configuration
	0x0220	32’hb1f8_0700	Enable analog0	Enable LVDS_EN_MB. Set LVDS_DUAL_CHANEL_SRC as 0 to enable dual-source single-screen mode. Enable LVDS_HPREN_DRVC and LVDS_HP REN_DRV to enable clane and dlane.
	0x0224	32’h0000_0000	It is the analog1 configuration. Here, analog1 is not used. To use analog1, refer to the analog0 configuration.	/
5	0x0088	32’h0000_0000	/	Select dclk0 and configure IO polarity not to toggle
	0x008c	32’he000_0000	1: Disable 0: Enable	Configure IO output enable
6	0x0008	32’h0010_0000	/	Configure the line interrupt trigger value is 12’h10.
	0x0004	32’h2000_0000	/	Configure LCD_LINE_INT_EN line interrupt enable
7	0x0040	32’h8000_0020	Turn on enable	Enable LCD_EN to turn on timing control logic.
	0x0000	32’h8000_0000	Enable vs and hs to start counting	Enable LCD_EN to turn on global enable

The above configuration procedures are based on the path of TCON_LCD -> LVDS_CTRL -> LVDS_PHY. In the path of TCON_LCD -> LVDS_CTRL -> COMBOPHY, the typical analog parameters of Step 4 should be like as below as the COMBOPHY0/1 configuration sources from DSI0/1

4	0x0084	32’hc010_0000	Digital: dual link mode; single link mode is configured by registers
	0x7110 (0x9110)	32’h0000_0007	combophy0 enable LVDS related functions

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

	0x7114 (0x9114)	32'h0000_0053	lvds vref tuning lvds ibias tuning
	0x705c (0x905c)	32'h04b3_0410	/

15.1.7.4 BT656 Interface Configuration

The BT.656 mode configuration process is similar to the parallel mode of HV interface. The following table is an example of typical parameter configuration.

Table 15-9 BT.656 Mode Configuration Example

Step	Register	Typical Value of Simulation	Description
1	LCD_HV_IF_REG (0x0058)	32'hC080_0000	Select parallel RGB
	LCD_CTL_REG (0x0040)	32'h0000_0021	Select data source
	/	/	Enable some functions such as 3DFIFO and FRM. (Optional)
2	LCD_DCLK_REG (0x0044)	32'hf000_0004	/
3	LCD_BASIC0_REG (0x0048)	32'h0117_0013	Set x and y.
	LCD_BASIC1_REG (0x004C)	32'h0513_0077	Set ht and hbp.
	LCD_BASIC2_REG (0x0050)	32'h0064_0018	Set vt and vbp.
	LCD_BASIC3_REG (0x0054)	32'h004f_0004	Set HSPW and VSPW to get the configured value. The actual value is equal to the configured value plus one.
4	LCD_IO_POL_REG (0x0088)	32'h0400_0000	/
	LCD_IO_TRI_REG (0x008C)	32'he000_0000	1: Disable 0: Enable
5	LCD_GINT1_REG (0x008)	32'h0000_0000	/
	LCD_GINT0_REG (0x004)	32'h8300_0003	/
6	LCD_CTL_REG (0x0040)	32'h8000_0041	Open module enable.
	LCD_GCTL_REG (0x0000)	32'h8000_0000	Enable vs and hs to count.

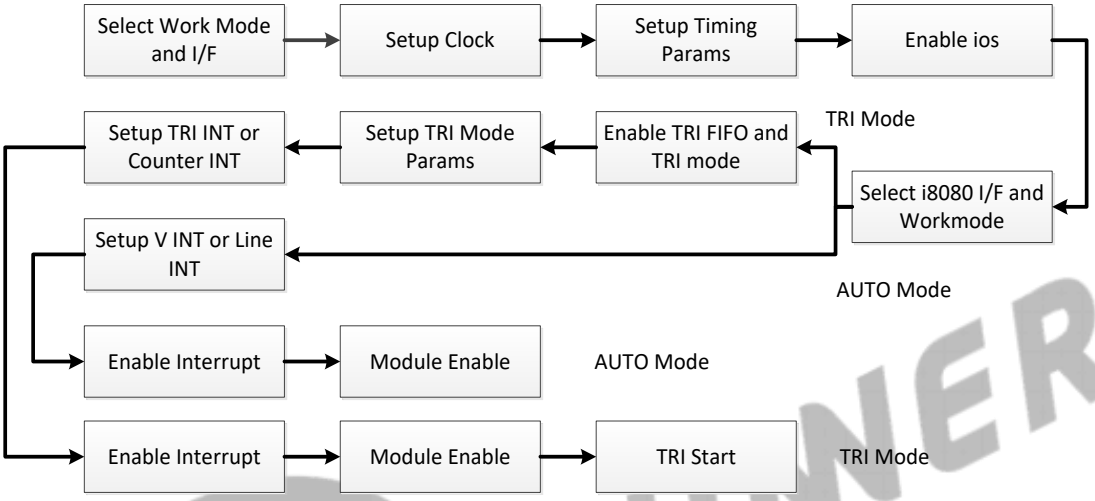
Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.1.7.5 BT601 Interface Configuration

The BT601 interface can be configured in accordance with HV interface timing in the section HV Interface (Sync+DE mode).

15.1.7.6 i8080 Interface Configuration

Figure 15-15 i8080 Interface Initial Process



Step 1 Select i8080 interface type.

Step 2 The step is the same as HV interface, but pulse adjustment function is invalid.

Step 3 The step is the same as HV interface.

Step 4 The step is the same as HV interface.

Step 5 Select type and operating mode of i8080, the operating mode includes TRI mode and AUTO mode, and the two operating modes are different in the following steps.

---------- **For TRI mode**----------

Step 6 Open TRI FIFO switch to enable TRI mode function.

Step 7 Set parameters of TRI mode, including block size, block space and block number.

NOTE

- When output interface is parallel mode, the setting value of block space parameter is not less than 20.
- When output interface is 2 cycle serial mode, the setting value of block space parameter is not less than 40.
- When output interface is 3 cycle serial mode, the setting value of block space parameter is not less than 60.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- When output interface is 4 cycle serial mode, the setting value of block space parameter is not less than 80.

Step 8 Set the tri interrupt or counter interrupt. When using the two interrupts, the tri start operation need be operated (the bit1 of LCD_CPU_IF_REG is set to"1") mainly in the interrupt service function. If using TE trigger interrupt, you can select the external input pin as a trigger signal, and then set the 0x8C register (bit[24]) to "1" to open up input of pad.

Step 9 Open the total switch of interrupt.

Step 10 Open the total enable of interrupt.

Step 11 Operate tri start operation (LCD_CPU_IF_REG (bit[1]) is set to "1").

---------- For Auto mode----------

Step 6 Set and open V interrupt or Line interrupt. The step is the same as HV interface.

Step 7 Open module total enable.

Table 15-10 i8080 Interface Configuration Example

Step	Register	Typical Value of Simulation	Description
1	LCD_HV_IF_REG (0x0058)	32'h0000_0000	Select parallel RGB
	LCD_CTL_REG (0x0040)	32'h8100_0001	Select data source
	/	/	Enable some functions such as 3DFIFO and FRM. (Optional)
2	LCD_DCLK_REG (0x0044)	32'hf000_0002	/
3	LCD_BASIC0_REG (0x0048)	32'h0063_000f	Set x and y.
	LCD_BASIC1_REG (0x004C)	32'h0095_0013	Set ht and hbp.
	LCD_BASIC2_REG (0x0050)	32'h0030_0001	Set vt and vbp.
	LCD_BASIC3_REG (0x0054)	32'h0009_0000	Set HSPW and VSPW to get the configured value. The actual value is equal to the configured value plus one.
4	LCD_IO_POL_REG (0x0088)	32'h0000_0000	/
	LCD_IO_TRI_REG (0x008C)	32'he000_0000	1: Disable 0: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step	Register	Typical Value of Simulation	Description
5	0x060	32'h0401_0005	Select the types and working mode of i8080 interface
TRI mode			
6	0x060	32'h0401_0005	Turn on TRI FIFO switch to enable TRI mode.
7	0x160	32'h00ff_031f	Set the parameters in the TRI mode
	0x164	32'h0000_01df	
8	0x004	bit[26] or bit[27] is set to 1	Select the parameters in the TRI mode
9	0x040	32'h8000_0000	Turn on the enable switch
	0x000	32'h8000_0000	
10	0x060	32'h0401_0007	Perform tri start operation
AUTO mode			
6	0x008	32'h0010_0000	
	0x004	32'h2000_0000	
7	0x040	32'h8100_0040	Turn on the enable switch
	0x000	32'h8000_0000	Enable VS and HS to start counting

15.1.8 Register List

Module Name	Base Address	Comments
VIDEO_OUT0_SYS		
VIDEO_OUT0_SYS	0x05500000	
TCON_LCD Controller		
TCON_LCD0	0x05501000	
TCON_LCD1	0x05502000	TCON_LCD1 register is the same with TCON_LCD0

Register Name	Offset	Description
VIDEO_OUT0_SYS		
DSI_SRC_SEL	0x0004	MIPI DSI Data Source Select Register
DUAL_DSI_SKEW	0x0008	Dual MIPI DSI Data Skew Register
LCD_CLK_SRC_COMB_CLK_SRC	0x000C	LCD Clock And Combophy Clock Source Select Register
VO0_MODULE_GATING	0x0020	TCON_LCD Output To LVDS/DSI Gating Register
TCON_LCD Controller		
LCD_GCTL_REG	0x0000	LCD Global Control Register
LCD_GINT0_REG	0x0004	LCD Global Interrupt Register0
LCD_GINT1_REG	0x0008	LCD Global Interrupt Register1
LCD_FRM_CTL_REG	0x0010	LCD FRM Control Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
LCD_FRM_SEED_REG	0x0014+N*0x04(N=0~5)	LCD FRM Seed Register
LCD_FRM_TAB_REG	0x002C+N*0x04(N=0~3)	LCD FRM Table Register
LCD_3D_FIFO_REG	0x003C	LCD 3D fifo Register
LCD_CTL_REG	0x0040	LCD Control Register
LCD_DCLK_REG	0x0044	LCD Data Clock Register
LCD_BASIC0_REG	0x0048	LCD Basic Timing Register0
LCD_BASIC1_REG	0x004C	LCD Basic Timing Register1
LCD_BASIC2_REG	0x0050	LCD Basic Timing Register2
LCD_BASIC3_REG	0x0054	LCD Basic Timing Register3
LCD_HV_IF_REG	0x0058	LCD HV Panel Interface Register
LCD_CPU_IF_REG	0x0060	LCD Cpu Panel Interface Register
LCD_CPU_WR_REG	0x0064	LCD Cpu Panel Write Data Register
LCD_CPU_RD0_REG	0x0068	LCD Cpu Panel Read Data Register0
LCD_CPU_RD1_REG	0x006C	LCD Cpu Panel Read Data Register1
LCD_LVDS_IF_REG	0x0084	LCD LVDS Interface Register
LCD_IO_POL_REG	0x0088	LCD IO Polarity Register
LCD_IO_TRI_REG	0x008C	LCD IO Control Register
LCD_DEBUG_REG	0x00FC	LCD Debug Register
LCD_CEU_CTL_REG	0x0100	LCD CEU Control Register
LCD_CEU_COEF_MUL_REG0	0x0110+N*0x4(N=0~2)	LCD CEU Coefficient Register0
LCD_CEU_COEF_MUL_REG1	0x0120+N*0x4(N=0~2)	LCD CEU Coefficient Register0
LCD_CEU_COEF_MUL_REG2	0x0130+N*0x4(N=0~2)	LCD CEU Coefficient Register0
LCD_CEU_COEF_ADD_REG	0x011C+N*0x10 (N=0~2)	LCD CEU Coefficient Register1
LCD_CEU_COEF_RANG_REG	0x0140+N*0x04(N=0~2)	LCD CEU Coefficient Register2
LCD_CPU_TRI0_REG	0x0160	LCD CPU Panel Trigger Register0
LCD_CPU_TRI1_REG	0x0164	LCD CPU Panel Trigger Register1
LCD_CPU_TRI2_REG	0x0168	LCD CPU Panel Trigger Register2
LCD_CPU_TRI3_REG	0x016C	LCD CPU Panel Trigger Register3
LCD_CPU_TRI4_REG	0x0170	LCD CPU Panel Trigger Register4
LCD_CPU_TRI5_REG	0x0174	LCD CPU Panel Trigger Register5
LCD_SAFE_PERIOD_REG	0x01F0	LCD Safe Period Register
LCD_LVDS_ANA0_REG	0x0220	LCD LVDS Analog Register0
LCD_LVDS_ANA1_REG	0x0224	LCD LVDS Analog Register1
FSYNC_GEN_CTRL_REG	0x0228	LCD FSYNC Generate Control Register
FSYNC_GEN_DLY_REG	0x022C	LCD FSYNC Generate Delay Register
LCD_SYNC_CTL_REG	0x0230	LCD Sync Control Register
LCD_LVDS_LMAP0_REG	0x0248	LCD LVDS Lane Map Register0
LCD_LVDS_LMAP1_REG	0x024C	LCD LVDS Lane Map Register1

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.1.9 VIDEO_OUT0_SYS Register Description

15.1.9.1 0x0004 MIPI DSI Data Source Select Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: DSI_SRC_SEL
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W	0x0	DSI1_SRC_SEL DSI1 Source Select 0: Data source is TCON_LCD1 1: Data source is TCON_LCD0
3:1	/	/	/
0	R/W	0x0	DSI0_SRC_SEL DSI0 Source Select 0: Data source is TCON_LCD0

15.1.9.2 0x0008 Dual MIPI DSI Data Skew Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: DUAL_DSI_SKEW
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	DSI1_SKEW_EN Enable DSI1 Skew Function 0: Disable 1: Enable
11:8	R/W	0x0	DSI1_SKEW_NUM DSI1 Skew Number The Value of DSI1 Skew Number is DSI1_SKEW_NUM +1
7:5	/	/	/
4	R/W	0x0	DSI0_SKEW_EN Enable DSI0 Skew Function 0: Disable 1: Enable
3:0	R/W	0x0	DSI0_SKEW_NUM DSI0 Skew Number The Value of DSI0 Skew Number is DSI0_SKEW_NUM +1

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.1.9.3 0x000C LCD Clock and Combophy Clock Source Select Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: LCD_CLK_SRC_COMB_CLK_SRC
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	COMBOPHY1_CLK_SRC_SEL Combophy1 Clock Source Select 0: CCU 1: Displl
4	R/W	0x0	COMBOPHY0_CLK_SRC_SEL Combophy0 Clock Source Select 0: CCU 1: Displl
3	/	/	/
2	/	/	/
1	R/W	0x0	LCD1_CLK_SRC_SEL LCD1_CLK Source Select 0: CCU 1: Displl
0	R/W	0x0	LCD0_CLK_SRC_SEL LCD0_CLK Source Select 0: CCU 1: Displl

15.1.9.4 0x0020 TCON_LCD Output To LVDS/DSI Gating Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: VO0_MODULE_GATING
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	LCD1_DSI_GATE LCD1 DSI Gate 0: Gating 1: Release
16	R/W	0x0	LCD0_DSI_GATE LCD0 DSI Gate 0: Gating 1: Release
15:0	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.1.10 TCON_LCD Register Description

15.1.10.1 0x0000 LCD Global Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: LCD_GCTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LCD_EN When it s disabled, the module will be reset to idle state. 0: Disable 1: Enable
30:0	/	/	/

15.1.10.2 0x0004 LCD Global Interrupt Register0 (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: LCD_GINT0_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LCD_VB_INT_EN Enable the Vb interrupt 0: Disable 1: Enable
30	/	/	/
29	R/W	0x0	LCD_LINE_INT_EN Enable the line interrupt. 0: Disable 1: Enable
28	/	/	/
27	R/W	0x0	LCD_TRI_FINISH_INT_EN Enable the trigger finish interrupt. 0: Disable 1: Enable
26	R/W	0x0	LCD_TRI_COUNTER_INT_EN Enable the trigger counter interrupt. 0: Disable 1: Enable
25:16	/	/	/
15	R/W0C	0x0	LCD_VB_INT_FLAG Asserted during vertical no-display period every frame. Write 0 to clear it.
14	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: LCD_GINT0_REG
Bit	Read/Write	Default/Hex	Description
13	R/W0C	0x0	LCD_LINE_INT_FLAG Trigger when SY0 match the current LCD scan line. Write 0 to clear it.
12	/	/	/
11	R/W0C	0x0	LCD_TRI_FINISH_INT_FLAG Trigger when CPU trigger mode finish. Write 0 to clear it.
10	R/W0C	0x0	LCD_TRI_COUNTER_INT_FLAG Trigger when tri counter reaches this value Write 0 to clear it.
9	R/W0C	0x0	LCD_TRI_UNDERFLOW_FLAG Only used in DSI video mode, tri when SYNC by DSI but not finish Write 0 to clear it.
8:3	/	/	/
2	R/W0C	0x0	FSYNC_INT_INV Enable the FSYNC interrupt set signal inverse polarity. When FSYNC is positive, this bit must be 1. And vice versa.
1	R/W0C	0x0	DE_INT_FLAG Asserted at the first valid line in every frame. Write 0 to clear it.
0	R/W0C	0x0	FSYNC_INT_FLAG Asserted at the FSYNC signal in every frame. Write 0 to clear it.

15.1.10.3 0x0008 LCD Global Interrupt Register1 (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: LCD_GINT1_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x0	LCD_LINE_INT_NUM Scan line for LCD line trigger (including inactive lines). Setting it for the specified line for trigger0. Note: SY0 is writable only when LINE_TRG0 disable.
15:0	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.1.10.4 0x0010 LCD FRM Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: LCD_FRM_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LCD_FRM_EN Enable the dither function. 0: Disable 1: Enable
30:7	/	/	/
6	R/W	0x0	LCD_FRM_MODE_R The R component output bits in dither function. 0: 6bit FRM output 1: 5bit FRM output
5	R/W	0x0	LCD_FRM_MODE_G The G component output bits in dither function. 0: 6bit FRM output 1: 5bit FRM output
4	R/W	0x0	LCD_FRM_MODE_B The B component output bits in dither function. 0: 6bit FRM output 1: 5bit FRM output
3:2	/	/	/
1:0	R/W	0x0	LCD_FRM_TEST Set the test mode of dither function. 00: FRM 01: Half 5/6bit, half FRM 10: Half 8bit, half FRM 11: Half 8bit, half 5/6bit

15.1.10.5 0x0014+N*0x04 (N=0-5) LCD FRM Seed Register (Default Value: 0x0000_0000)

Offset: 0x0014+N*0x04 (N=0-5)			Register Name: LCD_FRM_SEED_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:0	R/W	0x0	SEED_VALUE Set the seed for LFSR used in dither function. N=0: Pixel_Seed_R N=1: Pixel_Seed_G N=2: Pixel_Seed_B N=3: Line_Seed_R N=4: Line_Seed_G N=5: Line_Seed_B Note: avoid set it to 0.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.1.10.6 0x002C+N*0x04(N=0-3) LCD FRM Table Register (Default Value: 0x0000_0000)

Offset: 0x002C+N*0x04(N=0-3)			Register Name: LCD_FRM_TAB_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	FRM_TABLE_VALUE Set the data used in dither function. Usually set as follow: Table0 = 0x01010000 Table1 = 0x15151111 Table2 = 0x57575555 Table3 = 0x7f7f7777

15.1.10.7 0x003C LCD 3D FIFO Register (Default Value: 0x0000_0000)

Offset: 0x03C			Register Name: LCD_3D_FIFO_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:20	R/W	0x0	3D_FIFO_OVERLAP The number of overlap when dual dsi mode = 3D_FIFO_OVERLAP, only valid when 3D_FIFO_SETTING set as 2.
19:15	/	/	/
14:4	R/W	0x0	3D_FIFO_HALF_LINE_SIZE The number of data in half line = 3D_FIFO_HALF_LINE_SIZE+1, only valid when 3D_FIFO_SETTING set as 2.
3:2	/	/	/
1:0	R/W	0x0	3D_FIFO_SETTING Set the work mode of 3D FIFO 00: Bypass 01: Used as normal FIFO 10: Used as 3D interlace FIFO 11: Reserved

15.1.10.8 0x0040 LCD Control Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: LCD_CTL_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0040			Register Name: LCD_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LCD_EN It executes at the beginning of the first blank line of LCD timing. 0: Disable 1: Enable
30:26	/	/	/
25:24	R/W	0x0	LCD_IF Set the interface type of LCD controller. 00: HV(Sync+DE) 01: 8080 I/F 1x: Reserved
23	R/W	0x0	LCD_RB_SWAP Enable the function to swap red data and blue data in FIFO1. 0: Default 1: Swap RED and BLUE data at FIFO1
22	/	/	/
21	R/W	0x0	LCD_FIFO1_RST Write 1 and then 0 at this bit will reset FIFO 1 Note: 1 holding time must more than 1 DCLK
20:9	/	/	/
8:4	R/W	0x0	LCD_START_DLY LCD_START_DLY determines the period of de_sync staying high level. At the end of active area, de_sync signal is at high level and starts counting. When counting to LCD_STRT_DLY, the de_sync signal is switched to low level. The unit of delay is T_{line}. NOTE: Valid only when LCD_EN =1
3	/	/	/
2:0	R/W	0x0	LCD_SRC_SEL LCD Source Select 000: DE 001: Color Check 010: Grayscale Check 011: Black by White Check 100: Test Data all 0 101: Test Data all 1 110: Reversed 111: Gridding Check

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.1.10.9 0x0044 LCD Data Clock Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: LCD_DCLK_REG
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	LCD_DCLK_EN LCD clock enable. 0000: dclk_en = 0; dclk1_en = 0; dclk2_en = 0; 0001/0010: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; 0011: dclk_en = 1; dclk1_en = 1; dclk2_en = 0; 0101: dclk_en = 1; dclk1_en = 0; dclk2_en = 1; 1111: dclk_en = 1; dclk1_en = 1; dclk2_en = 1; Others: Reversed **Note:** 1) dclk_en indicates dclk, which is the pixel clock in the phase 0. 2) dclk1_en indicates dclk1, which is the pixel clock in the phase 1/3. 3) dclk2_en indicates dclk2, which is the pixel clock in the phase 2/3.
27:7	/	/	/
6:0	R/W	0x0	LCD_DCLK_DIV $f_{dclk} = f_{sclk}$ /DCLKDIV Note: 1) If dclk1&dclk2 is used, DCLKDIV >=6 2) If only dclk is used, DCLKDIV >=1

15.1.10.10 0x0048 LCD Basic Timing Register0 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: LCD_BASIC0_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x0	WIDTH_X Panel width is X+1
15:12	/	/	/
11:0	R/W	0x0	HEIGHT_Y Panel height is Y+1

15.1.10.11 0x04C LCD Basic Timing Register1 (Default Value: 0x0000_0000)

Offset: 0x04C			Register Name: LCD_BASIC1_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x04C			Register Name: LCD_BASIC1_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	HT Thcycle = (HT+1) * Tdclk Computation: 1) parallel:HT = X + BLANK Limitation: 1) parallel: HT >= (HBP +1) + (X+1) +2 2) serial 1: HT >= (HBP +1) + (X+1) *3+2 3) serial 2: HT >= (HBP +1) + (X+1) *3/2+2
15:12	/	/	/
11:0	R/W	0x0	HBP Horizontal back porch (in dclk) Thbp = (HBP +1) * Tdclk

15.1.10.12 0x0050 LCD Basic Timing Register2 (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: LCD_BASIC2_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	VT TVT = (VT)/2 * Thsync Note: VT/2 >= (VBP+1) + (Y+1) +2 VT[0] is used to determine whether progressive scanning or interlaced scanning is used. If VT[0] is 0, it will be progressive scanning; if VT[0] is 1, it will be interlaced scanning.
15:12	/	/	/
11:0	R/W	0x0	VBP Tvbp = (VBP +1) * Thsync

15.1.10.13 0x0054 LCD Basic Timing Register3 (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: LCD_BASIC3_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:16	R/W	0x0	HSPW Thspw = (HSPW+1) * Tdclk Note: HT > (HSPW+1)
15:10	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0054			Register Name: LCD_BASIC3_REG
Bit	Read/Write	Default/Hex	Description
9:0	R/W	0x0	VSPW Tvspw = (VSPW+1) * Thsync Note: VT/2 > (VSPW+1)

15.1.10.14 0x0058 LCD Hv Panel Interface Register (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: LCD_HV_IF_REG
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	HV_MODE Set the HV interface of LCD controller. 0000: 24bit/1cycle parallel mode 1000: 8bit/3cycle RGB serial mode(RGB888) 1010: 8bit/4cycle Dummy RGB(DRGB) 1011: 8bit/4cycle RGB Dummy(RGBD) 1100: 8bit/2cycle YUV serial mode(BT656)
27:26	R/W	0x0	RGB888_ODD_ORDER In the serial RGB888 mode, the output sequence of odd lines (line 1, 3, 5, 7...) 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B
25:24	R/W	0x0	RGB888_EVEN_ORDER In the serial RGB888 mode, the output sequence of even lines (line 1, 3, 5, 7...) 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B
23:22	R/W	0x0	YUV_SM In the serial YUV mode, the output sequence of 2-pixel pair of every scan line. 00: UYVY 01: VYUY 10: YVYU 11: YUYV

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0058			Register Name: LCD_HV_IF_REG
Bit	Read/Write	Default/Hex	Description
21:20	R/W	0x0	YUV_EAV_SAV_F_LINE_DLY YUV_EAV_SAV_F_LINE_DLY When the BT656_F_MASK bit of LCD_CEU_CTL_REG (offset: 0x0100) register is configured as 0, the F signal timing in BT.656 transmission is configured in this bit, and the value could be configured as maximum 3 lines. (The F signal is the odd and even field flag in the current transmission) 00: When a field counting ends, the F signal toggles immediately. 01: When the line counting value are 2, the F signal toggles. 10: When the line counting value are 3, the F signal toggles. 11: Reserved.
19	R/W	0x0	CCIR_CSC_DIS Select '0' LCD convert source from RGB to YUV. 0: Enable 1: Disable Only valid when HV interface is "1100".
18:0	/	/	/

15.1.10.15 0x0060 LCD CPU Panel Interface Register (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: LCD_CPU_IF_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0060			Register Name: LCD_CPU_IF_REG
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	CPU_MODE Set the cpu interface work mode 0000: 18bit/256K mode 0010: 18bit/256K mode (1st, 2nd, 3rd) 0100: 18bit/256K mode (1st and 2rd use D[12:5] 0110: 18bit/256K mode (1st and 2rd use D[23:18] 1000: 16bit 64K mode Output 1 pixel every one cycle 1010: 18bit 256K mode Output 1 pixel every two cycles 1100: 18bit 256K mode Output 1 pixel every three cycles 1110: 16bit 64K mode Output 1 pixel every two cycles xxx1: 24bit for DSI
27	/	/	/
26	R/W	0x0	DA CPU Mode 1) AUTO Transmission In the active region, the IO[3] port will output the DA value. In the non-active region, if the WR/RD operation is not executed, the IO[3] port will output the DA value. 2) FLUSH/TRI Transmission When LCD_FIFO is not empty, the IO[3] port will output the DA value. when LCD_FIFO is empty, and the WR/RD operation is not executed, the IO[3] will output the DA value.
25	R/W	0x0	CA CPU Mode AUTO Transmission In the non-active region, if WR/RD operation is executed, the IO[3] port will output the CA value; FLUSH/TRI Transmission When LCD_FIFO is empty and WR/RD operation is executed, the IO[3] port will output the CA value.
24	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0060			Register Name: LCD_CPU_IF_REG
Bit	Read/Write	Default/Hex	Description
23	R	0x0	WR_FLAG The status of write operation. 0: Write operation finishes 1: Write operation is pending
22	R	0x0	RD_FLAG The status of read operation. 0: Read operation is finishes 1: Read operation is pending
21:18	/	/	/
17	R/W	0x0	AUTO Auto Transfer Mode: Auto transmission: If configured as 1, the current frame data is transmitted in the active region, and the transmission is controlled by HV timing (only valid in 8080 m ode). This bit is sampled at the end of the active region.
16	R/W	0x0	LUSH Direct transfer mode: Flush transmission: When AUTO is 0 and FLUSH is configured as 1, pixel data can be output to the subsequent modules regardless of HV timing (only valid in 8080 mode) as long as the LCD_FIFO is not empty. Data output rate is controlled by DCLK.
15:3	/	/	/
2	R/W	0x0	TRI_FIFO_EN lcd_trigfifo Enable Enable the trigger FIFO. 0: Disable 1: Enable
1	R/W1S	0x0	TRI_START Write 1 by software to start a frame flush only when this flag is 0 . write 0 is invalid. This flag indicates the frame flush is running.
0	R/W	0x0	TRI_EN Enable trigger mode 0: Trigger mode disable 1: Trigger mode enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.1.10.16 0x0064 LCD CPU Panel Write Data Register (Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: LCD_CPU_WR_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	W	0x0	DATA_WR Under Auto transmission, when in the VBlank region and WR is valid, the DATA_WR value is output through D[23:0]; Under Flush/TRIG transmission, when lcd_fifo is empty and WR is valid, the DATA_WR value is output through D[23:0].

15.1.10.17 0x0068 LCD CPU Panel Read Data Register0 (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: LCD_CPU_RD0_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R	0x0	DATA_RD0 Data read on 8080 bus, launch a new read operation on 8080 bus.

15.1.10.18 0x06C LCD CPU Panel Read Data Register1 (Default Value: 0x0000_0000)

Offset: 0x06C			Register Name: LCD_CPU_RD1_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R	0x0	DATA_RD1 Data read on 8080 bus, without a new read operation on 8080 bus.

15.1.10.19 0x0084 LCD LVDS Interface Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: LCD_LVDS_IF_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LCD_LVDS_EN Enable LVDS interface. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0084			Register Name: LCD_LVDS_IF_REG
Bit	Read/Write	Default/Hex	Description
30	R/W	0x0	LCD_LVDS_LINK Select work in single link mode or dual link mode. 0: Single link 1: Dual link
29	R/W	0x0	LCD_LVDS_EVEN_ODD_DIR Set the order of even field and odd field. 0: Normal:lvds0-Odd, lvds1-Even 1: reverse:lvds0-Even, lvds1-Odd Note: Valid when in Dual Mode.
28	R/W	0x0	LCD_LVDS_DIR Set the LVDS direction. PHY input sequence control. 0: Normal 1: Reverse
27	R/W	0x0	LCD_LVDS_MODE Set the LVDS data mode. 0: NS mode(VESA) 1: JEIDA mode
26	R/W	0x0	LCD_LVDS_BITWIDTH Set the bit width of data. 0: 24bit 1: 18bit
25	R/W	0x0	LCD_LVDS_DEBUG_EN Enable LVDS debug function. 0: Disable 1: Enable
24	R/W	0x0	LCD_LVDS_DEBUG_MODE Set the output signal in debug mode 0: Mode0. Random data generated by PRBS10 1: Mode1. Output CLK period=7/2 LVDS CLK period
23	R/W	0x0	LCD_LVDS_CORRECT_MODE Set the LVDS correct mode. 0: Mode0. Phase calibration can be performed in any region. 1: Mode1. Phase calibration can be performed in the blank region of the image.
22:21	/	/	/
20	R/W	0x0	LCD_LVDS_CLK_SEL Select the clock source of LVDS. 0: Revered 1: LCD CLK

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0084			Register Name: LCD_LVDS_IF_REG
Bit	Read/Write	Default/Hex	Description
19:5	/	/	/
4:0	R/W	0x0	LCD_LVDS_DATA_POL Set the data/clk polarity of LVDS. 0: Reversed 1: Normal

15.1.10.20 0x0088 LCD IO Polarity Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: LCD_IO_POL_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	DCLK_SEL Set the phase offset of clock and data in hv mode. 00: Used DCLK0 (Normal phase offset) 01: Used DCLK1(1/3 phase offset) 10: Used DCLK2(2/3 phase offset) Others: Reserved
27	R/W	0x0	IO3_INV Enable invert function of IO3. 0: Not invert 1: Invert
26	R/W	0x0	IO2_INV Enable invert function of IO2. 0: Not invert 1: Invert
25	R/W	0x0	IO1_INV Enable invert function of IO1. 0: Not invert 1: Invert
24	R/W	0x0	IO0_INV Enable invert function of IO0. 0: Not invert 1: Invert
23:0	R/W	0x0	Data_INV LCD output port D[23:0] polarity control, with independent bit control. 0: Normal polarity 1: Invert the specify output

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.1.10.21 0x008C LCD IO Control Register (Default Value: 0x0FFF_FFFF)

Offset: 0x008C			Register Name: LCD_IO_TRI_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R/W	0x0	RGB_ENDIAN Set the endian of data bits. 0: Normal 1: Bits_invert. The RGB byte order remains unchanged, and the bits within the bytes are inverted.
27	R/W	0x1	IO3_OUTPUT_TRI_EN Enable the output of IO3. 1: Disable 0: Enable
26	R/W	0x1	IO2_OUTPUT_TRI_EN Enable the output of IO2. 1: Disable 0: Enable
25	R/W	0x1	IO1_OUTPUR_TRI_EN Enable the output of IO1. 1: Disable 0: Enable
24	R/W	0x1	IO0_OUTPUT_TRI_EN Enable the output of IO0. 1: Disable 0: Enable
23:0	R/W	0xFFFFFF	DATA_OUTPUT_TRI_EN LCD output port D[23:0] output enable, with independent bit control. 1: Disable 0: Enable

15.1.10.22 0x00FC LCD Debug Register (Default Value: 0x2000_0000)

Offset: 0x00FC			Register Name: LCD_DEBUG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W0C	0x0	LCD_FIFO_UNDERFLOW The flag shows whether the fifos are in the underflow status when the active region ends. 0: Not underflow 1: Underflow
30	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00FC			Register Name: LCD_DEBUG_REG
Bit	Read/Write	Default/Hex	Description
29	R	0x1	LCD_FIELD_POL The flag indicates the current LCD field polarity. The initial value is 1. 0: Second field 1: First field
28	/	/	/
27:16	R	0x0	LCD_CURRENT_LINE The current scan line. The initial value is 1, starting from VFP region.
15	R/W0C	0x0	WR Consistent with 0x060 WR_FLAG register, it is the flag bit of write screen register.
14	R/W0C	0x0	RD Consistent with 0x060 RD_FLAG register, it is the flag bit of read screen register.
13:0	/	/	/

15.1.10.23 0x0100 LCD CEU Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: LCD_CEU_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CEU_EN Enable CEU function 0: bypass 1: Enable
30	R/W	0x0	BT656_F_MASK The F signal generation mode selection enable during BT656 transmission. BT656 F Mask 0: Disable (F signal timing is configured in the YUV_EAV_SAV_F_LINE_DLY bit of LCD_HV_IF_REG register) 1: Enable (F signal timing is configured in the BT656_F_MASK_VALUE bit of LCD_CEU_CTL_REG register)
29	R/W	0x0	BT656_F_MASK_VALUE BT656 F Mask Value 0/1
28:0	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.1.10.24 0x0110+N*0x04 (N=0~2) LCD CEU Coefficient Register0 (Default Value: 0x0000_0000)

Offset: 0x0110+N*0x04 (N=0~2)			Register Name: LCD_CEU_COEF_MUL_REG0
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	CEU_COEF_MUL_VALUE Signed 13bit value, range of (-16,16). N=0: Rr N=1: Rg N=2: Rb

15.1.10.25 0x0120+N*0x04(N=0~2) LCD CEU Coefficient Register1 (Default Value: 0x0000_0000)

Offset: 0x0120+N*0x04(N=0~2)			Register Name: LCD_CEU_COEF_MUL_REG1
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	CEU_COEF_MUL_VALUE Signed 13bit value, range of (-16,16). N=0: Gr N=1: Gg N=2: Gb

15.1.10.26 0x0130+N*0x04 (N=0~2) LCD CEU Coefficient Register2 (Default Value: 0x0000_0000)

Offset: 0x0130+N*0x04 (N=0~2)			Register Name: LCD_CEU_COEF_MUL_REG2
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	CEU_COEF_MUL_VALUE Signed 13bit value, range of (-16,16). N=0: Br N=1: Bg N=2: Bb

15.1.10.27 0x011C+N*0x10 (N=0~2) LCD CEU Coefficient Register1 (Default Value: 0x0000_0000)

Offset: 0x011C+N*0x10 (N=0~2)			Register Name: LCD_CEU_COEF_ADD_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x011C+N*0x10 (N=0~2)			Register Name: LCD_CEU_COEF_ADD_REG
Bit	Read/Write	Default/Hex	Description
18:0	R/W	0x0	CEU_COEF_ADD_VALUE Signed 19bit value, range of (-16384, 16384). N=0: Rc N=1: Gc N=2: Bc

15.1.10.28 0x0140+N*0x04(N=0~2) LCD CEU Coefficient Register2 (Default Value: 0x0000_0000)

Offset: 0x0140+N*0x04(N=0~2)			Register Name: LCD_CEU_COEF_RANG_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	CEU_COEF_RANGE_MIN Unsigned 8bit value, range of [0,255].
15:8	/	/	/
7:0	R/W	0x0	CEU_COEF_RANGE_MAX Unsigned 8bit value, range of [0,255].

15.1.10.29 0x0160 LCD CPU Panel Trigger Register0 (Default Value: 0x0000_0000)

Offset: 0x160			Register Name: LCD_CPU_TRI0_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x0	BLOCK_SPACE Triggle mode: The time required to delay after reading a line from TRIGFIFO. Counting starts when a line of transmission ends. When the count value is equal to BLOCK_SPACE, TRIGFIFO can initiate the next line of reading. The spaces between data blocks. It should be set >20*pixel.
15:12	/	/	/
11:0	R/W	0x0	BLOCK_SIZE Triggle mode: The configuration value is the size of the effective display region X. The size of data block. It is usually set as X.

15.1.10.30 0x0164 LCD CPU Panel Trigger Register1 (Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: LCD_CPU_TRI1_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0164			Register Name: LCD_CPU_TRI1_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	BLOCK_CURRENT_NUM Shows the current data block transmitting to panel.
15:0	R/W	0x0	BLOCK_NUM The number of data blocks. It is usually set as Y.

15.1.10.31 0x0168 LCD CPU Panel Trigger Register2 (Default Value: 0x0020_0000)

Offset: 0x0168			Register Name: LCD_CPU_TRI2_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x20	START_DLY In the trigger mode, the period during which de_sync stays in high level T_{dly} = (Start_Delay +1) * dclk*8.
15	R/W	0x0	TRANS_START_MODE Select the FIFOs used in CPU mode. 0: 3D_FIFO+TRI_FIFO 1: TRI_FIFO
14:13	R/W	0x0	SYNC_MODE Set the sync mode in CPU interface. 0x: Auto 10: 0 de_sync = 0 11: 1 de_sunc = 1
12:0	R/W	0x0	TRANS_START_SET Transmission Start Trigger Value. When the amount of data in the buffer (selected in the TRANS_START_MODE bit) is not less than the configured value, the pixel data in TRIGFIFO can be transferred to LCD_FIFO. Usual set as the length of a line.

15.1.10.32 0x016C LCD CPU Panel Trigger Register3 (Default Value: 0x0000_0000)

Offset: 0x016C			Register Name: LCD_CPU_TRI3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x016C			Register Name: LCD_CPU_TRI3_REG
Bit	Read/Write	Default/Hex	Description
29:28	R/W	0x0	TRI_INT_MODE Configure the CPU to trigger interrupt mode. When configured as 01, it is Counter mode. The counting range is configured by CONTER_N and COUNTER_M, and the interrupt period is (Count_N+1)*(Count_M+1)*4dclk. 00: Disable 01: Counter mode 10: GPIO TRIGGLE signal high level trigger mode 11: GPIO TRIGGLE signal low level trigger mode
27:24	/	/	/
23:8	R/W	0x0	COUNTER_N Counting value in Counter mode, the counting period is COUNTER_N * (2*COUNTER_M*dclk).
7:0	R/W	0x0	COUNTER_M Counting value in Counter mode, the counting period is COUNTER_M*dclk.

15.1.10.33 0x0170 LCD CPU Panel Trigger Register4 (Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: LCD_CPU_TRI4_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	A1_First_Valid Valid in first Block. non-active region
23:0	R/W	0x0	D23_TO_D0_First_Valid Valid in first Block.

15.1.10.34 0x0174 LCD CPU Panel Trigger Register5 (Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: LCD_CPU_TRI5_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	A1_NON_First_Valid Valid in Block except first. (active zone)
23:0	R/W	0x0	D23_TO_D0_NON_First_Valid Valid in Block except first.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.1.10.35 0x01F0 LCD Safe Period Register (Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: LCD_SAFE_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	SAFE_PERIOD_FIFO_NUM When the data length in line buffer (lcd_3dfifo) is more than SAFE_PERIOD_FIFO_NUM,LCD controller will allow dram controller to stop working to change frequency.
15:4	R/W	0x0	SAFE_PERIOD_LINE Set a fixed line and during the line time, LCD controller allow dram controller to change frequency. The fixed line should be set in the blanking area.
3	/	/	/
2:0	R/W	0x0	SAFE_PERIOD_MODE Select the save mode 000: unsafe 001: safe 010: safe at FIFO_CURR_NUM > SAFE_PERIOD_FIFO_NUM (If 3D FIFO is bypassed, this mode is not available. 011: Safe at 2 and safe at sync active 100: Safe at line

15.1.10.36 0x0220 LCD LVDS Analog Register0 (Default Value: 0x0000_0000)

Offset: 0x0220			Register Name: LCD_LVDS_ANA0_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LVDS_EN_MB Enable the bias circuit of the LVDS_Ana module. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0220			Register Name: LCD_LVDS_ANA0_REG
Bit	Read/Write	Default/Hex	Description
30	R/W	0x0	LVDS_DUAL_CHANEL_SRC_SEL Dual-channel LVDS data source selection 0: LVDS0 outputs even pixels of TCON data source, while LVDS1 outputs odd pixels of TCON data source, which is called dual-source single-screen mode. 1: LVDS0 and LVDS1 displays the same data, without distinguishing between odd and even pixels, which is called synchronous output on dual display.
29	R/W	0x0	EN_LVDS Enable LVDS.
28	R/W	0x0	EN_24M Enable the 24M clock.
27:25	/	/	/
24	R/W	0x0	LVDS_HPREN_DRVC Enable clock channel drive. 0: Disable 1: Enable
23:20	R/W	0x0	LVDS_HPREN_DRV Enable data channel[3:0] drive. 0: Disable 1: Enable
19:17	R/W	0x0	LVDS_REG_C Adjust current flowing through Rload of Rx to change the differential signals amplitude. 0: 216mv 1: 252mv 2: 276mv 3: 312mv 4: 336mv 5: 372mv 6: 395mv 7: 432mv
16	R/W	0x0	LVDS_REG_DENC Choose data output or PLL test clock output in LVDS_tx.
15:12	R/W	0x0	LVDS_REG_DEN Choose data output or PLL test clock output in LVDS_tx.
11	/	/	/
10:8	R/W	0x0	LVDS_REG_R Adjust current flowing through Rload of Rx to change the common signals amplitude. 0: 0.925v 1: 0.950v 2: 0.975v 3: 1.000v 4: 1.025v 5: 1.050v 6: 1.075v 7: 1.100v
7	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0220			Register Name: LCD_LVDS_ANA0_REG
Bit	Read/Write	Default/Hex	Description
6:5	R/W	0x0	LVDS_TDATA_SEL 00: LVDS data channel outputs 0. 01: LVDS data channel outputs 1. 10: LVDS data channel outputs Vsync. 11: LVDS data channel outputs Hsync.
4	R/W	0x0	LVDS_REG_PLRC LVDS clock channel direction 0: Normal 1: Reverse
3:0	R/W	0x0	LVDS_REG_PLR LVDS data channel [3:0] direction 0: Normal 1: Reverse

15.1.10.37 0x0224 LCD LVDS Analog Register1 (Default Value: 0x0000_0000)

Offset: 0x0224			Register Name: LCD_LVDS_ANA1_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LVDS_EN_MB Enable the bias circuit of the LVDS_Ana module. 0: Disable 1: Enable
30	/	/	/
29	R/W	0x0	EN_LVDS Enable LVDS.
28	R/W	0x0	EN_24M Enable the 24M clock.
27:25	/	/	/
24	R/W	0x0	LVDS_HPREN_DRVC Enable clock channel drive. 0: Disable 1: Enable
23:20	R/W	0x0	LVDS_HPREN_DRV Enable data channel[3:0] drive. 0: Disable 1: Enable
19:17	R/W	0x0	LVDS_REG_C Adjust current flowing through Rload of Rx to change the differential signals amplitude. 0: 216mv 1: 252mv 2: 276mv 3: 312mv 4: 336mv 5: 372mv 6: 395mv 7: 432mv

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0224			Register Name: LCD_LVDS_ANA1_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	LVDS_REG_DENC Choose data output or PLL test clock output in LVDS_tx.
15:12	R/W	0x0	LVDS_REG_DEN Choose data output or PLL test clock output in LVDS_tx.
11	/	/	/
10:8	R/W	0x0	LVDS_REG_R Adjust current flowing through Rload of Rx to change the common signals amplitude. 0: 0.925v 1: 0.950v 2: 0.975v 3: 1.000v 4: 1.025v 5: 1.050v 6: 1.075v 7: 1.100v
7	/	/	/
6:5	R/W	0x0	LVDS_TDATA_SEL 00: LVDS data channel outputs 0. 01: LVDS data channel outputs 1. 10: LVDS data channel outputs Vsync. 11: LVDS data channel outputs Hsync.
4	R/W	0x0	LVDS_REG_PLRC LVDS clock channel direction. 0: Normal 1: Reverse
3:0	R/W	0x0	LVDS_REG_PLR LVDS data channel [3:0] direction. 0: Normal 1: Reverse

15.1.10.38 0x0228 LCD FSYNC Generate Control Register (Default Value: 0x0000_0000)

Offset: 0x0228			Register Name: FSYNC_GEN_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18:8	R/W	0x0	SENSOR_DIS_TIME The period of Fsync Disable delays 0~2047 Hsync Period. When hsync_pol_sel is 0, actual delay is sensor_dis_time-1. When hsync_pol_sel is 1, actual delay is sensor_dis_time.
7	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0228			Register Name: FSYNC_GEN_CTRL_REG
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	SENSOR_ACT1_VALUE Sensor Active1 Value is the Fsync ACT_1 Output Value 0: Fsync active_1 period output 0 1: Fsync active_1 period output 1
5	R/W	0x0	SENSOR_ACT0_VALUE Sensor Active0 Value is the Fsync ACT_0 Output Value 0: Fsync active_0 period output 0 1: Fsync active_0 period output 1
4	R/W	0x0	SENSOR_DIS_VALUE Sensor Disable Value is the Fsync Disable Output Value 0: Fsync disable period output 0 1: Fsync disable period output 1
3	/	/	/
2	R/W	0x0	HSYNC_POL_SEL Hsync Polarity Select 0: Normal 1: opposite hsync to hsync counter
1	R/W	0x0	SEL_VSYNC_EN Select Vsync Enable 0: Select vsync falling edge to trigger state machine toggle 1: Select vsync rising edge to trigger state machine toggle
0	R/W	0x0	FSYNC_GEN_EN Fsync Generate Enable 0: Disable 1: Enable

15.1.10.39 0x022C LCD FSYNC Generate Delay Register (Default Value: 0x0000_0000)

Offset: 0x022C			Register Name: FSYNC_GEN_DLY_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x0	SENSOR_ACT0_TIME The period of Fsync ACT0 delays 0~4095 Pixel clk Period. Actual delay is sensor_act0_time+1.
15:12	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x022C			Register Name: FSYNC_GEN_DLY_REG
Bit	Read/Write	Default/Hex	Description
11:0	R/W	0x0	SENSOR_ACT1_TIME The period of Fsync ACT1 delays 0~4095 Pixel clk Period. Actual delay is sensor_act1_time+1.

15.1.10.40 0x0230 LCD Sync Control Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: LCD_SYNC_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	LCD_CTRL_WORK_MODE LCD Controller Work mode 0: Single DSI mode 1: Dual DSI mode
7:0	/	/	/

15.1.10.41 0x248 LCD LVDS Lane Map Register0 (Default Value: 0x0000_0000)

Offset: 0x248			Register Name: LCD_LVDS_LMAP0_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LVDS_LMAP_EN 0: Disable channel mapping logic. 1: Enable channel mapping logic.
30:19	/	/	/
18:16	R/W	0x0	LANE4_MAP_SOURCE Physical channel lane4 mapping data source. 000: Data comes from address channel 0. 001: Data comes from address channel 1. 010: Data comes from address channel 2. 011: Data comes from address channel 3. 100: Data comes from address channel 4. Others: reserved
15	/	/	/
14:12	R/W	0x0	LANE3_MAP_SOURCE Physical channel lane3 mapping data source. 000: Data comes from address channel 0. 001: Data comes from address channel 1. 010: Data comes from address channel 2. 011: Data comes from address channel 3. 100: Data comes from address channel 4. Others: reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x248			Register Name: LCD_LVDS_LMAP0_REG
Bit	Read/Write	Default/Hex	Description
11	/	/	/
10:8	R/W	0x0	LANE2_MAP_SOURCE Physical channel lane2 mapping data source. 000: Data comes from address channel 0. 001: Data comes from address channel 1. 010: Data comes from address channel 2. 011: Data comes from address channel 3. 100: Data comes from address channel 4. Others: reserved
7	/	/	/
6:4	R/W	0x0	LANE1_MAP_SOURCE Physical channel lane1 mapping data source. 000: Data comes from address channel 0. 001: Data comes from address channel 1. 010: Data comes from address channel 2. 011: Data comes from address channel 3. 100: Data comes from address channel 4. Others: reserved
3	/	/	/
2:0	R/W	0x0	LANE0_MAP_SOURCE Physical channel lane0 mapping data source. 000: Data comes from address channel 0. 001: Data comes from address channel 1. 010: Data comes from address channel 2. 011: Data comes from address channel 3. 100: Data comes from address channel 4. Others: reserved

15.1.10.42 0x24C LCD LVDS Lane Map Register1 (Default Value: 0x0000_0000)

Offset: 0x24C			Register Name: LCD_LVDS_LMAP1_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LVDS_LMAP_EN 0: Disable channel mapping logic. 1: Enable channel mapping logic.
30:19	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x24C			Register Name: LCD_LVDS_LMAP1_REG
Bit	Read/Write	Default/Hex	Description
18:16	R/W	0x0	LANE4_MAP_SOURCE Physical channel lane4 mapping data source. 000: Data comes from address channel 0. 001: Data comes from address channel 1. 010: Data comes from address channel 2. 011: Data comes from address channel 3. 100: Data comes from address channel 4. Others: reserved
15	/	/	/
14:12	R/W	0x0	LANE3_MAP_SOURCE Physical channel lane3 mapping data source. 000: Data comes from address channel 0. 001: Data comes from address channel 1. 010: Data comes from address channel 2. 011: Data comes from address channel 3. 100: Data comes from address channel 4. Others: reserved
11	/	/	/
10:8	R/W	0x0	LANE2_MAP_SOURCE Physical channel lane2 mapping data source. 000: Data comes from address channel 0. 001: Data comes from address channel 1. 010: Data comes from address channel 2. 011: Data comes from address channel 3. 100: Data comes from address channel 4. Others: reserved
7	/	/	/
6:4	R/W	0x0	LANE1_MAP_SOURCE Physical channel lane1 mapping data source. 000: Data comes from address channel 0. 001: Data comes from address channel 1. 010: Data comes from address channel 2. 011: Data comes from address channel 3. 100: Data comes from address channel 4. Others: reserved
3	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x24C			Register Name: LCD_LVDS_LMAP1_REG
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x0	LANE0_MAP_SOURCE Physical channel lane0 mapping data source. 000: Data comes from address channel 0. 001: Data comes from address channel 1. 010: Data comes from address channel 2. 011: Data comes from address channel 3. 100: Data comes from address channel 4. Others: reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.2 TCON_TV

15.2.1 Overview

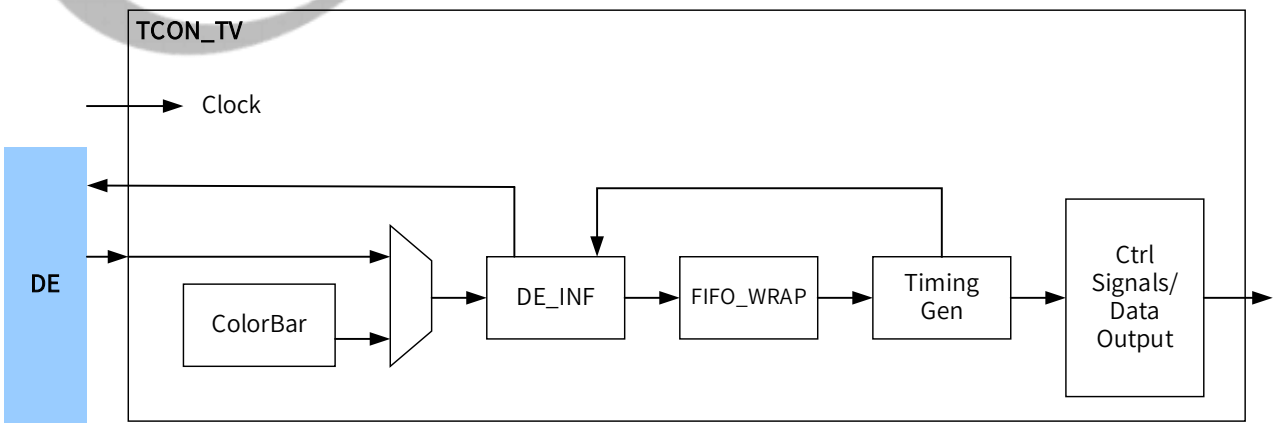
TCON_TV is a bridge module between DE and HDMI_TX/EDP_TX to generate video timing.

The TCON_TV includes the following features:

- Two TCON_TV controllers: TCON_TV0 and TCON_TV1
  - TCON_TV0 controls HDMI interface
  - TCON_TV1 controls eDP interface
- Supports configuring TCON_TV registers through AHB bus
- Supports outputting the video timing of HDMI2.0b and the video format of 4096×2160@60fps
- Supports 1/2/4 pixel interface mode.
- Supports 6/8/10 color depth.
- Supports RGB444, YCbCr444, YCbCr422, and YCbCr420 input.
- Supports generating interlaced-scanning odd and even field video timing, including VIC39.
- Supports 3D framepacking active space insert.
- Supports the colorbar testing of four kinds of patterns.
- Supports outputting DDR dynamic frequency modulation indication.
- Supports outputting the line-triggered and field-triggered maskable interrupts.
- Supports outputting the configurable polarity of the signals of HSYNC, VSYNC, DE, and data.

15.2.2 Block Diagram

Figure 15-16 TCON_TV Block Diagram



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

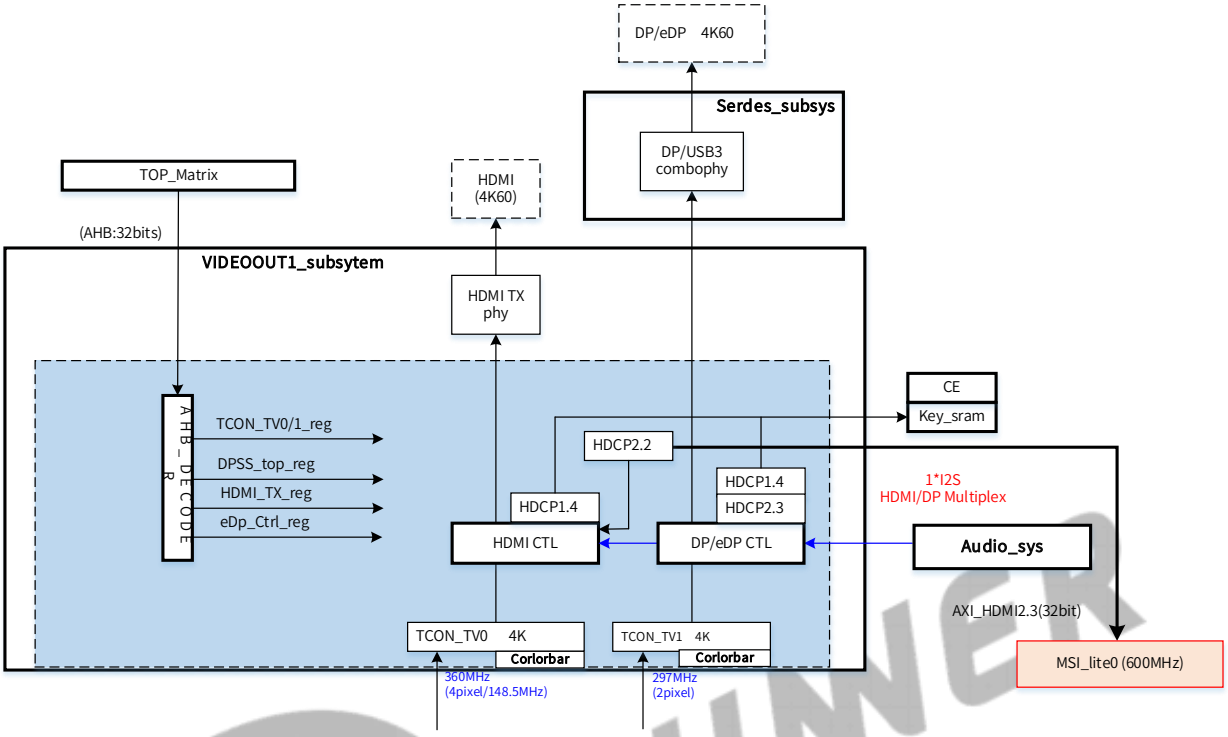
Figure 15-17 TCON_TV Sub-blocks

Sub-blocks	Description
ColorBar	It is the testing module. When the colorbar is enabled, it will generate the four testing patterns, including colorbar, lattice, grayscale, and grid. It can be configured as the output mode of 1/2/4 pixels. During the normal working, the colorbar should be disabled.
DE_INF	It is the interface processing module. According to the indication signal generated by ctrl_gen and the filling state of TVFIFO, it interacts with the previous stage DE and vdbist to obtain valid pixel data, so as to complete the pixel sampling, and generate the write and clear control of tvfifo.
FIFO_wrapper	It is the synchronized data caching module. It completes data writing according to the write control signal generated by ed_inf, and generate a filling status indication. Then, it completes data reading according to the read control signal generated by the ctrl_gen module.
ctrl_gen	It is the timing generation module. It generates the video timing according to the video format parameters configured by registers, including non-interlaced, interlaced, 3D mode and VRR timing; besides, it generates TVFIFO read control, and completes timing alignment. It can be configured as 1/2/4 pixel output mode.
ctrl_data_out	It is the output module of control and data signals. It completes the polarity adjustment based on the video timing signals generated by ctrl_gen.
ctrl_reg	Register Module

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.2.3 Environment Diagram

Figure 15-18 TCON_TV Environment Diagram



15.2.4 Clock Sources

The following table describes the clock sources of TCON_TV. For clock setting, configurations, and gating information, refer to the section Clock Controller Unit (CCU).

Module	Clock Sources	Description
TCON_TV0/1	VIDEO0PLL4X	Its frequency is 1188 MHz by default.
	VIDEO1PLL4X	Its frequency is 1188 MHz by default.
	VIDEO2PLL4X	Its frequency is 1188 MHz by default.
	PERI0PLL2X	Its frequency is 1.2 GHz by default.

15.2.5 External Signals

The following table describes the external I/O signals of HDMI. For the external I/O signals of eDP, refer to the section SERDES.

Table 15-11 HDMI External Signals

Signal Name	Description	Type
HTX0P	HDMI Positive TMDS Differential Line Driver Data0 Output	AO
HTX0N	HDMI Negative TMDS Differential Line Driver Data0 Output	AO
HTX1P	HDMI Positive TMDS Differential Line Driver Data1 Output	AO
HTX1N	HDMI Negative TMDS Differential Line Driver Data1 Output	AO
HTX2P	HDMI Positive TMDS Differential Line Driver Data2 Output	AO
HTX2N	HDMI Negative TMDS Differential Line Driver Data2 Output	AO

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

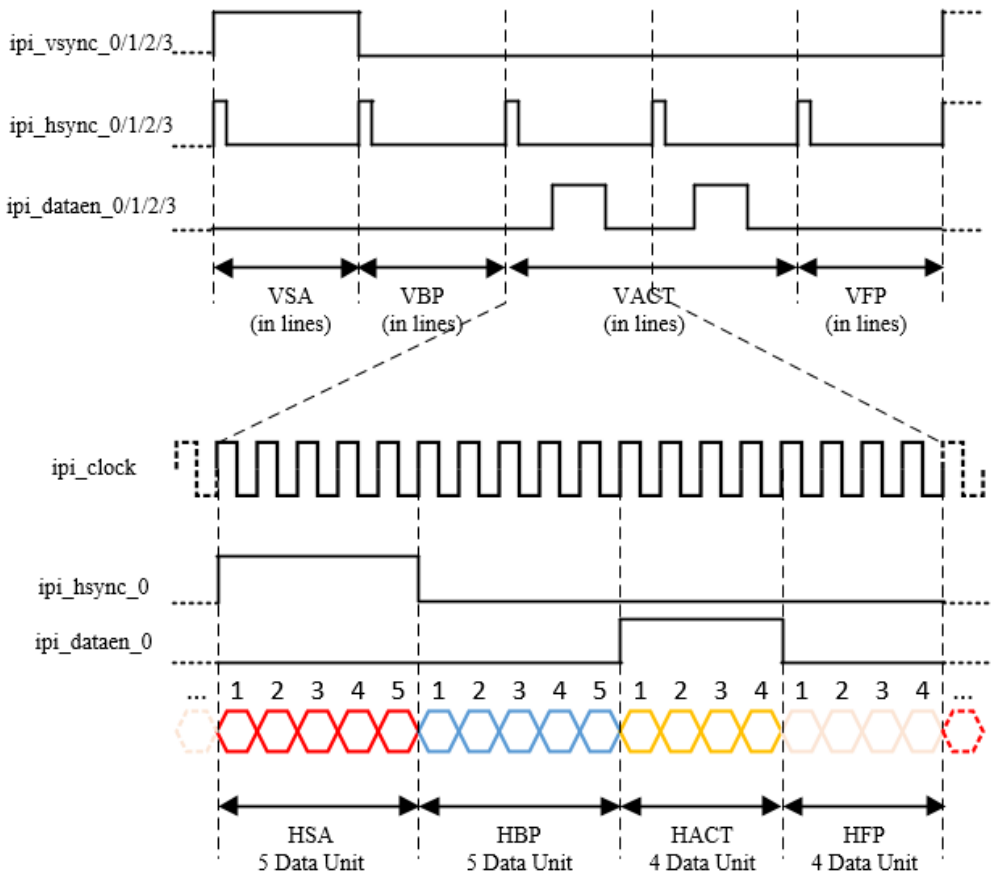
Signal Name	Description	Type
HTXCP	HDMI Positive TMDS Differential Line Driver Clock Output	AO
HTXCN	HDMI Negative TMDS Differential Line Driver Clock Output	AO
HSCL/HDMI-SCL	HDMI Serial Clock	OD
HSDA/HDMI-SDA	HDMI Serial Data	OD
HCEC/HDMI-CEC	HDMI Consumer Electronics Control	OD
HHPD	HDMI Hot Plug Detection Signal	AI
HREXT	HDMI Reference Resistance	AO
VCC18-HDMI	1.8V Analog Supply for HDMI IO	P
VDD08-HDMI	0.8V HDMI Digital Power Supply	P

15.2.6 Functional Description

15.2.6.1 Pixel Mode

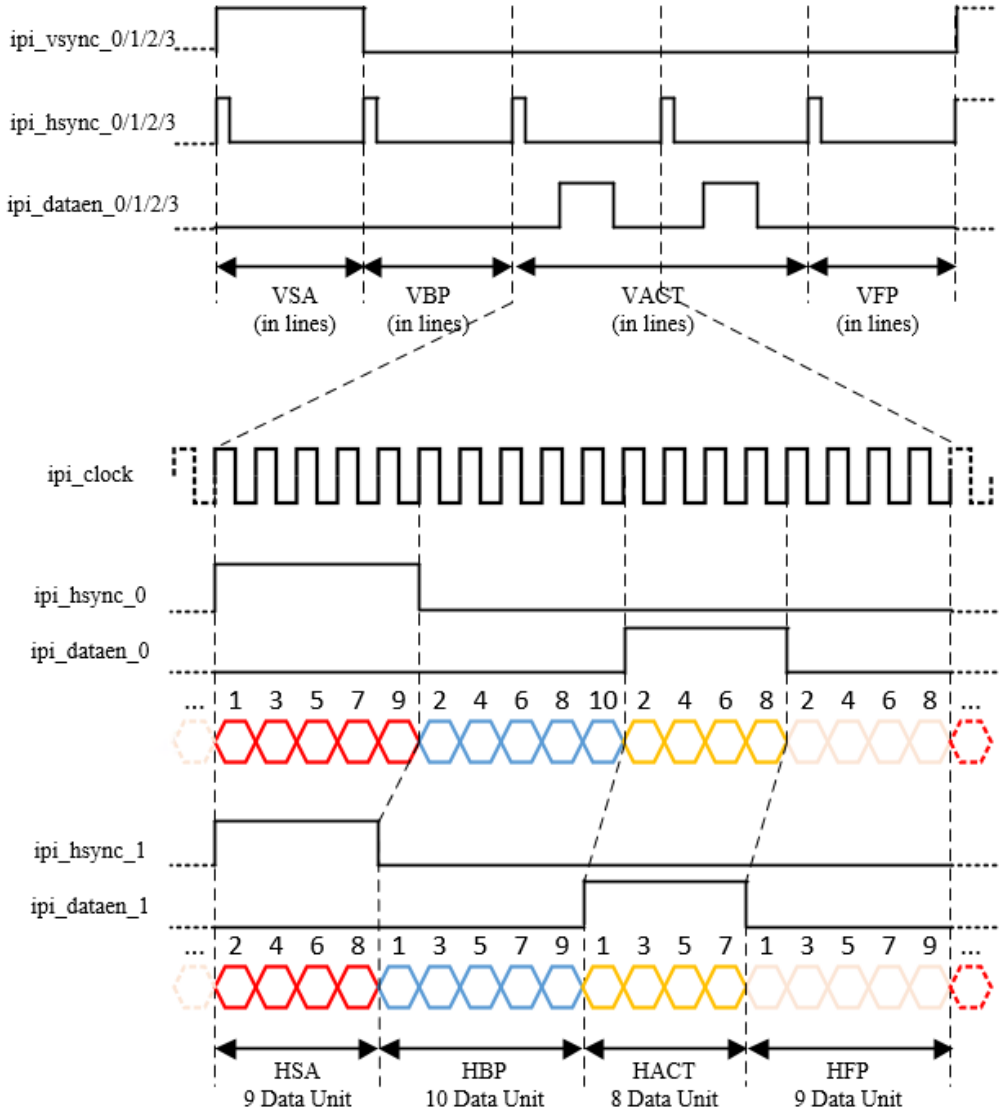
TCON_TV can be configured as single/dual/quad pixel modes through registers.

Figure 15-19 Single Pixel Mode



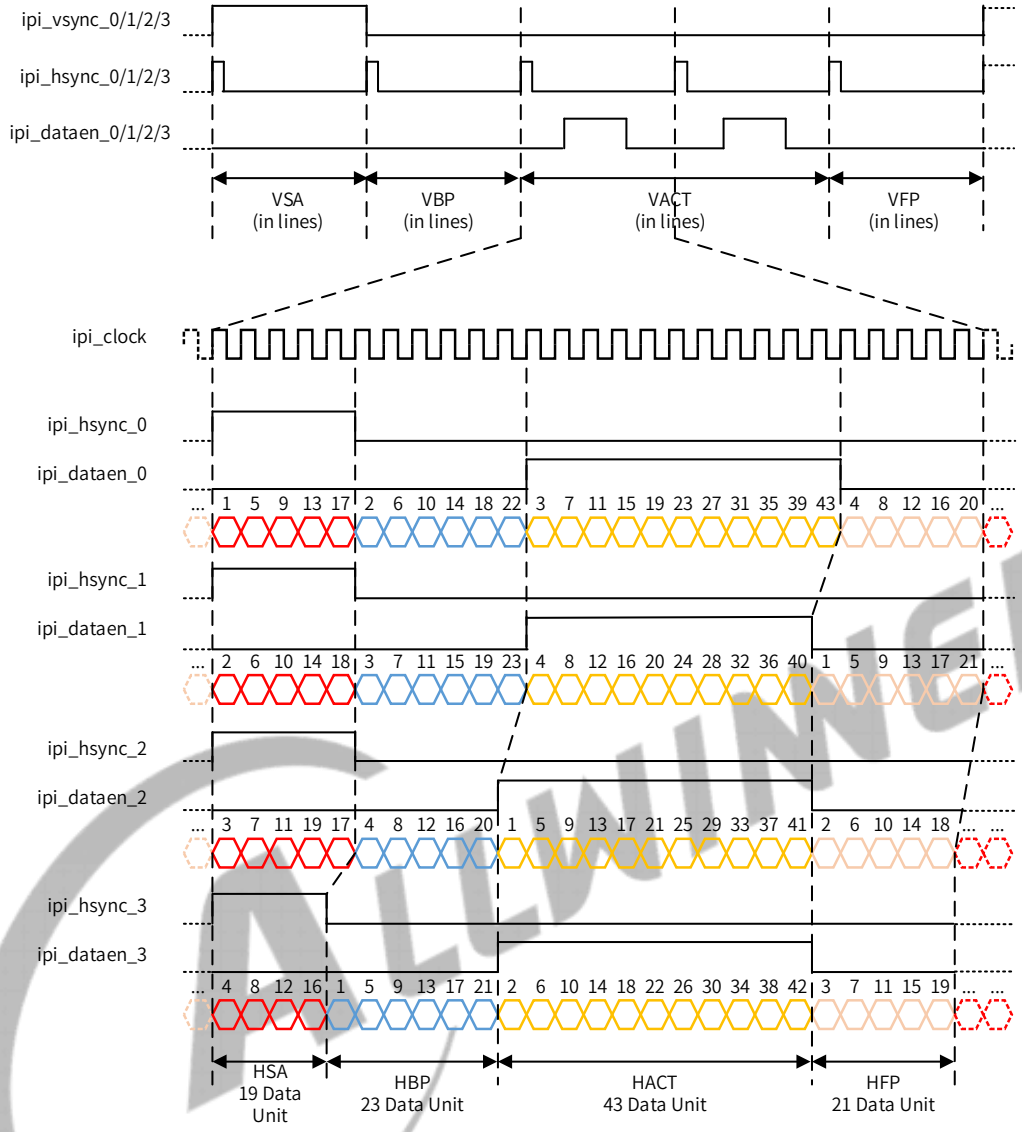
Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 15-20 Dual Pixel Mode



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 15-21 Quad Pixel Mode



a) The application instructions of pixel modes

The multiple modes are designed for lowering the high refreshing rate and the pixel clock frequency in the high resolution. For instance, in the 4 pixel mode, the video format of 8K@60fps can be lowered from 2376MHz to 594MHz, which is more friendly to timing restriction and backend implementation. In the other resolutions, it is recommended to use multiple modes as needed to effectively lower the requirements on the pixel clock frequency.

b) The application restrictions of pixel modes

The pixel modes of TCON_TV should be consistent with those of HDMI controller, eDP controller, and DE.

c) The configuration guidelines of pixel modes

The pixel modes are selected from 1/2/4 pixels in the TV_GCTL_REG.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.2.6.2 Unstrict Timing Mode

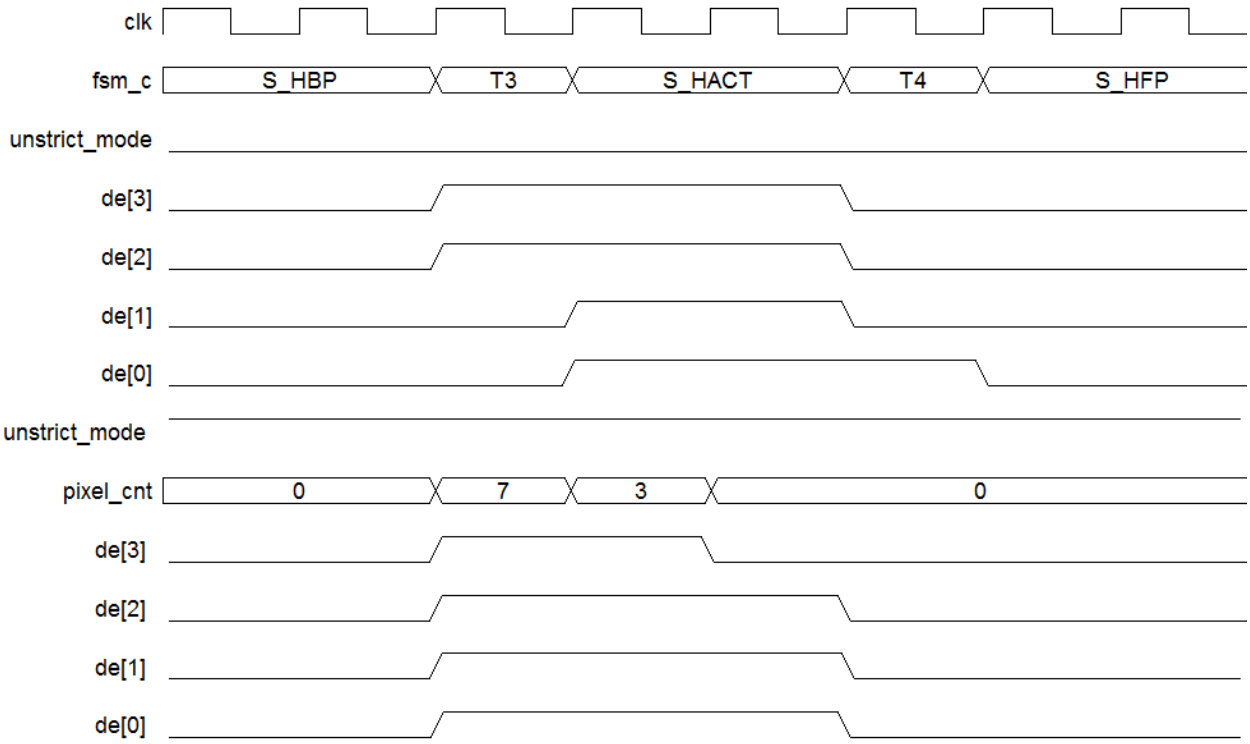
The requirements of unstrict timing mode on the data in the stage of Hactive are as follows.

Figure 15-22 4-Pixel Mode without Variable Pixel Dring-Picture Width=11 pixels

dsc_pxl_dat_i[4*PDW-1 : 3*PDW]	3	7		HBlank	3	7		HBlank	3	7		HBlank	3	7		HBlank	3	7		HBlank
dsc_pxl_dat_i[3*PDW-1 : 2*PDW]	2	6	10		2	6	10		2	6	10		2	6	10		2	6	10	
dsc_pxl_dat_i[2*PDW-1 : 1*PDW]	1	5	9		1	5	9		1	5	9		1	5	9		1	5	9	
dsc_pxl_dat_i[1*PDW-1 : 0*PDW]	0	4	8		0	4	8		0	4	8		0	4	8		0	4	8	
dsc_pxl_dat_vld_i	4'hF	4'hF	4'h7		4'hF	4'hF	4'h7		4'hF	4'hF	4'h7		4'hF	4'hF	4'h7		4'hF	4'hF	4'h7	
Line	Line-0				Line-1				Line-2				Line-3				Line-4			

In the multiple pixel mode of unstrict timing, the multiple lane synchronization is valid at the beginning of every effective pixel data except for last group. The unstrict timing mode is mainly for meeting the requirements of DSC and eDP, which is configured in the TV_GCTL_REG.

The following figure shows the differences of DE signals between non-strict timing and strict timing (Hactive=11)

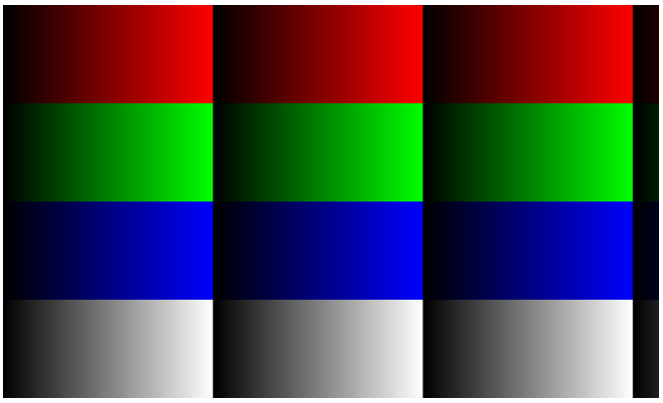


15.2.6.3 VDBIST

TCON_TV can generate the following pattern modes for the lane testing and debug of TCON_TV->HMDI(EDP)->Screen.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 15-23 RGB Colorbar Pattern



Theory: The display area is divided into 4 equal parts vertically, which are red, green, blue, and gray color bars.

Take an example of 8bit.

Red color bars: R=0X00+i G=0X00 B=0X00

Green color bars: R=0X00 G=0X00+i B=0X00

Blue color bars: R=0X00 G=0X00 B=0X00+i

Grey color bars: R=0X00+i G=0X00+i B=0X00+i

NOTE

The value of i ranges from 0~255. Only R component is variable.

Figure 15-24 Grey Pattern

Theory: The display area is horizontally divided based on the gray scale. When the screen width is less than that of gray scale, the gray scale of pixels in each line changes sequentially. When the screen width is larger than that of gray scale, multiple pixels in each line will be in the same gray scale.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

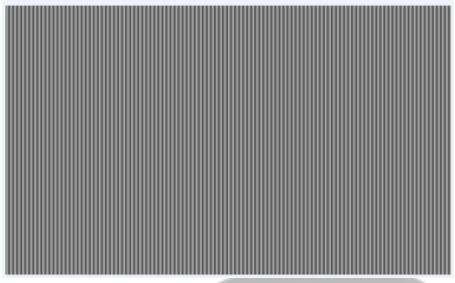
NOTE

The black bar on the right side of the screen is also gradient, although it is not visible to the naked eyes. Divide the display area into 4 equal parts vertically. The closer to the bottom of screen, the thinner the grey density.

Take an example of 8bit, the horizontal gray scale is as follows.

R=0X00+i G=0X00+i B=0X00+I (The color component ranges from 0~255)

Figure 15-25 Dot Pattern



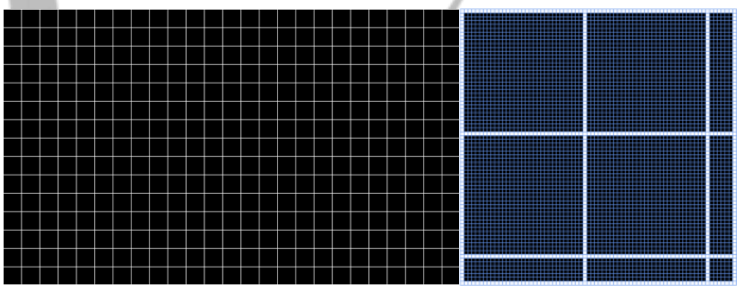
The pixels in each line alternate between white and black.

Take an example of 8bit.

Black: R=0X00 G=0X00 B=0X00

White: R=0XFF G=0XFF B=0XFF

Figure 15-26 Grid Pattern



Theory: The grid pattern consists of many 32x32 grids with white borders. In addition, the four borders of display area are white, and the rest are black.

Take an example of 8bit.

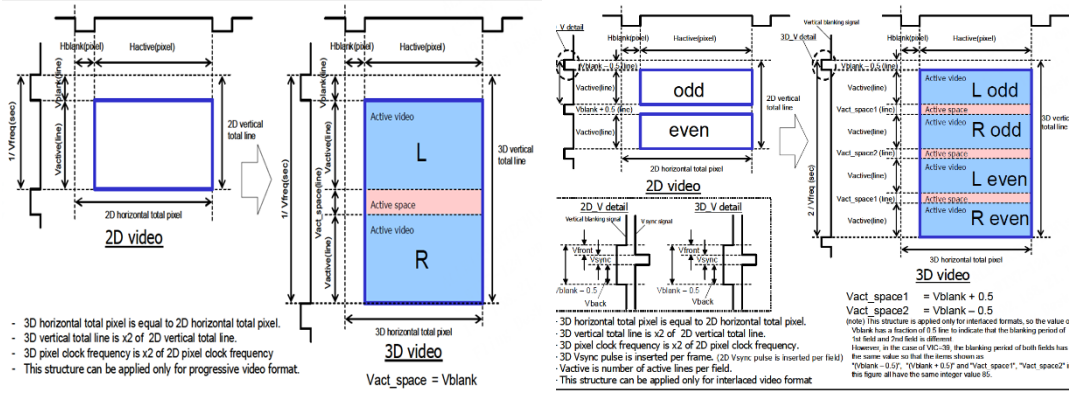
Black: R=0X00 G=0X00 B=0X00

White: R=0XFF G=0XFF B=0XFF

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.2.6.4 3D Mode

TCON_TV supports inserting the active space in the frame_packing mode. In this mode, the timing of 3D display is described as below. The left is progress scanning, and the right is interlaced scanning.



15.2.7 Programming Guidelines

15.2.7.1 Pixel Clock Configuration

TCON_TV supports connecting to HDMI and eDP.

In the HDMI mode, the pixel clock of TCON_TV is that of CCU or HDMI PHY, which can be selected by the hdmi_ck_phy_ccu_sel.

In the eDP mode, the pixel clock of TCON_TV is that of eDP PHY.

15.2.7.2 Module Configuration

Step 1 Select from 1/2/4 pixel modes in the TV_GCTL_REG[5:4].

Step 2 Configure color depth, video format, and even-odd field indication control in the TV_PIXELDEPTH_MODE_REG.

Step 3 Configure the video parameters, and set the line and field as required by the screen timing.

Step 4 Configure the DDR frequency modulation mode and frequency modulation line interval in the TV_SAFE_PERIOD_REG0 and TV_SAFE_PERIOD_REG1. (Optional. Frequency modulation is not permitted by default. Skip this step if no frequency modulation is needed.)

Step 5 Set and enable the line/field interrupts in the TV_GINT0_REG and TV_GINT1_REG. (Optional. Skip this step if no line/field interrupt needs to be enabled.)

Step 6 Decide whether to enable RGB output. (Optional. Skip this step if RGB output doesn t need to be enabled.)

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

CAUTION

When RGB output is enabled, only 1 Pixel Mode can be selected in the step 1.

Step 7 Select the data source and testing pattern from the TV_SRC_CTL_REG [0] and TV_SRC_CTL_REG [2:1].

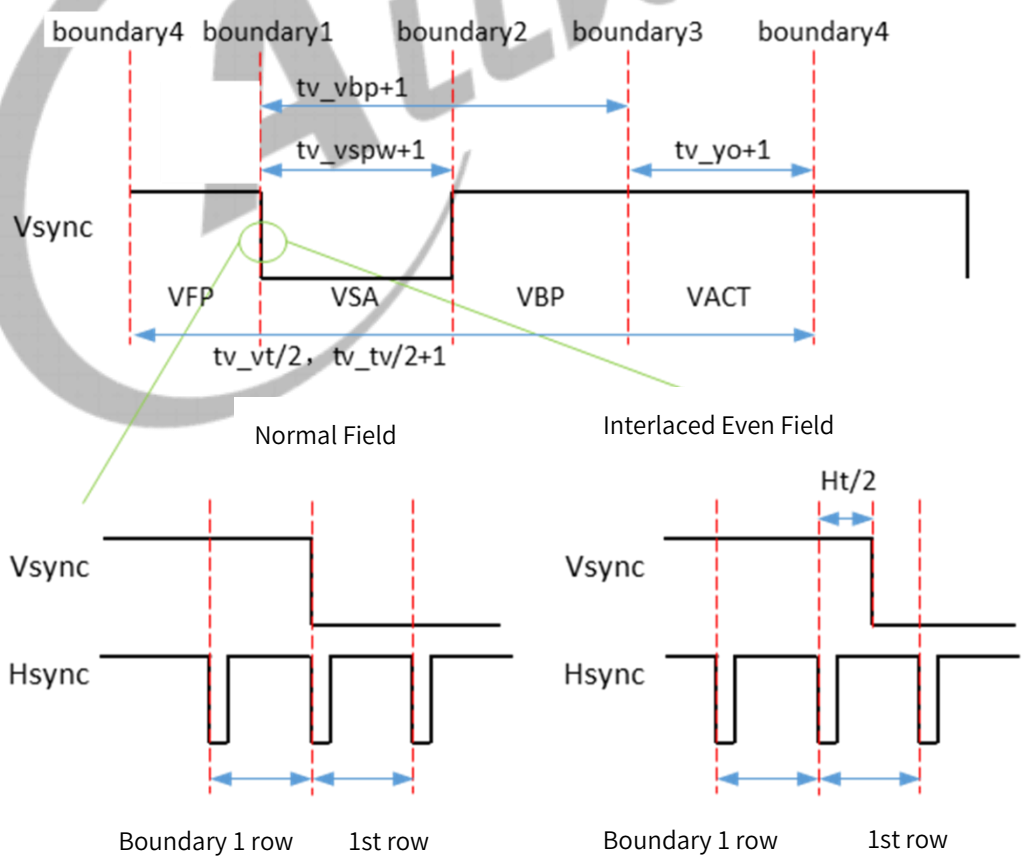
Step 8 Set the Start_Delay in the TV_CTL_REG [19:4] to control the time of de-asserting the sync signal to DE. Then enable the module in the TV_CTL_REG [31].

15.2.7.3 Line and Field Interrupt Configuration

TCON_TV provides a field interrupt. An interrupt will be generated after each field finishes (namely, the Vacvitive finishes transmitting). It provides four configurable line interrupts, which will be generated when the timing enters the triggering lines.

The line counting is shown as below. When the timing enters the VSA, the line counters starts counting from 1.

Figure 15-27 Line Counting



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

NOTE

a) A line indicates that the period from Hysync to Hfront.

b) A field indicates that the period from the first line of Vfront to the last line of Vactive.

15.2.7.4 Video Parameter Configuration

RGB444&YCbCr444&YCbCr422 Mode

Register	Configuration	Value
TV_XO	The effective lines of image in the field -1	Hactive - 1
HSPW	Line signal length-1	Hsync - 1
HBP	Field synchronization signal length + Field synchronization back porch length - 1	Hsync + Hback - 1
HT	Total pixel in a line of data –1	Htotal - 1

YCbCr420 Mode

Register	Configuration	Value
TV_XO	The effective lines of image in the field/2 -1	(Hactive/2) - 1
HSPW	Line signal length/2 -1	(Hsync/2) - 1
HBP	Field synchronization signal length + Field synchronization back porch length/2 -1	(Hsync/2) + (Hback/2) - 1
HT	Total pixel in a line of data/2 –1	(Htotal/2) - 1

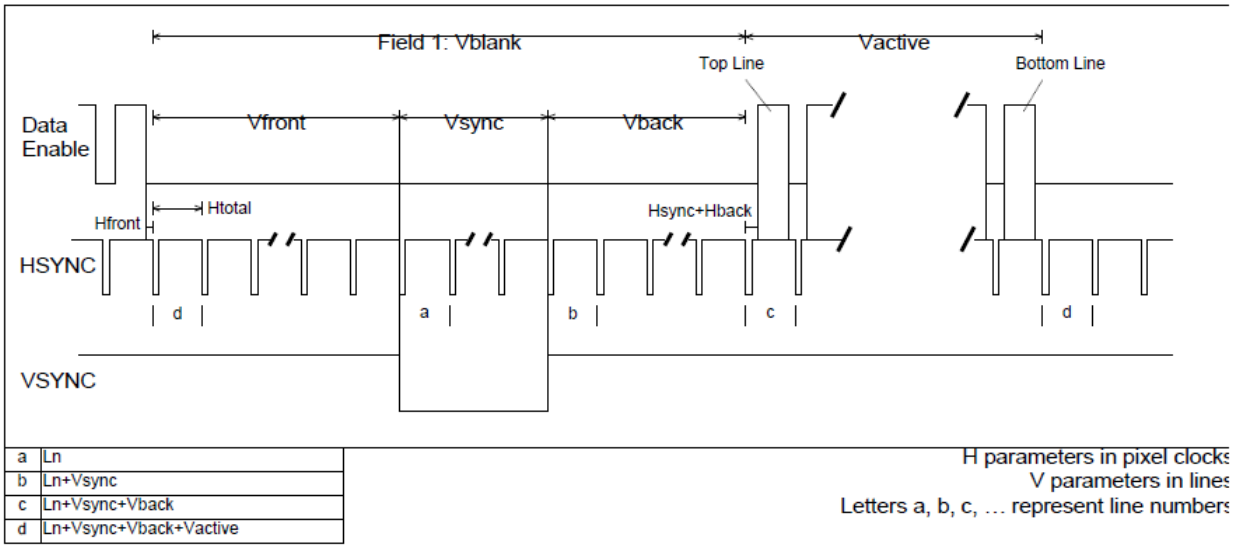
2D Mode

Progressive Scanning

In the 2D mode, the registers (TV_Fill_En, Fill_Begin, Fill_End, and Fill_Value) related to 3D needs no configuration.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 15-28 Progressive Scanning



Register	Configuration	Value
TV_YO	The effective lines of image in the field - 1	Vactive - 1
VT	All the lines in a frame of image *2 The VT is divided by 2 within the module	2*Vtotal
VBP	Field synchronization signal length + Field synchronization back porch length - 1	Vsync + Vback - 1
VSPW	Field synchronization signal length -1	Vsync - 1

Take an example of VIC1676, 1920×1080P@60Hz.

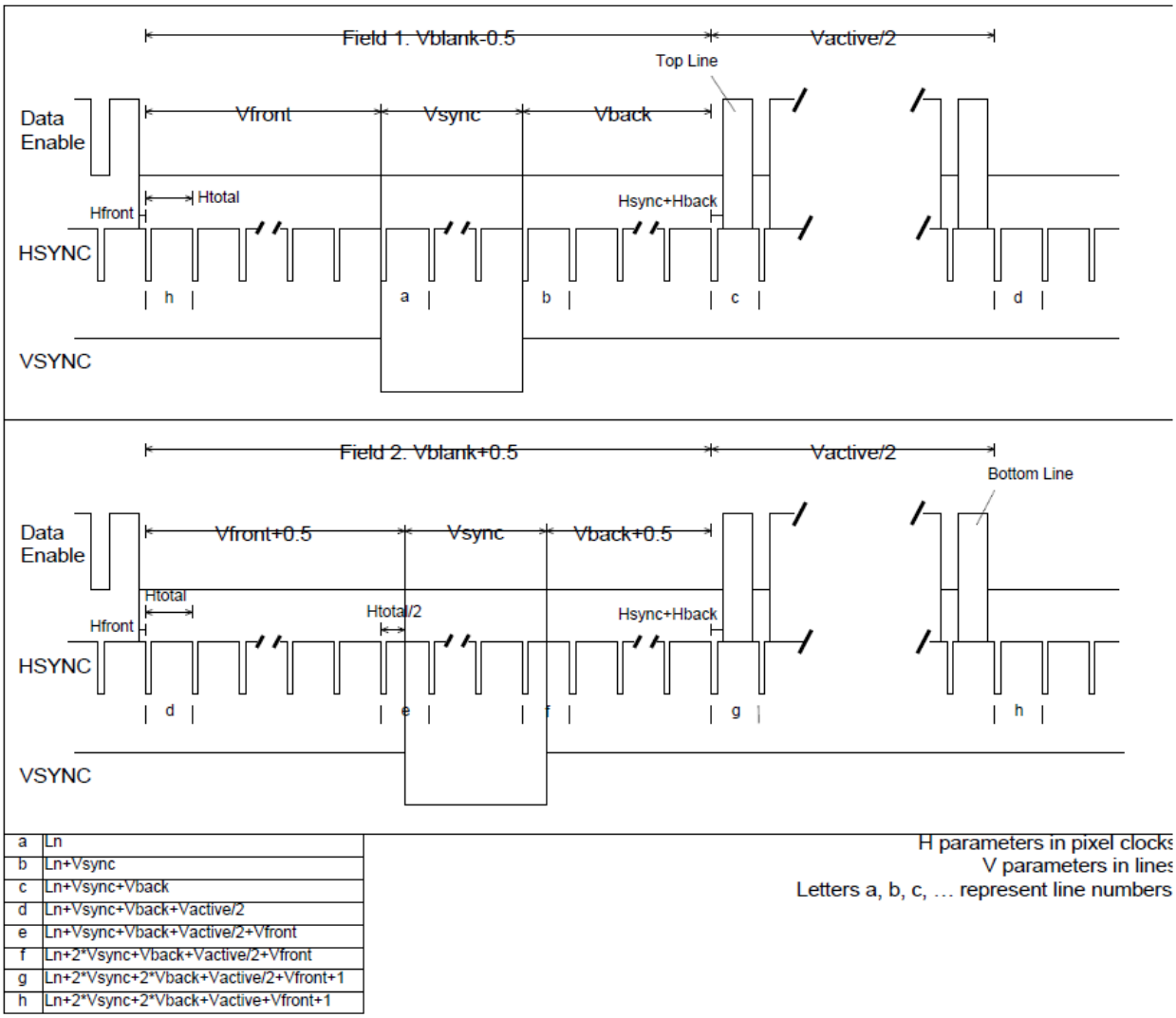
According to the CTA-861-H, Vactive=1080, Vfront=4, Vback=36, Vsync=5, Vtotal=1125 for the video format.

Thus, the values of registers are TV_YO=1079, VSPW=4, VBP=40, VT=2250.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Interlaced Scanning

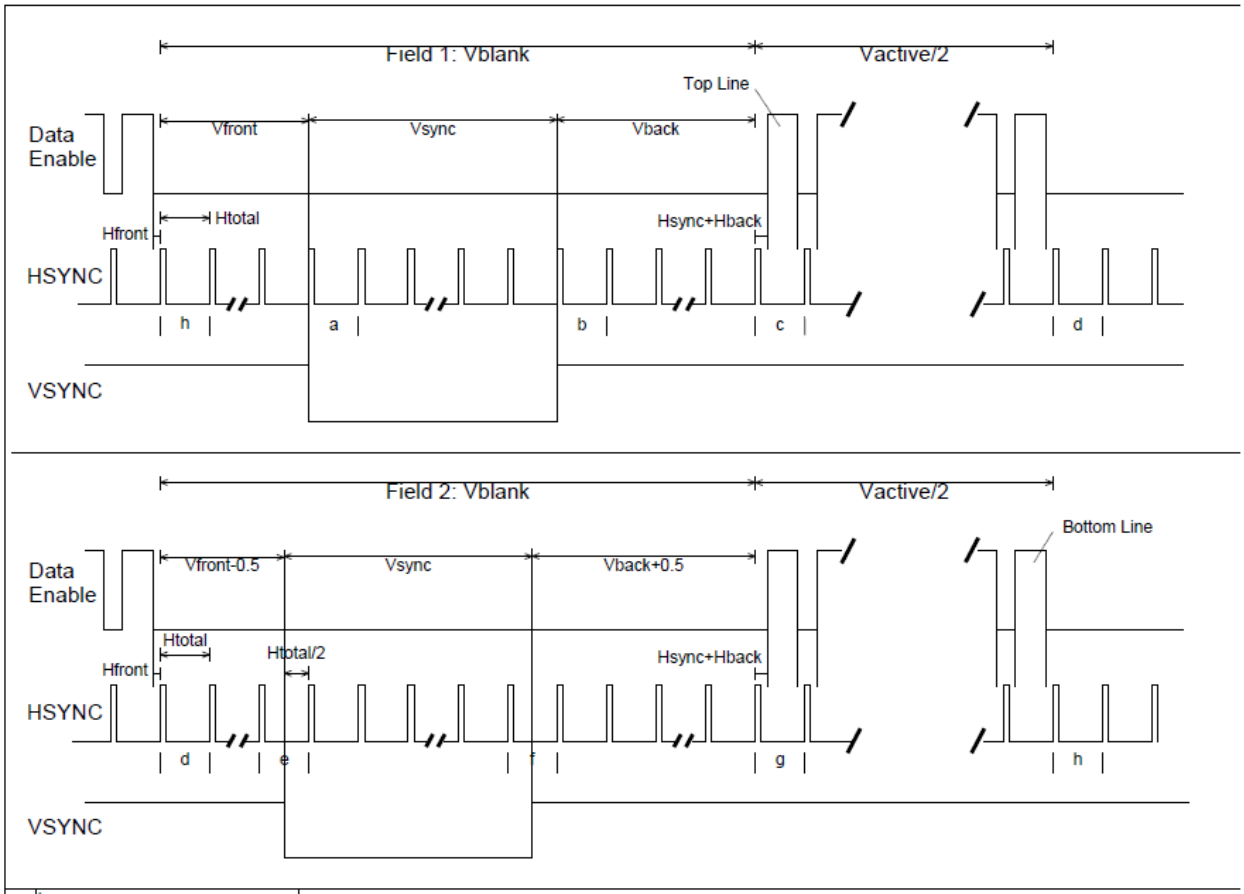
Figure 15-29 Interlaced Scanning



Register	Configuration	Value
VIC39IND	The current video format is VIC39	0
TV_YO	The effective lines of image in the field - 1	Vactive/2 - 1
VT	All the lines in a frame of image (odd field+even field). The actual lines of odd field and even field will be calculated within the module.	Vtotal
VBP	Field synchronization signal length + Field synchronization back porch length - 1	Vsync + Vback - 1
VSPW	Field synchronization signal length -1	Vsync - 1

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Special Interlaced Scanning (VIC39)



a	Ln
b	Ln+Vsync
c	Ln+Vsync+Vback
d	Ln+Vsync+Vback+Vactive/2
e	Ln+Vsync+Vback+Vactive/2+Vfront-1
f	Ln+2*Vsync+Vback+Vactive/2+Vfront-1
g	Ln+2*Vsync+2*Vback+Vactive/2+Vfront
h	Ln+2*Vsync+2*Vback+Vactive+Vfront

H parameters in pixel clocks
V parameters in lines
Letters a, b, c, ... represent line numbers

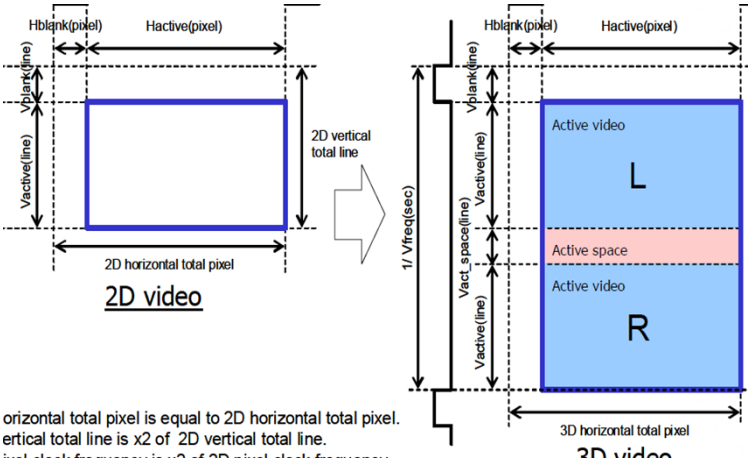
Register	Configuration	Value
VIC39IND	The current video format is VIC39	1
TV_YO	The effective lines of image in the field - 1	Vactive/2 - 1
VT	All the lines in a frame of image (odd field+even field). The actual lines of odd field and even field will be calculated within the module.	Vtotal
VBP	Field synchronization signal length + Field synchronization back porch length - 1	Vsync + Vback - 1
VSPW	Field synchronization signal length -1	Vsync - 1

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

3D Mode

Progressive Scanning

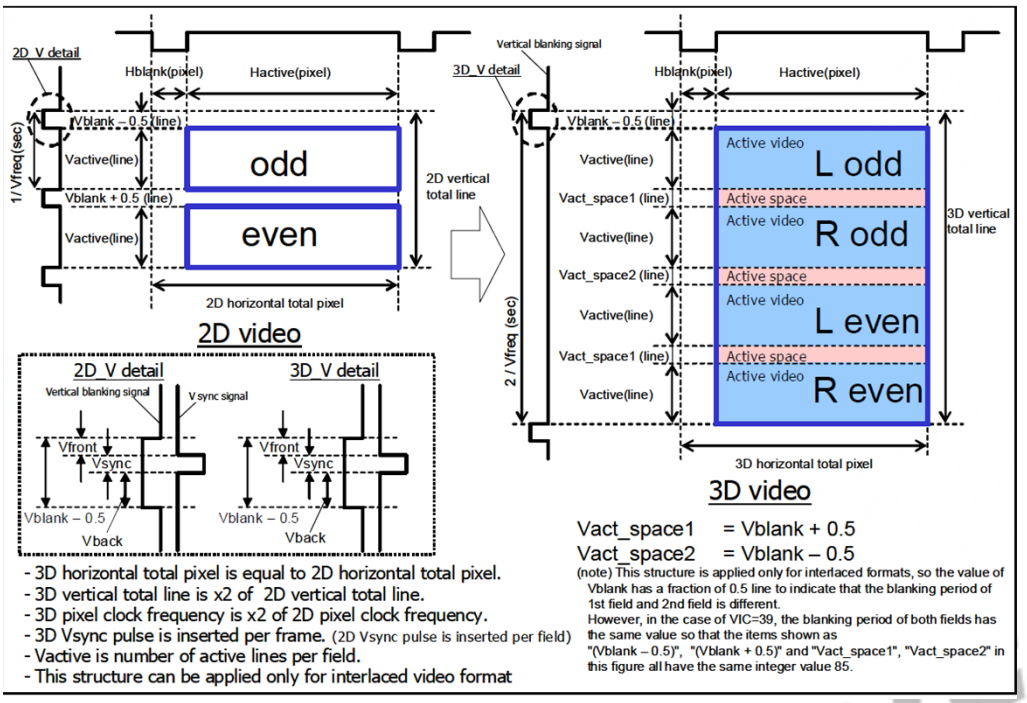
The following figure shows the frame format of progressive scanning in 3D Mode, in which a frame of data is equal to 2 frames of data in 2D mode, and the total lines are twice those of 2D mode. In the Active Space, valid data will not be transmitted; instead, the data configured by registers will be filled. The starting and ending lines to be filled are configured by registers.



Register	Configuration Description	Configuration Value
VIC39IND	The current video format is VIC39	0
TV_YO	The effective lines of image in the 3D mode - 1	2*Vtotol - Vfront - Vsync - Vback - 1
VT	The total lines of image in the 3D mode*2	4*Vtotal
VBP	Field synchronization signal length + Field synchronization back porch length - 1	Vsync + Vback - 1
VSPW	Field synchronization signal length -1	Vsync - 1
TV_Fill_En	3D filling enable	1
Fill_Begin1	The starting lines in the Active Space	Vsync + Vback + Vactive + 1
Fill_End1	The ending lines in the Active Space	Vtotol + Vsync + Vback
Fill_Value1	The filled data in the Active Space	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Interlaced Scanning

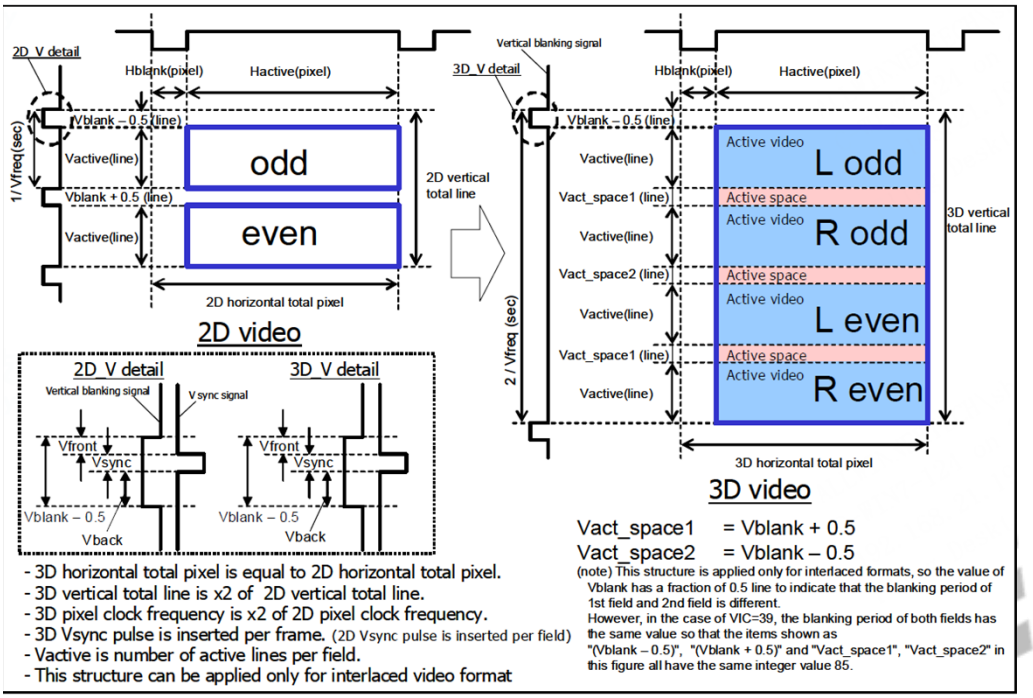


Register	Configuration	Value
VIC39IND	The current video format is VIC39	0
TV_YO	The effective lines of image in the 3D mode - 1	2*Vtotol - Vfront - Vsync - Vback - 1
VT	The total lines of image in the 3D mode*2	4*Vtotal
VBP	Field synchronization signal length + Field synchronization back porch length - 1	Vsync + Vback - 1
VSPW	Field synchronization signal length-1	Vsync - 1
TV_Fill_En	3D filling enable	1
Fill1_Begin	The starting line in Active Space1	Vsync + Vback + Vactive/2 + 1
Fill1_End	The ending line in Active Space1	2*Vsync + 2*Vback + Vactive/2 + Vfront + 1
Fill1_Value	The filled data in Active Space1	
Fill2_Begin	The starting line in Active Space2	2*Vsync + 2*Vback + Vactive + Vfront + 2
Fill2_End	The ending line in Active Space2	3*Vsync + 3*Vback + Vactive + 2*Vfront + 1
Fill2_Value	The filled data in Active Space2	
Fill3_Begin	The starting line in Active Space3	3*Vsync + 3*Vback + 1.5*Vactive + 2*Vfront + 2
Fill3_End	The ending line in Active Space3	4*Vsync + 4*Vback + 1.5*Vactive + 3*Vfront + 2

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Fill3_Value	The filled data in Active Space3	/

3D Mode Special Interlaced Scanning



Register	Configuration	Value
VIC39IND	The current video format is VIC39	0
TV_YO	The effective lines of image in the 3D mode - 1	2*Vtotol - Vfront - Vsync - Vback - 1
VT	The total lines of image in the 3D mode*2	4*Vtotal
VBP	Field synchronization signal length + Field synchronization back porch length - 1	Vsync + Vback - 1
VSPW	Field synchronization signal length-1	Vsync - 1
TV_Fill_En	3D filling enable	1
Fill1_Begin	The starting line in Active Space1	Vsync + Vback + Vactive/2 + 1
Fill1_End	The ending line in Active Space1	2*Vsync + 2*Vback + Vactive/2 + Vfront
Fill1_Value	The filled data in Active Space1	/
Fill2_Begin	The starting line in Active Space2	2*Vsync + 2*Vback + Vactive + Vfront + 1
Fill2_End	The ending line in Active Space2	3*Vsync + 3*Vback + Vactive + 2*Vfront
Fill2_Value	The filled data in Active Space2	
Fill3_Begin	The starting line in Active Space3	3*Vsync + 3*Vback + 1.5*Vactive + 2*Vfront + 1

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Fill3_End	The ending line in Active Space3	4*Vsync + 4*Vback + 1.5*Vactive + 3*Vfront
Fill3_Value	The filled data in Active Space3	

15.2.8 Register List

Module Name	Base Address
VIDEO_OUT1_SYS	
VIDEO_OUT1_SYS	0x05510000
TCON_TV Controller	
TCON_TV0	0x05730000
TCON_TV1	0x05731000

Register Name	Offset	Description
VIDEO_OUT1_SYS		
TV_CLK_EDP_I2S1_SRC	0x0000	TCON_TV Clock Select And EDP I2S1 Select Register
VO1_MODULE_GATING	0x0020	TCON_TV Output To HDMI Gating Register
TCON_TV Controller		
TV_GCTL_REG	0x0000	TV Global Control Register
TV_GINT0_REG	0x0004	TV Global Interrupt0 Register
TV_GINT1_REG	0x0008	TV Global Interrupt1 Register
TV_GINT2_REG	0x000C	TV Global Interrupt2 Register
TV_SRC_CTL_REG	0x0040	TV Source Control Select Register
TV_CTL_REG	0x0090	TV Control Register
TV_BASIC1_REG	0x0098	TV Basic Timing0 Register
TV_BASIC2_REG	0x009C	TV Basic Timing1 Register
TV_BASIC3_REG	0x00A0	TV Basic Timing2 Register
TV_BASIC4_REG	0x00A4	TV Basic Timing3 Register
TV_BASIC5_REG	0x00A8	TV Basic Timing4 Register
TV_IO_POL_REG	0x0088	TV SYNC Signal Polarity Control Register
TV_IO_TRI_REG	0x008C	TV SYNC Signal IO Enable Control Register
TV_DEBUG_REG	0x00FC	TV Debug Register
TV_SAFE_PERIOD0_REG	0x01F0	TV Safe Period0 Register
TV_SAFE_PERIOD1_REG	0x01F4	TV Safe Period1 Register
TV_FILL_CTL_REG	0x0300	TV Fill Data Control Register
TV_FILL_BEGIN_REG	0x0304+N*0x0C (N=0~2)	TV Fill Data Begin Register
TV_FILL_END_REG	0x0308+N*0x0C (N=0~2)	TV Fill Data End Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
TV_FILL_DATA_REG	0x030C+N*0x0C (N=0~2)	TV Fill Data Value Register
TV_FILL_DATAH1	0x0328	TV Fill Data High1 Value Register
TV_FILL_DATAH2	0x032C	TV Fill Data High2 Value Register
TV_DATA_IO_POL0_REG	0x0330	TV Data IO Polarity Control0 Register
TV_DATA_IO_POL1_REG	0x0334	TV Data IO Polarity Control1 Register
TV_DATA_IO_TRI0_REG	0x0338	TV Data IO Enable Control0 Register
TV_DATA_IO_TRI1_REG	0x033C	TV Data IO Enable Control1 Register
TV_PIXELDEPTH_MODE_REG	0x0340	TV Pixeldepth Mode Control Register

15.2.9 VIDEO_OUT1_SYS Register Description

15.2.9.1 0x0000 TCON_TV Clock Select and EDP I2S1 Select Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TV_CLK_EDP_I2S1_SRC
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	TCON_TV1_EDP_HDMI_CK_SEL 0: TCON_TV1 clock sources from HDMI 1: TCON_TV1 clock sources from EDP If TCON_TV1 is used for EDP, the bit should be set to 1.
4	R/W	0x0	TCON_TV1_CLK_SRC TCON TV1 Clock Source 0: Clock from CCMU 1: Clock from CVBSOUT1
3	R/W	0x0	TCON_TV0_HDMIPHY_CCU_CK_SEL 0: TCON_TV0 clock sources from HDMI PHY 1: TCON_TV0 clock sources from CCU If TCON_TV1 is used for HDMI, the bit should be set to 1 when HDMI works in the RFL mode.
2	/	/	/
1	R/W	0x0	TV0_EDP_HDMI_CK_SEL 0: TCON_TV0 clock sources from HDMI 1: TCON_TV0 clock sources from EDP If TCON_TV0 is used for HDMI, the bit should be set to 0.
0	R/W	0x0	TCON_TV0_CLK_SRC TCON TV0 Clock Source 0: Clock from CCMU 1: Clock from CVBSOUT0

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.2.9.2 0x0020 TCON_TV Output to HDMI Gating Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: VO1_MODULE_GATING
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R/W	0x0	TV0_HDMI_GATE TV0 HDMI Gate 0: Gating 1: Release
27:22	/	/	/
21	R/W	0x0	TV1_GATE TV1 Gate 0: Gating 1: Release
20	R/W	0x0	TV0_GATE TV0 Gate 0: Gating 1: Release
19:0	/	/	/

15.2.10 TCON_TV Register Description

15.2.10.1 0x0000 TV Global Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TV_GCTL_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5:4	R/W	0x0	PIXEL_MODE Pixel Mode Selection 00: 1 pixel 01: 2 pixel 10: 4 pixel 11: Reserved
3:1	/	/	/
0	R/W	0x0	UNSTRICT_TIMING_MODE_SEL 0: Strict timing mode 1: Unstrict timing mode

15.2.10.2 0x0004 TV Global Interrupt0 Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: TV_GINT0_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: TV_GINT0_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R/W	0x0	TV_VB_INT_EN Field Interrupt Enable 0: Disable 1: Enable When it is enabled, an interrupt will be generated in case that each field finishes.
29	/	/	/
28:25	R/W	0x0	TV_LINE_INT_EN Line Interrupt Enable 0: Disable 1: Enable When it is enabled, an interrupt will be generated in case that the image is output to the trigger line.
24	R/W	0x0	PSR_FORCE_SR_EN 0: Disable 1: Enable The interrupts of forcing the scrambling code to reset are enabled.
23:15	/	/	/
14	R/W0C	0x0	TV_VB_INT_FLAG Field Interrupt Flag It is asserted during vertical no-display period every frame. Write 0 to clear it.
13	/	/	/
12:9	R/W0C	0x0	TV_LINE_INT_FLAG Line Interrupt Flag Trigger when SY1 match the current TV scan line. Write 0 to clear it.
8	R/W0C	0x0	Psr_Force_Sr_Flag Scrambler Forced-reset Flag Write 0 to clear it. Exit or update PSR only after interrupts.
7:0	/	/	/

15.2.10.3 0x0008 TV Global Interrupt1 Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: TV_GINT1_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: TV_GINT1_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	TV_LINE_INT_NUM_1 Scan line for TV trigger line (including inactive lines) Set it for the specified line for trigger 1. Note: SY1 is writable only when LINE_TRG1 is disabled and can be written only before TV_Line_Int_En is disabled.
15:0	R/W	0x0	TV_LINE_INT_NUM_0 Line Triggering line 0 Scan line for TV line trigger (including inactive lines) Setting it for the specified line for trigger 1. Note: SY1 is writable only when LINE_TRG1 disable and can be written only before TV_Line_Int_En is disabled.

15.2.10.4 0x000C TV Global Interrupt2 Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: TV_GINT2_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	TV_LINE_INT_NUM_3 The set triggering line 3 scan line for TV line trigger (including inactive lines) Setting it for the specified line for trigger 1. Note: SY1 is writable only when LINE_TRG1 disable. Write only before TV_Line_Int_En is disabled.
15:0	R/W	0x0	TV_LINE_INT_NUM_2 The set triggering line 2 scan line for TV line trigger (including inactive lines) Setting it for the specified line for trigger 1. Note: SY1 is writable only when LINE_TRG1 disable. Write only before TV_Line_Int_En is disabled.

15.2.10.5 0x0040 TV Source Control Select Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: TV_SRC_CTL_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0040			Register Name: TV_SRC_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:1	R/W	0x0	TV_SRC_SEL It is used for selecting the testing pattern in the vdbist_mode. 00: Color Check 01: Grayscale Check 10: Black by White Check 11: Gridding Check
0	R/W	0x0	VDBIST_MODE 0: Select DE to provide data source 1: Select VDBIST to produce the testing pattern.

15.2.10.6 0x0090 TV Control Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: TV_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TV_EN 0: Disable 1: Enable It is used for enabling the modules in the field of TVCLK.
30:20	/	/	/
19:4	R/W	0x0	START_DELAY It is controlling the time of the SYNC signal release for DE. For example, when it is set to 2, the de_syn signal will be valid until the 2nd line finishes. Then, the control signal will pull down de_sync.
3:0	/	/	/

15.2.10.7 0x0098 TV Basic Timing1 Register (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: TV_BASIC1_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VIC39IND
30:17	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0098			Register Name: TV_BASIC1_REG
Bit	Read/Write	Default/Hex	Description
16:0	R/W	0x0	VT (in HD line) Tvt = VT/2 * Th In the case of 1920x1080i (VIC=20), it is the interlaced scanning. Configure 1125 in the odd-even field. Configure 2250 in the progressive scanning. Calculate the counter s boundary value by dividing by 2.

15.2.10.8 0x009C TV Basic Timing2 Register (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: TV_BASIC2_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:16	R/W	0x0	TV_XO width is TV_XO+1
15	/	/	/
14:0	R/W	0x0	TV_YO height is TV_YO+1

15.2.10.9 0x00A0 TV Basic Timing3 Register (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: TV_BASIC3_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	HT horizontal total time Thcycle = (HT+1) * Thdclk
15	/	/	/
14:0	R/W	0x0	HBP (HSPW+HBP) horizontal back porch Thbp = (HBP +1) * Thdclk The front porch can by calculated in the formula: (tv_ht+1)-(tv_xo+1)-(thbp+1)

15.2.10.10 0x00A4 TV Basic Timing4 Register (Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: TV_BASIC4_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00A4			Register Name: TV_BASIC4_REG
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14:0	R/W	0x0	VBP horizontal back porch (in HD line) Tvbp = (VBP +1) * Th Back porch is VBP-VSPW. Front porch is VT/2-(tv_yo+1)-(VBP+1).

15.2.10.11 0x00A8 TV Basic Timing5 Register (Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: TV_BASIC5_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x0	HSPW horizontal Sync Pulse Width (in dclk) Thspw = (HSPW+1) * Tdclk Note: HT> (HSPW+1)
15:12	/	/	/
11:0	R/W	0x0	VSPW vertical Sync Pulse Width (in lines) Tvspw = (VSPW+1) * Th Note: VT/2 > (VSPW+1)

15.2.10.12 0x0088 TV SYNC Signal Polarity Control Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: TV_IO_POL_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R/W	0x0	IO3_INV (de) 0: Not invert 1: Invert
26	R/W	0x0	IO2_ INV (pixel_clk) 0: Not invert 1: Invert
25	R/W	0x0	IO1_INV (hsync) 0: Not invert 1: Invert

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0088			Register Name: TV_IO_POL_REG
Bit	Read/Write	Default/Hex	Description
24	R/W	0x0	IO0_INV (vsync) 0: Not invert 1: Invert
23:0	/	/	/

15.2.10.13 0x008C TV SYNC Signal IO Enable Control Register (Default Value: 0x0F00_0000)

Offset: 0x008C			Register Name: TV_IO_TRI_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R/W	0x1	IO3_OUTPUT_TRI_EN 1: Disable 0: Enable
26	R/W	0x1	IO2_OUTPUT_TRI_EN 1: Disable 0: Enable
25	R/W	0x1	IO1_OUTPUT_TRI_EN 1: Disable 0: Enable
24	R/W	0x1	IO0_OUTPUT_TRI_EN 1: Disable 0: Enable
23:0	/	/	/

15.2.10.14 0x00FC TV Debug Register (Default Value: 0x0000_0000)

Offset: 0x00FC			Register Name: TV_DEBUG_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R/W0C	0x0	TV_FIFO_UNDER_FLOW If the read operation is perform although TVFIFO is empty, write 0 to clear when data supply problem appears.
29	R/W0C	0x0	LOSTWARN If the tvfifo is not null in the row check, it indicates that the data amount of DE, vdbist and ctril gen are different. Write 0 to clear.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00FC			Register Name: TV_DEBUG_REG
Bit	Read/Write	Default/Hex	Description
28	R	0x0	TV_FIELD_POLARITY Field Indication Signal 0: second field 1: first field After resetting, the status signal of ctrl_gen is 1.
27:16	/	/	/
15:0	R	0x0	TV_CURRENT_LINE The outputting current lines

15.2.10.15 0x01F0 TV Safe Period0 Register (Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: TV_SAFE_PERIOD_REG0
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	SAFE_PERIOD_LINENUMMAX It is used for setting the ending lines of safe period.
15:2	/	/	/
1:0	R/W	0x00	SAFE_PERIOD_MODE 00: Unsafe 01: Safe 10: Safe at sync active(de sync period 11: Safe at line (The lines defined by min and max, during which it is safe.)

15.2.10.16 0x01F4 TV Safe Period1 Register (Default Value: 0x0000_0000)

Offset: 0x01F4			Register Name: TV_SAFE_PERIOD_REG1
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	SAFE_PERIOD_LINENUMMIN It is used for setting the starting lines of safe period.

15.2.10.17 0x0300 TV Fill Data Control Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: TV_FILL_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TV_FILL_EN 0: Bypass 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0300			Register Name: TV_FILL_CTL_REG
Bit	Read/Write	Default/Hex	Description
30:0	/	/	/

15.2.10.18 0x304+N*0x0C (N=0~2) TV Fill Data Begin Register (Default Value: 0x0000_0000)

Offset: 0x304+N*0x0C (N=0~2)			Register Name: TV_FILL_BEGIN_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	FILL_BEGIN

15.2.10.19 0x308+N*0x0C (N=0~2) TV Fill Data End Register (Default Value: 0x0000_0000)

Offset: 0x308+N*0x0C (N=0~2)			Register Name: TV_FILL_END_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	FILL_END

15.2.10.20 0x30C+N*0x0C (N=0~2) TV Fill Data Value Register (Default Value: 0x0000_0000)

Offset: 0x30C+N*0x0C (N=0~2)			Register Name: TV_FILL_DATA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	FILL_VALUE

15.2.10.21 0x0328 TV Fill Data High1 Value Register (Default Value: 0x0000_0000)

Offset: 0x0328			Register Name: TV_FILL_DATA1_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	FILL_VALUE2 The high 16 bits of tv_fill_data2 need to be configured in the color depth 12/16.
15:0	R/W	0x0	FILL_VALUE1 The high 16 bits of tv_fill_data1 need to be configured in the color depth 12/16.

15.2.10.22 0x032C TV Fill Data High2 Value Register (Default Value: 0x0000_0000)

Offset: 0x032C			Register Name: TV_FILL_DATA2_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x032C			Register Name: TV_FILL_DATA2_REG
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x0	FILL_VALUE3 The high 16 bits of tv_fill_data3 need to be configured in the color depth 12/16.

15.2.10.23 0x0330 TV Data IO Polarity Control0 Register (Default Value: 0x0000_0000)

Offset: 0x0330			Register Name: TV_DATA_IO_POL0_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	R_DATA_INV R/Cb Channel Data_Inv 0: Normal polarity 1: Invert the specify output
15:0	R/W	0x0	G_DATA_INV G/Y Channel Data_Inv 0: Normal polarity 1: Invert the specify output

15.2.10.24 0x0334 TV Data IO Polarity Control1 Register (Default Value: 0x0000_0000)

Offset: 0x0334			Register Name: TV_DATA_IO_POL1_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	B_DATA_INV B/Cr Channel Data_Inv 0: Normal polarity 1: Invert the specify output
15:0	/	/	/

15.2.10.25 0x0338 TV Data IO Enable Control0 Register (Default Value: 0xffff_ffff)

Offset: 0x0338			Register Name: TV_DATA_IO_TRI0_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0xffff	R_TRI_EN R/Cb Channel Data_Output_Tri_En 1: Disable 0: Enable
15:0	R/W	0xffff	G_TRI_EN G/Y Channel Data_Output_Tri_En 1: Disable 0: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.2.10.26 0x033C TV Data IO Enable Control1 Register (Default Value: 0xffff_0000)

Offset: 0x033C			Register Name: TV_DATA_IO_TRI1_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0xffff	B_TRI_EN B/Cr Channel Data_Output_Tri_En 1: Disable 0: Enable
15:0	/	/	/

15.2.10.27 0x0340 TV Pixeldepth Mode Control Register (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: TV_PIXELDEPTH_MODE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	FIELD_EN Field Output Enable 1: Enable 0: Disable
30	R/W	0x0	FIELD_POL Field Polarity Reverse 1: Reverse 0: Not reverse
29:24	/	/	/
23:8	R/W	0x0	FIELD_LINE It is used for setting which field line is updated. 0: Update the field_out when the last line of Vactive in each field finishes the interlaced scanning Others: Update the field_out when the n line of Vactive in the last field finishes the interlaced scanning.
7	/	/	/
6:4	R/W	0x0	IPI_FORMAT 000: RGB 001: YCbCr4:2:2 010: YCbCr4:4:4 011: YCbCr4:2:0 100: Compressed Data
3	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0340			Register Name: TV_PIXELDEPTH_MODE_REG
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x0	PIXELDEPTH_MODE 000: 6-bit mode If the data source is the built-in colorbar, the 6-bit colorbar pattern will be transmitted. 001: 8-bit mode If the data source is the built-in colorbar, the 8-bit colorbar pattern will be transmitted. 010: 10-bit mode If the data source is the built-in colorbar, the 10-bit colorbar pattern will be transmitted. 011: 12-bit mode If the data source is the built-in colorbar, the 12-bit colorbar pattern will be transmitted. 100: 16-bit mode If the data source is the built-in colorbar, the 16-bit colorbar pattern will be transmitted. 101: 24-bit mode Only for compressed data, meaningless for colorbar 110: 48-bit mode Only for compressed data, meaningless for colorbar 111: color mode disabled, meaningless for colorbar
0	W/R	0x0	VRR_EN When this register is 1, it indicates that tcon_tv is in the VRR mode. To use VRR, this register needs to be well configured before TV_EN. If the VRR mode is not used, the registers related to VRR needs no configuration.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.3 HDMI

The High Definition Multimedia Interface (HDMI) is a wired digital interconnect that replaces the analog SCART connection. HDMI is capable of transferring uncompressed video, audio, and data using a single cable.

HDMI system architecture consists of sources (transmitter) and sinks (receiver). The HDMI cable and connectors carry four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA Data Display Channel (DDC). The DDC is used for configuration and status exchange between a single source and a single sink. The optional CEC protocol provides high-level control functions between all of the various audiovisual products in a user's environment.

The HDMI includes the follow features:

- Supports HDMI1.4/HDMI2.0
- Supports CEC, DDC, HPD
- Supports HDCP1.4/HDCP2.2
- Supports RGB888/YUV444/YUV422/YUV420 format and 8-/10-bit width
- Supports maximum 4K@60fps, and other typical video format like 4096x2160@60Hz/1920x1080@60Hz/1280x720@60Hz
- Supports 8-channel I2S audio transmission, up to 192 KHz sampling rate
- HDMI PHY on-chip reference clock frequency is 13.5-600M PCLK
- HDMI PHY supports hot plug detection
- HDMI PHY supports SCAN, I/O Continuity, BIST, and other test
- Supports exclusive PAD like CEC and DDC and embedded with reference resistor

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.4 eDP1.4

15.4.1 Overview

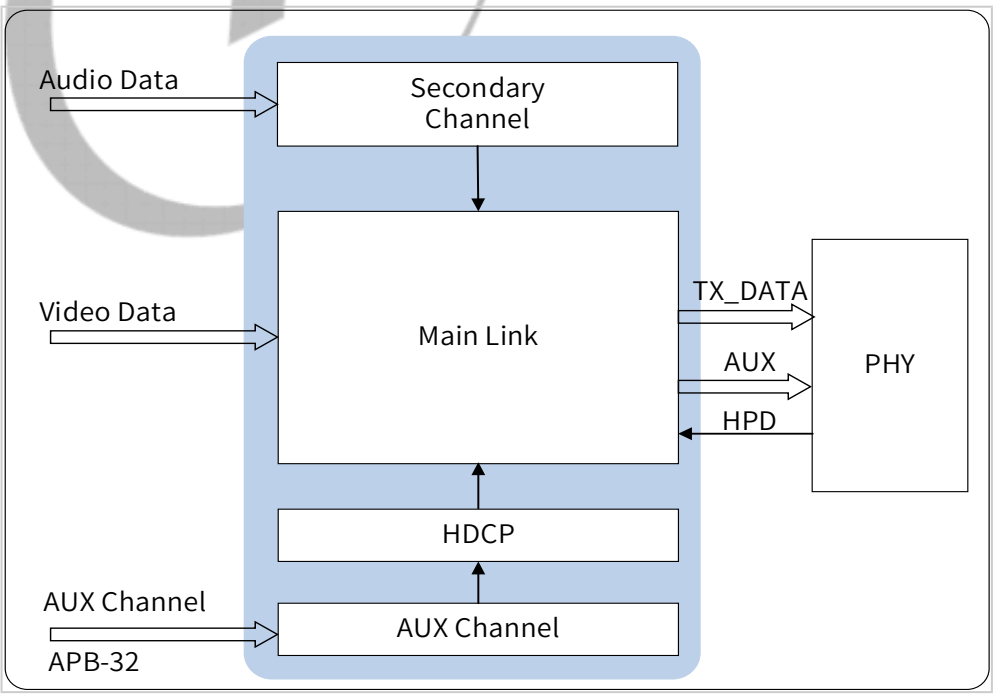
The embedded Display Port (eDP) is a standard protocol in the digital display field. It is completely compatible with DP and consists of main link, auxiliary channel, and hot plugging.

The eDP includes the following features:

- A set of eDP1.4b/DP1.4 TX
- Supports 1-lane, 2-lane, or 4-lane transmission, up to 5.4 Gbps/lane.
- Video formats: RGB, YCbCr4:4:4, YCbCr4:2:2, and YCbCr4:2:0
- Color depth: 6-bit, 8-bit, and 10-bit per channel
- Supports I2S interface
  - Supports 2, 5.1, and 7.1 sound channel.
  - Maximum sampling rate: 192 kHz
- Supports HDCP1.4 and HDCP2.3
- Supports Hot Plug detection
- The working frequency of AUX channel is 1MHz, and Manchester-II coding is used.
- Supports the timing standards of VESA DMT and CVT.

15.4.2 Block Diagram

Figure 15-30 eDP Block Diagram



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.4.3 Clock Sources

The following table describes the clock sources of eDP. For clock setting, configurations, and gating information, refer to the section CCU.

Module	Clock Sources	Description
eDP	VIDEO0PLL4X	Its frequency is 1188 MHz by default.
	VIDEO1PLL4X	Its frequency is 1188 MHz by default.
	VIDEO2PLL4X	Its frequency is 1188 MHz by default.
	PERI0PLL2X	Its frequency is 1.2 GHz by default.

15.4.4 Functional Descriptions

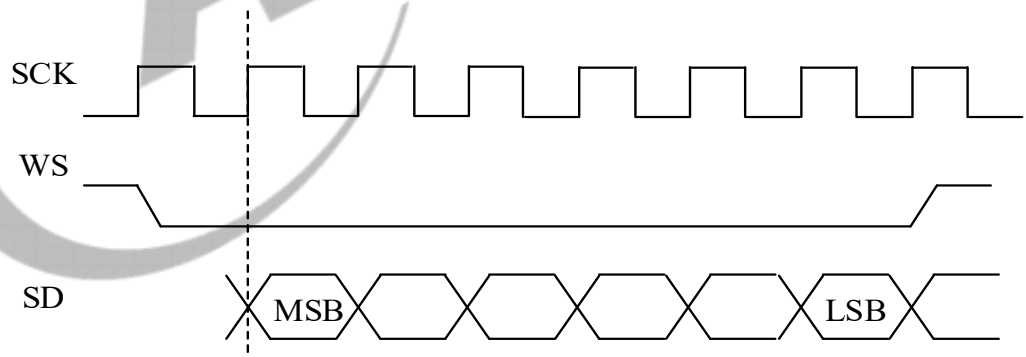
15.4.4.1 Pixel Mode

eDP can be configured as single/dual/quad pixel modes by altering clock parameters. For example, to transmit 1920x1080@60Hz videos, the pixel clock is 148.5 MHz in the single pixel mode, 74.25 MHz in the dual pixel mode, and 37.125 MHz in the quad pixel mode.

15.4.4.2 Audio Interface

For the input and output of audio information for secondary stream support, the DisplayPort Transmitter core supports the I2S interface. The core implements between 1 and 4 instances of the I2S interface. A single lane allows for the support of 2 channel data while 4 lanes are required to support 7.1 channel audio data.

Figure 15-31 I2S Sampling Timing



15.4.5 Programming Guidelines

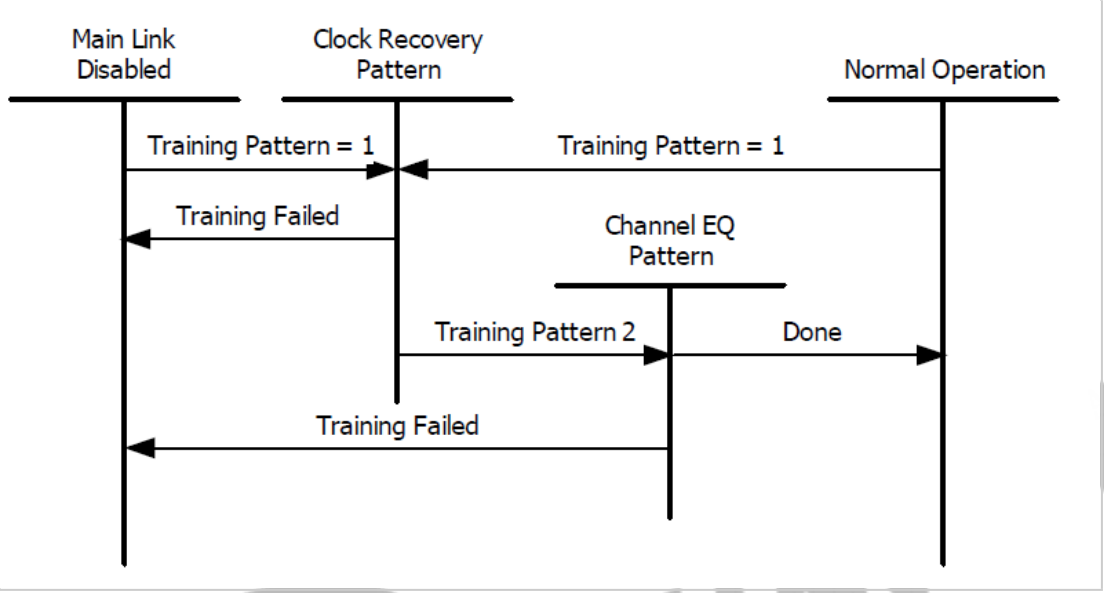
15.4.5.1 Link Training

The host processor initiates link training commands by writing to the internal control register set. When set into the link training mode, the functional data path is blocked and the link training controller issues either training pattern 1 for clock recovery or training pattern 2, 3 or 4 for symbol lock. Care must be taken to place the sink device in the proper link training mode using

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

AUX transactions before the transmitter begins issuing the training pattern. Otherwise, unpredictable results may occur. The link training process is summarized below. The DPTx core ships with a complete link policy make implemented in C that may be used directly or as a starting point for link training.

Figure 15-32 Link Training States



After the successful completion of the clock recovery and channel equalization phases of link training, the transmitter may write one or more of the SOURCE_ENABLE bits to a 1 to begin link symbol transmission. Training must be completed for each lane required to support a specific receiver. For DisplayPort 1.2 and higher, training pattern 3 is available for sink devices that indicate support for the advanced pattern. Similarly, training pattern 4 is available for DisplayPort 1.3 and higher compliant sink devices.

15.4.5.2 Transmitter Clock Generation

The transmitter internal architecture supports the asynchronous and synchronous clocking modes included in the DisplayPort Standard. The clocking mode is selected with bit 0 of the SRCx_MAIN_STREAM_MISC0 register in the Main Stream Attributes block. The SRCx_MAIN_STREAM_MISC0 register should be set to a 0, and the asynchronous clock mode is enabled. In the asynchronous clocking mode, the relationship between MVid and NVid is calculated and not fixed. In this mode, the transmitter core will transmit the required constant value for NVid (0x8000). The value of MVid will be calculated internally by the core using the input video pixel clock and the link symbol clock as a reference. On a read of the MVid host register, programmed value will be ignored and the computed MVid value will be returned.

15.4.5.3 Data Path Configuration

The DisplayPort Transmitter core must be properly configured through the host register set prior to enabling the transmission of any main link video stream.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Name	Description
SRC0_MAIN_STREAM_*	Main stream attributes transmitted in the MSA secondary data packet sent during the vertical blanking interval.
SRC0_TRANSFER_UNIT_CONFIG	Transaction Unit Size and payload configuration
SRC0_USER_DATA_COUNT	Number of active video data symbols per line
SRC0_USER_SYNC_POLARITY	Polarity control for the video input capture port.
SRC0_DATA_CONTROL	FIFO management and packet flow control.

The main stream attribute registers are directly mapped to the equivalent fields of the MSA secondary data packet. The DisplayPort specification contains complete information regarding the proper use of these fields.

The base transaction unit size is contained in the TRANSFER_UNIT_CONFIG_SRC_x register lower two bytes, bits 15:0. This value may be any multiple of two in the range supported by the DisplayPort standard which is 32 and 64. Odd values written to this register field will be rounded down to the next lowest even number.

For the number of valid data symbols carried within each Transaction Unit (TU), the transmitter core supports two modes of operation, automatic and manual. The automatic mode is enabled by setting the SYMBOLS_PER_TU_SRC_x field, bits 22:16, to a value of 0x00. In this mode, the transmitter core will automatically populate the video data symbols of the TU with the available data from the user input port. This mode provides ease of programming for most embedded applications but may not be compatible with all sink devices. For applications requiring box to box connections with a wide range of sink devices, the manual mode is recommended.

In the manual mode of determining the TU size, a calculation is performed using the equations in section 2.2.1.4 of the DisplayPort standard. The calculated value is programmed into the SYMBOLS_PER_TU_SRC_x field and limits the transmitter core to a maximum number of video data symbols per TU less than or equal to this value. The manual mode provides a consistent and predictable number of valid data bytes per transaction unit as required by some sink devices.

LinkBW = LINK_BW_SET * 27 * LANE_COUNT_SET

Data Rate = (Input Clock Rate * bits per pixel) / 8

Data Per TU = Data Rate / LinkBW * TU_SIZE

The core also requires a second calculation that determines the number of video data symbols per line of active video. This value is determined using the following equation and programmed into the USER_DATA_COUNT register.

The core also requires a second calculation that determines the number of video data symbols per line of active video. This value is determined using the following equation and programmed into the

USER_DATA_COUNT register.

SYMBOL_COUNT = ((HRES * bits per pixel) + 7) / 8

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

USER_DATA_COUNT = (SYMBOL_COUNT + lane_count – 1) / lane_count

The bits per pixel are the total number of bits used to represent a single pixel. For example, a 10-bit per color RGB source would require 30 bits to represent a single pixel. The lane_count is the currently configured number of lanes.

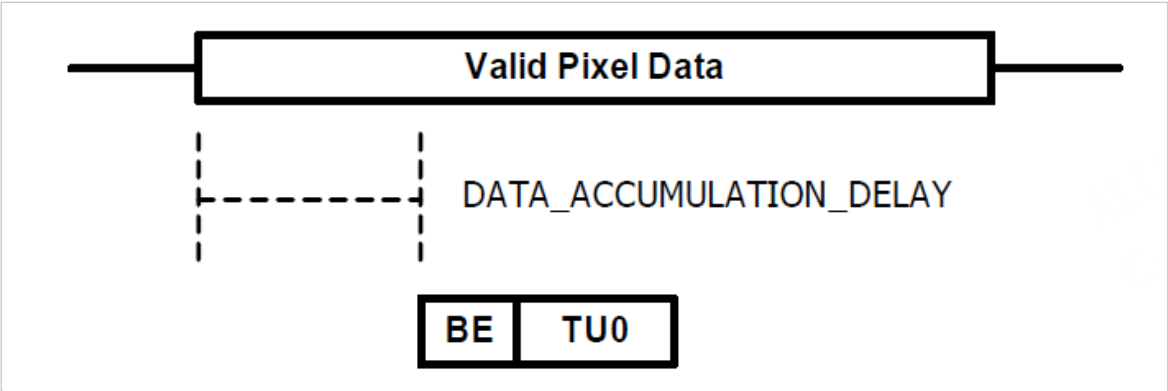
The final register that requires programming is the USER_SYNC_POLARITY. These four, single bit fields determine the polarity of the user data input control signals VSync, HSync, Data Enable and OddEven. A value of 1 for any of these bits indicates that the related input control signal is active high. Please note that this polarity is the opposite of the polarities specified in the DisplayPort Main Stream attribute packet.

Once the above register and register fields have been properly set, the main link may be enabled through the SOURCE_ENABLE and VIDEO_STREAM_ENABLE host registers. Output from the DisplayPort Transmitter link will be enabled at the first user input vertical sync after the host register has been programmed. Partial frames will not be sent over the link when the main link is either enabled or disabled. To ensure full compatibility for box-to-box DisplayPort connections, special attention must be given to the configuration of the SYMBOLS_PER_TU_SRC_X register. Embedded DisplayPort connections may be able to ignore this requirement based on the characteristics of the target panel by enabling the sparse mode described in the Embedded DisplayPort section of this document. The DisplayPort standard requires that the Blanking Start symbol occurs during the same symbol time for each active line and at the same symbol time during vertical blanking.

15.4.5.4 TU Data Accumulation Delay

In addition to the active data per transaction unit, the DATA_ACCUMULATION_DELAY field of the USER_DATA_CONTROL register must be properly set to allow for the internal rate control logic to provide a guaranteed number of active data symbols in each transaction unit. This delay also provides a fixed reference for the internal framing logic to properly place the BE symbol on the link. The value of this register should be set to a depth of at least one half of the TU size. For example, a TU size of 64 would require this field to be set to a minimum value of 32. The DATA_ACCUMULATION_DELAY register controls the number of link clock cycles that the TU packetization logic waits between the first valid pixel data received and the start of the first active packet.

Figure 15-33 Data Accumulation Delay



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

This delay allows for a fixed timing reference from the first active pixel to allow the first Transaction Unit of each line to be placed in the proper position on the link. A failure to set this register properly could result in an inconsistent time interval between Blanking Start symbols. Larger values may be used for this register with a maximum equal to the programmed TU size. Settings that are greater than one half of the TU size will result in an increased latency in the data processing pipeline.

15.4.5.5 TU FIFO Accumulation Delay

The internal data pipeline also provides the ability to allow for an accumulation of data in the internal FIFO to prevent any possible data underrun in the TU data stream. The FIFO_ACCUMULATION_DELAY field of the USER_DATA_CONTROL register allows the host to set the minimum FIFO depth before active data begins being transmitted for a specific line. While a wide range of values are acceptable for this register, there are specific guidelines that have been validated with a wide range of the video modes and color modes.

The transaction unit utilization is based on the percentage of active symbols that are present in each TU.

Figure 15-34 FIFO Accumulation Delay Settings

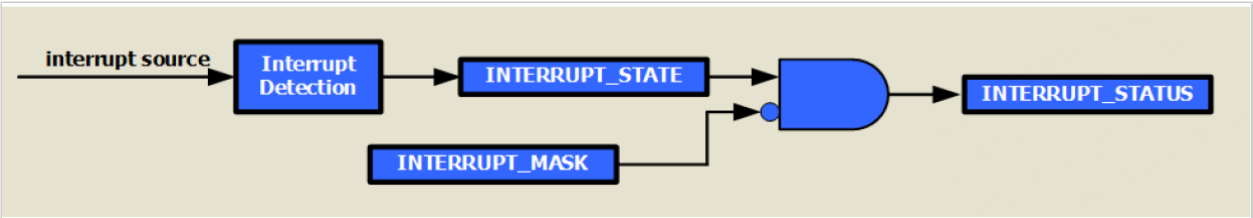
TU Utilization	FIFO_ACCUMULATION_DELAY
< 7%	8
26% - 74%	7
8% - 25%	6
75% - 92%	5
93%-100%	4

The FIFO has a maximum depth of thirty-two (32) entries. These recommendations are based on a classification of the link utilization for active data. If a large value is used for this register, the previous line may not complete transmission before the next active video line begins.

15.4.5.6 Host Interrupts

The DisplayPort Transmitter core generates an interrupt to the host processor under one or more possible conditions. When any one of these conditions is detected, the core will set the apb_int signal high. All interrupts are cleared when a read is performed from the INTERRUPT_STATUS register.

Figure 15-35 Interrupt Detection Logic



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.4.5.7 General-purpose Timer

The DisplayPort Transmitter core design includes a single general purpose 20-bit timer for use by the host processor system. Each timer has a resolution of one microsecond and can provide a timing reference between 1 microsecond and 1 second. The timer may be configured to automatically reload the count value and may also generate an interrupt. The general purpose timer is located in the GP_HOST_TIMER register and contains four fields that are used to control the operation of the timer.

15.4.5.8 Hot Plug Detection

The transmitter core continuously monitors the value of the hot plug detect (HD) input signal for an interrupt event or a disconnect event. For a detected active low pulse width between 500 microseconds and 1 millisecond, the sink device has requested an interrupt. The interrupt is passed to the host processer through the APB interface when the interrupt source is not masked.

When the HPD signal remains low for greater than 2 milliseconds, this indicates that the sink device has been disconnected and the link should be shut down. This condition is also passed through the APB interface as an interrupt when not masked. The host processor must properly determine the cause of the interrupt by reading the appropriate DPCD and/or host registers and take the appropriate action.

15.4.6 Register List

Module Name	Base Address
eDP_CTRL	0x05740000
eDP_REG_PAD	0x05760000

Register Name	Offset	Description
eDP_CTRL		
LINK_BW_SET	0x0000	Link BW Set Register
LANE_COUNT_SET	0x0004	Lane Count Set Register
ENHANCED_FRAME_EN	0x0008	Enhanced Frame Enable Register
TRAINING_PATTERN_SET	0x000C	Training Pattern Set Register
LINK_QUAL_PATTERN_SET	0x0010	Link Quality Pattern Set Register
SCRAMBLING_DISABLE	0x0014	Scrambling Disable Register
EDP_CAPABILITY_CONFIG	0x001C	EDP Capability Config Register
HBR2_COMPLIANCE_SCRAMBLER_RESET	0x0020	HBR2 Compliance Scramble Reset Register
ALPM_POWER_SET	0x0028	ALPM Power Set Register
LANE_REMAP_CONTROL	0x002C	Lane Remap Control Register
CUSTOM_80BIT_PATTERN_31_0	0x0030	Custom 80BIT Pattern 31:0 Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
CUSTOM_80BIT_PATTERN_63_32	0x0034	Custom 80BIT Pattern 63:32 Register
CUSTOM_80BIT_PATTERN_79_64	0x0038	Custom 80BIT Pattern 79:64 Register
TRANSMITTER_OUTPUT_ENABLE	0x0080	Transmitter Output Enable Register
SOFT_RESET	0x0090	Soft Reset Register
INPUT_SOURCE_ENABLE	0x0094	Input Source Enable Register
FEC_ENABLE	0x0098	FEC Enable Register
FORCE_SCRAMBLER_RESET	0x00C0	Force Scrambler Reset Register
CORE_CAPABILITIES	0x00F8	Core Capabilities Register
CORE_ID	0x00FC	Core ID Register
AUX_COMMAND	0x0100	AUX Command Register
AUX_WRITE_FIFO	0x0104	AUX Write FIFO Register
AUX_ADDRESS	0x0108	AUX Address Register
AUX_CLOCK_DIVIDER	0x010C	AUX Clock Divider Register
AUX_REPLY_TIMEOUT_INTERVAL	0x0110	AUX Replay Timeout Interval Register
HPD_INPUT_STATE	0x0128	HPD Input state Register
INTERRUPT_STATE	0x0130	Interrupt State Register
AUX_REPLY_DATA	0x0134	AUX Replay Data Register
AUX_REPLY_CODE	0x0138	AUX Replay Code Register
AUX_REPLY_COUNT	0x013C	AUX Replay Count Register
INTERRUPT_CAUSE	0x0140	Interrupt Cause Register
INTERRUPT_MASK	0x0144	Interrupt Mask Register
REPLY_DATA_COUNT	0x0148	Replay Data Count Register
AUX_STATUS	0x014C	AUX State Register
AUX_REPLY_CLOCK_WIDTH	0x0150	AUX Replay Clock Width Register
AUX_WAKE_ACK_DETECTED	0x0154	AUX Wake ACK Detected Register
GP_HOST_TIMER	0x0158	GP Host Timer Register
PHY_STATUS	0x0280	PHY Status Register
SST_SOURCE_SELECT	0x050C	SST Source Select Register
SRC0_SECONDARY_DATA_WINDOW	0x0808	SRC0 Secondary Data Window Register
SRC0_INPUT_STATUS	0x080C	SRC0 Input Status Register
SRC0_DATA_CONTROL	0x0810	SRC0 Data control Register
SRC0_COLORIMETRY_OVERRIDE	0x0814	SRC0 Colorimetry Override Register
SRC0_MAIN_STREAM_HTOTAL	0x0820	SRC0 Main Stream Htotal Register
SRC0_MAIN_STREAM_VTOTAL	0x0824	SRC0 Main Stream Vtotal Register
SRC0_MAIN_STREAM_POLARITY	0x0828	SRC0 Main Stream Polarity Register
SRC0_MAIN_STREAM_HSWIDTH	0x082C	SRC0 Main Stream HSwidth Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
SRC0_MAIN_STREAM_VSWIDTH	0x0830	SRC0 Main Stream VSwidth Register
SRC0_MAIN_STREAM_HRES	0x0834	SRC0 Main Stream HRES Register
SRC0_MAIN_STREAM_VRES	0x0838	SRC0 Main Stream VRES Register
SRC0_MAIN_STREAM_HSTART	0x083C	SRC0 Main Stream Hstart Register
SRC0_MAIN_STREAM_VSTART	0x0840	SRC0Main Stream Vstart Register
SRC0_MAIN_STREAM_MISC0	0x0844	SRC0 Main Stream MISC0 Register
SRC0_MAIN_STREAM_MISC1	0x0848	SRC0 Main Stream MISC1 Register
SRC0_MVID	0x084C	SRC0 MVID Register
SRC0_TRANSFER_UNIT_CONFIG	0x0850	SRC0 Transfer Unit Config Register
SRC0_NVID	0x0854	SRC0 NVID Register
SRC0_USER_PIXEL_COUNT	0x0858	SRC0 User Pixel Count Register
SRC0_USER_DATA_COUNT	0x085C	SRC0 User Data Count Register
SRC0_MAIN_STREAM_INTERLACED	0x0860	SRC0 Main Stream Interlaced Register
SRC0_USER_SYNC_POLARITY	0x0864	SRC0 User Sync Polarity Register
SRC0_USER _CONTROL	0x0868	SRC0 User Control Register
SRC0_USER_FIFO_STATUS	0x086C	SRC0 User FIFO Status Register
SRC0_USER_FRAMING_STATUS	0x0870	SRC0 User Framing Status Register
SEC0_AUDIO_ENABLE	0x0900	SEC0 Audio Enable Register
SEC0_AUDIO_INPUT_SELECT	0x0904	SEC0 Audio Input Select Register
SEC0_CHANNEL_COUNT	0x0908	SEC0 Channel Count Register
SEC0_OWA_CLOCK_COUNT	0x090C	SEC0 Clock Count Register
SEC0_INFOFRAME_ENABLE	0x0910	SEC0 Infoframe Enable Register
SEC0_INFOFRAME_RATE	0x0914	SEC0 Infoframe Rate Register
SEC0_MAUD	0x0918	SEC0 Maud Register
SEC_NAUD	0x091C	SEC Naud Register
SEC0_AUDIO_CLOCK_MODE	0x0920	SEC0 Audio Clock Mode
SEC0_3D_VSC_DATA	0x0924	SEC0 3D VSC Data Register
SEC0_AUDIO_FIFO	0x0928	SEC0 Audio FIFO Register
SEC0_AUDIO_FIFO_LAST	0x092C	SEC0 Audio FIFO Last Register
SEC0_AUDIO_FIFO_READY	0x0930	SEC0 Audio FIFO Ready
SEC0_INFOFRAME_SELECT	0x0934	SEC0 Infoframe Select Register
SEC0_SDP_BUFFER_DATA	0x0938	SEC0 SDP Buffer Data Register
SEC0_TIMESTAMP_INTERVAL	0x093C	SEC0 Time Stamp Interval Register
SEC0_CS_SOURCE_FORMAT	0x0940	SEC0 CS Source Format Register
SEC0_CS_CATEGORY_CODE	0x0944	SEC0 CS Category Code Register
SEC0_CS_LENGTH_ORIG_FREQ	0x0948	SEC0 CS Length ORIG FREQ Register
SEC0_CS_FREQ_CLOCK_ACCURACY	0x094C	SEC0 CS FREQ Clock Accuracy
SEC0_CS_COPYRIGHT	0x0950	SEC0 CS Copyright Register
SEC0_AUDIO_CHANNEL_MAP	0x0954	SEC0 Audio Channel Map Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
SEC0_AUDIO_FIFO_OVERFLOW	0x0958	SEC0 Audio FIFO Overflow Register
SEC0_PACKET_COUNT	0x095C	SEC0 Packet Count Register
SEC0_CS_USER_DATA	0x0960	SEC0 CS User Data Register
SEC0_ADAPTIVE_SYNC_ENABLE	0x0968	SEC0 Adaptive Sync Enable
SEC0_OWA_STATUS_READBACK	0x096C	SEC0 Status Readback Register
SEC0_GTC_COUNT_CONFIG	0x0980	SEC0 GTC Count Config Register
SEC_GTC_COMMAND_EDGE	0x0984	SEC GTC Command Edge Register
SEC_GTC_AUX_FRAME_SYNC	0x0988	SEC GTC AUX Frame SYNC Register
SRC0_EDP_CRC_ENABLE	0x0990	SRC0 EDP CRC Enable Register
SRC0_EDP_CRC_RED	0x0994	SRC0 EDP CRC Red Register
SRC0_EDP_CRC_GREEN	0x0998	SRC0 EDP CRC Green Register
SRC0_EDP_CRC_BLUE	0x099C	SRC0 EDP CRC Blue Register
eDP_REG_PAD		
DP_LNK_CLK_CFG	0x0000	DP LNK CLK CFG Register
DP_VID_CLK_CFG	0x0004	DP VID CLK CFG Register

15.4.7 eDP_CTRL Register description

15.4.7.1 0x0000 Link BW Set Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: LINK_BW_SET
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: LINK_BW_SET
Bit	Read/Write	Default/Hex	Description
7:0	RW	0x0	LINK_BW_SET Holds the value of the main link bandwidth setting. The register uses the same values as those supported by the DPCD register of the same name in the sink device. This value is not passed to the PHY layer which may require separate configuration of the link bandwidth.7:0 – LINK_BW_SET: Sets the value of the main link bandwidth for the sink device. The value of this register after a reset is indeterminate. The value of this register should be set to the desired link rate divided by 27. Some example link rates are: 0x06: 1.62 Gbps 0x08: 2.16 Gbps 0x09: 2.43 Gbps 0x0A: 2.7 Gbps 0x0C: 3.24 Gbps 0x10: 4.32 Gbps 0x14: 5.4 Gbps 0x1E: 8.1 Gbps

15.4.7.2 0x0004 Lane Count Set Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: LANE_COUNT_SET
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4:0	RW	0x0	LANE_COUNT_SET The transmitter uses this register to set the number of lanes that will be used to configure and operate the link. Unused lanes will not be active during training or video transmission.4:0 – This field is equivalent to the DPCD register of the same name. Supported values are 1, 2, or 4 lanes.

15.4.7.3 0x0008 Enhanced Frame Enable Register (Default Value: 0x0000_0001)

Offset: 0x0008			Register Name: ENHANCED_FRAME_EN
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: ENHANCED_FRAME_EN
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x1	ENHANCED_FRAME_EN Enables the enhanced framing mode as supported by the DisplayPort specification. Enhanced framing mode is required for all DisplayPort 1.2a and greater implementations. This mode must be used when supporting HDCP functions.0 – This register is fixed at 1 and cannot be changed. For DisplayPort 1.1a applications using standard framing mode only, please contact Technologies Technical Support.

15.4.7.4 0x000C Training Pattern Set Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: TRAINING_PATTERN_SET
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	RW	0x0	TRAINING_PATTERN_SET Settings this register to a non-zero value sets the output of the transmitter core to the specified training pattern. When set, all other main link information such as video and audio data are blocked in favor of the training pattern.2:0 – Set the link training pattern according to the two-bit code 000 = Training off001 = Training pattern 1, clock recovery010 = Training pattern 2, inter-lane alignment and symbol recovery 011 = Training pattern 3, inter-lane alignment and symbol recovery 100 = Training pattern 4, inter-lane alignment and symbol recovery

15.4.7.5 0x0010 Link Quality Pattern Set Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: LINK_QUAL_PATTERN_SET
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0010			Register Name: LINK_QUAL_PATTERN_SET
Bit	Read/Write	Default/Hex	Description
31:27	/	/	LINK_QUAL_PATTERN_SET This configuration register is used to instruct the transmitter core to enable one of the following test patterns for link quality measurements on the selected lane. These measurements are not required for the establishment and maintenance of the link and are supported for test purposes. 26:24 – LANE_3_PATTERN_SET 18:16 – LANE_2_PATTERN_SET 10:8 – LANE_1_PATTERN_SET 2:0 – LANE_0_PATTERN_SET Pattern Encoding 2:0 – Enable transmission of the link quality test patterns 000: Link quality test pattern not transmitted 001: D10.2 test pattern (unscrambled) transmitted 010: Symbol Error Rate measurement pattern 011: PRBS7 transmitted 100: 80-bit custom pattern 101: HBR2 eye pattern (CP2520, pattern 1) 110: CP2520, pattern 2 111: CP2520, pattern 3 Note: The PRBS7 test pattern is specific to the technology dependent PHY implementation and may not be supported on all platforms.
26:24	RW	0x0	LANE_3_PATTERN_SET
23:19	/	/	/
18:16	RW	0x0	LANE_2_PATTERN_SET
15:11	/	/	/
10:8	RW	0x0	LANE_1_PATTERN_SET
7:3	/	/	/
2:0	RW	0x0	LANE_0_PATTERN_SET

15.4.7.6 0x0014 Scrambling Disable Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: SCRAMBLING_DISABLE
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: SCRAMBLING_DISABLE
Bit	Read/Write	Default/Hex	Description
0	RW	0x0	SCRAMBLING_DISABLE This control register is used to disable the internal scrambling function of the DisplayPort transmitter. This bit must be set during the link training process when transmitting unscrambled patterns (TP1, TP2, TP3). 0 – Set to a 1 to disable the hardware scrambling function. Set to a 0 for normal operation.

15.4.7.7 0x001C EDP Capability Config Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: EDP_CAPABILITY_CONFIG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	
1:0	RW	0x0	EDP_CAPABILITY_CONFIG For embedded DisplayPort implementations, the core supports the use of the alternate scrambler reset pattern. This bit should only be enabled for embedded applications. Setting this bit in box-to-box DisplayPort applications will result in link failure. 1 – ENABLE_REDUCED_AUX_SYNC: For eDP applications only, enabling this control bit reduces the number of sync pulses sent during AUX channel transactions from 16 to 8. 0 – ALTERNATE_SCRAMBLER_RESET: Set this bit to a 1 to force the transmitter core to use the alternate scrambler reset value.

15.4.7.8 0x0020 HBR2 Compliance Scramble Reset Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: HBR2_COMPLIANCE_SCRAMBLER_RESET
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	RW	0x0	HBR2_COMPLIANCE_SCRAMBLER_RESET Defines the interval for the transmission of the scrambler reset pattern during the transmission of the HBR2 compliance link quality pattern. 15:0 – The value of this register should be set to the same value as reported by the DisplayPort sink device through the DPCD register address 0x0024A-0x0024B.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.4.7.9 0x0028 ALPM Power Set Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: ALPM_POWER_SET
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	RW	0x0	ALPM_POWER_SET Controls the transmission of the ML_PHY_SLEEP and ML_PHY_STANDBY data patterns on the link. Writing to this register will trigger a single transmission of the pattern. For multiple patterns, repeated writes to this register may be initiated with a minimum spacing of 100 nanoseconds between each write. 1:0 – Power state sequence request. Writing to this register will trigger a single transmission of the power state sequence.

15.4.7.10 0x002C Lane Remap Control Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: LANE_REMAP_CONTROL
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x002C			Register Name: LANE_REMAP_CONTROL
Bit	Read/Write	Default/Hex	Description
19:16	RW	0x0	LANE_REMAP_CONTROL Used to map the physical lanes of the DisplayPort link to the internal symbol lanes of the controller. Using these register bits, any of the four physical lanes may be mapped to any other internal lane for processing. 10-bit data transmitted on each lane may also be inverted. This operation occurs prior to sending the lane symbol data to the PHY layer. 19 – INVERT_LANE_3: Inverts the state of all bits transmitted to the PHY layer on lane 3. 18 – INVERT_LANE_2: Inverts the state of all bits transmitted to the PHY layer on lane 2. 17 – INVERT_LANE_1: Inverts the state of all bits transmitted to the PHY layer on lane 1. 16 – INVERT_LANE_0: Inverts the state of all bits transmitted to the PHY layer on lane 0. 8 – REMAP_ENABLE: Set to a 1 to enable the remapping function. When set to a 0, bits 7:0 of the LANE_REMAP control register will be ignored. 7:6 – REMAP_LANE_3: Specifies which internal lane number (0-3) will be mapped to the PHY lane 3. 5:4 – REMAP_LANE_2: Specifies which internal lane number (0-3) will be mapped to the PHY lane 2. 3:2 – REMAP_LANE_1: Specifies which internal lane number (0-3) will be mapped to the PHY lane 1. 1:0 – REMAP_LANE_0: Specifies which internal lane number (0-3) will be mapped to the PHY lane 0.
15:9	/	/	/
8:0	RW	0x0	/

15.4.7.11 0x0030 Custom 80BIT Pattern 31:0 Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: CUSTOM_80BIT_PATTERN_31_0
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	CUSTOM_80BIT_PATTERN_31_0 Contains the least significant thirty-two bits of the 80-bit custom pattern used in link quality testing. These bits should not be modified while the link quality pattern is active.31:0 – Bits 31:0 of the 80-bit custom pattern.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.4.7.12 0x0034 Custom 80BIT Pattern 63:32 Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: CUSTOM_80BIT_PATTERN_63_32
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	Contains the middle thirty-two bits of the 80-bit custom pattern used in link quality testing. These bits should not be modified while the link quality pattern is active.31:0 – Bits 63:32 of the 80-bit custom pattern.

15.4.7.13 0x0038 Custom 80BIT Pattern 79:64 Register ((Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: CUSTOM_80BIT_PATTERN_79_64
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	RW	0x0	CUSTOM_80BIT_PATTERN_79_64 Contains the most significant sixteen bits of the 80-bit custom pattern used in link quality testing. These bits should not be modified while the link quality pattern is active.15:0 – Bits 79:64 of the 80-bit custom pattern.

15.4.7.14 0x0080 Transmitter Output Enable Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: TRANSMITTER_OUTPUT_ENABLE
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	RW	0x0	TRANSMITTER_OUTPUT_ENABLE This bit is used to disable all output of the main link framing logic. When set to 0, the transmitter core will output only stuffing symbols onto the link. No control symbols or valid link data are transmitted when disabled. This bit prevents the link controller core from interfering with the PHY power up sequence.0 – Set to a 1 after the link output has been configured and the external PHY is ready to begin operations.

15.4.7.15 0x0090 Soft Reset Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: SOFT_RESET
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0090			Register Name: SOFT_RESET
Bit	Read/Write	Default/Hex	Description
31:0	WO	0x0	SOFT_RESET Performs a soft reset of specific core management functions. This reset only applies to the control portions of the core. The state of the programmable register set is not affected by the soft reset. 0 – VIDEO_SOFT_RESET: Writing a 1 performs a soft reset of the video capture section. 4 – LINK_SOFT_RESET: Writing a 1 performs a soft reset of the link management section.

15.4.7.16 0x0094 Input Source Enable Register (Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: INPUT_SOURCE_ENABLE
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4:0	RW	0x0	INPUT_SOURCE_ENABLE Enables the transmission of video and secondary channel audio data from one or more SST virtual sources. In SST mode, only bit 0 of this register is valid. Enabling the virtual source input will begin the transmission of the NO_VIDEO pattern if the video stream is not enabled.

15.4.7.17 0x0098 FEC Enable Register (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: FEC_ENABLE
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	RW	0x0	FEC_ENABLE Setting this bit to a 1 enables the internal forward error correction (FEC) logic if included in the core implementation. Transmission of the FEC protected data will start within 32 link clock cycles of this register being set. When cleared to a 0, the FEC logic will wait until the end of the next FEC frame to send the disable pattern on the link.0 – Write to a 1 to enable the FEC logic. This bit is 0 at reset.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.4.7.18 0x00C0 Force Scrambler Reset Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: FORCE_SCRAMBLER_RESET
Bit	Read/Write	Default/Hex	Description
31:0	WO	0x0	FORCE_SCRAMBLER_RESET Typically used for debug purposes, this register allows the host processor to force the link controller to insert a scrambler reset symbol into the stream. In normal operation, the scrambler reset replaces the blanking start symbol. When set to a 1, the link controller will replace the next scheduled blanking start symbol with a scrambler reset symbol. 0 – Write to a 1 to force a scrambler reset for debug purposes. This bit is write only and will always read back as a 0.

15.4.7.19 0x00F8 Core Capabilities Register (Default Value: 0x0144_1f04)

Offset: 0x00F8			Register Name: CORE_CAPABILITIES
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0144_1f04	CORE_CAPABILITIES Determines what functionality is available in a specific implementation of the core. Software may use this register to determine the configuration of the core. 22:20 – SECONDARY_SOURCE_COUNT: Reports the number of secondary channels supported. Valid values are 1 (SST). 12 – QUAD_INPUT_SUPPORT_PRESENT: Returns a 1 when support for 4 pixels per cycle is supported at the video input port. Returns 0 otherwise. 11 – FEC_PRESENT: Returns a 1 when support for Forward Error Correction is included in the core.10 – EMBEDDED_PRESENT: Returns 1 when support for embedded DisplayPort is present. Embedded DisplayPort 1.4b is always supported.9 – AUDIO_PRESENT: Returns 1 when audio functionality is included in the secondary channel implementation.8 – HDCP_PRESENT: Returns 1 when the HDCP cipher logic is present. 2:0 – LANE_COUNT: Indicates the number of lanes implemented in the current configuration of the core.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.4.7.20 0x00FC Core ID Register (Default Value: 0x000a_0509)

Offset: 0x00FC			Register Name: CORE_ID
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	CORE_ID Returns the unique identification code of the core and the current revision level. These values may be used by the software to determine the revision level of the core. 31:16 – Core ID is fixed at 0x000A15:0 – Core revision level in the form Major [15:8], Minor [7:0].

15.4.7.21 0x0100 AUX Command Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: AUX_COMMAND
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	AUX_COMMAND Initiates an AUX channel command of the specified length when written. This register is written last as part of the AUX channel request set up process. When written, the internal state machines will begin transmitting the request to the sink device. The AUX_ADDRESS and, when applicable, the AUX_WRITE_FIFO must be set up before writing this register.13 – AUX_PHY_WAKE: Set to a 1 to send the AUX_PHY_WAKE signal for embedded DisplayPort operations. This signal is sent as a standalone operation and is not sent as a part of a larger AUX transaction.12 – ADDRESS_ONLY: Set to a 1 to initiate an address only request.11:8 – COMMAND: AUX Channel Command. The field is equivalent to the commands defined in section 2.4.1 of the DisplayPort specification. 0x8 = AUX Write 0x9 = AUX Read 0x0 = twi over AUX Write 0x4 = twi over AUX Write, Middle of Transaction bit set 0x1 = twi over AUX Read 0x5 = twi over AUX Read, Middle of Transaction bit set 0x2 = twi over AUX Write Status3:0 – BYTE_COUNT: Specifies the number of bytes to transfer with the current command. The range of the register is 0 to 15 indicating between 1 and 16 bytes of data.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.4.7.22 0x0104 AUX Write FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: AUX_WRITE_FIFO
Bit	Read/Write	Default/Hex	Description
31:0	WO	0x0	AUX_WRITE_FIFO Before initiating a native or twi write request on the AUX channel, the host system must provide the write data to the FIFO mapped to this address. Only the number of bytes required to support the current transaction must be written to the FIFO. Subsequent writes to the FIFO must not be performed until the REQUEST_IN_PROGRESS bit is clear.7:0 – Write only AUX Channel byte data. A read from this register is not supported but will return the last data byte written.

15.4.7.23 0x0108 AUX Address Register (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: AUX_ADDRESS
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	AUX_ADDRESS Each AUX request requires a 20-bit address for native AUX requests or an 8-bit address for twi over AUX requests. This register specifies the address for the current AUX channel command. These bits are used without modification for the address field of the request.19:0 – Twenty-bit address for the start of the AUX Channel burst.

15.4.7.24 0x010C AUX Clock Divider Register (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: AUX_CLOCK_DIVIDER
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	AUX_CLOCK_DIVIDER Contains the clock divider value for generating the internal 1MHz clock from the APB host interface clock. The clock divider register provides integer division only and does not support fractional APB clock rates. (e.g. set to 75 for a 75MHz APB clock)8:0 – APB clock divider value. The valid range is 10 to 400.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.4.7.25 0x0110 AUX Replay Timeout Interval Register (Default Value: 0x0000_00190)

Offset: 0x0110			Register Name: AUX_REPLY_TIMEOUT_INTERVAL
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x190	AUX_REPLY_TIMEOUT_INTERVAL Specifies the number of microseconds that the Transmitter core AUX controller waits for a reply from the downstream sink device before signaling a timeout to the host. This register should only be modified at the direction of Technologies.8:0 – Wait time in microseconds. This register is initialized to a value of 400 upon reset.

15.4.7.26 0x0128 HPD Input State Register (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: HPD_INPUT_STATE
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	HPD_INPUT_STATE Provides the current state of the hot plug detect (HPD) input to the core. The external port is synchronized to the host clock domain and provided as status. Writes to this register are ignored.0 – Current state of the external HPD port.

15.4.7.27 0x0130 Interrupt State Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: INTERRUPT_STATE
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0130			Register Name: INTERRUPT_STATE
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	INTERRUPT_STATE Holds status bits which report the internal state of the interrupt management logic. These signals are used to generate interrupts and can be used as polled status for systems that do not implement interrupts. Interrupts will clear on a read of the INTERRUPT_CAUSE register. Reads from this register will not change the state of the interrupt. 5 – HDCP_TIMER_EVENT: A 1 indicates that an event has been generated by the HDCP timer block. 4 – GP_TIMER_EVENT: A 1 indicates that an event has been generated by the general purpose timer block. 3 – REPLY_TIMEOUT: A 1 indicates that a reply timeout has occurred. 2 – REPLY_RECEIVED: A 1 indicates that a reply has been received. 1 – HPD_IRQ: A 1 indicates that an IRQ interrupt has been received. 0 – HPD_EVENT: A 1 indicates that an HPD connect or disconnect event has been detected.

15.4.7.28 0x0134 AUX Replay Data Register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: AUX_REPLY_DATA
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	AUX_REPLY_DATA This read only address maps to the internal FIFO which contains up to 16 bytes of information received during the AUX channel reply. Reply data is read from the FIFO starting with byte 0. The number of valid bytes in the FIFO corresponds to the number of bytes received as indicated by the REPLY_DATA_COUNT register.7:0 – AUX reply data from the sink device. Each read advances the internal read pointer.

15.4.7.29 0x0138 AUX Replay Code Register (Default Value: 0x0000_0000)

Offset: 0x0138			Register Name: AUX_REPLY_CODE
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0138			Register Name: AUX_REPLY_CODE
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	AUX_REPLY_CODE Contains the reply code received from the most recent AUX Channel request. This code is the four-bit field received by the reply controller from the sink device. The value of the code maps to the DisplayPort specification section 2.4.1.2 which is repeated below for clarity.3:0 – AUX channel reply code received from the sink device. 0x0: Native AUX ACK 0x1: Native AUX NACK 0x2: Native AUX DEFER 0x0 = twi over AUX ACK 0x4: twi over AUX NACK 0x8: twi over AUX DEFER

15.4.7.30 0x013C AUX Replay Count Register (Default Value: 0x0000_0000)

Offset: 0x013C			Register Name: AUX_REPLY_COUNT
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	AUX_REPLY_COUNT Provides an internal count of the number of reply transactions received on the AUX Channel. Each reply received from the sink device increments the count by 1. The reply code is not considered when incrementing this counter. Writing a 1 to this register clears the count. 7:0 – Current reply count. The value of this register will automatically roll over after reaching 255 replies received. 0 – write a 1 to this bit to clear the value

15.4.7.31 0x0140 Interrupt Cause Register (Default Value: 0x0000_0000)

Offset: 0x0140			Register Name: INTERRUPT_CAUSE
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0140			Register Name: INTERRUPT_CAUSE
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	INTERRUPT_CAUSE The transmitter core interrupt status register contains the cause of an interrupt asserted by the core. The specific events that can cause an interrupt and the associated status bits are shown below. A read from this register clears all values. 14:7 – SOURCE_ERROR_IRQ: Reserved debug interrupt sources. 5 – HDCP_TIMER_IRQ: The HDCP internal timer has generated an interrupt. 4 – GP_TIMER_IRQ: The internal general-purpose timer has generated an interrupt. 3–REPLY_TIMEOUT: A reply timeout has occurred when the sink has not sent a response 400us after the transmitter has sent a request. 2–REPLY_RECIEVED: An AUX reply transaction has been detected. This value may be used to allow a system to process other events while waiting for a response from the sink device. 1–HPD_IRQ: An IRQ framed with the proper timing on the HPD signal has been detected. 0 – HPD_EVENT: The core has detected the presence of the HPD signal. This interrupt asserts immediately after the detection of HPD and after the loss of HPD for 2 msec.

15.4.7.32 0x0144 Interrupt Mask Register (Default Value: 0x0000_7FFF)

Offset: 0x0144			Register Name: INTERRUPT_MASK
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0144			Register Name: INTERRUPT_MASK
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x7FFF	INTERRUPT_MASK Each interrupt source for the transmitter core may be individually masked. When the corresponding bit in this register is set to a 1, an interrupt will not be generated for the event. At power up, all interrupt sources are masked, and this register will have a value of 0x3F. 14:7 – SOURCE_ERROR_MASK: Reserved debug interrupt masks. Should always be written to a 1 during normal operation. 5 – HDCP_TIMER_IRQ_MASK: A 0 in this control bit allows the internal HDCP timer to cause an interrupt to be asserted. 4 – GP_TIMER_IRQ_MASK: A 0 in this control bit allows the internal general purpose timer to cause an interrupt to be asserted. 3 – REPLY_TIMEOUT_MASK: Write a 0 to this bit to allow reply timeout events to cause an interrupt to be asserted. 2 – REPLY_RECEIVED_MASK: Write a 0 to this bit to allow reply received events to cause an interrupt. 1 – HPD_IRQ_MASK: Write a 0 to this bit to allow HPD_IRQ events to cause an interrupt 0 – HPD_EVENT_MASK: Write a 0 to this bit to allow HPD present events to cause an interrupt.

15.4.7.33 0x0148 Replay Data Count Register (Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: REPLY_DATA_COUNT
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	REPLY_DATA_COUNT Returns the total number of data bytes received during a reply transaction from the sink device. This register does not use the length byte of the transaction header. The reply controller independently counts the number of bytes. The value of this register is cleared when the transmitter initiates a request transaction. 4:0 – Total number of data bytes received during the reply phase of the AUX transaction.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.4.7.34 0x014C AUX State Register (Default Value: 0x0000_0000)

Offset: 0x014C			Register Name: AUX_STATUS
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	AUX_STATUS This register contains the status of the internal AUX channel controllers. The progress of request and reply transactions are monitored a reply transactions are checked for errors. These bits are always valid. 4 –EXPECT_REPLY: After sending an AUX request, the internal logic sets this flag to indicate that a reply is expected. This bit is cleared only after a complete reply is received. 3 – REPLY_ERROR: When set to a 1, the AUX reply logic has detected an error in the reply to the most recent AUX transaction. Errors are detected when the precharge and sync phases of the reply last more than 38 cycles instead of the maximum 32. This condition typically indicates noise on the AUX channel data signals. 2 – REQUEST_IN_PROGRESS: The AUX transaction request controller sets this bit to a 1 while actively transmitting a request on the AUX channel. The bit is set to 0 when the AUX transaction request controller is idle. 1 – REPLY_IN_PROGRESS: The AUX reply detection logic sets this bit to a 1 while receiving a reply on the AUX channel. The bit is 0 otherwise. 0 – REPLY_RECEIVED: This bit is set to 0 when the AUX request controller begins sending bits on the AUX serial bus. The AUX reply controller sets this bit to 1 when a complete and valid reply transaction has been received. This bit is cleared when a request transaction has been initiated by the request controller.

15.4.7.35 0x0150 AUX Replay Clock Width Register (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: AUX_REPLY_CLOCK_WIDTH
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0150			Register Name: AUX_REPLY_CLOCK_WIDTH
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	AUX_REPLY_CLOCK_WIDTH Reports the width of the AUX channel reply clock in APB_CLK cycles. This register is only valid after a properly formatted reply transaction has been received. The clock width is measured during the sync stage of the AUX channel transaction. 9:0 – Width of the AUX channel receive clock in APB_CLK cycles.

15.4.7.36 0x0154 AUX Wake ACK Detected Register (Default Value: 0x0000_0000)

Offset: 0x0154			Register Name: AUX_WAKE_ACK_DETECTED
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	AUX_WAKE_ACK_DETECTED Indicates that the AUX_PHY_WAKE signal from the connected sink device has been detected on the AUX channel. The bit is cleared at the start of any transmitter AUX transaction and is set when the AUX_PHY_WAKE signal is detected.0 – Set to a 1 when the AUX_PHY_WAKE signal has been detected. Clears upon starting the next AUX transaction.

15.4.7.37 0x0158 GP Host Timer Register (Default Value: 0x0000_0000)

Offset: 0x0158			Register Name: GP_HOST_TIMER
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	GP_HOST_TIMER General purpose 20-bit timer for use by the host processor. The DisplayPort Transmitter core does not use this timer for any internal function. The resolution of the timer is 1 microsecond.31 – ENABLE: set to a 1 to enable the timer 30 – RELOAD: set to a 1 to automatically reload when the timer reaches zero. When set to 0, the timer will only run once. 29 – INTERRUPT: set to a 1 to generate an interrupt when the timer reaches zero. 19:0 – TIMER_VALUE: a write will set the reload value for the timer. A read will return the current value of the timer.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.4.7.38 0x0280 PHY Status Register (Default Value: 0x0000_0000)

Offset: 0x0280			Register Name: PHY_STATUS
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	PHY_STATUS The transmitter PHY uses this register address to report the current status of the functional elements of the implementation. This register reports the real time value of these status signals. Reading from this register does not affect the value of any reported bits. Not all PHY implementations will support all of these status bits.31:0 – Please refer to the application note for the specific PHY implementation used with the core.

15.4.7.39 0x050C SST Source Select Register (Default Value: 0x0000_0000)

Offset: 0x050C			Register Name: SST_SOURCE_SELECT
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SST_SOURCE_SELECT When the transmitter software driver selects SST transmission mode, this register determines the video input to use as the main link video source. The software driver may select any one of the possible four video sources. 1:0 – Selects one of the four possible inputs for transmitting video data in SST mode.

15.4.7.40 0x0808 SRC0 Secondary Data Window Register (Default Value: 0x0000_0080)

Offset: 0x0808			Register Name: SRC0_SECONDARY_DATA_WINDOW
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x80	SRC0_SECONDARY_DATA_WINDOW Specifies the width in link symbol clocks of the horizontal blanking window during which secondary channel data packets are allowed to be transmitted. This valid data window should be programmed a value less than the horizontal blanking period between main link symbols.11:0 – Width of the data valid window. This value should be set using the following equation. Reg = HBLANK_PERIOD / LINK_SYMBOL_CLOCK_PERIOD * 0.9

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.4.7.41 0x080C SRC0 Input Status Register (Default Value: 0x0000_0000)

Offset: 0x080C			Register Name: SRC0_INPUT_STATUS
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	SRC0_INPUT_STATUS Provides a direct copy of the polarity corrected control signals from the user data interface. This register may be used to trigger specific events in the host system.3 – USER_CONTROL_ODDEVEN: State of the polarity corrected vid_oddeven control input. 2 – USER_CONTROL_DEN: Indicates that an active line of video is being received at the control input. This flag is set when the first pixel of data is received and clears at the leading edge of the horizontal sync pulse. 1 – USER_CONTROL_HSYNC: State of the polarity corrected vid_hsync control input. 0 – USER_CONTROL_VSYNC: State of the polarity corrected vid_vsync control input.

15.4.7.42 0x0810 SRC0 Data Control Register (Default Value: 0x0000_2004)

Offset: 0x0810			Register Name: SRC0_DATA_CONTROL
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0000_2004	SRC0_DATA_CONTROL Controls the internal user data path by allowing pixels to accumulate inside the core before transmitting. This register defaults to 0x00002004 and should not be modified unless directed by Technologies support engineering team.14:8 – DATA_ACCUMULATION_DELAY: Specifies the number of link clock cycles for the internal data path controller to wait before sending the first TU of an active line after detecting that valid data is ready to be transmitted. All seven bits are read-write, however, the internal logic will only recognize even multiples of 4 for this register. Bits 9 and 8 will be ignored by the internal framing logic.5:0 – FIFO_ACCUMULATION_DEPTH: Specifies the number of words that must accumulate inside the data path FIFO before attempting to send a valid data packet on the link. This value is only valid once per line during the first active data packet.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.4.7.43 0x0814 SRC0 Colorimetry Override Register (Default Value: 0x0000_0000)

Offset: 0x0814			Register Name: SRC0_COLORIMETRY_OVERRIDE
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SRC0_COLORIMETRY_OVERRIDE Provides a mechanism for overriding the colorimetry information provided in the MISC0 and MISC1 fields of the Main Stream Attributes packet. When bit 6 is set to a 1, the remainder of the bits in the register will replace the values from the MSA packet. This register should be used when the VSC method is used for colorimetry data. Refer to Table 2-96 in the DisplayPort 1.4a specification for the coding of these bit fields.6 –OVERRIDE_ENABLE: Set to a 1 to use the values in this register rather than the values in the MSA packet. When set to 0, all colorimetry information is determined by the MISC0/MISC1 fields of the MSA packet.5:3 – COLOR_SPACE_OVERRIDE: Determines the color space to be used when decoding pixel information from the link. Set to 100 for 4:2:0. Set to 101 for DSC byte mode.2:0 – BITS_PER_COMPONENT_OVERRIDE: Sets the number of bits per component for the selected color space. Encodings are determined by the selected color space. These bits are equivalent to bit 7-5 in the MISC0 field.

15.4.7.44 0x0820 SRC0 Main Stream Htotal Register (Default Value: 0x0000_0000)

Offset: 0x0820			Register Name: SRC0_MAIN_STREAM_HTOTAL
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SRC0_MAIN_STREAM_HTOTAL Specifies the total number of clocks in the horizontal framing period for the main stream video signal. This value is sent as the Main Stream Attribute Htotal.15:0 – Horizontal line length total in clocks

15.4.7.45 0x0824 SRC0 Main Stream Vtotal Register (Default Value: 0x0000_0000)

Offset: 0x0824			Register Name: SRC0_MAIN_STREAM_VTOTAL
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0824			Register Name: SRC0_MAIN_STREAM_VTOTAL
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SRC0_MAIN_STREAM_VTOTAL Provides the total number of lines between vertical sync pulses in the main stream video frame. This value is provided as the Main Stream Attribute Vtotal.15:0 – Total number of lines per video frame.

15.4.7.46 0x0828 SRC0 Main Stream Polarity Register (Default Value: 0x0000_0000)

Offset: 0x0828			Register Name: SRC0_MAIN_STREAM_POLARITY
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	:SRC0_MAIN_STREAM_POLARITY Provides the polarity values for the video horizontal and vertical sync signals. These bits are sent as a part of the Main Stream Attributes as VSP and HSP. Please note that this polarity is the opposite of the polarities specified for the user input port.1 – VSYNC_POLARITY: polarity of the vertical sync pulse. 0 = active high, 1 = active low 0 – HSYNC_POLARITY: polarity of the horizontal sync pulse. 0 = active high, 1 = active low

15.4.7.47 0x082C SRC0 Main Stream HSwidth Register (Default Value: 0x0000_0000)

Offset: 0x082C			Register Name: SRC0_MAIN_STREAM_HSWIDTH
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SRC0_MAIN_STREAM_HSWIDTH Sets the width of the horizontal sync pulse measured in pixel clock periods. This value is provided on the link as the Main Stream Attribute field HSW.14:0 – Horizontal sync width in clock cycles.

15.4.7.48 0x0830 SRC0 Main Stream VSwidth Register (Default Value: 0x0000_0000)

Offset: 0x0830			Register Name: SRC0_MAIN_STREAM_VSWIDTH
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0830			Register Name: SRC0_MAIN_STREAM_VSWIDTH
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SRC0_MAIN_STREAM_VSWIDTH Sets the width of the vertical sync pulse in lines. The Main Stream Attribute VSW is used to carry this information on the link.14:0 – Width of the vertical sync in lines.

15.4.7.49 0x0834 SRC0 Main Stream HRES Register (Default Value: 0x0000_0000)

Offset: 0x0834			Register Name: SRC0_MAIN_STREAM_HRES
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SRC0_MAIN_STREAM_HRES Horizontal resolution of the main stream video source. This value is the number of active pixels per line and is represented in the Main Stream Attributes as the Hwidth field.15:0 – Number of active pixels per line of the main stream video.

15.4.7.50 0x0838 SRC0 Main Stream VRES Register (Default Value: 0x0000_0000)

Offset: 0x0838			Register Name: SRC0_MAIN_STREAM_VRES
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SRC0_MAIN_STREAM_VRES Vertical resolution of the main stream video source. The resolution is the number of active lines per frame. The Main Stream Attribute field Vheight carries this information to the sink.15:0 – Number of active lines of video in the main stream video source.

15.4.7.51 0x083C SRC0 Main Stream Hstart Register (Default Value: 0x0000_0000)

Offset: 0x083C			Register Name: SRC0_MAIN_STREAM_HSTART
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SRC0_MAIN_STREAM_HSTART Specifies the number of clocks between the leading edge of the horizontal sync and the start of active data. This value is used for the Main Stream Attribute Hstart and is measured in pixel clocks.15:0 – Horizontal start clock count

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.4.7.52 0x0840 SRC0Main Stream Vstart Register (Default Value: 0x0000_0000)

Offset: 0x0840			Register Name: SRC0_MAIN_STREAM_VSTART
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SRC0_MAIN_STREAM_VSTART Number of lines between the leading edge of the vertical sync and the first line of active data. This value is carried in the Main Stream Attributes as the Vstart field.15:0 – Vertical start line count.

15.4.7.53 0x0844 SRC0 Main Stream MISC0 Register (Default Value: 0x0000_0000)

Offset: 0x0844			Register Name: SRC0_MAIN_STREAM_MISC0
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SRC0_MAIN_STREAM_MISC0 This 8-bit value contains information about the main link video stream clocking and color representation. These bits are mapped from the DisplayPort specification MISC0 register definitions.7:5 – BIT_DEPTH: number of bits per color 000 = 6 bits 001 = 8 bits 010 = 10 bits 011 = 12 bits 100 = 16 bits 101, 110, 111 = Reserved4 – YCBCR_COLORIMETRY: colorimetry of the main link video 0 = ITU-R BT601-5 1 = ITU-R BT709-53 – DYNAMIC_RANGE: color range for each plane 0 = VESA range 1 = CEA range2:1 – COMPONENT_FORMAT: color representation format 00 = RGB 01 = YCbCr 4:2:210 = YCbCr 4:4:4 11 = Reserved0 – SYNCHRONOUS_CLOCK: clocking mode for the user data 0 = asynchronous clock 1 = synchronous clock

15.4.7.54 0x0848 SRC0 Main Stream MISC1 Register (Default Value: 0x0000_0000)

Offset: 0x0848			Register Name: SRC0_MAIN_STREAM_MISC1
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0848			Register Name: SRC0_MAIN_STREAM_MISC1
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SRC0_MAIN_STREAM_MISC1 These bits represent the Main Stream Attribute field MISC1 as defined in the DisplayPort specification. These bits provide interlaced and stereo video information.7 – ONE_COMPONENT_COLOR_FORMAT: Set to a 1 to indicate a color format with a single component including the Y-only and RAW modes.6 – VSC_COLORIMETRY: When set to a 1, this bit indicates that the DP sink device should use the contents of the VSC packet to determine the Pixel Encoding/Colorimetry information. The bit encodings of the MISC0/MISC1 fields should be ignored when this bit is set.5:3 – ZERO This field must be set to a 0 for proper operation. Any other value in this field may cause unpredictable operation.2:1 – STEREO_VIDEO_ATTRIBUTE: 00 = No stereo video transported 01 = Top field or frame is for the RIGHT eye 10 = Reserved 11 = Top field or frame is for the LEFT eye0 – INTERLACED_TOTAL_EVEN: 0 = number of lines per interlaced frame is odd 1 = number of lines per interlaced frame is even

15.4.7.55 0x084C SRC0 MVID Register (Default Value: 0x0000_0000)

Offset: 0x084C			Register Name: SRC0_MVID
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x084C			Register Name: SRC0_MVID
Bit	Read/Write	Default/Hex	Description
31:0	RW/R O	0x0	SRC0_MVID Contains the MVid clocking value for the main stream video. In the synchronous clocking mode, this register is read/write. In the asynchronous clocking mode, this register is read-only. In synchronous mode, this value must be calculated by the host processor and provided in this register for transmission to the sink device. For most applications, this value can be set to the user data pixel clock value in KHz.23:0 – unsigned value for MVid. In asynchronous mode, this register is read-only and will return the value computed by the internal logic based on the input video clock. In synchronous mode, this register is read-write and should be set to the pixel clock rate multiplied by 100000. For example, this register should be set to 65000 for a 65MHz pixel clock or 148500 for a 148.5MHz pixel clock.

15.4.7.56 0x0850 SRC0 Transfer Unit Config Register (Default Value: 0x0000_0040)

Offset: 0x0850			Register Name: SRC0_TRANSFER_UNIT_CONFIG
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x40	SRC0_TRANSFER_UNIT_CONFIG A transfer unit is a DisplayPort packet and represents both valid data symbols and stuffing symbols. This register value sets the size of a transfer unit in the transmitter framing logic. Due to the design of the core, only values that are a multiple of 4 are supported by this register. When configured for the Sparse TU mode, only the TRANSFER_UNIT_SIZE field of this register is valid. All other fields are ignored.27:24 – FRAC_SYMBOLS_PER_TU: sets the fractional number of valid symbols per TU in units of 1/16th. An accumulator is used to increase the number of data per transaction unit by 1 every 1/N TUs.23:16 – SYMBOLS_PER_TU: configures the number of valid symbols to transmit with each transaction unit. For most applications, this register can be set to a value of 64 (0x40) which allows the core to automatically manage the TU rate control. For bandwidth limited applications, this value can be set to any number less than or equal to 64.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.4.7.57 0x0854 SRC0 NVID Register (Default Value: 0x0000_0000)

Offset: 0x0854			Register Name: SRC0_NVID
Bit	Read/Write	Default/Hex	Description
31:0	RW/R O	0x0	SRC0_NVID Holds the NVid clocking value for the Main Stream Attributes and is set based upon the link rate and clocking mode. This value, when used in conjunction with the M-VID value allows the sink device to recover the frequency of the user data pixel clock.23:0 – unsigned value for NVid. In asynchronous mode, this register is read-only and will return 0x8000. In synchronous mode, this register is read-write and should be set to the link rate multiplied by 100000. For example, this register should be set to 162000 when operating the link in 1.62Gbps mode, 270000 when operating the link in 2.7Gbps mode, or 540000 when operating the link is 5.4Gbps mode.

15.4.7.58 0x0858 SRC0 User Pixel Count Register (Default Value: 0x0000_0001)

Offset: 0x0858			Register Name: SRC0_USER_PIXEL_COUNT
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0000_0001	SRC0_USER_PIXEL_COUNT The user data interface to the transmitter core accepts one, two or four pixels per clock cycle. This register selects the width of the user data input port and should be set before main link video is enabled. At reset, this register defaults to 1.2:0 – Set to a value of 1 for a single pixel wide interface, 2 for a dual pixel wide interface or 4 for a quad pixel wide interface.

15.4.7.59 0x085C SRC0 User Data Count Register (Default Value: 0x0000_0000)

Offset: 0x085C			Register Name: SRC0_USER_DATA_COUNT
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x085C			Register Name: SRC0_USER_DATA_COUNT
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SRC0_USER_DATA_COUNT Determines the total data count for the transmitter framing logic to read from the user FIFO before sending a blanking start symbol. This value is the total number of symbols in a line of active data for each active link lane. The calculated value should be rounded up.17:0 – The equation for setting the value of this register is shown below. SYMBOL_COUNT = ((HRES * bits per pixel) + 7) / 8 UDC = (SYMBOL_COUNT + lane_count – 1) / lane_count

15.4.7.60 0x0860 SRC0 Main Stream Interlaced Register (Default Value: 0x0000_0000)

Offset: 0x0860			Register Name: SRC0_MAIN_STREAM_INTERLACED
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SRC0_MAIN_STREAM_INTERLACED Informs the DisplayPort transmitter main link that the source video is interlaced. By setting this bit to a 1, the transmitter will set the appropriate fields in the VBID value and Main Stream Attributes. This bit must be set to a 1 for the proper transmission of interlaced sources.0 – Set to a 1 when transmitting interlaced images or 0 for progressive sources.

15.4.7.61 0x0864 SRC0 User Sync Polarity Register (Default Value: 0x0000_000f)

Offset: 0x0864			Register Name: SRC0_USER_SYNC_POLARITY
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0864			Register Name: SRC0_USER_SYNC_POLARITY
Bit	Read/Write	Default/Hex	Description
31:0	RW	0xf	SRC0_USER_SYNC_POLARITY Indicates the polarity of the video source sync signals. Set each bit to a 1 for active high or a 0 for active low. Note that these polarities are configured in an opposite state to those carried by the DisplayPort Main Stream Attributes packet.3 – USER_ODDEVEN_POLARITY: polarity of the input odd/even field flag.2 – USER_DATA_ENABLE_POLARITY: polarity of the input user data enable signal. 1 – USER_VSYNC_POLARITY: polarity of the input user vertical sync pulse. 0 – USER_HSYNC_POLARITY: polarity of the input user horizontal sync

15.4.7.62 0x0868 SRC0 User Control Register (Default Value: 0x0000_0000)

Offset: 0x0868			Register Name: SRC0_USER _CONTROL
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SRC0_USER _CONTROL Controls the behavior of the user data FIFO in each active lane of the transmitter core. 2 – BYPASS_NO_VIDEO_DELAY: By default, the transmitter SST framing logic waits for the transmission of 5 NO_VIDEO symbol patterns as required by the DisplayPort specification. This control bit is intended for debug purposes only and disables that delay. 1 – USER_STREAM_ENABLE_NO_VSYNC: When set to a 1, the main and secondary streams become active immediately rather than waiting for the next input vertical sync pulse. 0 – USER_SPARSE_MODE_ENABLE: A variable number of valid data symbols per transaction unit are supported when this bit is set to a 1. The value of the SYMBOLS_PER_TU and FRAC_SYMBOLS_PER_TU fields of the TRANSFER_UNIT_CONFIG register will be ignored when the sparse mode is enabled.

15.4.7.63 0x086C SRC0 User FIFO Status Register (Default Value: 0x0000_0000)

Offset: 0x086C	Register Name: SRC0_USER_FIFO_STATUS

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	SRC0_USER_FIFO_STATUS These read-only bits report the internal status of the video data FIFO buffers. A one in either of these bits indicates a programming error for the current video mode. These bits are cleared at the input vsync of every frame. bit1 – UNDERFLOW: A 1 indicates that the internal user FIFO has detected a video data underflow condition. This can occur if the TU transmit data rate is greater than the input data rate. bit0 – OVERFLOW: A 1 indicates that the internal user FIFO has detected an overflow condition. This can occur if the TU transmit data rate is less than the input data rate.

15.4.7.64 0x0870 SRC0 User Framing Status Register (Default Value: 0x0000_0000)

Offset: 0x0870			Register Name: SRC0_USER_FRAMING_STATUS
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	SRC0_USER_FRAMING_STATUS Reports the internal status of the link packet framing logic. When the internal packet generation logic detects either of these conditions, the appropriate control bit will be set. These bits will clear on read. bit1 – VBI_TIMING_ERROR: This bit will be set when the trailing edge of the input vertical sync is detected and the internal control logic has not finished transmitting all of the pixel data from the previous frame. bit0–DATA_UNDERFLOW: The framing state machine will set this bit to a 1 when a TU packet is being sent and the internal FIFO reports that it is empty.

15.4.7.65 0x0900 SEC0 Audio Enable Register (Default Value: 0x0000_0002)

Offset: 0x0900			Register Name: SEC0_AUDIO_ENABLE
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0900			Register Name: SEC0_AUDIO_ENABLE
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x2	SEC0_AUDIO_ENABLE This control register determines if audio packets are enabled and the transmitted state of the audio mute bit in the VBID packet.1 – AUDIO_MUTE: Determines the state of the audio mute bit in the VBID packet.0 – AUDIO_PACKET_ENABLE: Writing a 1 to this bit will globally enable the secondary channel audio functions. The control registers should be properly set before enabling the secondary channel audio. Writing a 0 will disable all secondary channel audio packets.

15.4.7.66 0x0904 SEC0 Audio Input Select Register (Default Value: 0x0000_0000)

Offset: 0x0904			Register Name: SEC0_AUDIO_INPUT_SELECT
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SEC0_AUDIO_INPUT_SELECT Selects the source for the secondary audio channel data. When set to OWA, only non- compressed, two channel audio is supported.1:0 – Audio source select.00 = I2S 01 = DMA mode 10 = APB host writes 11 = OWA interface (future enhancement)

15.4.7.67 0x0908 SEC0 Channel Count Register (Default Value: 0x0000_0000)

Offset: 0x0908			Register Name: SEC0_CHANNEL_COUNT
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SEC0_CHANNEL_COUNT Used to select the number of audio channels included in the secondary audio stream. Up to eight (8) channels can be supported over I2S while only 2 channels are supported in the OWA format.3:0 – Number of audio channels.0000 = Audio mute set in the VBID field. 0010 = Two channel audio0011 = Two channel audio with LFE 0110 = 5.1 channel surround sound 1000 = 7.1 channel surround sound

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.4.7.68 0x090C SEC0 OWA Clock Count Register (Default Value: 0x0000_0000)

Offset: 0x090C			Register Name: SEC0_OWA_CLOCK_COUNT
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SEC0_OWA_CLOCK_COUNT This register must be programmed prior to enabling the OWA input mode. This register determines the closest integer value representing the number of APB clock cycles per OWA bi- phase encoding clock period. The following equation should be used to determine the value of this register. The result of the calculation should be rounded to the nearest integer.count = (1000.0 * apb_clock_freq_in_mhz) / (audio_sample_rate_in_khz * 128.0) 7:0 – Calculated number of APB clock cycles.

15.4.7.69 0x0910 SEC0 Infoframe Enable Register (Default Value: 0x0000_0000)

Offset: 0x0910			Register Name: SEC0_INFOFRAME_ENABLE
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SEC0_INFOFRAME_ENABLE Each bit in this register will enable the transmission of one of the seven supported generic secondary data packets. 6:0 - Set the corresponding bit to a 0 to disable the transmission of the InfoFrame. When the bit is set to a 1, the transmitter core will send each enabled packet with the frequency determined by the SEC_SDP_PACKET_RATE register.

15.4.7.70 0x0914 SEC0 Infoframe Rate Register (Default Value: 0x0000_0000)

Offset: 0x0914			Register Name: SEC0_INFOFRAME_RATE
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0914			Register Name: SEC0_INFOFRAME_RATE
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SEC0_INFOFRAME_RATE Selects the frequency at which each generic secondary data packet is transmitted to the Sink device. Packets may be sent once, immediate mode, or once per frame, frame mode.6:0 – Set the bit corresponding to the generic SDP to a 1 to enable continuous transmission every frame. Set to a 0 to transmit the generic SDP once when the enable bit transitions from a 0 to a 1. Continuous transmission is defined as one packet sent once per frame during the vertical blanking interval.

15.4.7.71 0x0918 SEC0 Maud Register (Default Value: 0x0000_0000)

Offset: 0x0918			Register Name: SEC0_MAUD
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SEC0_MAUD This register is used when the audio clock generation has been set to the synchronous mode. The clocking values for the secondary channel audio must be calculated by the host system and provided in this register for transmission to the sink device. Example Maud and Naud values may be found in section 2.2.5.2.2 of the DisplayPort specification.23:0 – Unsigned value computed in the asynchronous clock mode

15.4.7.72 0x091C SEC Naud Register (Default Value: 0x0000_0000)

Offset: 0x091C			Register Name: SEC_NAUD
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SEC_NAUD This register is used when the audio clock generation has been set to the synchronous mode. The clocking values for the secondary channel audio must be calculated by the host system and provided in this register for transmission to the sink device. Example Maud and Naud values may be found in section 2.2.5.2.2 of the DisplayPort specification.23:0 – Unsigned value computed in the asynchronous clock mode

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.4.7.73 0x0920 SEC0 Audio Clock Mode (Default Value: 0x0000_0000)

Offset: 0x0920			Register Name: SEC0_AUDIO_CLOCK_MODE
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SEC0_AUDIO_CLOCK_MODE Sets the clock mode for the generation of the Maud and Naud values. The M and N values for audio are transmitted in the audio time stamp packet as well as the LSBs in the Main Link.0 – Set this value to a 1 for synchronous clock mode. Set this value to a 0 for asynchronous clock mode.

15.4.7.74 0x0924 SEC0 3D VSC Data Register (Default Value: 0x0000_0000)

Offset: 0x0924			Register Name: SEC0_3D_VSC_DATA
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SEC0_3D_VSC_DATA Data byte for carrying additional video stream configuration information in 3D stereo applications. The contents of this byte are specified in section 2.2.5.6.2 of the DisplayPort specification.3:0 – Stereo Interface Method Code 7:4 - Stereo Interface Method-Specific Parameter

15.4.7.75 0x0928 SEC0 Audio FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0928			Register Name: SEC0_AUDIO_FIFO
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SEC0_AUDIO_FIFO Sample FIFO for direct writes of audio data to the secondary channel. Samples must be written to the FIFO in reverse channel order with Channel 1, Sample 0 being written first. The data order increments by channel number first followed by sample number. Once eight samples have been written, a secondary audio channel packet will be automatically generated.31:0 – Sample FIFO entry. The internal sample FIFO pointers will automatically increment after writing. Reading from this register will return the last data written.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.4.7.76 0x092C SEC0 Audio FIFO Last Register (Default Value: 0x0000_0000)

Offset: 0x092C			Register Name: SEC0_AUDIO_FIFO_LAST
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SEC0_AUDIO_FIFO_LAST Contains the number of maximum number of samples to be stored in the audio sample FIFO. When a number of samples equal to this value are written to the FIFO, the FIFO ready flag will de-assert. This value is used primarily in DMA applications.9:0 – Number of audio samples that may be stored in the direct audio sample FIFO before the ready flag de-asserts.

15.4.7.77 0x0930 SEC0 Audio FIFO Ready (Default Value: 0x0000_0001)

Offset: 0x0930			Register Name: SEC0_AUDIO_FIFO_READY
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x1	SEC0_AUDIO_FIFO_READY Single bit flag indicating that the depth of the direct audio sample FIFO is less than the depth specified by the SEC_AUDIO_FIFO_DEPTH register.0 – The direct audio sample FIFO is ready to accept additional samples.

15.4.7.78 0x0934 SEC0 Infoframe Select Register (Default Value: 0x0000_0000)

Offset: 0x0934			Register Name: SEC0_INFOFRAME_SELECT
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SEC0_INFOFRAME_SELECT Selects the Infoframe packet buffer to be written to the internal storage SRAM. After a write to this register, the address offset into the SRAM is set to the start of the selected packet.2:0 – Index of the Infoframe SDP. Valid values are 0 through 6.

15.4.7.79 0x0938 SEC0 SDP Buffer Data Register (Default Value: 0x0000_0000)

Offset: 0x0938			Register Name: SEC0_SDP_BUFFER_DATA
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0938			Register Name: SEC0_SDP_BUFFER_DATA
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SEC0_SDP_BUFFER_DATA Writes to this register will store the contents of the byte to the generic SDP SRAM as determined by the SEC_SDP_BUFFER_SELECT register. The internal address will be automatically incremented after each write.7:0 – Byte value to write to the SDP SRAM. Reading from this register will return the last value written.

15.4.7.80 0x093C SEC0 Time Stamp Interval Register (Default Value: 0x0000_0000)

Offset: 0x093C			Register Name: SEC0_TIMESTAMP_INTERVAL
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SEC0_TIMESTAMP_INTERVAL Specifies the number of microseconds to wait between transmissions of each audio timestamp packet. An audio timestamp packet will be sent during the vertical blanking interval shortly after the vertical sync pulse. Subsequent packets will be generated every N microseconds during the video frame as specified by this register.14:0 – Number of microseconds to wait after the initial audio timestamp packet to send a subsequent audio timestamp packet. Timestamp packets will continue to be generated during the video frame. A value of 0 in this register will cause the transmitter to send only a single audio timestamp packet during the vertical blanking interval.

15.4.7.81 0x0940 SEC0 CS Source Format Register (Default Value: 0x0000_0000)

Offset: 0x0940			Register Name: SEC0_CS_SOURCE_FORMAT
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0940			Register Name: SEC0_CS_SOURCE_FORMAT
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SEC0_CS_SOURCE_FORMAT This packed register is used to define the fields in the channel status information sent with each audio frame. The appropriate bits are automatically inserted in to the channel status field of the audio frame. 7:4 – SOURCE_NUMBER: Four bit code with a unique source number identifier. 3 – LINEAR_PCM: 0 for linear PCM samples, 1 for encoded samples 2:0 – PCM_AUDIO_FORMAT: Three bit code corresponding to bits 5-3 of the channel status.

15.4.7.82 0x0944 SEC0 CS Category Code Register (Default Value: 0x0000_0000)

Offset: 0x0944			Register Name: SEC0_CS_CATEGORY_CODE
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SEC0_CS_CATEGORY_CODE Channel status category code for the audio stream channel status bits.7:0 – CATEGORY_CODE: 8-bit category code indicating the type of equipment that generates the digital audio signal as defined in the relevant annex of IEC60958-3.

15.4.7.83 0x0948 SEC0 CS Length ORIG FREQ Register (Default Value: 0x0000_0000)

Offset: 0x0948			Register Name: SEC0_CS_LENGTH_ORIG_FREQ
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SEC0_CS_LENGTH_ORIG_FREQ Channel status word length and original sampling frequency. These values are inserted into the appropriate fields within the Channel Status bits of the audio stream secondary data packets. 7:4 – SAMPLE_WORD_LENGTH: Reflects the length of each sample word as specified in bits 32- 35 of the channel status field in the IEC 60958-3 specification. 3:0 – ORIG_SAMPLING_FREQ: Original sampling frequency of the carried audio signal. These bits reflect the value of bits 39-36 in the IEC60958-3 channel status field.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.4.7.84 0x094C SEC0 CS FREQ Clock Accuracy (Default Value: 0x0000_0000)

Offset: 0x094C			Register Name: SEC0_CS_FREQ_CLOCK_ACCURACY
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SEC0_CS_FREQ_CLOCK_ACCURACY Channel status category code.7:4 – SAMPLING_FREQ: Sampling frequency of the current audio signal with the value reflecting bits 24-27. 3:0 – CLOCK_ACCURACY: Clock accuracy code for the current sampling frequency. This code is equivalent to bits 28-29 of the channel status field.

15.4.7.85 0x0950 SEC0 CS Copyright Register (Default Value: 0x0000_0000)

Offset: 0x0950			Register Name: SEC0_CS_COPYRIGHT
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SEC0_CS_COPYRIGHT Channel status copyright codes for the audio stream channel status bits.2:1 – CGMS-A: Copy Generation Management System information for the current audio stream. 0 – COPYRIGHT: CP-bit for copyright assertion. The mode of alternating the value of this bit to indicate an unknown state is not supported.

15.4.7.86 0x0954 SEC0 Audio Channel Map Register (Default Value: 0x0000_0000)

Offset: 0x0954			Register Name: SEC0_AUDIO_CHANNEL_MAP
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0954			Register Name: SEC0_AUDIO_CHANNEL_MAP
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SEC0_AUDIO_CHANNEL_MAP Allows for any of the eight input audio channels from the audio stream secondary data packet to be mapped to any of the eight output audio channels.31:28 – CHANNEL_7_MAP: remaps the input audio channel 7 to the selected output audio channel. Values from 0 to 7 are valid for this register. 27:24 – CHANNEL_6_MAP 23:20 – CHANNEL_5_MAP 19:16 – CHANNEL_4_MAP 15:12 – CHANNEL_3_MAP 11:8 – CHANNEL_2_MAP 7:4 – CHANNEL_1_MAP 3:0 – CHANNEL_0_MAP

15.4.7.87 0x0958 SEC0 Audio FIFO Overflow Register (Default Value: 0x0000_0000)

Offset: 0x0958			Register Name: SEC0_AUDIO_FIFO_OVERFLOW
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	SEC0_AUDIO_FIFO_OVERFLOW Status bit from the internal secondary data audio packet FIFO. This bit is set when the number of sample packets in the audio packet FIFO exceeds the depth of the buffer. When an overflow occurs, previous sample packets in the audio FIFO will be overwritten.0 – A value of 1 in this status register indicates that an overflow has occurred. The status bit is only cleared by setting the SEC_AUDIO_ENABLE bit to a 0.

15.4.7.88 0x095C SEC0 Packet Count Register (Default Value: 0x0000_0000)

Offset: 0x095C			Register Name: SEC0_PACKET_COUNT
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x095C			Register Name: SEC0_PACKET_COUNT
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	SEC0_PACKET_COUNT Internal debug register containing a running count of the number of secondary data packets that have been transmitted since the secondary channel was enabled. This register clears to zero when the secondary channel is disabled.11:0 – Running count of the number of secondary packets transmitted.

15.4.7.89 0x0960 SEC0 CS User Data Register (Default Value: 0x0000_0000)

Offset: 0x0960			Register Name: SEC0_CS_USER_DATA
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SEC0_CS_USER_DATA This field allows for the Source transmitter to send user defined data with the channel status information. The format of the channel status user data is defined in IEC60958-3.7:0 – Eight-bit field of user data to be transmitted with the channel status.

15.4.7.90 0x0968 SEC0 Adaptive Sync Enable (Default Value: 0x0000_0000)

Offset: 0x0968			Register Name: SEC0_ADAPTIVE_SYNC_ENABLE
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SEC0_ADAPTIVE_SYNC_ENABLE This register controls the transmission of the Adaptive Sync secondary data packet. This bit may be written at any time to enable the transmission of the packet.0 – Set this bit to a 1 to enable transmission of the adaptive sync SDP. Setting this bit to a 0 will disable transmission of the packet.

15.4.7.91 0x096C SEC0 OWA Status Readback Register (Default Value: 0x0000_0000)

Offset: 0x096C			Register Name: SEC0_OWA_STATUS_READBACK
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x096C			Register Name: SEC0_OWA_STATUS_READBACK
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	SEC0_OWA_STATUS_READBACK Valid clock recovery flag for each OWA input lane. When set to a 1, the status bit indicates that the clock/data recovery block has detected OWA compatible signal transitions. If no signal is detected or an incompatible signal is detected, then this status bit will read as a 0.3 – OWA input lane 3 status. 2 – OWA input lane 2 status. 1 – OWA input lane 1 status. 0 – OWA input lane 0 status.

15.4.7.92 0x0980 SEC0 GTC Count Config Register (Default Value: 0x0000_0000)

Offset: 0x0980			Register Name: SEC0_GTC_COUNT_CONFIG
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SEC0_GTC_COUNT_CONFIG Configures the internal accumulator for the management of the global time code function. The accumulator consists of an 8-bit integer part and a 16 bit fractional part. At each host clock cycle, the fractional and integer portions are added to their respective counters. When the fractional counter exceeds the 16-bit range, an additional count is added to the integer portion.23:16 - GTC_COUNT_INT: Integer portion of the GTC accumulator count.15:0 - GTC_COUNT_FRAC: Fractional portion of the GTC accumulator count. This value should be programmed to the decimal portion of the count times 65536.

15.4.7.93 0x0984 SEC GTC Command Edge Register (Default Value: 0x0000_0000)

Offset: 0x0984			Register Name: SEC_GTC_COMMAND_EDGE
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	SEC_GTC_COMMAND_EDGE Returns the value of the global time code at the last AUX command edge event tracked by the transmitter core. This value is identical to the value transmitted to the sink device during a GTC update event. The register is provided for information purposes only.31:0 – Internal GTC counter value.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.4.7.94 0x0988 SEC GTC AUX Frame SYNC Register (Default Value: 0x0000_0000)

Offset: 0x0988			Register Name: SEC_GTC_AUX_FRAME_SYNC
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	SEC_GTC_AUX_FRAME_SYNC Contains the most recent sampled value of the global time code for AUX frame sync. This value is updated once per frame at the start of the first active pixel in a frame. 31:0 – Global time code for the AUX frame sync value. This value is automatically transmitted when a write to DPCD address 0x0015C is performed.

15.4.7.95 0x0990 SRC0 EDP CRC Enable Register (Default Value: 0x0000_0000)

Offset: 0x0990			Register Name: SRC0_EDP_CRC_ENABLE
Bit	Read/Write	Default/Hex	Description
31:0	RW	0x0	SRC0_EDP_CRC_ENABLE Global enable for the CRC calculation logic when required for the support of panel self-refresh mode. Set this value to a 1 to enable the CRC function. 0 – Set to a 1 in eDP PSR or PSR2 mode to enable CRC data calculation.

15.4.7.96 0x0994 SRC0 EDP CRC Red Register (Default Value: 0x0000_0000)

Offset: 0x0994			Register Name: SRC0_EDP_CRC_RED
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	SRC0_EDP_CRC_RED Result of the most recent CRC calculation for the RED color channel. The value of this register is updated at the end of an active PSR or PSR2 frame. 15:0 – Most recent calculated RED CRC value.

15.4.7.97 0x0998 SRC0 EDP CRC Green Register (Default Value: 0x0000_0000)

Offset: 0x0998			Register Name: SRC0_EDP_CRC_GREEN
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0998			Register Name: SRC0_EDP_CRC_GREEN
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	SRC0_EDP_CRC_GREEN Result of the most recent CRC calculation for the GREEN color channel. The value of this register is updated at the end of an active PSR or PSR2 frame.15:0 – Most recent calculated GREEN CRC value.

15.4.7.98 0x099C SRC0 EDP CRC Blue Register (Default Value: 0x0000_0000)

Offset: 0x099C			Register Name: SRC0_EDP_CRC_BLUE
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	SRC0_EDP_CRC_BLUE Result of the most recent CRC calculation for the BLUE color channel. The value of this register is updated at the end of an active PSR or PSR2 frame.15:0 – Most recent calculated BLUE CRC value.

15.4.8 eDP_REG_PAD Register Description

15.4.8.1 0x0000 DP LNK CLK CFG Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: DP_LNK_CLK_CFG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	DP_LNK_CLK_CFG LNK_CLK_GATIING 1: OPEN 0: Gating

15.4.8.2 0x0004 DP VID CLK CFG Register (Default Value: 0x0000_0000)

Offset: 0x004			Register Name: DP_VID_CLK_CFG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W	0x0	VID1_CLK_GATIING 1: OPEN 0: Gating
3:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x004			Register Name: DP_VID_CLK_CFG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	DP_LNK_CLK_CFG VID0_CLK_GATIING 1: OPEN 0: Gating

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.5 MIPI DSI

15.5.1 Overview

The Display Serial Interface is a high-speed interface between a host processor and peripheral devices that adhere to MIPI Alliance specifications for mobile device interfaces. This DSI module is composed of a DSI controller which is compliance with MIPI DSI specification V1.02 and a D-PHY module which is compliance with MIPI DPHY specification V1.0.

The MIPI DSI includes the following features:

DSI Host Features

- Compliance with MIPI DSI v1.02
- Supports up to 4 lanes
- Without DSC, single-link DSI supports up to 1920*1200@60fps
- Dual-link DSI supports 2.5K@60fps and 4K@45fps
- Only DSI0 supports DSC function, supporting up to 2000x1200@120fps
- Supports non-burst mode with sync pulse/sync event, burst mode
- Supports pixel format: RGB888, RGB666, RGB666 loosely packed and RGB565
- Supports continuous lane clock mode and non-continuous lane clock mode
- Compliance with MIPI DCS v1.01, bidirectional communication in LP through data lane 0
- Supports bidirectional communication of all generic commands in LP through data lane 0
- Supports Low Power Data Transmission
- Supports ULPS and Escape modes
- Hardware Checksum capabilities

D-PHY Features

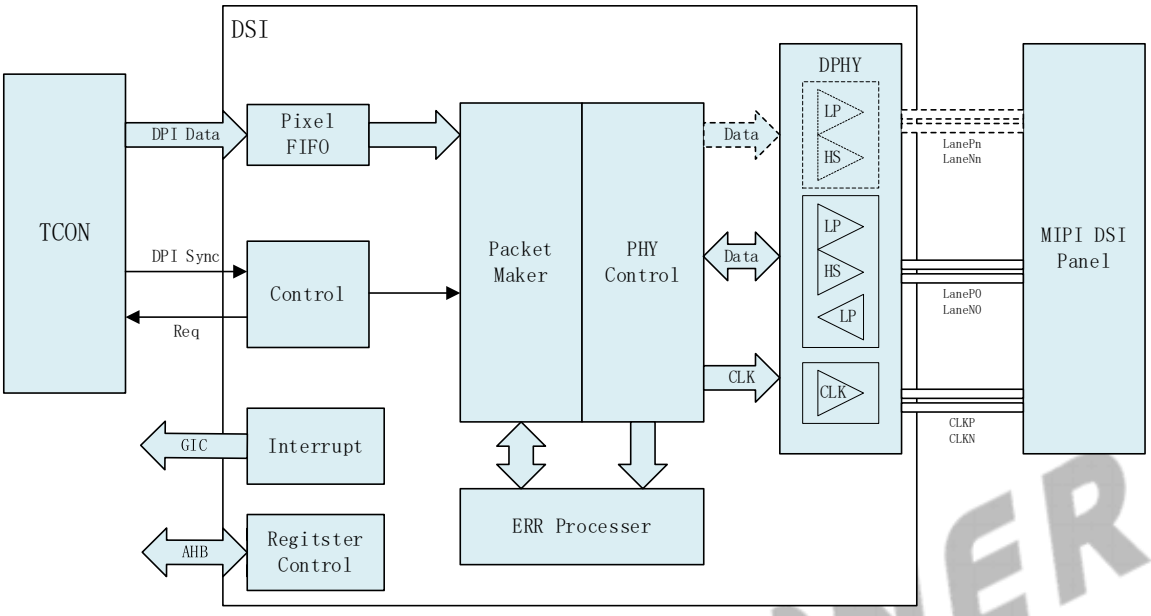
- Compliance with D-PHY V1.2
- Supports up to 4 lanes
- Aggregate throughput up to 6 Gbps with 4 data lanes
- Bidirectional communication in Low Power mode through data lane 0
- Supports Low Power Escape modes and Ultra Low Power state
- Supports multiplex with GPIO, GPIO can work in 3.3V or 1.8V power supply
- 1.8V±5% analog supply operation

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.5.2 Block Diagram

The following figure shows a block diagram of the MIPI DSI.

Figure 15-36 MIPI DSI Block Diagram



15.5.3 Clock Sources

The following table describes the clock sources of MIPI DSI. For clock setting, configurations, and gating information, refer to the section CCU.

Module	Clock Sources	Description
MIPI DSI0/1	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.
	PERI0_200M	Its frequency is 200 MHz by default.
	PERI0_150M	Its frequency is 150 MHz by default.

15.5.4 External Signals

The following table describes the external signals of MIPI DSI.

Table 15-12 MIPI DSI External Signals

Signal Name	Description	Type
DSI0-CKN	DSI0 Differential Clock Negative Signal	AO
DSI0-CKP	DSI0 Differential Clock Positive Signal	AO
DSI0-D3N	DSI0 Differential Data 3 Negative Signal	AO
DSI0-D2N	DSI0 Differential Data 2 Negative Signal	AO
DSI0-D1N	DSI0 Differential Data 1 Negative Signal	AO
DSI0-D0N	DSI0 Differential Data 0 Negative Signal	AI/O
DSI0-D3P	DSI0 Differential Data 3 Positive Signal	AO
DSI0-D2P	DSI0 Differential Data 2 Positive Signal	AO
DSI0-D1P	DSI0 Differential Data 1 Positive Signal	AO

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

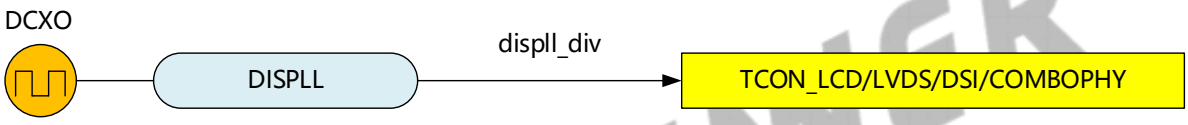
Signal Name	Description	Type
DSI0-D0P	DSI0 Differential Data 0 Positive Signal	AI/O
DSI1-CKN	DSI1 Differential Clock Negative Signal	AO
DSI1-CKP	DSI1 Differential Clock Positive Signal	AO
DSI1-D[3:0]N	DSI1 Differential Data[3:0] Negative Signal	AO
DSI1-D[3:0]P	DSI1 Differential Data[3:0] Positive Signal	AO
DSI-TRIG-LCD-TE1	Screen Trigger Signal	AI

15.5.5 Functional Description

15.5.5.1 DISPLL Distribution

The following figure shows the DISPLL distribution for modules.

Figure 15-37 DISPLL Distribution



DISPLL is located inside the VIDEO_OUT_SYS system and mainly provides the function clock for the TCON_LCD/LVDS/DSI/COMBOPHY module.

DISPLL can output two clocks:

- **clk_hs**: 1 GHz at max. mainly used as DPHY serial clock (only used for output to the DSI interface).
- **clk_ls**: 1.2 GHz at max. It serves as the function clock for the TCON_LCD module (used to output RGB/LVDS/DSI interface timing). This clock is divided internally in TCON_LCD to obtain the DSI/LVDS module function clock.

15.5.5.2 DISPLL Specifications

The specifications of DISPLL are shown in the following table.

Table 15-13 DISPLL Specifications

PLL	Stable Operating Frequency	Actual Operating Frequency	Spread Spectrum	Linear FM	Pk-Pk	Lock Time
DISPLL	1.26 GHz-2.52 GHz	2.4 GHz	Yes	Yes	70ps@1GHz	0.1 ms

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.5.6 Programming Guidelines

NOTE

Frequent PLL enable/disable is not recommended, as the PLL enable/disable will arise the mutual interference of PLLs and system instability.

15.5.6.1 Enable PLL

Step 1 Write 1 to the PLL_EN, EN_LVS, and, LDO_EN of the DPHY_PLL_REG0.

Step 2 Set LOCK_ENABLE as 1 in the DPHY_PLL_REG1.

Step 3 Wait the lock status to change to 1. Perform the adjudgement for three times.

Step 4 Wait 20 us latency.

Step 5 Configure the M0/M1, M2/M3, P, N factors in the DPHY_PLL_REG0.

Step 6 Write 1 to the PLL_UPDATE of the DPHY_PLL_REG0.

Step 7 Wait the PLL_UPDATE of the DPHY_PLL_REG0 to be cleared.

Step 8 Wait the lock status to change to 1. Perform the adjudgement for three times.

Step 9 Wait 20 us latency, and then the PLL is available.

15.5.6.2 Disable PLL

Step 1 Set LOCK_ENABLE as 0 in the DPHY_PLL_REG1.

Step 2 Write 0 to the PLL_PLL_EN and PLL_LDO_EN of the DPHY_PLL_REG0.

15.5.6.3 PLL Pre-Divider Frequency Modulation

The PLL linear frequency modulation supports smooth transition to target N value at a certain modulation rate value without re-locking. However, only the linear frequency modulation of N value is supported. When the pre-divider factor alters, PLL should be re-locked.

When not enabling linear frequency modulation, or when the pre-divider should be adjusted in the condition that liner frequency modulation is enabled. Follow the steps below to perform PLL pre-divider frequency modulation.

Step 1 Set the LOCK_ENABLE in the DPHY_PLL_REG1 as 0.

Step 2 Set the LOCK_ENABLE in the DPHY_PLL_REG1 as 1.

Step 3 Configure N, M1, M0, and P in the DPHY_PLL_REG0.

Step 4 Set the PLL_UPDATE in the DPHY_PLL_REG0 as 1.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 5 Set the PLL_UPDATE in the DPHY_PLL_REG0 as 1.

Step 6 Wait the lock status to change to 1. Perform the adjudgement for three times.

Step 7 Wait 20 us latency.

15.5.6.4 PLL Linear Frequency Modulation

The linear PLL frequency modulation mode is designed to address the re-locking issue encountered when switching N values in integer frequency duplication. In this mode, the N value can be directly configured, and the PLL will smoothly converge the N value to the target frequency point based on the configured frequency slope.

When configuring linear frequency modulation, static parameters in the fractional divider need to be set, while the control parameters are automatically managed by the linear frequency modulation.

Step 1 Set PLL_EN in the DPHY_PLL_REG0 as 1, and wait DISPLL lock state is stable.

Step 2 Set Spread Frequency Mode in the DPHY_PLL_PAT0_CTL_REG as 10 or 11. Set PLL_PI_EN as 1 and SDM Smooth Enable as 0 in the DPHY_PLL_PAT1_CTL_REG.

Step 3 Set PLL_LFM_STEP in the DPHY_PLL_LFM_REG. STEP is 12 bit. The formula is as below:

FREQ = FCLK*FCLK*STEP/2^17

In the above formula. FREQ is the target modulation rate at the unit of MHz/us. The FCLK is reference clock frequency at the unit of MHz. Thus, the step can be gotten by the formula as below:

STEP = FREQ*2^17/FCLK/FCLK

Step 4 Set the PLL_LFM_EN in the DPHY_PLL_LFM_REG as 1.

Step 5 Set the Reg_update in the DPHY_PLL_REG0 as 1.

Step 6 Wait the Reg_update in the DPHY_PLL_REG0 to be 0.

Step 7 Set the FB_DIV in the DPHY_PLL_REG0 and then write 1 to the PLL_UPDATE.

Step 8 Wait the Reg_update to be 0, indicating the linear frequency modulation completes.

Step 9 To re-configure N value, go back to the step 7.

Step 10 To disable linear frequency modulation, set PLL_LFM_EN in the DPHY_PLL_LFM_REG as 0, and set Reg_update in the DPHY_PLL_REG0 as 1.

15.5.6.5 PLL Spreading/Fractional Division

The fractional division is to add a fractional value to the divider N of a PLL to achieve a more precise frequency configuration. By applying fractional division, the multiplication factor N of the PLL can be expressed as N.x, where N represents the added fractional value.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

The PLL spreading is to add a triangular wave to the N value of a PLL to let the final output frequency exhibit a triangular wave variation. Spreading parameters consist of spread amplitude and spread spectrum period. The spread amplitude refers to the range of variation in the output frequency; while the spread spectrum period is the duration of one cycle of the triangular wave modulation, whose reciprocal is spread spectrum frequency.

PLL spreading/fractional division is configured through DPHY_PLL_PAT0_CTL_REG and DPHY_PLL_PAT1_CTL_REG; therefore, the generic/linear PLL spreading/fractional division procedures are the same. All the parameters in the two types of registers are divided into static parameters and control parameters.

Static parameters are used to adjust the order and phase interpolation of the fractional division loop and don't support dynamic switching. To alter parameters, disable PLL spreading/fractional division, configure static parameters, and then enable PLL spreading/fractional division. The parameters are shown as below.

- SPR_FREQ_MODE: SDM mode switching.
- PLL_PI_EN: It is used to decide whether to enable phase interpolation (PI) mode.
- PLL_PI_CFG: PI circuit current control.
- SMOOTH_EN: It is used to enable frequency modulation smooth.
- DITHER_EN: It is used to enable dither. When dither is enabled, a pseudo-random sequence will be added to the frequency modulation curve.

Control parameters are used to control frequency modulation curve and support dynamic switching. It should be reminded that if the SMOOTH_EN is set, control parameters only can be switched in the condition that SDM_BUSY is set to 0. The control parameters are shown as below.

- WAVE_STEP: Spreading step. The formula is shown as below.

  $$WAVE_STEP = 2^{17}*(x2-x1)*2/(Fclk/FREQ)$$

  x2 is the upper limit; x2 is the lower limit; Fclk is the PLL reference clock frequency; FREQ is the spreading slope. PLL multiplication factors range from N.x1 to N.x2.

- WAVE_BOT: Spreading starting point. The formula is shown as below.

  for upward frequency spreading, $SDM_BOT = x1*2^{17}$

  for downward frequency spreading, $SDM_BOT = x2*2^{17}$

- FREQ: Spreading slope. To dynamically switch this parameter, switch WAVE_STEP at the same time.
- SDM_DIRECTION: Spreading direction, including upward frequency spreading and downward frequency spreading. During upward frequency spreading, the curve starts from x1 and then adjusts to x2 before reversing; during downward frequency spreading, the curve starts from x2 and then adjusts to x1 before reversing. To dynamically switch this parameter, switch WAVE_BOT at the same time.
- FRAC_EN: Fractional division enable.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- FRAC_IN: Fractional division frequency point. The formula is shown as below.

FRAC_IN = x*2^17

The master switch of PLL spreading/fractional division is SIG_DELT_PAT_EN. It should be enabled before PLL spreading/fractional division usage.

PLL spreading/fractional division configuration is shown as below.

SIG_DELT_PAT_EN	FRAC_EN	WAVE_STEP	FRAN_IN	MODE
1	0	Not equal to 0	/	PLL spreading
1	0	Equal to 0	/	fractional division
1	1	/	Arbitrary	fractional division

The PLL spreading/fractional division procedure is as follows.

Step 1 Enable PLL by referring to section Enable PLL.

Step 2 Configure static parameters as follows.

- SPR_FREQ_MODE: It is recommended to be 2 or 3.
- PLL_PI_EN: It is recommended to be 1.
- PLL_PI_CFG: It is recommended to use default value.
- SMOOTH_EN: It is recommended to be 1.
- DITHER: It is recommended to be 0.

Step 3 Configure WAVE_STEP, WAVE_BOT, FREQ, SDM_DIRECTION, FRAC_IN, and FRAC_EN according to formulas described in this section.

Step 4 Configure SIG_DELT_PAT_EN and other parameters to enable PLL spreading/fractional division.

Step 5 To adjust static parameters, configure SIG_DELT_PAT_EN as 0. When SDM_BUSY is 0, go back to Step 1

Step 6 To adjust control parameters after PLL spreading/fractional division is enabled, configure WAVE_STEP, WAVE_BOT, FREQ, SDM_DIRECTION, and FRAC_IN.

Step 7 To disable PLL spreading, set SIG_DELT_PAT_EN as 0. To enable it again, judge that SDM_BUSY is 0.

15.5.6.6 Configure clk_hs and clk_ls Frequency

clk_hs = fvco/(postdiv0*postdiv1)

clk_ls = fvco/(postdiv2*postdiv3)

Table 15-14 Parameter Configuration

Parameters	Configuration Register	
prediv = p<3:0>+1	p[3:0] is configured in bit [19:16].	DPHY_PLL_REG0 (Offset:

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Parameters	Configuration Register	
postdiv0 = m0<1:0>+1	m0[1:0] is configured in bit [5:4].	0x1104)
postdiv1 = m1<3:0>+1	m1[3:0] is configured in bit [3:0].	
postdiv2 = m2<1:0>+1	m2[1:0] is configured in bit [29:28].	
postdiv3 = m3<3:0>+1	m3[3:0] is configured in bit [27:24].	
fvco=fref*n<7:0>/prediv	n[7:0] is configured in bit [15:8].	

15.5.7 Register List

Module Name	Base Address
COMBO_PHY_TX_DSI0	0x05506000
COMBO_PHY_TX_DSI1	0x05508000

Register Name	Offset	Description
DPHY_CTL_REG	0x1000	DPHY Control Register
DPHY_TX_CTL_REG	0x1004	DPHY TX Control Register
DPHY_RX_CTL_REG	0x1008	DPHY RX Control Register
DPHY_TX_TIME0_REG	0x1010	DPHY TX Timing Parameter 0 Register
DPHY_TX_TIME1_REG	0x1014	DPHY TX Timing Parameter 1 Register
DPHY_TX_TIME2_REG	0x1018	DPHY TX Timing Parameter 2 Register
DPHY_TX_TIME3_REG	0x101C	DPHY TX Timing Parameter 3 Register
DPHY_RX_TIME0_REG	0x1030	DPHY RX Timing Parameter 0 Register
DPHY_RX_TIME1_REG	0x1034	DPHY RX Timing Parameter 1 Register
DPHY_RX_TIME3_REG	0x1040	DPHY RX Timing Parameter 3 Register
DPHY_ANA0_REG	0x104C	DPHY Analog 0 Register
DPHY_ANA1_REG	0x1050	DPHY Analog 1 Register
DPHY_ANA2_REG	0x1054	DPHY Analog 2 Register
DPHY_ANA3_REG	0x1058	DPHY Analog 3 Register
DPHY_ANA4_REG	0x105C	DPHY Analog 4 Register
DPHY_INT_EN0_REG	0x1060	DPHY Interrupt Enable 0 Register
DPHY_INT_EN1_REG	0x1064	DPHY Interrupt Enable 1 Register
DPHY_INT_EN2_REG	0x1068	DPHY Interrupt Enable 2 Register
DPHY_INT_PD0_REG	0x1070	DPHY Interrupt Pending 0 Register
DPHY_INT_PD1_REG	0x1074	DPHY Interrupt Pending 1 Register
DPHY_INT_PD2_REG	0x1078	DPHY Interrupt Pending 2 Register
DPHY_DBG0_REG	0x10E0	DPHY Debug 0 Register
DPHY_DBG1_REG	0x10E4	DPHY Debug 1 Register
DPHY_DBG2_REG	0x10E8	DPHY Debug 2 Register
DPHY_DBG3_REG	0x10EC	DPHY Debug 3 Register
DPHY_DBG4_REG	0x10F0	DPHY Debug 4 Register
DPHY_DBG5_REG	0x10F4	DPHY Debug 5 Register
DPHY_TX_SKEW_REG0	0x10F8	DPHY TX Skew Register0

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
DPHY_TX_SKEW_REG1	0x10FC	DPHY TX Skew Register1
DPHY_TX_SKEW_REG2	0x1100	DPHY TX Skew Register2
DPHY_PLL_REG0	0x1104	DPHY PLL Register0
DPHY_PLL_REG1	0x1108	DPHY PLL Register1
COMBO_PHY_REG0	0x1110	COMBO PHY Register0
COMBO_PHY_REG1	0x1114	COMBO PHY Register1
DPHY_PLL_REG3	0x1124	DPHY PLL Register3
DPHY_PLL_PAT0_CTL_REG	0x1130	DPHY PLL Patten0 Control Register
DPHY_PLL_PAT1_CTL_REG	0x1134	DPHY PLL Patten1 Control Register
DPHY_PLL_LFM_REG	0x1138	DPHY PLL LFM Register

15.5.8 Register Description

15.5.8.1 0x1000 DPHY Control Register (Default Value: 0x0000_0000)

Offset: 0x1000			Register Name: DPHY_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5:4	R/W	0x0	LANE_NUM Lane Number 00: 1 data lane 01: 2 data lane 10: 3 data lane 11: 4 data lane Note: this bits determine lane number used for transmission.
3:1	/	/	/
0	R/W	0x0	MODULE_EN When it's disabled, the module will be reset to idle state. 0: Disable 1: Enable

15.5.8.2 0x1004 DPHY TX Control Register (Default Value: 0x0000_0000)

Offset: 0x1004			Register Name: DPHY_TX_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1004			Register Name: DPHY_TX_CTL_REG
Bit	Read/Write	Default/Hex	Description
29	R/W	0x0	ULPSTX_ENTER Ulpstx Enter 0: Direct (enter LP-00 after ULPS command) 1: Indirect (enter MARK-I after ULPS command then LP-00)
28	R/W	0x0	HSTX_CLK_CONT When this bit is enable, clk lane continue in HS mode. When this bit is disable, clk lane anto enter LP mode. 0: Disable 1: Enable
27	R/W	0x0	SKEWCAL_STP_SET When this bit is enable, data lane is forced to enter skewcal mode. 0: Disable 1: Enable
26	/	/	/
25	R/W	0x0	HSTX_CLK_EXIT Hstx Clock Exit 0: No effect 1: Force clock lane exit from HS
24	R/W	0x0	HSTX_DATA_EXIT Hstx Data Exit 0: No effect 1: Force all data lanes exit from HS
23:21	/	/	/
20	R/W	0x0	ULPSTX_CLK_EXIT Ulpstx Clk Exit 0: No effect 1: Force Clock lane exit from ULPS
19	R/W	0x0	ULPSTX_DATA3_EXIT Ulpstx Data3 Exit 0: No effect 1: Force data lane 3 exit from ULPS
18	R/W	0x0	ULPSTX_DATA2_EXIT Ulpstx Data2 Exit 0: No effect 1: Force data lane 2 exit from ULPS
17	R/W	0x0	ULPSTX_DATA1_EXIT Ulpstx Data1 Exit 0: No effect 1: Force data lane 1 exit from ULPS

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1004			Register Name: DPHY_TX_CTL_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	ULPSTX_DATA0_EXIT Ulpstx Data0 Exit 0: No effect 1: Force data lane 0 exit from ULPS
15:13	/	/	/
12	R/W	0x0	FORCE_LP11 Force LP11 0: No effect 1: Force module work in LP11
11	R/W	0x0	HSTX_8B9B_EN HSTX 8B9B Enable 0: 8B9B Encoding disable 1: 8B9B Encoding enable
10	R/W	0x0	LPTX_8B9B_EN LPTX 8B9B Enable 0: 8B9B Encoding disable 1: 8B9B Encoding enable
9	R/W	0x0	HSTX_ENDIAN HSTX Endian 0: LSB first 1: MSB first
8	R/W	0x0	LPTX_ENDIAN LPTX Endian 0: LSB first 1: MSB first
7:5	/	/	/
4	R/W	0x0	TX_CLK_FORCE Write 1 force into tx default state(lp00), write 0 has no effect.
3	R/W	0x0	TX_D3_FORCE Write 1 force into tx default state(lp00), write 0 has no effect.
2	R/W	0x0	TX_D2_FORCE Write 1 force into tx default state(lp00), write 0 has no effect.
1	R/W	0x0	TX_D1_FORCE Write 1 force into tx default state(lp00), write 0 has no effect.
0	R/W	0x0	TX_D0_FORCE Write 1 force into tx default state(lp00), write 0 has no effect.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.5.8.3 0x1008 DPHY RX Control Register (Default Value: 0x0000_0000)

Offset: 0x1008			Register Name: DPHY_RX_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DBC_EN Debounce enable
30:25	/	/	/
24	R/W	0x0	RX_CLK_FORCE 0: No effect 1: Force rx
23	R/W	0x0	RX_D3_FORCE 0: No effect 1: Force rx
22	R/W	0x0	RX_D2_FORCE 0: No effect 1: Force rx
21	R/W	0x0	RX_D1_FORCE 0: No effect 1: Force rx
20	R/W	0x0	RX_D0_FORCE 0: No effect 1: Force rx
19:16	R/W	0x0	LPRX_TRND_MASK 0: Not mask 1: Mask, no ack to turnaround in LPRX
15:11	/	/	/
10	R/W	0x0	LPRX_8B9B_EN 0: 8B9B Decoding disable 1: 8B9B Decoding enable
9	/	/	/
8	R/W	0x0	LPRX_ENDIAN 0: LSB first 1: MSB first
7:0	/	/	/

15.5.8.4 0x1010 DPHY TX Timing Parameter 0 Register (Default Value: 0x0000_0000)

Offset: 0x1010			Register Name: DPHY_TX_TIME0_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	HS_TRAIL_SET HS trail = (HS_TRAIL_SET + 2) * Tbyteclk + (2~3)*Tclk - (3~4)*Tclkd8.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1010			Register Name: DPHY_TX_TIME0_REG
Bit	Read/Write	Default/Hex	Description
23:16	R/W	0x0	HS_PRE_SET The setting of hs prepare time: Begin with LP00, end after (HS_PRE_SET + 4)*Tclk.
15:8	/	/	/
7:0	R/W	0x0	LPX_TM_SET LP pulse = (LPX_TM_SET + 1)*Tclk.

15.5.8.5 0x1014 DPHY TX Timing Parameter 1 Register (Default Value: 0x0000_0000)

Offset: 0x1014			Register Name: DPHY_TX_TIME1_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	CK_POST_SET CK_Post_set cannot be 0. After the falling edge of entx, keep it for (CK_POST_SET + 2)* Tclk and then turn off the clk.
23:16	R/W	0x0	CK_PRE_SET Clk pre = ((CK_PRE_SET + 2)+ (0 ~ LPX_TM_SET))* Tclk
15:8	R/W	0x0	CK_ZERO_SET CK_Zero_set cannot be 0. When entxc is set 1,after (CK_ZERO_SET + 3)* Tclk, the enckq will be set as 1.
7:0	R/W	0x0	CK_PREP_SET Clk prepare = （ CK_PREP_SET + 4 ）* clk

15.5.8.6 0x1018 DPHY TX Timing Parameter 2 Register (Default Value: 0x0000_0000)

Offset: 0x1018			Register Name: DPHY_TX_TIME2_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R/W	0x0	HS_DLY_MODE The setting of HS zero time depending on HS_DLYMODE: when HS_DLYMODE=0, HS_ZERO_TIME > 20*Tbyteclk When HS_DLYMODE=1, HS_ZERO_TIME = (HS_DLY_SET + 4)*Tclk - 2*(LPX_TM_SET + 1)*Tclk + (20~23)*Tbyteclk - (HS_PRE_SET + 4)*Tclk

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1018			Register Name: DPHY_TX_TIME2_REG
Bit	Read/Write	Default/Hex	Description
27:24	/	/	/
23:8	R/W	0x0	HS_DLY_SET Use this value to prolong the time before LP switch to HS, cut down the length of HS-Zero.
7:0	R/W	0x0	CK_TRAIL_SET CK_TRAIL_SET clk tail =(CK_TRAIL_SET + 2)* Tclk

15.5.8.7 0x101C DPHY TX Timing Parameter 3 Register (Default Value: 0x0000_0000)

Offset: 0x101C			Register Name: DPHY_TX_TIME3_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	LPTX_ULPS_EXIT_SET ULPS exit Cycles.

15.5.8.8 0x1030 DPHY RX Timing Parameter 0 Register (Default Value: 0x0000_0000)

Offset: 0x1030			Register Name: DPHY_RX_TIME0_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	HSRX_SYNC_ERR_TO When HS SOT is not detected until reaching the hs sync error timeout counter, the SOT_ERR should be flagged. Only valid for data lane.
23:16	R/W	0x0	HSRX_CLK_MISS When clock lane is detected no clock until hs rx clock miss counter, the receiver disconnects the terminal resister. Only valid for clock lane.
15:8	R/W	0x0	LPRX_TO The timeout counter for receiver in LP mode.
7:6	/	/	/
5	R/W	0x0	HSRX_SYNC_ERR_TO_EN HSRX Sync Error To Enable 0: Disable 1: Enable HSRX_SYNC_ERR_TO counter
4	R/W	0x0	HSRX_CLK_MISS_EN HSRX Clock Miss Enable 0: Disable 1: Enable HSRX_CLK_MISS counter
3:2	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1030			Register Name: DPHY_RX_TIME0_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	FREQ_CNT_EN FREQ Count Enable 0: Disable 1: Enable When enabled, the FREQ_CNT counter is counted by DPhy Clock between 1000 Byte Clock.
0	R/W	0x0	LPRX_TO_EN LP RX timeout enable 0: Disable 1: Enable

15.5.8.9 0x1034 DPHY RX Timing Parameter 1 Register (Default Value: 0x0000_0000)

Offset: 0x1034			Register Name: DPHY_RX_TIME1_REG
Bit	Read/Write	Default/Hex	Description
31:20	R/W	0x0	RX_DLY The time that DPhy process hs fifo data and pull off data valid signal to protocal after DPhy has detected the lane state from HS to LP. It should be more than 8 byte clock cycle time.
19:0	R/W	0x0	LPRX_ULPS_WP When receivers detect MARK-I for ULPS Wakeup Cycles, the corresponding ULPS WP is pending. (Valid for clock lane and all data lane)

15.5.8.10 0x1040 DPHY RX Timing Parameter 3 Register (Default Value: 0x0000_0000)

Offset: 0x1040			Register Name: DPHY_RX_TIME3_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	LPRST_DLY The added delay time that reset the hs-fifo after the DPhy has detected the HS-to-LP.
15:0	R	0x0	FREQ_CNT The value of FREQ_CNT counter is counted by DPhy Clock between 1000 Byte Cock.

15.5.8.11 0x104C DPHY Analog 0 Register (Default Value: 0x0000_0044)

Offset: 0x104C	Register Name: DPHY_ANA0_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:20	R/W	0x0	dsi_reg_preemph0 Data lane0 hstx preemphasis tuning.
19:16	R/W	0x0	dsi_reg_preemph1 Data lane1 hstx preemphasis tuning.
15:12	R/W	0x0	dsi_reg_preemph2 Data lane2 hstx preemphasis tuning.
11:8	R/W	0x0	dsi_reg_preemph3 Data lane3 hstx preemphasis tuning.
7	/	/	/
6:4	R/W	0x4	dsi_reg_lptx_setc clock lane lptx enable
3	/	/	/
2:0	R/W	0x4	dsi_reg_lptx_setr LPtx output resistance tuning.

15.5.8.12 0x1050 DPHY Analog 1 Register (Default Value: 0x0000_0000)

Offset: 0x1050			Register Name: DPHY_ANA1_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	envtt_mode vtt mode select.
30:27	/	/	/
26	R/W	0x0	dsi_en_phback_lock Back sync clk lock enable.
25	R/W	0x0	dsi_en_phback_sync Back sync clk enable.
24	R/W	0x0	dsi_en_soft_phsel Resister control enable for sync clk.
23:22	R/W	0x0	dsi_reg_soft_phsel Resister tuning for sync clk.
21:20	R/W	0x0	dsi_reg_phsync_set digital clock phase set for parallel data.
19:16	R/W	0x0	dsi_en_clkpatd Hstx clk pattern enable for data lane0 to lane 0to3.
15	/	/	/
14:11	R/W	0x0	dsi_en_vtt_test Hstx vtt test enable for data lane0 to lane3.
10	R/W	0x0	dsi_en_vtt_testc Hstx vtt test enable for clk lane.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1050			Register Name: DPHY_ANA1_REG
Bit	Read/Write	Default/Hex	Description
9:6	R/W	0x0	dsi_reg_hstx_plr Data lane0 to lane3 hs tx polar reverse.
5	R/W	0x0	dsi_reg_hstxck_plr Clk lane hs tx polar reverse.
4:1	R/W	0x0	dsi_en_vlptx_test Data lane0 to lane3 LPtx analog point test enable
0	R/W	0x0	dsi_en_vlptx_testc Clk lane LPtx analog point test enable.

15.5.8.13 0x1054 DPHY Analog 2 Register (Default Value: 0x0000_0000)

Offset: 0x1054			Register Name: DPHY_ANA2_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0x0	EN_P2S Enable signal for HS p2s module in Data Lane<3:0>
23:20	R/W	0x0	EN_RX Debug signal, HS RX module data lane enable Only EN_RX [0] could output to GPIO.
19:16	R/W	0x0	EN_TERM Debug signal, HS RX module terminal resistance enable in data lane. Only EN_TREM[0] could output to GPIO.
15	/	/	/
14	R/W	0x0	EN_RXC Debug signal, HS RX module clock lane enable
13	R/W	0x0	EN_TERMC Debug signal, HS RX module terminal resistance enable in clock lane.
12	/	/	/
11:8	R/W	0x0	EN_TXTERM Enable signal for HStx termination in Data Lane<3:0>
7	/	/	/
6	R/W	0x0	EN_CLKQ Only when ANA_CPU_EN = 1, this bit will be valid. 1: Combophy output enable 0: Combophy output disable, indicating the differential pair of the output clock is 0.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1054			Register Name: DPHY_ANA2_REG
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	EN_TXTREMC Enable signal for HStx termination in Clock Lane
4	R/W	0x0	EN_CLK clock module enable.
3:2	/	/	/
1	R/W	0x0	EN_IREF lvds clk lane test clock select,
0	R/W	0x0	ANA_CPU_EN Enable all register with cpu, when disable, those bits are control by circuit automatic

15.5.8.14 0x1058 DPHY Analog 3 Register (Default Value: 0x0000_0000)

Offset: 0x1058			Register Name: DPHY_ANA3_REG
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EN_VDRVLDO_ON Enable signal for HS TX LDO in Data Lane<3:0> Set as "1111" when hstx
27	R/W	0x0	EN_VDRVLDO_ONC Enable signal for HS TX LDO in Clock Lane Set as "1" when hstx
26	R/W	0x0	EN_DIV2 Enable signal for input clock divided by 2. Set as "1"
25	R/W	0x0	EN_LVCK Enable signal for clock power LDO is active DSI set as "1";CSI set as "0"
24	R/W	0x0	EN_LV Enable signal for data power LDO is active Set as "1"
23	R/W	0x0	EN_ULPSC CLK Lane LP contention detect threshold tuning.
22:19	R/W	0x0	EN_ULPS Data Lane LP contention detect threshold tuning.
18	R/W	0x0	EN_VREF Enable signal for reference power LDO is active Set as "1"
17:15	/	/	/
14	R/W	0x0	EN_LPCDC Enable signal for LP cd module is active in Clock Lane

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1058			Register Name: DPHY_ANA3_REG
Bit	Read/Write	Default/Hex	Description
13	R/W	0x0	EN_LPTXC Enable signal for LP tx module is active in Clock Lane
12	R/W	0x0	EN_LPRXC Enable signal for LP rx module is active in Clock Lane
11:8	R/W	0x0	EN_LPCD Enable signal for LP cd module is active in Data Lane<3:0>
7:4	R/W	0x0	EN_LPRX Enable signal for LP rx module is active in Data Lane<3:0>
3:0	R/W	0x0	EN_LPTX Enable signal for LP tx module is active in Data Lane<3:0>

15.5.8.15 0x105C DPHY Analog 4 Register (Default Value: 0x04b3_0410)

Offset: 0x105C			Register Name: DPHY_ANA4_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	dsi_en_mipi Mipi dsi enable.
30	R/W	0x0	dsi_en_comtest Common test enable.
29:28	R/W	0x0	dsi_reg_comtest Common test config. 00: vp 01: vpck 10: vres 11: ib5u_test
27	/	/	/
26:24	R/W	0x4	dsi_reg_ib common ibias tuning
23	R/W	0x1	reg_vref_source Common vbias tuning 0: 1.2v (from anabias) 1: 1.8v (from vph)
22:20	R/W	0x3	dsi_reg_vres_set vref0p2 tuning.
19	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x105C			Register Name: DPHY_ANA4_REG
Bit	Read/Write	Default/Hex	Description
18:16	R/W	0x3	dsi_reg_vtt_set vref0p4 tuning.
15	/	/	/
14:12	R/W	0x0	dsi_reg_vlptx_set LPtx reference voltage tuning.
11	/	/	/
10:8	R/W	0x4	dsi_reg_vlv_set vref0p9 tuning.
7	R/W	0x0	dsi_en_rescal Resistance calibration enable.
6	R/W	0x0	dsi_on_rescal Resistance calibration on.
5	R/W	0x0	dsi_en_soft_rcal Software Resistance calibration enable.
4:0	R/W	0x10	dsi_reg_soft_rcal Software Resistance calibration enable.

15.5.8.16 0x1060 DPHY Interrupt Enable 0 Register (Default Value: 0x0000_0000)

Offset: 0x1060			Register Name: DPHY_INT_EN0_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CD_LP1_ERR_D3_INT Contention Detection detects LP1 error interrupt
30	R/W	0x0	CD_LP0_ERR_D3_INT Contention Detection detects LP0 error interrupt
29	R/W	0x0	CD_LP1_ERR_D2_INT Contention Detection detects LP1 error interrupt
28	R/W	0x0	CD_LP0_ERR_D2_INT Contention Detection detects LP0 error interrupt
27	R/W	0x0	CD_LP1_ERR_D1_INT Contention Detection detects LP1 error interrupt
26	R/W	0x0	CD_LP0_ERR_D1_INT Contention Detection detects LP0 error interrupt

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1060			Register Name: DPHY_INT_EN0_REG
Bit	Read/Write	Default/Hex	Description
25	R/W	0x0	CD_LP1_ERR_D0_INT Contention Detection detects LP1 error interrupt
24	R/W	0x0	CD_LP0_ERR_D0_INT Contention Detection detects LP0 error interrupt
23	R/W	0x0	CD_LP1_ERR_CLK_INT Contention Detection detects LP1 error interrupt
22	R/W	0x0	CD_LP0_ERR_CLK_INT Contention Detection detects LP0 error interrupt
21:16	/	/	/
15	R/W	0x0	RX_ALG_ERR_D3_INT The payload that DPHY RX received is not aligned to 8bit or 9bit, which depends on HSRX_8B9B_EN
14	R/W	0x0	RX_ALG_ERR_D2_INT The payload that DPHY RX received is not aligned to 8bit or 9bit, which depends on HSRX_8B9B_EN
13	R/W	0x0	RX_ALG_ERR_D1_INT The payload that DPHY RX received is not aligned to 8bit or 9bit, which depends on HSRX_8B9B_EN
12	R/W	0x0	RX_ALG_ERR_D0_INT The payload that DPHY RX received is not aligned to 8bit or 9bit, which depends on HSRX_8B9B_EN.
11	R/W	0x0	SOT_SYNC_ERR_D3_INT DPHY RX cannot detected SOT sequence at Data Lane 0 interrupt.
10	R/W	0x0	SOT_SYNC_ERR_D2_INT DPHY RX cannot detected SOT sequence at Data Lane 0 interrupt.
9	R/W	0x0	SOT_SYNC_ERR_D1_INT DPHY RX cannot detected SOT sequence at Data Lane 0 interrupt.
8	R/W	0x0	SOT_SYNC_ERR_D0_INT DPHY RX cannot detected SOT sequence at Data Lane 0 interrupt.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1060			Register Name: DPHY_INT_EN0_REG
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	SOT_ERR_D3_INT DPHY RX detected SOT sequence with 1-bit error at Data Lane 0 interrupt.
6	R/W	0x0	SOT_ERR_D2_INT DPHY RX detected SOT sequence with 1-bit error at Data Lane 0 interrupt.
5	R/W	0x0	SOT_ERR_D1_INT DPHY RX detected SOT sequence with 1-bit error at Data Lane 0 interrupt.
4	R/W	0x0	SOT_ERR_D0_INT DPHY RX detected SOT sequence with 1-bit error at Data Lane 0 interrupt.
3	R/W	0x0	SOT_D3_INT SOT D3 Interrupt 0: Disable 1: Enable DPHY RX detected SOT sequence at Data Lane 3 interrupt.
2	R/W	0x0	SOT_D2_INT SOT D2 Interrupt 0: Disable 1: Enable DPHY RX detected SOT sequence at Data Lane 2 interrupt.
1	R/W	0x0	SOT_D1_INT SOT D1 Interrupt 0: Disable 1: Enable DPHY RX detected SOT sequence at Data Lane 1 interrupt.
0	R/W	0x0	SOT_D0_INT SOT D0 Interrupt 0: Disable 1: Enable DPHY RX detected SOT sequence at Data Lane 0 interrupt.

15.5.8.17 0x1064 DPHY Interrupt Enable 1 Register (Default Value: 0x0000_0000)

Offset: 0x1064			Register Name: DPHY_INT_EN1_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1064			Register Name: DPHY_INT_EN1_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	FALSE_CTL_D3_INT A false control occurs at Data Lane 3 interrupt.
30	R/W	0x0	FALSE_CTL_D2_INT A false control occurs at Data Lane 2 interrupt.
29	R/W	0x0	FALSE_CTL_D1_INT A false control occurs at Data Lane 1 interrupt.
28	R/W	0x0	FALSE_CTL_D0_INT A false control occurs at Data Lane 0 interrupt.
27	R/W	0x0	ESC_CMD_ERR_D3_INT DPHY RX received cannot recognize the Escape Entry Command at Data Lane 3 interrupt.
26	R/W	0x0	ESC_CMD_ERR_D2_INT DPHY RX received cannot recognize the Escape Entry Command at Data Lane 2 interrupt.
25	R/W	0x0	ESC_CMD_ERR_D1_INT DPHY RX received cannot recognize the Escape Entry Command at Data Lane 1 interrupt.
24	R/W	0x0	ESC_CMD_ERR_D0_INT DPHY RX received cannot recognize the Escape Entry Command at Data Lane 0 interrupt.
23	R/W	0x0	RST_D3_INT DPHY RX detected Reset Trigger sequence at Data Lane 3 interrupt.
22	R/W	0x0	RST_D2_INT DPHY RX detected Reset Trigger sequence at Data Lane 2 interrupt.
21	R/W	0x0	RST_D1_INT DPHY RX detected Reset Trigger sequence at Data Lane 1 interrupt.
20	R/W	0x0	RST_D0_INT DPHY RX detected Reset Trigger sequence at Data Lane 0 interrupt.
19	R/W	0x0	UNDEF5_D0_INT DPHY RX received undefined 5 sequence at Data Lane 0 interrupt.
18	R/W	0x0	UNDEF4_D0_INT DPHY RX received undefined 4 sequence at Data Lane 0 interrupt.
17	R/W	0x0	UNDEF3_D0_INT DPHY RX received undefined 3 sequence at Data Lane 0 interrupt.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1064			Register Name: DPHY_INT_EN1_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	UNDEF2_D0_INT DPHY RX received undefined 2 sequence at Data Lane 0 interrupt.
15	R/W	0x0	UNDEF1_D0_INT DPHY RX received undefined 1 sequence at Data Lane 0 interrupt.
14	R/W	0x0	TX_TRND_ERR_D0_INT DPHY TX turn around error at Data Lane 0 interrupt.
13	R/W	0x0	RX_TRND_D0_INT DPHY RX received turn around sequence at Data Lane 0 interrupt.
12	R/W	0x0	LPDT_D0_INT DPHY RX complete LPDT transfer at Data Lane 0 interrupt.
11:10	/	/	/
9	R/W	0x0	ULPS_WP_CLK_INT DPHY RX detected ULPS wakeup at Clock Lane interrupt.
8	R/W	0x0	ULPS_CLK_INT DPHY RX detected ULPS sequence at Clock Lane interrupt.
7	R/W	0x0	ULPS_WP_D3_INT DPHY RX detected ULPS wakeup at Data Lane 3 interrupt.
6	R/W	0x0	ULPS_WP_D2_INT DPHY RX detected ULPS wakeup at Data Lane 2 interrupt.
5	R/W	0x0	ULPS_WP_D1_INT DPHY RX detected ULPS wakeup at Data Lane 1 interrupt.
4	R/W	0x0	ULPS_WP_D0_INT DPHY RX detected ULPS wakeup at Data Lane 0 interrupt.
3	R/W	0x0	ULPS_D3_INT DPHY RX detected ULPS sequence at Data Lane 3 interrupt.
2	R/W	0x0	ULPS_D2_INT DPHY RX detected ULPS sequence at Data Lane 2 interrupt.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1064			Register Name: DPHY_INT_EN1_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	ULPS_D1_INT DPHY RX detected ULPS sequence at Data Lane 1 interrupt.
0	R/W	0x0	ULPS_D0_INT DPHY RX detected ULPS sequence at Data Lane 0 interrupt.

15.5.8.18 0x1068 DPHY Interrupt Enable 2 Register (Default Value: 0x0000_0000)

Offset: 0x1068			Register Name: DPHY_INT_EN2_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	DISPLL_UNLOCK_INT 0: Disable 1: Enable DISPLL detected lock signal unstable interrupt.

15.5.8.19 0x1070 DPHY Interrupt Pending 0 Register (Default Value: 0x0000_0000)

Offset: 0x1070			Register Name: DPHY_INT_PD0_REG
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	CD_LP1_ERR_D3_PD Contention Detection detects LP1 error interrupt pending.
30	R/W1C	0x0	CD_LP0_ERR_D3_PD Contention Detection detects LP0 error interrupt pending.
29	R/W1C	0x0	CD_LP1_ERR_D2_PD Contention Detection detects LP1 error interrupt pending.
28	R/W1C	0x0	CD_LP0_ERR_D2_PD Contention Detection detects LP0 error interrupt pending.
27	R/W1C	0x0	CD_LP1_ERR_D0_PD Contention Detection detects LP1 error interrupt pending.
26	R/W1C	0x0	CD_LP0_ERR_D0_PD Contention Detection detects LP0 error interrupt pending.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1070			Register Name: DPHY_INT_PD0_REG
Bit	Read/Write	Default/Hex	Description
25	R/W1C	0x0	CD_LP1_ERR_D1_PD Contention Detection detects LP1 error interrupt pending.
24	R/W1C	0x0	CD_LP0_ERR_D1_PD Contention Detection detects LP0 error interrupt pending.
23	R/W1C	0x0	CD_LP1_ERR_CLK_PD Contention Detection detects LP1 error interrupt pending.
22	R/W1C	0x0	CD_LP0_ERR_CLK_PD Contention Detection detects LP0 error interrupt pending.
21:16	/	/	/
15	R/W1C	0x0	RX_ALG_ERR_D3_PD Asserted if the payload that DPHY RX received is not aligned to 8bit or 9bit, which depends on HSRX_8B9B_EN.
14	R/W1C	0x0	RX_ALG_ERR_D2_PD Asserted if the payload that DPHY RX received is not aligned to 8bit or 9bit, which depends on HSRX_8B9B_EN.
13	R/W1C	0x0	RX_ALG_ERR_D1_PD Asserted if the payload that DPHY RX received is not aligned to 8bit or 9bit, which depends on HSRX_8B9B_EN.
12	R/W1C	0x0	RX_ALG_ERR_D0_PD Asserted if the payload that DPHY RX received is not aligned to 8bit or 9bit, which depends on HSRX_8B9B_EN.
11	R/W1C	0x0	SOT_SYNC_ERR_D3_PD Asserted if DPHY RX cannot detect SOT sequence at Data Lane3. The SoT Leader sequence is corrupted in a way that proper synchronization cannot be expected.
10	R/W1C	0x0	SOT_SYNC_ERR_D2_PD Asserted if DPHY RX cannot detect SOT sequence at Data Lane2. The SoT Leader sequence is corrupted in a way that proper synchronization cannot be expected.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1070			Register Name: DPHY_INT_PD0_REG
Bit	Read/Write	Default/Hex	Description
9	R/W1C	0x0	SOT_SYNC_ERR_D1_PD Asserted if DPHY RX cannot detect SOT sequence at Data Lane1. The SoT Leader sequence is corrupted in a way that proper synchronization cannot be expected.
8	R/W1C	0x0	SOT_SYNC_ERR_D0_PD Asserted if DPHY RX cannot detect SOT sequence at Data Lane0. The SoT Leader sequence is corrupted in a way that proper synchronization cannot be expected.
7	R/W1C	0x0	SOT_ERR_D3_PD Asserted if DPHY RX detected SOT sequence with 1-bit error at Data Lane 3. The confidence in the payload data is lower.
6	R/W1C	0x0	SOT_ERR_D2_PD Asserted if DPHY RX detected SOT sequence with 1-bit error at Data Lane 2. The confidence in the payload data is lower.
5	R/W1C	0x0	SOT_ERR_D1_PD Asserted if DPHY RX detected SOT sequence with 1-bit error at Data Lane 1. The confidence in the payload data is lower.
4	R/W1C	0x0	SOT_ERR_D0_PD Asserted if DPHY RX detected SOT sequence with 1-bit error at Data Lane 0. The confidence in the payload data is lower.
3	R/W1C	0x0	SOT_D3_PD Asserted if DPHY RX detected SOT sequence at Data Lane 3.
2	R/W1C	0x0	SOT_D2_PD Asserted if DPHY RX detected SOT sequence at Data Lane 2.
1	R/W1C	0x0	SOT_D1_PD Asserted if DPHY RX detected SOT sequence at Data Lane 1.
0	R/W1C	0x0	SOT_D0_PD Asserted if DPHY RX detected SOT sequence at Data Lane 0.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

15.5.8.20 0x1074 DPHY Interrupt Pending 1 Register (Default Value: 0x0000_0000)

Offset: 0x1074			Register Name: DPHY_INT_PD1_REG
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	FALSE_CTL_D3_PD Asserted if a LP-Rqst (LP-10) is not followed by the remainder of a valid Escape sequence or a HS-Rqst (LP-01) is not correctly followed by a Bridge State (LP-00).
30	R/W1C	0x0	FALSE_CTL_D2_PD Asserted if a LP-Rqst (LP-10) is not followed by the remainder of a valid Escape sequence or a HS-Rqst (LP-01) is not correctly followed by a Bridge State (LP-00).
29	R/W1C	0x0	FALSE_CTL_D1_PD Asserted if a LP-Rqst (LP-10) is not followed by the remainder of a valid Escape sequence or a HS-Rqst (LP-01) is not correctly followed by a Bridge State (LP-00).
28	R/W1C	0x0	FALSE_CTL_D0_PD Asserted if a LP-Rqst (LP-10) is not followed by the remainder of a valid Escape sequence or a HS-Rqst (LP-01) is not correctly followed by a Bridge State (LP-00).
27	R/W1C	0x0	ESC_CMD_ERR_D3_PD Asserted if DPHY RX received cannot recognize the Escape Entry Command at Data Lane 3.
26	R/W1C	0x0	ESC_CMD_ERR_D2_PD Asserted if DPHY RX received cannot recognize the Escape Entry Command at Data Lane 2.
25	R/W1C	0x0	ESC_CMD_ERR_D1_PD Asserted if DPHY RX received cannot recognize the Escape Entry Command at Data Lane 1.
24	R/W1C	0x0	ESC_CMD_ERR_D0_PD Asserted if DPHY RX received cannot recognize the Escape Entry Command at Data Lane 0.
23	R/W1C	0x0	RST_D3_PD Asserted if DPHY RX detected Reset Trigger sequence at Data Lane3.
22	R/W1C	0x0	RST_D2_PD Asserted if DPHY RX detected Reset Trigger sequence at Data Lane2.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1074			Register Name: DPHY_INT_PD1_REG
Bit	Read/Write	Default/Hex	Description
21	R/W1C	0x0	RST_D1_PD Asserted if DPHY RX detected Reset Trigger sequence at Data Lane1.
20	R/W1C	0x0	RST_D0_PD Asserted if DPHY RX detected Reset Trigger sequence at Data Lane0.
19	R/W1C	0x0	UNDEF5_D0_PD Asserted if DPHY RX received undefined 5 sequence at Data Lane0. "10100000"
18	R/W1C	0x0	UNDEF4_D0_PD Asserted if DPHY RX received undefined 4 sequence at Data Lane0. "00100001"
17	R/W1C	0x0	UNDEF3_D0_PD Asserted if DPHY RX received undefined 3 sequence at Data Lane0. "01011101"
16	R/W1C	0x0	UNDEF2_D0_PD Asserted if DPHY RX received undefined 2 sequence at Data Lane0. "11011110"
15	R/W1C	0x0	UNDEF1_D0_PD Asserted if DPHY RX received undefined 1 sequence at Data Lane0. "10011111"
14	R/W1C	0x0	TX_TRND_ERR_D0_PD Asserted if DPHY TX turn around error at Data Lane 0.
13	R/W1C	0x0	RX_TRND_D0_PD Asserted if DPHY RX received turn around sequence at Data Lane0.
12	R/W1C	0x0	LPDT_D0_PD Asserted if DPHY RX complete LPDT transfer at Data Lane 0. "11100001"
11:10	/	/	/
9	R/W1C	0x0	ULPS_WP_CLK_PD Asserted if DPHY RX detected ULPS wakeup at Clock Lane.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1074			Register Name: DPHY_INT_PD1_REG
Bit	Read/Write	Default/Hex	Description
8	R/W1C	0x0	ULPS_CLK_PD Asserted if DPHY RX detected ULPS sequence at Clock Lane.
7	R/W1C	0x0	ULPS_WP_D3_PD Asserted if DPHY RX detected ULPS wakeup at Data Lane 3.
6	R/W1C	0x0	ULPS_WP_D2_PD Asserted if DPHY RX detected ULPS wakeup at Data Lane 2.
5	R/W1C	0x0	ULPS_WP_D1_PD Asserted if DPHY RX detected ULPS wakeup at Data Lane 1.
4	R/W1C	0x0	ULPS_WP_D0_PD Asserted if DPHY RX detected ULPS wakeup at Data Lane 0.
3	R/W1C	0x0	ULPS_D3_PD Asserted if DPHY RX detected ULPS sequence at Data Lane 3.
2	R/W1C	0x0	ULPS_D2_PD Asserted if DPHY RX detected ULPS sequence at Data Lane 2.
1	R/W1C	0x0	ULPS_D1_PD Asserted if DPHY RX detected ULPS sequence at Data Lane 1.
0	R/W1C	0x0	ULPS_D0_PD Asserted if DPHY RX detected ULPS sequence at Data Lane 0. "00011110"

15.5.8.21 0x1078 DPHY Interrupt Pending 2 Register (Default Value: 0x0000_0000)

Offset: 0x1078			Register Name: DPHY_INT_PD2_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W1C	0x0	DISPLL_UNLOCK_PD DISPLL detects lock unstable interrupt pending.

15.5.8.22 0x10E0 DPHY Debug 0 Register (Default Value: 0x0000_0000)

Offset: 0x10E0	Register Name: DPHY_DBG0_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R	0x0	DIR Direction 0: No lane switches into HS transmission 1: At least one lane switch into HS transmission
27	/	/	/
26	R	0x0	LOCK 0: Unlocked 1: Locked(It indicates that the PLL has been stable)
25	R	0x0	SOFT_RCAL_CMPO Resistance calibration comparator output.
24	R	0x0	SOFT_RCAL_FLAG Resistance calibration completion flag.
23:19	R	0x0	SOFT_RCAL_VALUE Resistance calibration bit return to system.
18:16	R	0x0	LPTX_STA_CLK LPTX Status Clock 000: STP_ST 001: HSRQ_ST 010: ESRQ_ST 011: TNRD_ST 100: ULPS_ST 101: HS_ST 110: ESP_ST 111: RX_ST
15	/	/	/
14:12	R	0x0	LPTX_STA_D3 LPTX Status D3 000: STP_ST 001: HSRQ_ST 010: ESRQ_ST 011: TNRD_ST 100: ULPS_ST 101: HS_ST 110: ESP_ST 111: RX_ST
11	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

10:8	R	0x0	LPTX_STA_D2 LPTX Status D2 000: STP_ST 001: HSRQ_ST 010: ESRQ_ST 011: TNRD_ST 100: ULPS_ST 101: HS_ST 110: ESP_ST 111: RX_ST
7	/	/	/
6:4	R	0x0	LPTX_STA_D1 LPTX Status D1 000: STP_ST 001: HSRQ_ST 010: ESRQ_ST 011: TNRD_ST 100: ULPS_ST 101: HS_ST 110: ESP_ST 111: RX_ST
3	/	/	/
2:0	R	0x0	LPTX_STA_D0 LPTX Status D0 000: STP_ST 001: HSRQ_ST 010: ESRQ_ST 011: TNRD_ST 100: ULPS_ST 101: HS_ST 110: ESP_ST 111: RX_ST

15.5.8.23 0x10E4 DPHY Debug 1 Register (Default Value: 0x0000_0000)

Offset: 0x10E4			Register Name: DPHY_DBG1_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DIV_DBG_EN
30	/	/	/
29:28	R/W	0x0	LOCK_STEP
27:22	/	/	/
21	R/W	0x0	LPC_SET
20	R/W	0x0	TURN_DISMODEC
19	R/W	0x0	TURN_DISMODE3

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x10E4			Register Name: DPHY_DBG1_REG
Bit	Read/Write	Default/Hex	Description
18	R/W	0x0	TURN_DISMODE2
17	R/W	0x0	TURN_DISMODE1
16	R/W	0x0	TURN_DISMODE0
15:14	/	/	/
13:12	R/W	0x0	LPTX_SET_CK Clock Lane output state as follow: 00: LP-00 01: LP-01 10: LP-10 11: LP-11
11:10	R/W	0x0	LPTX_SET_D3 Data Lane 3 output state as follow: 00: LP-00 01: LP-01 10: LP-10 11: LP-11
9:8	R/W	0x0	LPTX_SET_D2 Data Lane 2 output state as follow: 00: LP-00 01: LP-01 10: LP-10 11: LP-11
7:6	R/W	0x0	LPTX_SET_D1 Data Lane 1 output state as follow: 00: LP-00 01: LP-01 10: LP-10 11: LP-11
5:4	R/W	0x0	LPTX_SET_D0 Data Lane 0 output state as follow: 00: LP-00 01: LP-01 10: LP-10 11: LP-11
3	/	/	/
2	R/W	0x0	DSI_PRBS_EN
1	R/W	0x0	HSTX_DBG_EN HSTX Debug Enable 0: Normal mode 1: Debug mode

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x10E4			Register Name: DPHY_DBG1_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	LPTX_DBG_EN LPTX Debug Enable 0: Normal mode 1: Debug mode

15.5.8.24 0x10E8 DPHY Debug 2 Register (Default Value: 0x0000_0000)

Offset: 0x10E8			Register Name: DPHY_DBG2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	HSTX_Data Bit31-24: D3_DATA Bit23-16: D2_DATA Bit15-08: D1_DATA Bit07-00: D0_DATA

15.5.8.25 0x10EC DPHY Debug 3 Register (Default Value: 0x0000_0000)

Offset: 0x10EC			Register Name: DPHY_DBG3_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:16	R	0x0	LPRX_STA_CLK LPRX Status Clock 0000: LP00S 0001: LP01S 0010: LP10S 0011: LP11S 0100: TRNDS 0101: HS_S 0110: LPDTS 0111: ESCPS 1000: ULPSS 1001: RSETS 1010: UDF1S 1011: UDF2S 1100: UDF3S 1101: UDF4S 1110: UDF5S Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x10EC			Register Name: DPHY_DBG3_REG
Bit	Read/Write	Default/Hex	Description
15:12	R	0x0	LPRX_STA_D3 LPRX Status D3 0000: LP00S 0001: LP01S 0010: LP10S 0011: LP11S 0100: TRNDS 0101: HS_S 0110: LPDTS 0111: ESCPS 1000: ULPSS 1001: RSETS 1010: UDF1S 1011: UDF2S 1100: UDF3S 1101: UDF4S 1110: UDF5S Others: Reserved
11:8	R	0x0	LPRX_STA_D2 LPRX Status D2 0000: LP00S 0001: LP01S 0010: LP10S 0011: LP11S 0100: TRNDS 0101: HS_S 0110: LPDTS 0111: ESCPS 1000: ULPSS 1001: RSETS 1010: UDF1S 1011: UDF2S 1100: UDF3S 1101: UDF4S 1110: UDF5S Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x10EC			Register Name: DPHY_DBG3_REG
Bit	Read/Write	Default/Hex	Description
7:4	R	0x0	LPRX_STA_D1 LPRX Status D1 0000: LP00S 0001: LP01S 0010: LP10S 0011: LP11S 0100: TRNDS 0101: HS_S 0110: LPDTS 0111: ESCPS 1000: ULPSS 1001: RSETS 1010: UDF1S 1011: UDF2S 1100: UDF3S 1101: UDF4S 1110: UDF5S
3:0	R	0x0	LPRX_STA_D0 LPRX Status D0 0000: LP00S 0001: LP01S 0010: LP10S 0011: LP11S 0100: TRNDS 0101: HS_S 0110: LPDTS 0111: ESCPS 1000: ULPSS 1001: RSETS 1010: UDF1S 1011: UDF2S 1100: UDF3S 1101: UDF4S 1110: UDF5S Others: Reserved

15.5.8.26 0x10F0 DPHY Debug 4 Register (Default Value: 0x0000_0000)

Offset: 0x10F0			Register Name: DPHY_DBG4_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x10F0			Register Name: DPHY_DBG4_REG
Bit	Read/Write	Default/Hex	Description
25:24	R	0x0	LPCD_PHY_CLK LPCD PHY Clock 00: LP-00 01: LP-01 10: LP-10 11: LP-11
23:22	R	0x0	LPCD_PHY_D3 LPCD PHY D3 00: LP-00 01: LP-01 10: LP-10 11: LP-11
21:20	R	0x0	LPCD_PHY_D2 LPCD PHY D2 00: LP-00 01: LP-01 10: LP-10 11: LP-11
19:18	R	0x0	LPCD_PHY_D1 LPCD PHY D1 00: LP-00 01: LP-01 10: LP-10 11: LP-11
17:16	R	0x0	LPCD_PHY_D0 LPCD PHY D0 00: LP-00 01: LP-01 10: LP-10 11: LP-11
15:10	/	/	/
9:8	R	0x0	LPRX_PHY_CLK LPRX PHY Clock 00: LP-00 01: LP-01 10: LP-10 11: LP-11

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x10F0			Register Name: DPHY_DBG4_REG
Bit	Read/Write	Default/Hex	Description
7:6	R	0x0	LPRX_PHY_D3 LPRX PHY D3 00: LP-00 01: LP-01 10: LP-10 11: LP-11
5:4	R	0x0	LPRX_PHY_D2 LPRX PHY D2 00: LP-00 01: LP-01 10: LP-10 11: LP-11
3:2	R	0x0	LPRX_PHY_D1 LPRX PHY D1 00: LP-00 01: LP-01 10: LP-10 11: LP-11
1:0	R	0x0	LPRX_PHY_D0 LPRX PHY D0 00: LP-00 01: LP-01 10: LP-10 11: LP-11

15.5.8.27 0x10F4 DPHY Debug 5 Register (Default Value: 0x0000_0000)

Offset: 0x10F4			Register Name: DPHY_DBG5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	HSRX_DATA Bit31-24: LANE_D3 Bit23-16: LANE_D2 Bit15-08: LANE_D1 Bit07-00: LANE_D0

15.5.8.28 0x10F8 DPHY TX Skew Register0 (Default Value: 0x0000_0000)

Offset: 0x10F8			Register Name: DPHY_TX_SKEW_REG0
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x10F8			Register Name: DPHY_TX_SKEW_REG0
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	SKEWCAL_ZERO_SET HS-Zero duration in Skew Calibration mode, unit: byteclk
23:16	R/W	0x0	SKEWCAL_TRAIL_SET HS-Trail duration in Skew Calibration mode, unit: byteclk
15:8	R/W	0x0	REG_SKEWCAL Clock Pattern Content : 8'b0101_0101 / 8'b1010_1010
7:0	R/W	0x0	reg_skewcal_sync Skewcal sync Pattern Content : 8'b1111_1111

15.5.8.29 0x10FC DPHY TX Skew Register1 (Default Value: 0x0000_0000)

Offset: 0x10FC			Register Name: DPHY_TX_SKEW_REG1
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	SKEWCAL_SYNC_SET SkewCal-Sync Duration, unit: byteclk.
23:16	R/W	0x0	SKEWCAL_PEDIC_SET Periodic Mode SkewCal Duration, unit: byteclk.
15:0	R/W	0x0	SKEWCAL_INIT_SET Initial mode SkewCal Duration, unit: byteclk.

15.5.8.30 0x1100 DPHY TX Skew Register2 (Default Value: 0x0000_0000)

Offset: 0x1100			Register Name: DPHY_TX_SKEW_REG2
Bit	Read/Write	Default/Hex	Description
10	R/W	0x0	EN_SKEWCAL_INIT Enable Skewcal Init
9	R/W	0x0	EN_SKEWCAL_PERDIC Enable Skewcal Perdic
8	R/W	0x0	SKEWCAL_TRAIL_INV Skewcal Trail Inv
7:0	R/W	0x0	SKEWCAL_PREPARE_LP00 LP-00 duration, unit: byteclk.

15.5.8.31 0x1104 DPHY PLL Register0 (Default Value: 0x00C0_3280)

Offset: 0x1104			Register Name: DPHY_PLL_REG0
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1104			Register Name: DPHY_PLL_REG0
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	REG_UPDATE write q update the cfg to pll, auto clear
30	/	/	/
29:28	R/W	0x0	POST_DIV0_CLK_LS M2, post divider0= 1/2/3/4
27:24	R/W	0x0	POST_DIV1_CLK_LS m3, post divider1= m1+1
23	/	/	/
22	R/W	0x1	LDO_EN Enable Signal of 0.9V LDO for V &DV
21	R/W	0x0	EN_LVS Enable Gating For l2h Level_Shift
20	R/W	0x0	PLL_EN Enable Signal for PLL
19:16	R/W	0x0	PRE_DIV p, pre divider = p+1
15:8	R/W	0x32	FB_DIV n, feedback divider = n (4,5,8,9,10,12-255)
7:6	/	/	/
5:4	R/W	0x0	POST_DIV0_CLK_HS m0, post divider0= 1/2/3/4
3:0	R/W	0x0	POST_DIV1_CLK_HS m1, post divider1= m1+1

15.5.8.32 0x1108 DPHY PLL Register1 (Default Value: 0x000f_0480)

Offset: 0x1108			Register Name: DPHY_PLL_REG1
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0xF	PLL_CP Charge Pump Current Adjustment
15:14	R/W	0x0	UNLOCK_MDSEL Unlock Mdsel 00: 21-29 clock cycles 01: 22-28 clock cycles
13	R/W	0x0	LOCKMDSEL Lockmdsel 0: 24-26 clock cycles 1: 23-27 clock cycles

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1108			Register Name: DPHY_PLL_REG1
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	LOCKDET_EN Lockdet Enable 0: Disable 1: Enable
11:9	R/W	0x2	VSETA Reference Voltage Regulation for LDO AV vseta <2:0>: 000: 0.8 V 001: 0.85 V 010: 0.9 V 011: 0.95 V 100: 1.0 V 101: 1.05 V 110: 1.1 V 111: 1.15 V
8:6	R/W	0x5	VSETD Reference Voltage Regulation for LDO DV vsetd<2:0>: 000: 0.8 V 001: 0.85 V 010: 0.9 V 011: 0.95 V 100: 1.0 V 101: 1.05 V 110: 1.1 V 111: 1.15 V
5:3	/	/	/
2:1	R/W	0x3	ATEST_SEL Atest Select 00: DV 01: V 10: ICP 11: VC_OD
0	R/W	0x0	TEST_EN Test Enable For Ck_Test & Ana_Test

15.5.8.33 0x1110 COMBO PHY Register0 (Default Value: 0x0000_1F00)

Offset: 0x1110			Register Name: COMBO_PHY_REG0
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1110			Register Name: COMBO_PHY_REG0
Bit	Read/Write	Default/Hex	Description
12	R/W	0x1	EN_LVDS_CLANE 0: Disable 1: Enable
11:8	R/W	0xf	EN_LVDS_DLANE 0: Disable 1: Enable
7:4	/	/	/
3	R/W	0x0	EN_MIPI MIPI PHY Enable
2	R/W	0x0	EN_LVDS LVDS PHY Enable
1	/	/	/
0	R/W	0x0	EN_CP MIPI LDO test enable

15.5.8.34 0x1114 COMBO PHY Register1 (Default Value: 0x0000_0053)

Offset: 0x1114			Register Name: COMBO_PHY_REG1
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x5	DSI_REG_C Adjust current flowing through Rload of Rx to change the differential signals amplitude. 000: 216mv 001: 252mv 010: 276mv 011: 312mv 100: 336mv 101: 372mv 110: 395mv 111: 432mv
3	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1114			Register Name: COMBO_PHY_REG1
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x3	DSI_REG_R Adjust current flowing through Rload of Rx to change the common signals amplitude. 000: 0.925v 001: 0.950v 010: 0.975v 011: 1.000v 100: 1.025v 101: 1.050v 110: 1.075v 111: 1.100v

15.5.8.35 0x1124 DPHY PLL Register3 (Default Value: 0x0000_0000)

Offset: 0x1124			Register Name: DPHY_PLL_REG3
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R	0x0	pll_cfg Output as DPHY_PLL_REG0[23:0]

15.5.8.36 0x1130 DPHY PLL Patten0 Control Register (Default Value: 0x0000_0000)

Offset: 0x1130			Register Name: DPHY_PLL_PAT0_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode. 00: Reserved 01: Triangular (1bit) 10: Triangular (2bit) 11: Triangular (3bit)
28:20	R/W	0x0	WAVE_STEP Wave STEP
19	R/W	0x0	SDM direction. 0: UP 1: DOWN

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1130			Register Name: DPHY_PLL_PAT0_CTL_REG
Bit	Read/Write	Default/Hex	Description
18:17	R/W	0x0	Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

15.5.8.37 0x1134 DPHY PLL Patten1 Control Register (Default Value: 0x3020_0000)

Offset: 0x1134			Register Name: DPHY_PLL_PAT1_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_PI_EN Fraction PI Enable. 0: Disable 1: Enable
30:28	R/W	0x3	PI bias current control signal
27	R/W	0x0	PLL SDM Enable. 0: Disable 1: Enable
26	R	0x0	SDM Busy Status. 0: Not Busy 1: Busy Note: When Smooth is enable, need to check SDM_BUSY before update SDM parameters. Cannot update parameters if sdm is busy.
25	R/W	0x0	SDM Smooth Enable. 0: Disable 1: Enable
24	R/W	0x0	Dither Enable.
23:22	/	/	/
21	R/W	0x1	VCO_START_ENABLE
20	R/W	0x0	Fraction Enable.
19:17	/	/	/
16:0	R/W	0x3	Fraction In.

15.5.8.38 0x1138 DPHY PLL LFM Register (Default Value: 0x4000_0001)

Offset: 0x1138			Register Name: DPHY_PLL_LFM_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1138			Register Name: DPHY_PLL_LFM_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_LFM_EN 0: Disable 1: Enable
30	R/W	0x1	PLL_LFM_RSTN LFM RSTN bake up
29	R/W	0xCCCA	PLL_LFM_CLK_SEL LFM CLK Select 0: pll_clk_sdm(pll_lock_div) 1: ref_clk
28:12	/	/	/
11:0	R/W	0x0	PLL_LFM_STEP LFM frequency = fclk*fclk*step/2^17. fclk is reference clock frequency at the unit of MHz. The frequency modulation slope rate is MHz/us. 0x001: 0.00439MHz/us (fclk = 24MHz) 0x002: 0.00879MHz/us (fclk = 24MHz) 0x004: 0.01758MHz/us (fclk = 24MHz) 0x008: 0.03516MHz/us (fclk = 24MHz) 0x010: 0.07031MHz/us (fclk = 24MHz) 0x020: 0.14062MHz/us (fclk = 24MHz) 0x040: 0.28125MHz/us (fclk = 24MHz) 0x080: 0.56250MHz/us (fclk = 24MHz) 0x100: 1.12500MHz/us (fclk = 24MHz) 0x200: 2.25000MHz/us (fclk = 24MHz) 0x400: 4.50000MHz/us (fclk = 24MHz) 0x800: 9.00000MHz/us (fclk = 24MHz)

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16 Video Input

16.1 CSIC

16.1.1 Overview

The CMOS Sensor Interface Controller (CSIC) is an image or video data receiver, which can receive image or video data via camera interface. The controller can transfer valid data to embedded ISP or store the data in memory directly.

The CSIC includes the following features:

MIPI CSI

- Supports 4+4+2-lane MIPI interface
  - MIPI PHY A 4 data lane
  - MIPI PHY B 4 data lane
  - MIPI PHY C 2 data lane
- Conforms to MIPI CSI2 V1.1 and MIPI DPHY V1.2. Supports 2.0 Gbit/s per lane
- Supports Crop Function
- Supports Frame Rate Down
- Supports 8M@60fps, size 3264(H) x 2448(V)
- Supports max resolution 3264(H) x 4224(V) (ISP on-line), 5664(H) x 4248(V) (ISP off-line)
- Supports Sensor Fsync

Parallel CSI

- 8/10/12/16-bit width
- Supports DC, BT.656, BT.601, BT.1120 protocol
- DDR sample mode with pixel clock up to 148.5MHz
- BT1120 4CH up to 1080P@30fps
- BT656 4CH up to 4-ch 720P@30fps

BK

- BK0/1 supports up to 20M@30fps or 24M@25fps; BK2/3 supports up to 2.5K@60fps; BK4/5 supports up to 1080P@30fps
- BK supports independent frame-done interrupts. Up to 4 groups, with arbitrary allocation among groups.
- BK0/1/2/3 supports 4-lane time-division multiplexing.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- Supports 6 DMA for 6 video stream storage
- Supports converting interlaced input into progressive output. No anti-aliasing, noise reduction functions.
- Supports conversion for YUV422 to YUV420, YUV422 to YUV400, YUV420 to YUV400
- Supports horizontal and vertical flip for YUV422/YUV420/RAW format

16.1.2 Block Diagram

The following figure shows block diagram of the CSIC.

Figure 16-1 CSIC Block Diagram

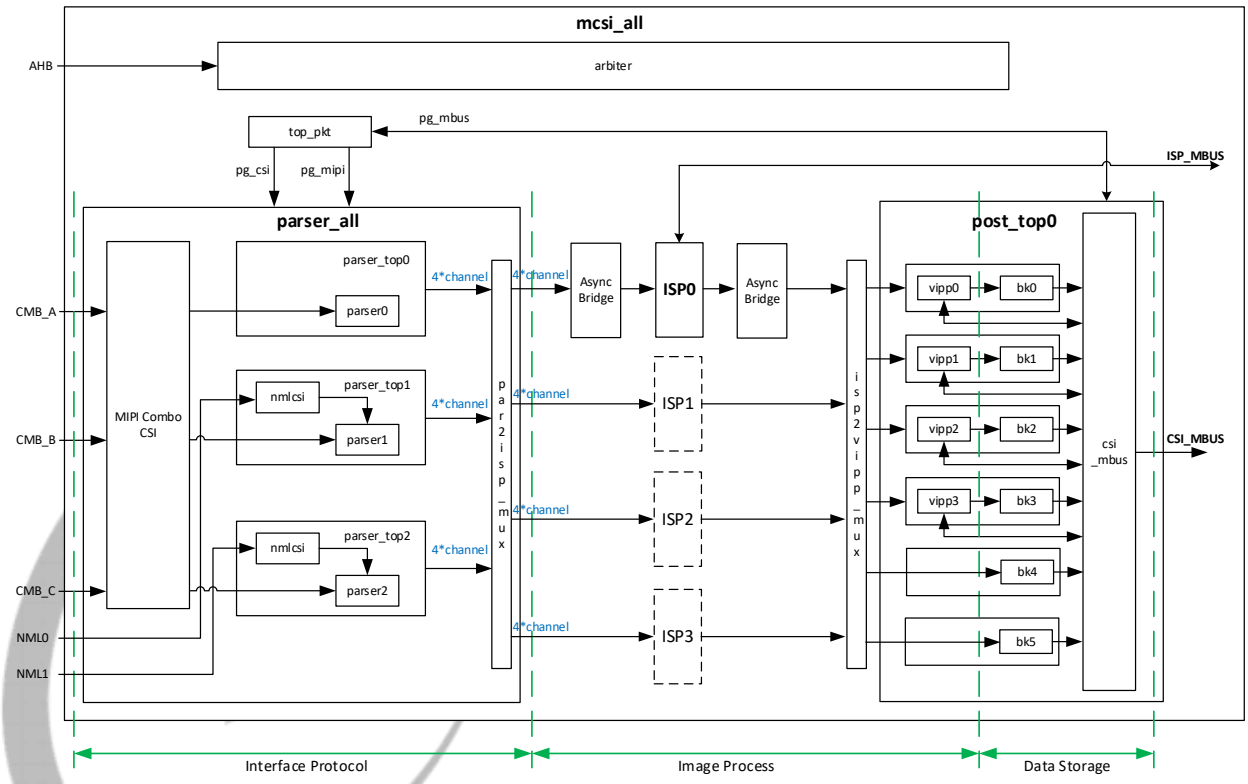


Table 16-1 CSIC Sub-blocks

Sub-blocks	Description
MIPI Combo	Combo is the CMOS input interface module. It supports MIPI CSI RX interface and multiple lane combination modes.
Parser	Parser is used to covert the MIPI data format into internal common format.
nmlcsi	Normal CSI. It is used to receive the digital image input from a digital parallel port, and convert it into the output of AIDB BUS in the mcsi_clk clock domain and parser.
Async Bridge	Asynchronous bridge is used to deal with the problem of clock domain crossing between parser and ISP, ISP and Post.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Sub-blocks	Description
ISP	Image signal Processor. It is used to process the sensor raw data, including lens compensation, and the removal of bad spots, gain, gamma and so on. (ISP1/2/3 is merely used as the data strobe path. Only ISP0 process data)
VIPP	Image post-processing. It can scale down the image.
BK	Write Back. It is used to write the image data back to the controller module of SDRAM.

16.1.3 Clock Sources

The following table describes the clock sources of CSIC. For clock setting, configurations, and gating information, refer to the section Clock Controller Unit (CCU).

Module	Clock Sources	Description
CSI Master0/1/2	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.
	VIDEO0PLL4X	Its frequency is 1188 MHz by default.
	VIDEO0PLL3X	Its frequency is 792 MHz by default.
	VIDEO1PLL4X	Its frequency is 1188 MHz by default.
	VIDEO1PLL3X	Its frequency is 792 MHz by default.
	VIDEO2PLL4X	Its frequency is 1188 MHz by default.
	VIDEO2PLL3X	Its frequency is 792 MHz by default.
CSI	VIDEO2PLL4X	Its frequency is 1188 MHz by default.
	DEPLL4X	Its frequency is 1044 MHz by default.
	PERI0_480M	Its frequency is 480 MHz by default.
	PERI0_400M	Its frequency is 400 MHz by default.
	PERI0_600M	Its frequency is 600 MHz by default.
	VIDEO0PLL4X	Its frequency is 1188 MHz by default.
	VIDEO1PLL4X	Its frequency is 1188 MHz by default.

16.1.4 External Signals

Table 16-2 CSIC External Signals

Signal Name	Description	Type
MIPI CSI		
MCSIA-D[3:0]N	MIPI CSI Controller A Data[3:0] Negative Signal	AI
MCSIA-D[3:0]P	MIPI CSI Controller A Data[3:0] Positive Signal	AI
MCSIA-CKN	MIPI CSI Controller A Clock Negative Signal	AI
MCSIA-CKP	MIPI CSI Controller A Clock Positive Signal	AI
MCSI0-MCLK	Master Clock for MIPI Sensor	O
MCSIB-D[3:0]N	MIPI CSI Controller B Data[3:0] Negative Signal	AI
MCSIB-D[3:0]P	MIPI CSI Controller B Data[3:0] Positive Signal	AI
MCSIB-CKN	MIPI CSI Controller B Clock Negative Signal	AI

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Signal Name	Description	Type
MCSIB-CKP	MIPI CSI Controller B Clock Positive Signal	AI
MCSI1-MCLK	Master Clock for MIPI Sensor	O
MCSIC-D[1:0]N	MIPI CSI Controller C Data[1:0] Negative Signal	AI
MCSIC-D[1:0]P	MIPI CSI Controller C Data[1:0] Positive Signal	AI
MCSIC-CKN	MIPI CSI Controller C Clock Negative Signal	AI
MCSIC-CKP	MIPI CSI Controller C Clock Positive Signal	AI
MCSI2-MCLK	Master Clock for MIPI Sensor	O
VCC-MCSI	Power supply for MIPI CSI	P
Parallel CSI		
NCSI0-MCLK	Parallel CSI Master Clock	O
NCSI0-PCLK	Parallel CSI Pixel Clock	I
NCSI0-HSYNC	Parallel CSI Horizontal Synchronous	I
NCSI0-VSYNC	Parallel CSI Vertical Synchronous	I
NCSI0-D[7:0]	Parallel CSI Data Bit	I
NCSI1-PCLK	Parallel CSI Master Clock	O
NCSI1-MCLK	Parallel CSI Pixel Clock	I
NCSI1-HSYNC	Parallel CSI Horizontal Synchronous	I
NCSI1-VSYNC	Parallel CSI Vertical Synchronous	I
NCSI1-D[15:0]	Parallel CSI Data Bit	I
CSI0-XHS	Sensor External Hsync	I/O
CSI1-XHS	Sensor External Hsync	I/O
CSI0-XVS-FSYNC	CSI Vertical SYNC/Frame SYNC	I/O
CSI1-XVS-FSYNC	CSI Vertical SYNC/Frame SYNC	I/O

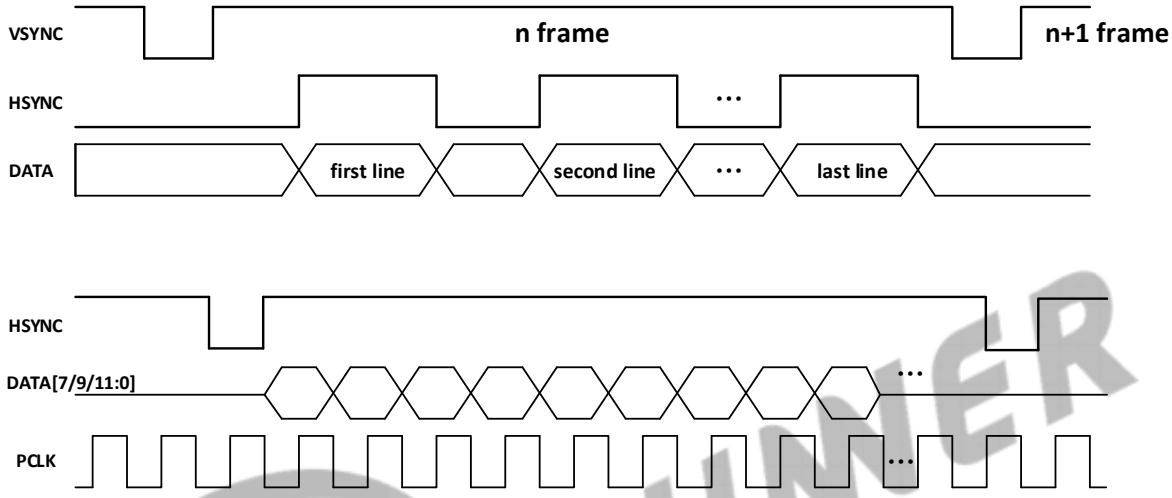
Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.5 Functional Description

16.1.5.1 CSIC Input Timing

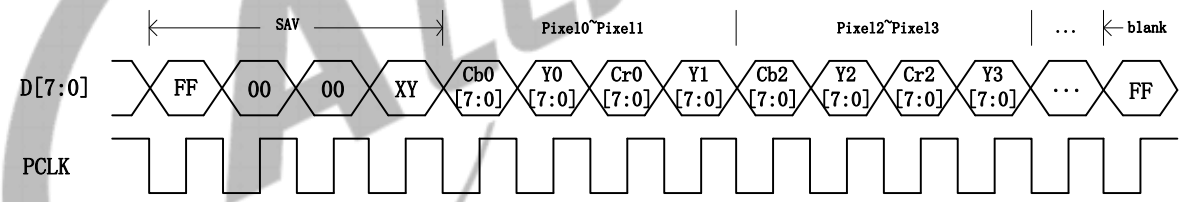
The following figure shows the timing of 8-bit CMOS Sensor Interface. Clock, vsync and hsync is high valid.

Figure 16-2 8-bit DC Sensor Interface Timing



The following figure shows the timing of 8-bit YCbCr4:2:2 with embedded syncs (BT.656).

Figure 16-3 8-bit YCbCr4:2:2 with Embedded Syncs (BT.656)



The following table shows the header code of BT.656.

Table 16-3 BT.656 Header Code

Data Bit	First Word(0xFF)	Second Word(0x00)	Third Word(0x00)	Fourth Word
CS D[7] (MSB)	1	0	0	1
CS D[6]	1	0	0	F
CS D[5]	1	0	0	V
CS D[4]	1	0	0	H
CS D[3]	1	0	0	P3
CS D[2]	1	0	0	P2
CS D[1]	1	0	0	P1
CS D[0]	1	0	0	P0

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

The following table shows the Header Data Bit Definition of BT.656.

Table 16-4 BT.656 Header Data Bit Definition

Decode	F	V	H	P3	P2	P1	P0
Field 1 start of active video (SAV)	0	0	0	0	0	0	0
Field 1 end of active video (EAV)	0	0	1	1	1	0	1
Field 1 SAV (digital blanking)	0	1	0	1	0	1	1
Field 1 EAV (digital blanking)	0	1	1	0	1	1	0
Field 2 SAV	1	0	0	0	1	1	1
Field 2 EAV	1	0	1	1	0	1	0
Field 2 SAV (digital blanking)	1	1	0	1	1	0	0
Field 2 EAV (digital blanking)	1	1	1	0	0	0	1

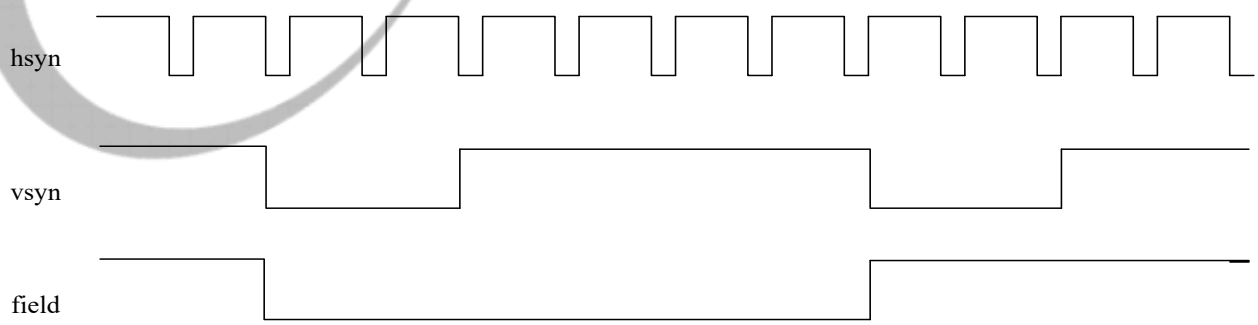
Note: P0-P3 is used for verification in Channel 1 and channel ID marking in Channel 2/4.

Except for 16-bit data width, BT1120 is same to BT656, including EAV and SAV encoding. On the 16-bit data bus of BT1120, the low 8 bits are for transmitting UV components and the high 8 bits are for transmitting Y components, or the low 8 bits are for transmitting Y components and the high 8 bits are for transmitting UV components. In addition, EAV and SAV encoding still use low 8 bits. BT1120 also supports 2-/4-channel time-division multiplexing for image data transmission.

BT601 supports transmitting interlaced YUV422 data with 8-bit signal lines. The information synchronization such as field, vsyn, hsyn is completed with independent signal lines. Different from the standard CSI, its field signals can be embedded in the vsyn signals in the v2f_mode or vsyn signals can be embedded in the field signals in the f2v_mode. Both field and vsyn can exist in the vf_mode.

In the v2f_mode, field signals are obtained from vsyn and hsyn signals. If the vsyn goes down at the falling edge of hsyn, field 0 is obtained; if the vsyn goes down at the rising edge of hsyn, field 1 is obtained.

Figure 16-4 BT601 v2f mode Timing



16.1.5.2 CSIC FIFO Distribution

Table 16-5 CSIC FIFO Distribution

Input format	YUV422/YUV420	Raw

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Input format	YUV422/YUV420		Raw
Output format	Planar	UV combined	Raw
FIFO0	Y	Y	All pixels data
FIFO1	Cb (U)	CbCr (UV)	-
FIFO2	Cr (V)	-	-

16.1.5.3 Pixel Format Arrangement

The following figures show the Pixel Format Arrangement.

Figure 16-5 RAW-8 Format

Raw data 3[7:0]	Raw data 2[7:0]	Raw data 1[7:0]	Raw data 0[7:0]

MSB LSB

Figure 16-6 YUV-8 Format

Y 3[7:0]	Y 2[7:0]	Y 1[7:0]	Y 0[7:0]

MSB LSB

Figure 16-7 UV-Combined Format

V/U 1[7:0]	U/V 1[7:0]	V/U 0[7:0]	U/V 0[7:0]

MSB LSB

16.1.5.4 Offset Definition

Offset in horizontal and vertical can be added when receiving image. Unit is pixel.

- For YUV422 format, pixel unit is a YU/YV combination.
- For YUV420 format, pixel unit is a YU/YV combination in YC line, and only a Y in Y line.
- For Bayer and RAW format, pixel unit is a R/G/B single component.

16.1.5.5 Flip Definition

Both horizontal and vertical flip are supported at the same time. This function is implemented in the process of each FIFO writing data to memory, only flipping the data of separate FIFO, not changing component to FIFO distribution.

If horizontal flip is enabled, one or more pixels will be taken as a unit:

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

For YUV format, a unit of Y0U0Y1V1 will parser and flip the Y component in one channel, and UV will be treated as a whole. In planar output mode, U and V will be flipped separately. In UV combined output mode, UV will be flipped as a whole. So, a sequence of Y1U0Y0V1 will be.

For Bayer_raw format, situation is much like. A GR/BG sequence will be changed to BG/RG. A unit of square has four pixels.

16.1.6 Programming Guidelines

16.1.6.1 Async Bridge Configuration

- If the working clock frequency of ISP is lower than that of parser and post.

Step 1 Configure the field ISP_BRIDGE_EN (bit [3]) of CSIC_TOP_EN_REG as 1 to enable async bridge.

Step 2 Configure the field MCSI_PARSER_CLK_MODE (bit [0]) of CCU_CLK_MODE_REG as 1 to make CSI parser work in CSI clock.

Step 3 Configure the field MCSI_POST_CLK_MODE (bit [1]) of CCU_CLK_MODE_REG as 1 to make CSI post work in CSI clock.

- If the working clock frequency of ISP is same as that of parser and post.

Step 1 Configure the field ISP_BRIDGE_EN (bit [3]) of CSIC_TOP_EN_REG as 1 b0 to disable and bypass async bridge.

Step 2 Configure the field MCSI_PARSER_CLK_MODE (bit [0]) of CCU_CLK_MODE_REG as 0 to make CSI parser work in ISP core clock.

Step 3 Configure the field MCSI_POST_CLK_MODE (bit [1]) of CCU_CLK_MODE_REG as 0 to make CSI post work in ISP core clock.

16.1.6.2 CSI and SDRAM Dynamic Frequency Modulation

Step 1 After the CSIC reset is de-asserted, configure the FACTOR_N and FACTOR_M in the CSIC_CCU_CHFREQ_CLK_CTRL_REG to set the working clock of chfreq. It is 1 MHz by default.

Step 2 Set CHFREQ_CLK_GATING(bit[0]) as 1 in the CSIC_CCU_CHFREQ_CLK_CTRL_REG to enable chfreq_clk.

Step 3 Configure CHFREQ_PAR2ISP_SEL(bit[31:16]) in the CSIC_CHFREQ_CFG0_REG as required by the application.

Step 4 Set CHFREQ_RST[bit0] as 1 in the CSIC_CHFREQ_CFG0_REG to de-assert the dynamic frequency module.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 5 Execute the steps providing that CSI must join dynamic frequency modulation. Set the CHFREQ_ALLOW[bit1] as 1 in the CSIC_CHFREQ_CFG0_REG. Then, enable the corresponding ISPs, VIPPs, and BKs. Prolong the period of DDR dynamic frequency modulation, and then configure the procedure of sensor sending data.

Step 6 Execute the steps providing that the data stream output by the current sensor modes is judged to determine that CSI join dynamic frequency modulation. Set the CHFREQ_RDY_MASK[bit3] as 1 in the CSIC_CHFREQ_CFG0_REG. Prolong the period of DDR dynamic frequency modulation, enable the corresponding ISPs, VIPPs, and then configure sensor the procedure of sensor sending data. Repeatedly read back CHFREQ_FRM_DONE_TIME and CSIC_CHFREQ_OBS_REG (bit[31:16]), and CHFREQ_VBLANK_LENGTH (bit[15:0]) in the CSIC_CHFREQ_OBS_REG to observe their values and stability. Afterwards, determine whether to set CHFREQ_ALLOW (bit[1]) as 1 after considering the period of the DDR dynamic frequency modulation. Then, set CHFREQ_RDY_MASK (bit[3]) as 0 in the CSIC_CHFREQ_CFG0_REG and set the CHFREQ_ALLOW (bit[1]) as 0 or 1 as required.

16.1.6.3 CSI Clock Frequency Configuration

The minimum clock configuration requirements for CSI_CLK are as follows:

One-pixel mode: CSI_CLK = lanespeed/8

Two-pixel mode: CSI_CLK = lanespeed/8/2

Unit: lanespeed – Gbit/s or Mbit/s; CSI_CLK — GHz or MHz

NOTE

Only 4-lane CSI supports two-pixel mode.

16.1.6.4 Interrupt Coalescing and Timestamp Configuration

Step 1 After the CSIC reset is de-asserted, configure the FACTOR_N and FACTOR_M in the CSIC_CCU_CHFREQ_CLK_CTRL_REG to set the working clock of chfreq. It is 1 MHz by default.

Step 2 Set BK_INTPOOL_CLK_GATING (bit[0]) as 1 in the CSIC_CCU_BK_INTPOOL_CLK_CTRL_REG to enable the chfreq_clk.

Step 3 Configure INT_SRC_SEL (bit[1]) of CSIC_BK_INTPOOLx_CFG0_REG to select the source of BK interrupt coalescing. If it is 1 (default configuration), select the VS_INT of BK as the source of BK interrupts; if it is 0, select the FD_INT of BK as the source of BK interrupts.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 4 Configure CSIC_BK_INTPOOLx_CFG0_REG (bit[31:16]) and CSIC_BK_INTPOOLx_CFG1_REG (bit[31:0]) to select the channel source of coalesced interrupts. All the BK channels doesn't coalesce by default. If some channel wants to join interrupt coalescing, set the corresponding SRC_MSK_BK*_CH* as 0.

Step 5 Configure TRIG_MOD (bit[2]) in the CSIC_BK_INTPOOLx_CFG0_REG to select trigger mode. If it is set as 0 (default configuration), the fifo_level trigger mode will be selected. In the mode, fifo level needs to be set. When the number of BK interrupts in the INT FIFO is more than the set value, interrupts will be triggered. After receiving interrupts, the software will get data in the INT fifo. For the following steps, refer to Step 6. If it is set as 1, the target trigger mode will be selected. In the mode, target BK ID and target channel number need to be set. When one interrupt is stored in INT FIFO, whose BK ID is equal to target BK ID and the channel number is equal to the target channel number, an interrupt will be triggered. After receiving interrupts, the software will get data in the INT FIFO. For the following steps, refer to Step 7.

Step 6 Configure FIFO_AVL_INT_EN (bit[0]) in the CSIC_BK_INTPOOLx_INT_EN0_REG to enable FIFO_AVL interrupts. Configure TRIG_LEVEL (bit[9:4]) ranging from 1 to 63 in the CSIC_BK_INTPOOLx_CFG0_REG. Then, configure BK_INT_POOL_EN (bit[0]) as 1 in the CSIC_BK_INTPOOLx_CFG0_REG to dis-assert the reset of BK INT POOL circuit. Afterwards, when the total interrupt number in the INT FIFO is larger than or equal to the set TRIG_LEVEL, report the FIFO_AVL interrupts. If they are received by software, read the CSIC_BK_INT_FIFO_REG for the times of TRIG_LEVEL to obtain the BK interrupts. Then, it is recommended to read again the FIFO_LEVEL (bit[6:0]) in the CSIC_BK_INTPOOL_OBS0_REG to query how many BK interrupts are stored in INT FIFO by hardware in the course of reading CSIC_BK_INT_FIFO_REG. Then, fetch the latest stored interrupts by reading CSIC_BK_INT_FIFO_REG until the FIFO_LEVEL (bit[6:0]) in the CSIC_BK_INTPOOL_OBS0_RE is 0. Then, read the ACCESS_DELAY (bit[15:0]) in the CSIC_BK_INTPOOL_OBS1_REG. Finally, write 1 to FIFO_AVL_INT_PD (bit[0]) in the CSIC_BK_INTPOOL_INT_STA0_REG to clear the pending interrupts. The format of 32-bit data fetched from CSIC_BK_INT_FIFO_REG is {4'h0,Time Stamp Delta (20 bit),2'h0,Channel Number(2 bit),BK ID(4 bit)}. Among them, Time Stamp Delta indicates the time intervals between the currently read interrupt and last read interrupt; Channel Number indicates the channel number of current read interrupt source; BK ID indicates the BK ID of current read interrupt source.

Step 7 Configure FIFO_AVL_INT_EN (bit[0]) in the CSIC_BK_INTPOOLx_INT_EN0_REG to enable FIFO_AVL interrupts. Configure TRIG_ID (bit[13:10]) from 0 to 11 and TRIG_CH (bit[15:14]) from 0 to 3 in the CSIC_BK_INTPOOLx_CFG0_REG. Set BK_INT_POOL_EN (bit[0]) in the CSIC_BK_INTPOOL_CFG0_REG to de-assert the reset of BK INT POOL circuit. Afterwards, when the BK ID is equal to TRIG ID among interrupts stored in the INT FIFO, and channel number is equal to the interrupts of TRIG_CH, report FIFO_AVL interrupts. If they are

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

received by software, read the CSIC_BK_INT_FIFO_REG until the interrupts that BK ID is equal to TRIG_ID and channel number is equal to TRIG_CH. Then, it is recommended to read again the TRIG_TGT_LEVEL (bit[22:16]) in the CSIC_BK_INTPOOLx_OBS0_REG to query how many BK interrupts are stored in INT FIFO by hardware in the course of reading CSIC_BK_INT_FIFO_REG. Then, fetch the latest stored interrupts by reading CSIC_BK_INT_FIFO_REG until the TRIG_TGT_LEVEL (bit[22:16]) in the CSIC_BK_INTPOOL_OBS0_RE is 0. Then, read the ACCESS_DELAY bit[15:0] in the CSIC_BK_INTPOOL_OBS1_REG. Finally, write 1 to FIFO_AVL_INT_PD (bit[0]) in the CSIC_BK_INTPOOL_INT_STA0_REG to clear the pending interrupts.

16.1.6.5 Timestamp Restoration Calculation

For instance, if the TRIG_MOD is set as 0 and FIFO_level is set as 3, the fifo_avl interrupts will be reported when more than 3 BK interrupts are stored in the INT FIFO. Assuming that four interrupts are read by software after reception.

Interrupts	BK ID	Channel Number	Time Stamp Delta	Time interval measured by software
The 1st interrupt	1	0	5	NA
The 2nd interrupt	0	1	6	NA
The 3rd interrupt	2	0	34	NA
The 4th interrupt	1	1	50	1000 us

When the 4th interrupt is read, record the current system time by software, and then read the ACCESS_DELAY bit[15:0] in the CSIC_BK_INTPOOL_OBS1_REG. Assuming that the value of ACCESS_DELAY is 200 us, it indicates that the time interval of the 4th interrupt from being written into INT FITO to being read out is 200 us. Therefore,

The 4th interrupt time is 1000 us – 200 us =800 us

The 3rd interrupt time is 800 us – 50 us = 750 us

The 2nd interrupt time is 750 us – 34 us = 716 us

The 1st interrupt time is 716 us – 6 us = 710 us

You can restore the time stamp successively in the above way.

16.1.6.6 Exception Handling

There are two exception interrupts in the hardware, which are FIFO_FULL_INT in the CSIC_BK_INTPOOL_INT_STA0_REG and BK*_CH*_INT_LOST in the CSIC_BK_INTPOOL_INT_STA0/1_REG.

The FIFO_FULL_INT will be reported in case that the INT FIFO is full. Then, back pressure on the previous stage circuit will occur. Therefore, the interrupts already stored in the INT FIFO will not be overridden by the new interrupts. Once FIFO FULL interrupts are triggered, they should be

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

handled immediately by repeatedly reading CSIC_BK_INT_FIFO_REG and FIFO_LEVEL bit[6:0] in the CSIC_BK_INTPOOL_OBS0_REG to read out the interrupts in the INT FIFO until it is empty. You can restore the time stamp of interrupts when the FIFO is full by reading FULL_ ACCESS_DELAY (bit[31:16]) and taking into consideration of the time of reading the last interrupt recorded by the software.

BK*_CH*_INT_LOST interrupts will be reported when the interrupts of BK and Channel are lost. If the previous interrupt of BK channel is yet to be written into INT FIFO, and a new interrupt is triggered, interrupt lost will occur. This kind of exception needs to be handled immediately, too.

The above exception interrupts can be enabled in the CSIC_BK_INTPOOL_INT_EN0_REG and CSIC_BK_INTPOOL_INT_EN1_REG.

16.1.6.7 BK Image Cache Address Self-refreshing Mode

The steps to configure the BK image buffer address self-refresh mode are as follows:

Step 8 Write 1 to the BUF_ADDR_MODE of the CSIC_DMA_CH3_EN_REG register.

Step 9 Configure the CPU to write plural sets of buffer addresses into the buffer address FIFO.

Step 10 Configure the CSIC_DMA_BUF_ADDR_FIFO_THRESHOLD bit and the CSIC_DMA_STORED_FRM_THRESHOLD bit of the CSIC_DMA_CHx_BUF_TH_REG (x = 0 to 3).

Each time when a new frame of image is input, the hardware will check whether the number of remaining addresses in the buffer FIFO is equal to or less than the threshold set by the CSIC_DMA_BUF_ADDR_FIFO_THRESHOLD bit. If so, an interrupt will be asserted to remind the software to configure a new address; if the hardware checks that the FIFO of the current buffer address is empty, the input data of the current frame will be automatically ignored and a frame loss interrupt will be generated.

Each time when a new frame of image buffering ends, check whether the number of cached images has reached the threshold set by the CSIC_DMA_STORED_FRM_THRESHOLD bit. If so, an interrupt that replaces the frm_done interrupt in the register mode will be generated to remind the software to fetch the cached image data and clear the cached frame counting value.

Notice that every output format (1 FIFO, 2 FIFO, and 3 FIFO) needs to be configured with Y, U, and V addresses in the course of image cache address FIFO configuration. The addresses that will not be used can be configured as 0. In addition, when the cap_done interrupt is asserted after capture, you need to check the CSIC_DMA_STORED_FRM_CNT of the CSIC_DMA_CHx_STORED_FRM_CNT_REG (x = 0 to 3) register to confirm whether there is any cached frame that is yet to reach the threshold set by the CSIC_DMA_STORED_FRM_THRESHOLD bit.

16.1.6.8 Configuration Notes

- The CCU_CLK_GATING_DISABLE bit (bit [31]) of CCU_CLK_MODE_REG register is configured as 0 by default, that is, the clock in CSIC CCU is valid by default.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- The MCSI_POST_CLK_MODE bit (bit [1]) and MCSI_PARSER_CLK_MODE bit (bit [0]) of CCU_CLK_MODE_REG register are configured as 1 by default, that is, CSI clock is selected by default.
- The sequence of CSI reset, CSIC clock enable, and PPU power-on is as follows:

  CSIC reset -> PPU power-on -> CSIC clock enable (including: ISP_Clock, CSI Clock, ISP MCLK, CSI MCLK, CSI BUS GATING, and CSI Master0/1/2/3 Clock)
- There are four soft reset bits for MBUS:

Table 16-6 Soft Reset bits for MBUS

Bits	Registers	Description
MISP_MBUS_RST (bit [9:8], high active)	CCU_ISP_CLK_EN_REG	Reset the MBUS interfaces logic circuit in ISP.
MCSI_POST0_MBUS_RST (bit [21:20], high active)	CSIC_CCU_POST0_CLK_EN_REG	Reset the MBUS interfaces logic circuit in POST0.

16.1.7 Register List

Module Name	Base Address	Comments
CSIC_CCU	0x05800000	CSIC CCU Register
CSIC_TOP	0x05800800	CSIC TOP Register
CSIC_PHY		
PHY_COMMON	0x05810000	
PHYA_DIGITAL_LAYER	0x05810100	
PHYB_DIGITAL_LAYER	0x05810200	PHYB_DIGITAL_LAYER register is the same with PHYA_DIGITAL_LAYER.
PHYC_DIGITAL_LAYER	0x05810300	PHYC_DIGITAL_LAYER register is the same with PHYA_DIGITAL_LAYER.
PORT0_PAYLOAD_LAYER	0x05811000	
PORT1_PAYLOAD_LAYER	0x05811400	PORT1_PAYLOAD_LAYER register is the same with PORT0_PAYLOAD_LAYER.
PORT2_PAYLOAD_LAYER	0x05811800	PORT2_PAYLOAD_LAYER register is the same with PORT0_PAYLOAD_LAYER.
CSIC_ PARSER		
CSIC_PARSER0	0x05820000	CSIC PARSER0 Register
CSIC_PARSER1	0x05821000	CSIC PARSER1 Register is same with CSIC_PARSER0
CSIC_PARSER2	0x05822000	CSIC PARSER2 Register is same with CSIC_PARSER0
CSIC_DMA		
CSIC_DMA0	0x05830000	CSIC DMA0 Register
CSIC_DMA1	0x05831000	CSIC DMA1 Register is same with CSIC_DMA0
CSIC_DMA2	0x05832000	CSIC DMA2 Register is same with CSIC_DMA0
CSIC_DMA3	0x05833000	CSIC DMA3 Register is same with CSIC_DMA0

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Module Name	Base Address	Comments
CSIC_DMA4	0x05834000	CSIC DMA4 Register is same with CSIC_DMA0
CSIC_DMA5	0x05835000	CSIC DMA5 Register is same with CSIC_DMA0

16.1.7.1 CSIC_CCU Register List

Module Name	Base Address	Comments
CSIC_CCU	0x05800000	CSIC CCU Register

Register Name	Offset	Description
CSIC_CCU_CLK_MODE_REG	0x0000	CSIC CCU Clock Mode Register
CSIC_CCU_PARSER_CLK_EN_REG	0x0004	CSIC CCU Parser Clock Enable Register
CCU_ISP_CLK_EN_REG	0x0008	CSIC CCU ISP Clock Enable Register
CSIC_CCU_POST0_CLK_EN_REG	0x000C	CSIC CCU Post0 Clock Enable Register
CSIC_CCU_CHFREQ_CLK_CTRL_REG	0x0014	CSIC CCU Chfreq Clock Control Register
CSIC_CCU_BK_INTPOOL_CLK_CTRL_REG	0x0018	CSIC CCU BK Intpool Clock Control Register

16.1.7.2 CSIC_TOP Register List

Module Name	Base Address	Comments
CSIC_TOP	0x05800800	CSIC TOP Register

Register Name	Offset	Description
CSIC_TOP_EN_REG	0x0000	CSIC TOP Enable Register
CSIC_PTN_GEN_EN_REG	0x0004	CSIC Pattern Generation Enable Register
CSIC_PTN_CTRL_REG	0x0008	CSIC Pattern Control Register
CSIC_PTN_VBLANK_CYCLE	0x0010	CSIC Pattern Vblank Cycle Register
CSIC_PTN_LEN_REG	0x0020	CSIC Pattern Generation Length Register
CSIC_PTN_ADDR_REG	0x0024	CSIC Pattern Generation Address Register
CSIC_PTN_ISP_SIZE_REG	0x0028	CSIC Pattern ISP Size Register
CSIC_ISP0_INPUT0_SEL_REG	0x0030	CSIC ISP0 Input0 Select Register
CSIC_ISP0_INPUT1_SEL_REG	0x0034	CSIC ISP0 Input1 Select Register
CSIC_ISP0_INPUT2_SEL_REG	0x0038	CSIC ISP0 Input2 Select Register
CSIC_ISP0_INPUT3_SEL_REG	0x003C	CSIC ISP0 Input3 Select Register
CSIC_ISP1_INPUT0_SEL_REG	0x0040	CSIC ISP1 Input0 Select Register
CSIC_ISP1_INPUT1_SEL_REG	0x0044	CSIC ISP1 Input1 Select Register
CSIC_ISP1_INPUT2_SEL_REG	0x0048	CSIC ISP1 Input2 Select Register
CSIC_ISP1_INPUT3_SEL_REG	0x004C	CSIC ISP1 Input3 Select Register
CSIC_ISP2_INPUT0_SEL_REG	0x0050	CSIC ISP2 Input0 Select Register
CSIC_ISP2_INPUT1_SEL_REG	0x0054	CSIC ISP2 Input1 Select Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
CSIC_ISP2_INPUT2_SEL_REG	0x0058	CSIC ISP2 Input2 Select Register
CSIC_ISP2_INPUT3_SEL_REG	0x005C	CSIC ISP2 Input3 Select Register
CSIC_ISP3_INPUT0_SEL_REG	0x0060	CSIC ISP3 Input0 Select Register
CSIC_ISP3_INPUT1_SEL_REG	0x0064	CSIC ISP3 Input1 Select Register
CSIC_ISP3_INPUT2_SEL_REG	0x0068	CSIC ISP3 Input2 Select Register
CSIC_ISP3_INPUT3_SEL_REG	0x006C	CSIC ISP3 Input3 Select Register
CSIC_ISP_BRG_BUF_MAXUSE_CNT_CLR_REG	0x0070	CSIC ISP Bridge Buffer Maxuse Counter Clear Register
CSIC_ISP0_BRG01_BUF_MAXUSE_CNT_REG	0x0074	CSIC ISP0 Bridge01 Buffer Maxuse Counter Register
CSIC_ISP0_BRG23_BUF_MAXUSE_CNT_REG	0x0078	CSIC ISP0 Bridge23 Buffer Maxuse Counter Register
CSIC_ISP0_BRG_INT_EN_REG	0x0084	CSIC ISP0 Bridge Interrupt Enable Register
CSIC_ISP0_BRG_INT_PD_REG	0x008C	CSIC ISP0 Bridge Interrupt Pending Register
CSIC_DMA0_INPUT_SEL_REG	0x00A0	CSIC DMA0 Input Select Register
CSIC_DMA1_INPUT_SEL_REG	0x00A4	CSIC DMA1 Input Select Register
CSIC_DMA2_INPUT_SEL_REG	0x00A8	CSIC DMA2 Input Select Register
CSIC_DMA3_INPUT_SEL_REG	0x00AC	CSIC DMA3 Input Select Register
CSIC_DMA4_INPUT_SEL_REG	0x00B0	CSIC DMA4 Input Select Register
CSIC_DMA5_INPUT_SEL_REG	0x00B4	CSIC DMA5 Input Select Register
CSIC_MBUS_REQ_MAX_REG	0x00F0	CSIC MBUS REQ MAX Register
CSIC_MBUS_WAIT_MAX_REG	0x00F8	CSIC MBUS WAIT MAX Register
CSIC_MULF_MOD_REG	0x0100	CSIC Multi-Frame Mode Register
CSIC_MULF_INT_REG	0x0104	CSIC Multi-Frame Interrupt Register
CSIC_CHFREQ_CFG0_REG	0x0108	CSIC Change Frequency Configuration 0 Register
CSIC_CHFREQ_CFG1_REG	0x010C	CSIC Change Frequency Configuration 1 Register
CSIC_CHFREQ_OBS_REG	0x0110	CSIC Change Frequency Observation Register
CSIC_CHFREQ_INT_REG	0x0114	CSIC Change Frequency Interrupt Register
CSIC_CHFREQ_DBG_OBS_REG	0x0118	CSIC Change Frequency Debug Observation Register
CSIC_ISP_BYP_CFG_REG	0x0120	CSIC ISP Bypass Software Configuration Register
CSIC_BK_INTPOOL0_CFG0_REG	0x0130	CSIC BK INTERRUPT Pool0 Configuration 0 Register
CSIC_BK_INTPOOL0_CFG1_REG	0x0134	CSIC BK INTERRUPT Pool0 Configuration 1 Register
CSIC_BK_INT_FIFO0_REG	0x0138	CSIC BK INTERRUPT FIFO0 Register
CSIC_BK_INTPOOL0_OBS0_REG	0x013C	CSIC BK INTERRUPT Pool0 Observation 0 Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
CSIC_BK_INTPOOL0_OBS1_REG	0x0140	CSIC BK INTERRUPT Pool0 Observation 1 Register
CSIC_BK_INTPOOL0_INT_EN0_REG	0x0144	CSIC BK INTERRUPT Pool0 Interrupt Enable 0 Register
CSIC_BK_INTPOOL0_INT_EN1_REG	0x0148	CSIC BK INTERRUPT Pool0 Interrupt Enable 1 Register
CSIC_BK_INTPOOL0_INT_STA0_REG	0x014C	CSIC BK INTERRUPT Pool0 Interrupt Status 0 Register
CSIC_BK_INTPOOL0_INT_STA1_REG	0x0150	CSIC BK INTERRUPT Pool0 Interrupt Status 1 Register
CSIC_BK_INTPOOL1_CFG0_REG	0x0160	CSIC BK INTERRUPT Pool1 Configuration 0 Register
CSIC_BK_INTPOOL1_CFG1_REG	0x0164	CSIC BK INTERRUPT Pool1 Configuration 1 Register
CSIC_BK_INT_FIFO1_REG	0x0168	CSIC BK INTERRUPT FIFO1 Register
CSIC_BK_INTPOOL1_OBS0_REG	0x016C	CSIC BK INTERRUPT Pool1 Observation 0 Register
CSIC_BK_INTPOOL1_OBS1_REG	0x0170	CSIC BK INTERRUPT Pool1 Observation 1 Register
CSIC_BK_INTPOOL1_INT_EN0_REG	0x0174	CSIC BK INTERRUPT Pool1 Interrupt Enable 0 Register
CSIC_BK_INTPOOL1_INT_EN1_REG	0x0178	CSIC BK INTERRUPT Pool1 Interrupt Enable 1 Register
CSIC_BK_INTPOOL1_INT_STA0_REG	0x017C	CSIC BK INTERRUPT Pool1 Interrupt Status 0 Register
CSIC_BK_INTPOOL1_INT_STA1_REG	0x0180	CSIC BK INTERRUPT Pool1 Interrupt Status 1 Register
CSIC_BK_INTPOOL2_CFG0_REG	0x0190	CSIC BK INTERRUPT Pool2 Configuration 0 Register
CSIC_BK_INTPOOL2_CFG1_REG	0x0194	CSIC BK INTERRUPT Pool2 Configuration 1 Register
CSIC_BK_INT_FIFO2_REG	0x0198	CSIC BK INTERRUPT FIFO2 Register
CSIC_BK_INTPOOL2_OBS0_REG	0x019C	CSIC BK INTERRUPT Pool2 Observation 0 Register
CSIC_BK_INTPOOL2_OBS1_REG	0x01A0	CSIC BK INTERRUPT Pool2 Observation 1 Register
CSIC_BK_INTPOOL2_INT_EN0_REG	0x01A4	CSIC BK INTERRUPT Pool2 Interrupt Enable 0 Register
CSIC_BK_INTPOOL2_INT_EN1_REG	0x01A8	CSIC BK INTERRUPT Pool2 Interrupt Enable 1 Register
CSIC_BK_INTPOOL2_INT_STA0_REG	0x01AC	CSIC BK INTERRUPT Pool2 Interrupt Status 0 Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
CSIC_BK_INTPOOL2_INT_STA1_REG	0x01B0	CSIC BK INTERRUPT Pool2 Interrupt Status 1 Register

16.1.7.3 CSIC_PHY Register List

PHY_COMMON

Module Name	Base Address	Comments
PHY_COMMON	0x05810000	

Register Name	Offset	Description
PHY_TOP_CTL_REG	0x0000	PHY Top Control Register
PHY_TRESCAL_REG	0x0004	PHY Terminal Resistor Calibration Register

PHYA_DIGITAL_LAYER

Module Name	Base Address	Comments
PHYA_DIGITAL_LAYER	0x05810100	
PHYB_DIGITAL_LAYER	0x05810200	PHYB_DIGITAL_LAYER register is the same with PHYA_DIGITAL_LAYER.
PHYC_DIGITAL_LAYER	0x05810300	PHYC_DIGITAL_LAYER register is the same with PHYA_DIGITAL_LAYER.

Register Name	Offset	Description
PHY_CTL_REG	0x0000	PHY Control Register
PHY_EQ_REG	0x0004	PHY Equalization Register
PHY_OFSCAL_REG0	0x0008	PHY Offset Calibration Register0
PHY_OFSCAL_REG1	0x000C	PHY Offset Calibration Register1
PHY_OFSCAL_REG2	0x0010	PHY Offset Calibration Register2
PHY_DESKEW_REG0	0x0014	PHY Deskew Register0
PHY_DESKEW_REG1	0x0018	PHY Deskew Register1
PHY_DESKEW_REG2	0x001C	PHY Deskew Register2
PHY_TERM_CTL_REG	0x0020	PHY Terminal Control Register
PHY_HS_CTL_REG	0x0024	PHY High Speed Control Register
PHY_S2P_CTL_REG	0x0028	PHY Serial To Parallel Control Register
PHY_MIPIRX_CTL_REG	0x002C	PHY MIPIRX Control Register
PHY_MIPIRX_SYNC_TIMEOUT_REG	0x0030	PHY MIPIRX Synchronization Timeout Register
PHY_FREQ_CNT_REG	0x0034	PHY Frequency Counter Register
PHY_MIPI_LP_TIMEOUT_REG	0x0038	PHY MIPI LP Timeout Register
PHY_MIPI_ULPSEXIT_REG0	0x0040	PHY MIPI ULPSEXIT Register0

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
PHY_INT_EN_REG	0x0080	PHY Interrupt Enable Register
PHY_INT_PD_REG	0x0084	PHY Interrupt Pending Register
PHY_DESKEW_REG3	0x00E0	PHY Deskew Register3

PORT0_PAYLOAD_LAYER

Module Name	Base Address	Comments
PORT0_PAYLOAD_LAYER	0x05811000	
PORT1_PAYLOAD_LAYER	0x05811400	PORT1_PAYLOAD_LAYER register is the same with PORT0_PAYLOAD_LAYER.
PORT2_PAYLOAD_LAYER	0x05811800	PORT2_PAYLOAD_LAYER register is the same with PORT0_PAYLOAD_LAYER.

Register Name	Offset	Description
PORT_CTL_REG	0x0000	PORT Control Register
PORT_LANE_MAP_REG0	0x0004	PORT Lane Mapping Register0
PORT_WDR_MODE_REG	0x000C	PORT WDR Mode Register
PORT_FID_SEL_REG	0x0010	PORT Frame ID Select Register
PORT_MIPI_CFG_REG	0x0100	PORT MIPI Configuration Register
PORT_MIPI_NO_UNPAK_NUM_REG	0x0104	PORT MIPI No Unpacket Number Register
PORT_MIPI_DI_REG	0x0108	PORT MIPI Data Identity Register
PORT_MIPI_USER_DT_REG	0x010C	PORT MIPI User Data Type Register
PORT_MIPI_CH0_DT_TRIG_EN_REG	0x0110	PORT MIPI Channel0 Data Type Trigger Register
PORT_MIPI_CH0_INT_EN_REG	0x0114	PORT MIPI Channel0 Interrupt Enable Register
PORT_MIPI_CH0_INT_PD_REG	0x0118	PORT MIPI Channel0 Interrupt Pending Register
PORT_MIPI_CH0_PH_REG	0x011C	PORT MIPI Channel0 Packet Header Register
PORT_MIPI_CH0_ECC_REG	0x0120	PORT MIPI Channel0 ECC Register
PORT_MIPI_CH0_CKSUM_REG	0x0124	PORT MIPI Channel0 Checksum Register
PORT_MIPI_CH0_FRM_NUM_REG	0x0128	PORT MIPI Channel0 Frame Number Register
PORT_MIPI_CH0_LINE_NUM_REG	0x012C	PORT MIPI Channel0 Line Number Register
PORT_MIPI_CH1_DT_TRIG_EN_REG	0x0130	PORT MIPI Channel1 Data Type Trigger Register
PORT_MIPI_CH1_INT_EN_REG	0x0134	PORT MIPI Channel1 Interrupt Enable Register
PORT_MIPI_CH1_INT_PD_REG	0x0138	PORT MIPI Channel1 Interrupt Pending Register
PORT_MIPI_CH1_PH_REG	0x013C	PORT MIPI Channel1 Packet Header Register
PORT_MIPI_CH1_ECC_REG	0x0140	PORT MIPI Channel1 ECC Register
PORT_MIPI_CH1_CKSUM_REG	0x0144	PORT MIPI Channel1 Checksum Register
PORT_MIPI_CH1_FRM_NUM_REG	0x0148	PORT MIPI Channel1 Frame Number Register
PORT_MIPI_CH1_LINE_NUM_REG	0x014C	PORT MIPI Channel1 Line Number Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
PORT_MIPI_CH2_DT_TRIG_EN_REG	0x0150	PORT MIPI Channel2 Data Type Trigger Register
PORT_MIPI_CH2_INT_EN_REG	0x0154	PORT MIPI Channel2 Interrupt Enable Register
PORT_MIPI_CH2_INT_PD_REG	0x0158	PORT MIPI Channel2 Interrupt Pending Register
PORT_MIPI_CH2_PH_REG	0x015C	PORT MIPI Channel2 Packet Header Register
PORT_MIPI_CH2_ECC_REG	0x0160	PORT MIPI Channel2 ECC Register
PORT_MIPI_CH2_CKSUM_REG	0x0164	PORT MIPI Channel2 Checksum Register
PORT_MIPI_CH2_FRM_NUM_REG	0x0168	PORT MIPI Channel2 Frame Number Register
PORT_MIPI_CH2_LINE_NUM_REG	0x016C	PORT MIPI Channel2 Line Number Register
PORT_MIPI_CH3_DT_TRIG_EN_REG	0x0170	PORT MIPI Channel3 Data Type Trigger Register
PORT_MIPI_CH3_INT_EN_REG	0x0174	PORT MIPI Channel3 Interrupt Enable Register
PORT_MIPI_CH3_INT_PD_REG	0x0178	PORT MIPI Channel3 Interrupt Pending Register
PORT_MIPI_CH3_PH_REG	0x017C	PORT MIPI Channel3 Packet Header Register
PORT_MIPI_CH3_ECC_REG	0x0180	PORT MIPI Channel3 ECC Register
PORT_MIPI_CH3_CKSUM_REG	0x0184	PORT MIPI Channel3 Checksum Register
PORT_MIPI_CH3_FRM_NUM_REG	0x0188	PORT MIPI Channel3 Frame Number Register
PORT_MIPI_CH3_LINE_NUM_REG	0x018C	PORT MIPI Channel3 Line Number Register
PORT_MIPI_LANE_ERR_INT_EN_REG	0x01F0	PORT MIPI Lane Error Interrupt Register
PORT_MIPI_LANE_ERR_INT_PD_REG	0x01F4	PORT MIPI Lane Error Interrupt Pending Register

16.1.7.4 CSI_PARSER0 Register List

Register Name	Offset	Description
CSIC_PRS_EN_REG	0x0000	CSIC Parser Enable Register
CSIC_PRS_NCSIC_IF_CFG_REG	0x0004	CSIC Parser NCSIC Interface Configuration Register
CSIC_PRS_MCSI_IF_CFG_REG	0x0008	CSIC Parser MCSIC Interface Configuration Register
CSIC_PRS_CAP_REG	0x000C	CSIC Parser Capture Register
CSIC_PRS_SIGNAL_STA_REG	0x0010	CSIC Parser Signal Status Register
CSIC_PRS_NCSIC_BT656_HEAD_CFG_REG	0x0014	CSIC Parser NCSIC BT656 Header Configuration Register
CSIC_PRS_CAP_FRM_MSK_0_REG	0x0018	CSIC Parser Capture Frame Mask 0 Register
CSIC_PRS_CAP_FRM_MSK_1_REG	0x001C	CSIC Parser Capture Frame Mask 1 Register
CSIC_PRS_CH0_IN_DMSK_PERIOD_REG	0x0020	CSIC Parser Channel_0 Input Dmask Setting Register
CSIC_PRS_CH0_INFMT_REG	0x0024	CSIC Parser Channel_0 Input Format Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
CSIC_PRS_CH0_OUTPUT_HSIZE_REG	0x0028	CSIC Parser Channel_0 Output Horizontal Size Register
CSIC_PRS_CH0_OUTPUT_VSIZE_REG	0x002C	CSIC Parser Channel_0 Output Vertical Size Register
CSIC_PRS_CH0_INPUT_PARA0_REG	0x0030	CSIC Parser Channel_0 Input Parameter0 Register
CSIC_PRS_CH0_INPUT_PARA1_REG	0x0034	CSIC Parser Channel_0 Input Parameter1 Register
CSIC_PRS_CH0_INPUT_PARA2_REG	0x0038	CSIC Parser Channel_0 Input Parameter2 Register
CSIC_PRS_CH0_INPUT_PARA3_REG	0x003C	CSIC Parser Channel_0 Input Parameter3 Register
CSIC_PRS_CH0_INT_EN_REG	0x0040	CSIC Parser Channel_0 Interrupt Enable Register
CSIC_PRS_CH0_INT_STA_REG	0x0044	CSIC Parser Channel_0 Interrupt Status Register
CSIC_PRS_CH0_LINE_TIME_REG	0x0048	CSIC Parser Channel_0 Line Time Register
CSIC_PRS_CH0_FRM_PRE_MSK_REG	0x004C	CSIC Parser Channel_0 Frame Pre Mask Setting Register
CSIC_PRS_CH1_IN_DMSK_PERIOD_REG	0x0120	CSIC Parser Channel_1 Input Dmask Setting Register
CSIC_PRS_CH1_INFMT_REG	0x0124	CSIC Parser Channel_1 Input Format Register
CSIC_PRS_CH1_OUTPUT_HSIZE_REG	0x0128	CSIC Parser Channel_1 Output Horizontal Size Register
CSIC_PRS_CH1_OUTPUT_VSIZE_REG	0x012C	CSIC Parser Channel_1 Output Vertical Size Register
CSIC_PRS_CH1_INPUT_PARA0_REG	0x0130	CSIC Parser Channel_1 Input Parameter0 Register
CSIC_PRS_CH1_INPUT_PARA1_REG	0x0134	CSIC Parser Channel_1 Input Parameter1 Register
CSIC_PRS_CH1_INPUT_PARA2_REG	0x0138	CSIC Parser Channel_1 Input Parameter2 Register
CSIC_PRS_CH1_INPUT_PARA3_REG	0x013C	CSIC Parser Channel_1 Input Parameter3 Register
CSIC_PRS_CH1_INT_EN_REG	0x0140	CSIC Parser Channel_1 Interrupt Enable Register
CSIC_PRS_CH1_INT_STA_REG	0x0144	CSIC Parser Channel_1 Interrupt Status Register
CSIC_PRS_CH1_LINE_TIME_REG	0x0148	CSIC Parser Channel_1 Line Time Register
CSIC_PRS_CH1_FRM_PRE_MSK_REG	0x014C	CSIC Parser Channel_1 Frame Pre Mask Setting Register
CSIC_PRS_CH2_IN_DMSK_PERIOD_REG	0x0220	CSIC Parser Channel_2 Input Dmask Setting Register
CSIC_PRS_CH2_INFMT_REG	0x0224	CSIC Parser Channel_2 Input Format Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
CSIC_PRS_CH2_OUTPUT_HSIZE_REG	0x0228	CSIC Parser Channel_2 Output Horizontal Size Register
CSIC_PRS_CH2_OUTPUT_VSIZE_REG	0x022C	CSIC Parser Channel_2 Output Vertical Size Register
CSIC_PRS_CH2_INPUT_PARA0_REG	0x0230	CSIC Parser Channel_2 Input Parameter0 Register
CSIC_PRS_CH2_INPUT_PARA1_REG	0x0234	CSIC Parser Channel_2 Input Parameter1 Register
CSIC_PRS_CH2_INPUT_PARA2_REG	0x0238	CSIC Parser Channel_2 Input Parameter2 Register
CSIC_PRS_CH2_INPUT_PARA3_REG	0x023C	CSIC Parser Channel_2 Input Parameter3 Register
CSIC_PRS_CH2_INT_EN_REG	0x0240	CSIC Parser Channel_2 Interrupt Enable Register
CSIC_PRS_CH2_INT_STA_REG	0x0244	CSIC Parser Channel_2 Interrupt Status Register
CSIC_PRS_CH2_LINE_TIME_REG	0x0248	CSIC Parser Channel_2 Line Time Register
CSIC_PRS_CH2_FRM_PRE_MSK_REG	0x024C	CSIC Parser Channel_2 Frame Pre Mask Setting Register
CSIC_PRS_CH3_IN_DMSK_PERIOD_REG	0x0320	CSIC Parser Channel_3 Input Dmask Setting Register
CSIC_PRS_CH3_INFMT_REG	0x0324	CSIC Parser Channel_3 Input Format Register
CSIC_PRS_CH3_OUTPUT_HSIZE_REG	0x0328	CSIC Parser Channel_3 Output Horizontal Size Register
CSIC_PRS_CH3_OUTPUT_VSIZE_REG	0x032C	CSIC Parser Channel_3 Output Vertical Size Register
CSIC_PRS_CH3_INPUT_PARA0_REG	0x0330	CSIC Parser Channel_3 Input Parameter0 Register
CSIC_PRS_CH3_INPUT_PARA1_REG	0x0334	CSIC Parser Channel_3 Input Parameter1 Register
CSIC_PRS_CH3_INPUT_PARA2_REG	0x0338	CSIC Parser Channel_3 Input Parameter2 Register
CSIC_PRS_CH3_INPUT_PARA3_REG	0x033C	CSIC Parser Channel_3 Input Parameter3 Register
CSIC_PRS_CH3_INT_EN_REG	0x0340	CSIC Parser Channel_3 Interrupt Enable Register
CSIC_PRS_CH3_INT_STA_REG	0x0344	CSIC Parser Channel_3 Interrupt Status Register
CSIC_PRS_CH3_LINE_TIME_REG	0x0348	CSIC Parser Channel_3 Line Time Register
CSIC_PRS_CH3_FRM_PRE_MSK_REG	0x034C	CSIC Parser Channel_3 Frame Pre Mask Setting Register
CSIC_PRS_NCSIC_RX_SIGNAL0_DLY_ADJ_REG	0x0500	CSIC Parser NCSIC RX Signal0 Delay Adjust Register
CSIC_PRS_NCSIC_RX_SIGNAL3_DLY_ADJ_REG	0x050C	CSIC Parser NCSIC RX Signal3 Delay Adjust Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
CSIC_PRS_NCSIC_RX_SIGNAL4_DLY_ADJ_REG	0x0510	CSIC Parser NCSIC RX Signal4 Delay Adjust Register
CSIC_PRS_NCSIC_RX_SIGNAL5_DLY_ADJ_REG	0x0514	CSIC Parser NCSIC RX Signal5 Delay Adjust Register
CSIC_PRS_NCSIC_RX_SIGNAL6_DLY_ADJ_REG	0x0518	CSIC Parser NCSIC RX Signal6 Delay Adjust Register
CSIC_PRS_SYNC_EN_REG	0x0520	CSIC Parser SYNC EN Register
CSIC_PRS_SYNC_CFG_REG	0x0524	CSIC Parser SYNC CFG Register
CSIC_PRS_VS_WAIT_N_REG	0x0528	CSIC Parser VS WAIT N Register
CSIC_PRS_VS_WAIT_M_REG	0x052C	CSIC Parser VS WAIT M Register
CSIC_PRS_XSYNC_ENABLE_REG	0x0540	CSIC Parser XSYNC ENABLE Register
CSIC_PRS_XVS_PERIOD_REG	0x0544	CSIC Parser XVS Period Register
CSIC_PRS_XHS_PERIOD_REG	0x0548	CSIC Parser XHS Period Register
CSIC_PRS_XVS_LENGTH_REG	0x054C	CSIC Parser XVS LENGTH Register
CSIC_PRS_XHS_LENGTH_REG	0x0550	CSIC Parser XHS LENGTH Register
CSIC_PRS_SYNC_DLY_REG	0x0554	CSIC Parser SYNC DELAY Register

16.1.7.5 CSIC_DMA0 Register List

Register Name	Offset	Description
CSIC_DMA_TOP_REG	0x0000	CSIC DMA TOP Register
CSIC_DMA_MUL_CH_CFG_REG	0x0004	CSIC DMA Multi-Channel Configuration Register
CSIC_DMA_FIFO_POINTER_REG	0x0008	CSIC DMA FIFO Pointer Register
CSIC_DMA_WRITE_CNT_REG	0x000C	CSIC DMA Write Counter Register
CSIC_DMA_FRM_CLK_CNT_REG	0x0010	CSIC DMA Frame Rate Clock Counter Register
CSIC_DMA_ACC_ITNL_CLK_CNT_REG	0x0014	CSIC DMA Accumulated and Internal Clock Counter Register
CSIC_DMA_FS_FRM_CNT_REG	0x0020	CSIC DMA Fsync Frame Counter Register
CSIC_DMA_VI_TO_TH0_REG	0x0040	CSIC DMA Video Input Timeout Threshold0 Register
CSIC_DMA_VI_TO_TH1_REG	0x0044	CSIC DMA Video Input Timeout Threshold1 Register
CSIC_DMA_VI_TO_CNT_VAL_REG	0x0048	CSIC DMA Video Input Timeout Counter Value Register
CSIC_DMA_VE_FRM_CNT_REG	0x0050	CSIC DMA VE Frame Counter Value Register
CSIC_DMA_VE_LINE_CNT_REG	0x0054	CSIC DMA VE Line Counter Value Register
CSIC_DMA_VE_CUR_FRM_ADDR_REG	0x0058	CSIC DMA VE Current Frame Address Register
CSIC_DMA_VE_LAST_FRM_ADDR_REG	0x005C	CSIC DMA VE Last Frame Address Register
CSIC_DMA_FIFO_STAT_REG	0x0080	CSIC DMA FIFO Statistic Register
CSIC_DMA_FIFO_THRS_REG	0x0084	CSIC DMA FIFO Threshold Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

CSIC_DMA_TOP_INT_EN_REG	0x0100	CSIC DMA TOP Interrupt Enable Register
CSIC_DMA_TOP_INT_STA_REG	0x0104	CSIC DMA TOP Interrupt Status Register
CSIC_DMA_FEATURE_REG	0x01F4	CSIC DMA Feature List Register
CSIC_DMA_CH0_EN_REG	0x0200	CSIC DMA Channel0 Enable Register
CSIC_DMA_CH0_CFG_REG	0x0204	CSIC DMA Channel0 Configuration Register
CSIC_DMA_CH0_FRM_LOST_CNT_REG	0x0208	CSIC DMA Channel0 Frame Lost Counter Register
CSIC_DMA_CH0_FRM_MSK_CFG_REG	0x020C	CSIC DMA Channel0 Frame Mask Configuration Register
CSIC_DMA_CH0_HSIZE_REG	0x0210	CSIC DMA Channel0 Horizontal Size Register
CSIC_DMA_CH0_VSIZE_REG	0x0214	CSIC DMA Channel0 Vertical Size Register
CSIC_DMA_CH0_VCROP_CFG_REG	0x0218	CSIC DMA Channel0 Vertical Crop Mode Register
CSIC_DMA_CH0_F0_BUFA_REG	0x0220	CSIC DMA Channel0 FIFO 0 Output Buffer-A Address Register
CSIC_DMA_CH0_F0_BUFA_RESULT_REG	0x0224	CSIC DMA Channel0 FIFO 0 Output Buffer-A Address Result Register
CSIC_DMA_CH0_F1_BUFA_REG	0x0228	CSIC DMA Channel0 FIFO 1 Output Buffer-A Address Register
CSIC_DMA_CH0_F1_BUFA_RESULT_REG	0x022C	CSIC DMA Channel0 FIFO 1 Output Buffer-A Address Result Register
CSIC_DMA_CH0_F2_BUFA_REG	0x0230	CSIC DMA Channel0 FIFO 2 Output Buffer-A Address Register
CSIC_DMA_CH0_F2_BUFA_RESULT_REG	0x0234	CSIC DMA Channel0 FIFO 2 Output Buffer-A Address Result Register
CSIC_DMA_CH0_BUF_LEN_REG	0x0238	CSIC DMA Channel0 Buffer Length Register
CSIC_DMA_CH0_FLIP_SIZE_REG	0x023C	CSIC DMA Channel0 Flip Size Register
CSIC_DMA_CH0_CAP_STA_REG	0x024C	CSIC DMA Channel0 Capture Status Register
CSIC_DMA_CH0_INT_EN_REG	0x0250	CSIC DMA Channel0 Interrupt Enable Register
CSIC_DMA_CH0_INT_STA_REG	0x0254	CSIC DMA Channel0 Interrupt Status Register
CSIC_DMA_CH0_LINE_CNT_REG	0x0258	CSIC DMA Channel0 Line Counter Register
CSIC_DMA_CH0_LINE_STAT_REG	0x0268	CSIC DMA Channel0 Line Statistic Register
CSIC_DMA_CH0_PCLK_STAT_REG	0x0270	CSIC DMA Channel0 PCLK Statistic Register
CSIC_DMA_CH0_BUF_ADDR_FIFO0_ENTRY_REG	0x0280	CSIC DMA Channel0 BUF Address FIFO0 Entry Register
CSIC_DMA_CH0_BUF_ADDR_FIFO1_ENTRY_REG	0x0284	CSIC DMA Channel0 BUF Address FIFO1 Entry Register
CSIC_DMA_CH0_BUF_ADDR_FIFO2_ENTRY_REG	0x0288	CSIC DMA Channel0 BUF Address FIFO2 Entry Register
CSIC_DMA_CH0_BUF_TH_REG	0x028C	CSIC DMA Channel0 BUF Threshold Register
CSIC_DMA_CH0_BUF_ADDR_FIFO_CON_REG	0x0290	CSIC DMA Channel0 BUF Address FIFO Content Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

CSIC_DMA_CH0_STORED_FRM_CNT_REG	0x0294	CSIC DMA Channel0 Stored Frame Counter Register
CSIC_DMA_CH0_ABN_MSK_REG	0x0298	CSIC DMA Channel0 Abnormal Mask Register
CSIC_DMA_CH0_PIXELS_ADD_EN_REG	0x029C	CSIC DMA Channel0 Pixels Add Enable Register
CSIC_DMA_CH0_PIXELS_ADD_VAL_REG	0x02A0	CSIC DMA Channel0 Pixels Add Value Register
CSIC_DMA_CH1_EN_REG	0x0400	CSIC DMA Channel1 Enable Register
CSIC_DMA_CH1_CFG_REG	0x0404	CSIC DMA Channel1 Configuration Register
CSIC_DMA_CH1_FRM_LOST_CNT_REG	0x0408	CSIC DMA Channel1 Frame Lost Counter Register
CSIC_DMA_CH1_FRM_MSK_CFG_REG	0x040C	CSIC DMA Channel1 Frame Mask Configuration Register
CSIC_DMA_CH1_HSIZE_REG	0x0410	CSIC DMA Channel1 Horizontal Size Register
CSIC_DMA_CH1_VSIZE_REG	0x0414	CSIC DMA Channel1 Vertical Size Register
CSIC_DMA_CH1_VCROP_CFG_REG	0x0418	CSIC DMA Channel1 Vertical Crop Mode Register
CSIC_DMA_CH1_F0_BUFA_REG	0x0420	CSIC DMA Channel1 FIFO 0 Output Buffer-A Address Register
CSIC_DMA_CH1_F0_BUFA_RESULT_REG	0x0424	CSIC DMA Channel1 FIFO 0 Output Buffer-A Address Result Register
CSIC_DMA_CH1_F1_BUFA_REG	0x0428	CSIC DMA Channel1 FIFO 1 Output Buffer-A Address Register
CSIC_DMA_CH1_F1_BUFA_RESULT_REG	0x042C	CSIC DMA Channel1 FIFO 1 Output Buffer-A Address Result Register
CSIC_DMA_CH1_F2_BUFA_REG	0x0430	CSIC DMA Channel1 FIFO 2 Output Buffer-A Address Register
CSIC_DMA_CH1_F2_BUFA_RESULT_REG	0x0434	CSIC DMA Channel1 FIFO 2 Output Buffer-A Address Result Register
CSIC_DMA_CH1_BUF_LEN_REG	0x0438	CSIC DMA Channel1 Buffer Length Register
CSIC_DMA_CH1_FLIP_SIZE_REG	0x043C	CSIC DMA Channel1 Flip Size Register
CSIC_DMA_CH1_CAP_STA_REG	0x044C	CSIC DMA Channel1 Capture Status Register
CSIC_DMA_CH1_INT_EN_REG	0x0450	CSIC DMA Channel1 Interrupt Enable Register
CSIC_DMA_CH1_INT_STA_REG	0x0454	CSIC DMA Channel1 Interrupt Status Register
CSIC_DMA_CH1_LINE_CNT_REG	0x0458	CSIC DMA Channel1 Line Counter Register
CSIC_DMA_CH1_LINE_STAT_REG	0x0468	CSIC DMA Channel1 Line Statistic Register
CSIC_DMA_CH1_PCLK_STAT_REG	0x0470	CSIC DMA Channel1 PCLK Statistic Register
CSIC_DMA_CH1_BUF_ADDR_FIFO0_ENTRY_REG	0x0480	CSIC DMA Channel1 BUF Address FIFO0 Entry Register
CSIC_DMA_CH1_BUF_ADDR_FIFO1_ENTRY_REG	0x0484	CSIC DMA Channel1 BUF Address FIFO1 Entry Register
CSIC_DMA_CH1_BUF_ADDR_FIFO2_ENTRY_REG	0x0488	CSIC DMA Channel1 BUF Address FIFO2 Entry Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

CSIC_DMA_CH1_BUF_TH_REG	0x048C	CSIC DMA Channel1 BUF Threshold Register
CSIC_DMA_CH1_BUF_ADDR_FIFO_CON_REG	0x0490	CSIC DMA Channel1 BUF Address FIFO Content Register
CSIC_DMA_CH1_STORED_FRM_CNT_REG	0x0494	CSIC DMA Channel1 Stored Frame Counter Register
CSIC_DMA_CH1_ABN_MSK_REG	0x0498	CSIC DMA Channel1 Abnormal Mask Register
CSIC_DMA_CH1_PIXELS_ADD_EN_REG	0x049C	CSIC DMA Channel1 Pixels Add Enable Register
CSIC_DMA_CH1_PIXELS_ADD_VAL_REG	0x04A0	CSIC DMA Channel1 Pixels Add Value Register
CSIC_DMA_CH2_EN_REG	0x0600	CSIC DMA Channel2 Enable Register
CSIC_DMA_CH2_CFG_REG	0x0604	CSIC DMA Channel2 Configuration Register
CSIC_DMA_CH2_FRM_LOST_CNT_REG	0x0608	CSIC DMA Channel2 Frame Lost Counter Register
CSIC_DMA_CH2_FRM_MSK_CFG_REG	0x060C	CSIC DMA Channel2 Frame Mask Configuration Register
CSIC_DMA_CH2_HSIZE_REG	0x0610	CSIC DMA Channel2 Horizontal Size Register
CSIC_DMA_CH2_VSIZE_REG	0x0614	CSIC DMA Channel2 Vertical Size Register
CSIC_DMA_CH2_VCROP_CFG_REG	0x0618	CSIC DMA Channel2 Vertical Crop Mode Register
CSIC_DMA_CH2_F0_BUFA_REG	0x0620	CSIC DMA Channel2 FIFO 0 Output Buffer-A Address Register
CSIC_DMA_CH2_F0_BUFA_RESULT_REG	0x0624	CSIC DMA Channel2 FIFO 0 Output Buffer-A Address Result Register
CSIC_DMA_CH2_F1_BUFA_REG	0x0628	CSIC DMA Channel2 FIFO 1 Output Buffer-A Address Register
CSIC_DMA_CH2_F1_BUFA_RESULT_REG	0x062C	CSIC DMA Channel2 FIFO 1 Output Buffer-A Address Result Register
CSIC_DMA_CH2_F2_BUFA_REG	0x0630	CSIC DMA Channel2 FIFO 2 Output Buffer-A Address Register
CSIC_DMA_CH2_F2_BUFA_RESULT_REG	0x0634	CSIC DMA Channel2 FIFO 2 Output Buffer-A Address Result Register
CSIC_DMA_CH2_BUF_LEN_REG	0x0638	CSIC DMA Channel2 Buffer Length Register
CSIC_DMA_CH2_FLIP_SIZE_REG	0x063C	CSIC DMA Channel2 Flip Size Register
CSIC_DMA_CH2_CAP_STA_REG	0x064C	CSIC DMA Channel2 Capture Status Register
CSIC_DMA_CH2_INT_EN_REG	0x0650	CSIC DMA Channel2 Interrupt Enable Register
CSIC_DMA_CH2_INT_STA_REG	0x0654	CSIC DMA Channel2 Interrupt Status Register
CSIC_DMA_CH2_LINE_CNT_REG	0x0658	CSIC DMA Channel2 Line Counter Register
CSIC_DMA_CH2_LINE_STAT_REG	0x0668	CSIC DMA Channel2 Line Statistic Register
CSIC_DMA_CH2_PCLK_STAT_REG	0x0670	CSIC DMA Channel2 PCLK Statistic Register
CSIC_DMA_CH2_BUF_ADDR_FIFO0_ENTRY_REG	0x0680	CSIC DMA Channel2 BUF Address FIFO0 Entry Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

CSIC_DMA_CH2_BUF_ADDR_FIFO1_ENTRY_REG	0x0684	CSIC DMA Channel2 BUF Address FIFO1 Entry Register
CSIC_DMA_CH2_BUF_ADDR_FIFO2_ENTRY_REG	0x0688	CSIC DMA Channel2 BUF Address FIFO2 Entry Register
CSIC_DMA_CH2_BUF_TH_REG	0x068C	CSIC DMA Channel2 BUF Threshold Register
CSIC_DMA_CH2_BUF_ADDR_FIFO_CON_REG	0x0690	CSIC DMA Channel2 BUF Address FIFO Content Register
CSIC_DMA_CH2_STORED_FRM_CNT_REG	0x0694	CSIC DMA Channel2 Stored Frame Counter Register
CSIC_DMA_CH2_ABN_MSK_REG	0x0698	CSIC DMA Channel2 Abnormal Mask Register
CSIC_DMA_CH2_PIXELS_ADD_EN_REG	0x069C	CSIC DMA Channel2 Pixels Add Enable Register
CSIC_DMA_CH2_PIXELS_ADD_VAL_REG	0x06A0	CSIC DMA Channel2 Pixels Add Value Register
CSIC_DMA_CH3_EN_REG	0x0800	CSIC DMA Channel3 Enable Register
CSIC_DMA_CH3_CFG_REG	0x0804	CSIC DMA Channel3 Configuration Register
CSIC_DMA_CH3_FRM_LOST_CNT_REG	0x0808	CSIC DMA Channel3 Frame Lost Counter Register
CSIC_DMA_CH3_FRM_MSK_CFG_REG	0x080C	CSIC DMA Channel3 Frame Mask Configuration Register
CSIC_DMA_CH3_HSIZE_REG	0x0810	CSIC DMA Channel3 Horizontal Size Register
CSIC_DMA_CH3_VSIZE_REG	0x0814	CSIC DMA Channel3 Vertical Size Register
CSIC_DMA_CH3_VCROP_CFG_REG	0x0818	CSIC DMA Channel3 Vertical Crop Mode Register
CSIC_DMA_CH3_F0_BUFA_REG	0x0820	CSIC DMA Channel3 FIFO 0 Output Buffer-A Address Register
CSIC_DMA_CH3_F0_BUFA_RESULT_REG	0x0824	CSIC DMA Channel3 FIFO 0 Output Buffer-A Address Result Register
CSIC_DMA_CH3_F1_BUFA_REG	0x0828	CSIC DMA Channel3 FIFO 1 Output Buffer-A Address Register
CSIC_DMA_CH3_F1_BUFA_RESULT_REG	0x082C	CSIC DMA Channel3 FIFO 1 Output Buffer-A Address Result Register
CSIC_DMA_CH3_F2_BUFA_REG	0x0830	CSIC DMA Channel3 FIFO 2 Output Buffer-A Address Register
CSIC_DMA_CH3_F2_BUFA_RESULT_REG	0x0834	CSIC DMA Channel3 FIFO 2 Output Buffer-A Address Result Register
CSIC_DMA_CH3_BUF_LEN_REG	0x0838	CSIC DMA Channel3 Buffer Length Register
CSIC_DMA_CH3_FLIP_SIZE_REG	0x083C	CSIC DMA Channel3 Flip Size Register
CSIC_DMA_CH3_CAP_STA_REG	0x084C	CSIC DMA Channel3 Capture Status Register
CSIC_DMA_CH3_INT_EN_REG	0x0850	CSIC DMA Channel3 Interrupt Enable Register
CSIC_DMA_CH3_INT_STA_REG	0x0854	CSIC DMA Channel3 Interrupt Status Register
CSIC_DMA_CH3_LINE_CNT_REG	0x0858	CSIC DMA Channel3 Line Counter Register
CSIC_DMA_CH3_LINE_STAT_REG	0x0868	CSIC DMA Channel3 Line Statistic Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

CSIC_DMA_CH3_PCLK_STAT_REG	0x0870	CSIC DMA Channel3 PCLK Statistic Register
CSIC_DMA_CH3_BUF_ADDR_FIFO0_ENTRY_REG	0x0880	CSIC DMA Channel3 BUF Address FIFO0 Entry Register
CSIC_DMA_CH3_BUF_ADDR_FIFO1_ENTRY_REG	0x0884	CSIC DMA Channel3 BUF Address FIFO1 Entry Register
CSIC_DMA_CH3_BUF_ADDR_FIFO2_ENTRY_REG	0x0888	CSIC DMA Channel3 BUF Address FIFO2 Entry Register
CSIC_DMA_CH3_BUF_TH_REG	0x088C	CSIC DMA Channel3 BUF Threshold Register
CSIC_DMA_CH3_BUF_ADDR_FIFO_CON_REG	0x0890	CSIC DMA Channel3 BUF Address FIFO Content Register
CSIC_DMA_CH3_STORED_FRM_CNT_REG	0x0894	CSIC DMA Channel3 Stored Frame Counter Register
CSIC_DMA_CH3_ABN_MSK_REG	0x0898	CSIC DMA Channel3 Abnormal Mask Register
CSIC_DMA_CH3_PIXELS_ADD_EN_REG	0x089C	CSIC DMA Channel3 Pixels Add Enable Register
CSIC_DMA_CH3_PIXELS_ADD_VAL_REG	0x08A0	CSIC DMA Channel3 Pixels Add Value Register

16.1.8 CSIC CCU Register Description

16.1.8.1 0x0000 CSIC CCU Clock Mode Register (Default Value: 0x0000_0003)

Offset: 0x0000			Register Name: CSIC_CCU_CLK_MODE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CCU_CLK_GATING_DISABLE CCU Clock Gating Disable 0: CCU Clock Gating Registers(0x0004~0x0010) takes effect 1: CCU Clock Gating Registers(0x0004~0x0010) has no effect
30:2	/	/	/
1	R/W	0x1	MCSI_POST_CLK_MODE MCSI Post Clock Mode 0: CSI Post works in isp core clock 1: CSI Post works in csi clock
0	R/W	0x1	MCSI_PARSER_CLK_MODE MCSI Parser Clock Mode 0: CSI Parser works in isp core clock 1: CSI Parser works in csi clock

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.8.2 0x0004 CSIC CCU Parser Clock Enable Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: CSIC_CCU_PARSER_CLK_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	MCSI_COMBO0_CLK_ENABLE MCSI Combo0 Clock Enable 0: Combo0 clock disable 1: Combo0 clock enable
7:3	/	/	/
2	R/W	0x0	MCSI_PARSER2_CLK_ENABLE MCSI Parser2 clock gating 0: CSI Parser2 clock disable 1: CSI Parser2 clock enable
1	R/W	0x0	MCSI_PARSER1_CLK_ENABLE MCSI Parser0 clock gating 0: CSI Parser1 clock disable 1: CSI Parser1 clock enable
0	R/W	0x0	MCSI_PARSER0_CLK_ENABLE MCSI Parser1 clock gating Parser0 clock gating 0: CSI Parser0 clock disable 1: CSI Parser0 clock enable

16.1.8.3 0x0008 CSIC CCU ISP Clock Enable Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CCU_ISP_CLK_EN_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20	R/W	0x0	MISP0_BRIDGE_CH_CLK_GATING_DISABLE Async Bridge Channel Clock Gating Disable 0: Async Bridge channel 0~3 Registers (MISP0_F2S0_BRIDGE_CH_CLK_EN and MISP0_S2F0_BRIDGE_CH_CLK_EN) effect 1: Async Bridge channel 0~3 Registers (MISP0_F2S0_BRIDGE_CH_CLK_EN and MISP0_S2F0_BRIDGE_CH_CLK_EN) not effect

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: CCU_ISP_CLK_EN_REG
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0x0	MISP0_S2F0_BRIDGE_CH_CLK_EN Async Bridge channel 0~3 from isp to post clock enable Bit[16]: channel0,Bit[17]:channel1,Bit[18]:channel2,Bit[19]:channel3 0: Disable 1: Enable
15:12	R/W	0x0	MISP0_F2S0_BRIDGE_CH_CLK_EN Async Bridge channel 0~3 from parser to isp clock enable Bit[12]:channel0,Bit[13]:channel1,Bit[14]:channel2,Bit[15]:channel3 0: Disable 1: Enable
11:10	/	/	/
9	R/W	0x0	MISP_MBUS_MEM_RST MISP Mbus Mem Reset 0: ISP0 mbus mem reset de-assert 1: ISP0 mbus mem reset assert
8	R/W	0x0	MISP_MBUS_VE_RST MISP Mbus Ve Reset 0: ISP0 mbus ve reset de-assert 1: ISP0 mbus ve reset assert
7:5	/	/	/
4	R/W	0x0	MISP0_BRIDGE_CLK_ENABLE MISP Bridge Clock Enable 0: ISP0 bridge clock disable 1: ISP0 bridge clock enable
3:1	/	/	/
0	R/W	0x0	MISP0_CLK_ENABLE MISP Clock Enable 0: ISP0 clock disable 1: ISP0 clock enable

16.1.8.4 0x000C CSIC CCU Post0 Clock Enable Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: CSIC_CCU_POST0_CLK_EN_REG
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x000C			Register Name: CSIC_CCU_POST0_CLK_EN_REG
Bit	Read/Write	Default/Hex	Description
21	R/W	0x0	MCSI_POST0_MBUS_MEM_RST MCSI Post0 Mbus Mem Reset 0: POST0 mbus mem reset de-assert 1: POST0 mbus mem reset assert
20	R/W	0x0	MCSI_POST0_MBUS_VE_RST MCSI Post0 Mbus Ve Reset 0: POST0 mbus ve reset de-assert 1: POST0 mbus ve reset assert
19:17	/	/	/
16	R/W	0x0	MCSI_POST0_CLK_ENABLE Post0 clock gating 0: POST0 clock disable 1: POST0 clock enable
15:12	/	/	/
11	R/W	0x0	MCSI_VIPP3_CLK_ENABLE VIPP3 Clock Gating 0: VIPP3 clock disable 1: VIPP3 clock enable, when MCSI_POST0_CLK_ENABLE is 1
10	R/W	0x0	MCSI_VIPP2_CLK_ENABLE VIPP2 Clock Gating 0: VIPP2 clock disable 1: VIPP2 clock enable, when MCSI_POST0_CLK_ENABLE is 1
9	R/W	0x0	MCSI_VIPP1_CLK_ENABLE VIPP1 Clock Gating 0: VIPP1 clock disable 1: VIPP1 clock enable, when MCSI_POST0_CLK_ENABLE is 1
8	R/W	0x0	MCSI_VIPP0_CLK_ENABLE VIPP0 Clock Gating 0: VIPP0 clock disable 1: VIPP0 clock enable, when MCSI_POST0_CLK_ENABLE is 1
7:6	/	/	/
5	R/W	0x0	MCSI_BK5_CLK_ENABLE BK5 Clock Gating 0: BK5 clock disable 1: BK5 clock enable, when MCSI_POST0_CLK_ENABLE is 1

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x000C			Register Name: CSIC_CCU_POST0_CLK_EN_REG
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	MCSI_BK4_CLK_ENABLE BK4 Clock Gating 0: BK4 clock disable 1: BK4 clock enable, when MCSI_POST0_CLK_ENABLE is 1
3	R/W	0x0	MCSI_BK3_CLK_ENABLE BK3 Clock Gating 0: BK3 clock disable 1: BK3 clock enable, when MCSI_POST0_CLK_ENABLE is 1
2	R/W	0x0	MCSI_BK2_CLK_ENABLE BK2 Clock Gating 0: BK2 clock disable 1: BK2 clock enable, when MCSI_POST0_CLK_ENABLE is 1
1	R/W	0x0	MCSI_BK1_CLK_ENABLE BK1 Clock Gating BK1 clock gating 0: BK1 clock disable 1: BK1 clock enable, when MCSI_POST0_CLK_ENABLE is 1
0	R/W	0x0	MCSI_BK0_CLK_ENABLE BK0 Clock Gating BK0 clock gating 0: BK0 clock disable 1: BK0 clock enable, when MCSI_POST0_CLK_ENABLE is 1

16.1.8.5 0x0014 CSIC CCU Chfreq Clock Control Register (Default Value: 0x0000_1700)

Offset: 0x0014			Register Name: CSIC_CCU_CHFREQ_CLK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x00	FACTOR_N Factor N N= FACTOR_N +1. FACTOR_N is from 0 to 31
15:13	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: CSIC_CCU_CHFREQ_CLK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
12:8	R/W	0x17	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31
7:1	/	/	/
0	R/W	0x0	CHFREQ_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON CHFREQ_CLK = Clock Source/M/N. Clock Source is clk24m.

16.1.8.6 0x0018 CSIC CCU BK Intpool Clock Control Register (Default Value: 0x0000_1700)

Offset: 0x0018			Register Name: CSIC_CCU_BK_INTPOOL_CLK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x00	FACTOR_N Factor N N= FACTOR_N +1. FACTOR_N is from 0 to 31
15:13	/	/	/
12:8	R/W	0x17	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31
7:1	/	/	/
0	R/W	0x0	BK_INTPOOL_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON BK_INTPOOL_CLK = Clock Source/M/N. Clock Source is clk24m.

16.1.9 CSIC TOP Register Description

16.1.9.1 0x0000 CSIC TOP Enable Register (Default Value: 0x0000_0000)

Offset: 0x0000	Register Name: CSIC_TOP_EN_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VER_EN CSIC Version Register Read Enable: 0: Disable 1: Enable
30:21	/	/	/
20	R/W	0x0	ISP_BRIDGE_CH_EN_DISABLE ISP Async Bridge Channel Disable 0: Async Bridge channel 0~3 Registers (ISP_S2F0_BRIDGE_CH_EN and ISP_F2S0_BRIDGE_CH_EN) effect 1: Async Bridge channel 0~3 Registers (ISP_S2F0_BRIDGE_CH_EN and ISP_F2S0_BRIDGE_CH_EN) not effect
19:16	R/W	0x0	ISP_S2F0_BRIDGE_CH_EN Enable Async Bridge channel 0~3 from isp to post, when isp uses different clock source from csi_top_clk. Bit [16]: channel0, Bit[17]: channel1,Bit[18]:channel2,Bit[19]:channel3 0: Disable 1: Enable
15:12	R/W	0x0	ISP_F2S0_BRIDGE_CH_EN Enable Async Bridge channel 0~3 from parser to isp, when isp uses different clock source from csi_top_clk. Bit[12]:channel0,Bit[13]:channel1,Bit[14]:channel2,Bit[15]:channel3 0: Disable 1: Enable
11:4	/	/	/
3	R/W	0x0	ISP_BRIDGE_EN Enable Async Bridge from parser to isp and isp to post, when isp uses different clock source from csi_top_clk 0: Disable 1: Enable
2:0	/	/	/

16.1.9.2 0x0004 CSIC Pattern Generation Enable Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: CSIC_PTN_GEN_EN_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: CSIC_PTN_GEN_EN_REG
Bit	Read/Write	Default/Hex	Description
23:16	R/W	0x0	PTN_CYCLE Pattern generating cycle counter. The pattern in dram will be generated in cycles of PTN_CYCLE+1.
15:5	/	/	/
4	R/WAC	0x0	PTN_START CSIC Pattern Generating Start 0: Finish other: Start Software write this bit to "1" to start pattern generating from DRAM. When finished, the hardware will clear this bit to "0" automatically. Generating cycles depends on PTN_CYCLE.
3:1	/	/	/
0	R/W	0x0	PTN_GEN_EN Pattern Generation Enable

16.1.9.3 0x0008 CSIC Pattern Control Register (Default Value: 0x0000_000F)

Offset: 0x0008			Register Name: CSIC_PTN_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	PTN_PORT_SEL Pattern Generator output port selection 101: NCSIC3 110: COMBO others: Reserved
23:22	/	/	/
21:20	R/W	0x0	PTN_GEN_DATA_WIDTH Pattern Generator output data width 00: 8bit 01: 10bit 10: 12bit 11:reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: CSIC_PTN_CTRL_REG
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0x0	PTN_MODE Pattern mode selection 0000: mipi 1-lane 0001: mipi 2-lane 0010: mipi 3-lane 0011: mipi 4-lane 0100: NCSIC with max 12-bit data {field,vsyn,hsyn,1'b0,data[11:0]} 0101: NCSIC with max 16-bit data {12'h0,field,vsyn,hsyn,1'b0,data[15:0]} 0110: NCSIC with max 24-bit data {field,vsyn,hsyn,5'h0,data[23:0]} 0111: Reserved 1000: BT656 8 bits' width 1001: BT656 16 bits' width 1010: BT656 24 bits' width 1011: Reserved 1100: BAYER 12 bits for ISPFE 1101: UYVY422 12 bits for ISPFE 1110: UYVY420 12 bits for ISPFE 1111: Reserved
15:10	/	/	/
9:8	R/W	0x0	PTN_GEN_CLK_DIV Packet generator clock divider
7:0	R/W	0xF	PTN_GEN_DLY Clocks delayed before pattern generating start.

16.1.9.4 0x0010 CSIC Pattern Vblank Cycle Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CSIC_PTN_VBLANK_CYCLE
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	PTN_VBLANK_CYCLE Set clock cycles between two patterns as vblank

16.1.9.5 0x0020 CSIC Pattern Generation Length Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: CSIC_PTN_LEN_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PTN_LEN The pattern length in byte when generating pattern.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.9.6 0x0024 CSIC Pattern Generation Address Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: CSIC_PTN_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PTN_ADDR The pattern DRAM address when generating pattern.

16.1.9.7 0x0028 CSIC Pattern ISP Size Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: CSIC_PTN_ISP_SIZE_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	Height Vertical size, only valid for ISP mode pattern generation.
15:13	/	/	/
12:0	R/W	0x0	Width Horizontal size, only valid for ISP mode pattern generation.

16.1.9.8 0x0030 CSIC ISP0 Input0 Select Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: CSIC_ISP0_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0030			Register Name: CSIC_ISP0_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	ISP0_INPUT0_SEL ISP0 Input0 select 0000: Input from Parser0 CH0 0001: Input from Parser0 CH1 0010: Input from Parser0 CH2 0011: Input from Parser0 CH3 0100: Input from Parser1 CH0 0101: Input from Parser1 CH1 0110: Input from Parser1 CH2 0111: Input from Parser1 CH3 1000: Input from Parser2 CH0 1001: Input from Parser2 CH1 1010: Input from Parser2 CH2 1011: Input from Parser2 CH3 1100: Input from Parser3 CH0 1101: Input from Parser3 CH1 1110: Input from Parser3 CH2 1111: Input from Parser3 CH3 Others: Reserved

16.1.9.9 0x0034 CSIC ISP0 Input1 Select Register (Default Value: 0x0000_0001)

Offset: 0x0034			Register Name: CSIC_ISP0_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0034			Register Name: CSIC_ISP0_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x1	ISP0_INPUT1_SEL ISP0 Input1 select 0000: Input from Parser0 CH0 0001: Input from Parser0 CH1 0010: Input from Parser0 CH2 0011: Input from Parser0 CH3 0100: Input from Parser1 CH0 0101: Input from Parser1 CH1 0110: Input from Parser1 CH2 0111: Input from Parser1 CH3 1000: Input from Parser2 CH0 1001: Input from Parser2 CH1 1010: Input from Parser2 CH2 1011: Input from Parser2 CH3 1100: Input from Parser3 CH0 1101: Input from Parser3 CH1 1110: Input from Parser3 CH2 1111: Input from Parser3 CH3 Others: Reserved

16.1.9.10 0x0038 CSIC ISP0 Input2 Select Register (Default Value: 0x0000_0002)

Offset: 0x0038			Register Name: CSIC_ISP0_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0038			Register Name: CSIC_ISP0_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x2	ISP0_INPUT2_SEL ISP0 Input2 select 0000: Input from Parser0 CH0 0001: Input from Parser0 CH1 0010: Input from Parser0 CH2 0011: Input from Parser0 CH3 0100: Input from Parser1 CH0 0101: Input from Parser1 CH1 0110: Input from Parser1 CH2 0111: Input from Parser1 CH3 1000: Input from Parser2 CH0 1001: Input from Parser2 CH1 1010: Input from Parser2 CH2 1011: Input from Parser2 CH3 1100: Input from Parser3 CH0 1101: Input from Parser3 CH1 1110: Input from Parser3 CH2 1111: Input from Parser3 CH3 Others: Reserved

16.1.9.11 0x003C CSIC ISP0 Input3 Select Register (Default Value: 0x0000_0003)

Offset: 0x003C			Register Name: CSIC_ISP0_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x003C			Register Name: CSIC_ISP0_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x3	ISP0_INPUT3_SEL ISP0 Input3 select 0000: Input from Parser0 CH0 0001: Input from Parser0 CH1 0010: Input from Parser0 CH2 0011: Input from Parser0 CH3 0100: Input from Parser1 CH0 0101: Input from Parser1 CH1 0110: Input from Parser1 CH2 0111: Input from Parser1 CH3 1000: Input from Parser2 CH0 1001: Input from Parser2 CH1 1010: Input from Parser2 CH2 1011: Input from Parser2 CH3 1100: Input from Parser3 CH0 1101: Input from Parser3 CH1 1110: Input from Parser3 CH2 1111: Input from Parser3 CH3 Others: Reserved

16.1.9.12 0x0040 CSIC ISP1 Input0 Select Register (Default Value: 0x0000_0004)

Offset: 0x0040			Register Name: CSIC_ISP1_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0040			Register Name: CSIC_ISP1_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x4	ISP1_INPUT0_SEL ISP1 Input0 select (note that no ISP1 exists, ISP1 is a virtual concept here and referring to a pass-through channel) 0000: Input from Parser0 CH0 0001: Input from Parser0 CH1 0010: Input from Parser0 CH2 0011: Input from Parser0 CH3 0100: Input from Parser1 CH0 0101: Input from Parser1 CH1 0110: Input from Parser1 CH2 0111: Input from Parser1 CH3 1000: Input from Parser2 CH0 1001: Input from Parser2 CH1 1010: Input from Parser2 CH2 1011: Input from Parser2 CH3 1100: Input from Parser3 CH0 1101: Input from Parser3 CH1 1110: Input from Parser3 CH2 1111: Input from Parser3 CH3

16.1.9.13 0x0044 CSIC ISP1 Input1 Select Register (Default Value: 0x0000_0005)

Offset: 0x0044			Register Name: CSIC_ISP1_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0044			Register Name: CSIC_ISP1_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x5	ISP1_INPUT1_SEL ISP1 Input1 select (note that no ISP1 exists, ISP1 is a virtual concept here and referring to a pass-through channel) 0000: Input from Parser0 CH0 0001: Input from Parser0 CH1 0010: Input from Parser0 CH2 0011: Input from Parser0 CH3 0100: Input from Parser1 CH0 0101: Input from Parser1 CH1 0110: Input from Parser1 CH2 0111: Input from Parser1 CH3 1000: Input from Parser2 CH0 1001: Input from Parser2 CH1 1010: Input from Parser2 CH2 1011: Input from Parser2 CH3 1100: Input from Parser3 CH0 1101: Input from Parser3 CH1 1110: Input from Parser3 CH2 1111: Input from Parser3 CH3

16.1.9.14 0x0048 CSIC ISP1 Input2 Select Register (Default Value: 0x0000_0006)

Offset: 0x0048			Register Name: CSIC_ISP1_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0048			Register Name: CSIC_ISP1_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x6	ISP1_INPUT2_SEL ISP1 Input2 select (note that no ISP1 exists, ISP1 is a virtual concept here and referring to a pass-through channel) 0000: Input from Parser0 CH0 0001: Input from Parser0 CH1 0010: Input from Parser0 CH2 0011: Input from Parser0 CH3 0100: Input from Parser1 CH0 0101: Input from Parser1 CH1 0110: Input from Parser1 CH2 0111: Input from Parser1 CH3 1000: Input from Parser2 CH0 1001: Input from Parser2 CH1 1010: Input from Parser2 CH2 1011: Input from Parser2 CH3 1100: Input from Parser3 CH0 1101: Input from Parser3 CH1 1110: Input from Parser3 CH2 1111: Input from Parser3 CH3

16.1.9.15 0x004C CSIC ISP1 Input3 Select Register (Default Value: 0x0000_0007)

Offset: 0x004C			Register Name: CSIC_ISP1_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x004C			Register Name: CSIC_ISP1_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x7	ISP1_INPUT3_SEL ISP1 Input3 select (note that no ISP1 exists, ISP1 is a virtual concept here and referring to a pass-through channel) 0000: Input from Parser0 CH0 0001: Input from Parser0 CH1 0010: Input from Parser0 CH2 0011: Input from Parser0 CH3 0100: Input from Parser1 CH0 0101: Input from Parser1 CH1 0110: Input from Parser1 CH2 0111: Input from Parser1 CH3 1000: Input from Parser2 CH0 1001: Input from Parser2 CH1 1010: Input from Parser2 CH2 1011: Input from Parser2 CH3 1100: Input from Parser3 CH0 1101: Input from Parser3 CH1 1110: Input from Parser3 CH2 1111: Input from Parser3 CH3

16.1.9.16 0x0050 CSIC ISP2 Input0 Select Register (Default Value: 0x0000_0008)

Offset: 0x0050			Register Name: CSIC_ISP2_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0050			Register Name: CSIC_ISP2_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x8	ISP2_INPUT0_SEL ISP2 Input0 select (note that no ISP2 exists, ISP2 is a virtual concept here and referring to a pass-through channel) 0000: Input from Parser0 CH0 0001: Input from Parser0 CH1 0010: Input from Parser0 CH2 0011: Input from Parser0 CH3 0100: Input from Parser1 CH0 0101: Input from Parser1 CH1 0110: Input from Parser1 CH2 0111: Input from Parser1 CH3 1000: Input from Parser2 CH0 1001: Input from Parser2 CH1 1010: Input from Parser2 CH2 1011: Input from Parser2 CH3 1100: Input from Parser3 CH0 1101: Input from Parser3 CH1 1110: Input from Parser3 CH2 1111: Input from Parser3 CH3

16.1.9.17 0x0054 CSIC ISP2 Input1 Select Register (Default Value: 0x0000_0009)

Offset: 0x0054			Register Name: CSIC_ISP2_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0054			Register Name: CSIC_ISP2_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x9	ISP2_INPUT1_SEL ISP2 Input1 select (note that no ISP2 exists, ISP2 is a virtual concept here and referring to a pass-through channel) 0000: Input from Parser0 CH0 0001: Input from Parser0 CH1 0010: Input from Parser0 CH2 0011: Input from Parser0 CH3 0100: Input from Parser1 CH0 0101: Input from Parser1 CH1 0110: Input from Parser1 CH2 0111: Input from Parser1 CH3 1000: Input from Parser2 CH0 1001: Input from Parser2 CH1 1010: Input from Parser2 CH2 1011: Input from Parser2 CH3 1100: Input from Parser3 CH0 1101: Input from Parser3 CH1 1110: Input from Parser3 CH2 1111: Input from Parser3 CH3

16.1.9.18 0x0058 CSIC ISP2 Input2 Select Register (Default Value: 0x0000_000a)

Offset: 0x0058			Register Name: CSIC_ISP2_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0058			Register Name: CSIC_ISP2_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xa	ISP2_INPUT2_SEL ISP2 Input2 select (note that no ISP2 exists, ISP2 is a virtual concept here and referring to a pass-through channel) 0000: Input from Parser0 CH0 0001: Input from Parser0 CH1 0010: Input from Parser0 CH2 0011: Input from Parser0 CH3 0100: Input from Parser1 CH0 0101: Input from Parser1 CH1 0110: Input from Parser1 CH2 0111: Input from Parser1 CH3 1000: Input from Parser2 CH0 1001: Input from Parser2 CH1 1010: Input from Parser2 CH2 1011: Input from Parser2 CH3 1100: Input from Parser3 CH0 1101: Input from Parser3 CH1 1110: Input from Parser3 CH2 1111: Input from Parser3 CH3

16.1.9.19 0x005C CSIC ISP2 Input3 Select Register (Default Value: 0x0000_000b)

Offset: 0x005C			Register Name: CSIC_ISP2_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x005C			Register Name: CSIC_ISP2_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xb	ISP2_INPUT3_SEL ISP2 Input3 select (note that no ISP2 exists, ISP2 is a virtual concept here and referring to a pass-through channel) 0000: Input from Parser0 CH0 0001: Input from Parser0 CH1 0010: Input from Parser0 CH2 0011: Input from Parser0 CH3 0100: Input from Parser1 CH0 0101: Input from Parser1 CH1 0110: Input from Parser1 CH2 0111: Input from Parser1 CH3 1000: Input from Parser2 CH0 1001: Input from Parser2 CH1 1010: Input from Parser2 CH2 1011: Input from Parser2 CH3 1100: Input from Parser3 CH0 1101: Input from Parser3 CH1 1110: Input from Parser3 CH2 1111: Input from Parser3 CH3

16.1.9.20 0x0060 CSIC ISP3 Input0 Select Register (Default Value: 0x0000_000c)

Offset: 0x0060			Register Name: CSIC_ISP3_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0060			Register Name: CSIC_ISP3_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xc	ISP3_INPUT0_SEL ISP3 Input0 select (note that no ISP3 exists, ISP3 is a virtual concept here and referring to a pass-through channel) 0000: Input from Parser0 CH0 0001: Input from Parser0 CH1 0010: Input from Parser0 CH2 0011: Input from Parser0 CH3 0100: Input from Parser1 CH0 0101: Input from Parser1 CH1 0110: Input from Parser1 CH2 0111: Input from Parser1 CH3 1000: Input from Parser2 CH0 1001: Input from Parser2 CH1 1010: Input from Parser2 CH2 1011: Input from Parser2 CH3 1100: Input from Parser3 CH0 1101: Input from Parser3 CH1 1110: Input from Parser3 CH2 1111: Input from Parser3 CH3

16.1.9.21 0x0064 CSIC ISP3 Input1 Select Register (Default Value: 0x0000_000d)

Offset: 0x0064			Register Name: CSIC_ISP3_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0064			Register Name: CSIC_ISP3_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xd	ISP3_INPUT1_SEL ISP3 Input1 select (note that no ISP3 exists, ISP3 is a virtual concept here and referring to a pass-through channel) 0000: Input from Parser0 CH0 0001: Input from Parser0 CH1 0010: Input from Parser0 CH2 0011: Input from Parser0 CH3 0100: Input from Parser1 CH0 0101: Input from Parser1 CH1 0110: Input from Parser1 CH2 0111: Input from Parser1 CH3 1000: Input from Parser2 CH0 1001: Input from Parser2 CH1 1010: Input from Parser2 CH2 1011: Input from Parser2 CH3 1100: Input from Parser3 CH0 1101: Input from Parser3 CH1 1110: Input from Parser3 CH2 1111: Input from Parser3 CH3

16.1.9.22 0x0068 CSIC ISP3 Input2 Select Register (Default Value: 0x0000_000e)

Offset: 0x0068			Register Name: CSIC_ISP3_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0068			Register Name: CSIC_ISP3_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xe	ISP3_INPUT2_SEL ISP3 Input2 select (note that no ISP3 exists, ISP3 is a virtual concept here and referring to a pass-through channel) 0000: Input from Parser0 CH0 0001: Input from Parser0 CH1 0010: Input from Parser0 CH2 0011: Input from Parser0 CH3 0100: Input from Parser1 CH0 0101: Input from Parser1 CH1 0110: Input from Parser1 CH2 0111: Input from Parser1 CH3 1000: Input from Parser2 CH0 1001: Input from Parser2 CH1 1010: Input from Parser2 CH2 1011: Input from Parser2 CH3 1100: Input from Parser3 CH0 1101: Input from Parser3 CH1 1110: Input from Parser3 CH2 1111: Input from Parser3 CH3

16.1.9.23 0x006C CSIC ISP3 Input3 Select Register (Default Value: 0x0000_000f)

Offset: 0x006C			Register Name: CSIC_ISP3_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x006C			Register Name: CSIC_ISP3_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xf	ISP3_INPUT3_SEL ISP3 Input3 select (note that no ISP3 exists, ISP3 is a virtual concept here and referring to a pass-through channel) 0000: Input from Parser0 CH0 0001: Input from Parser0 CH1 0010: Input from Parser0 CH2 0011: Input from Parser0 CH3 0100: Input from Parser1 CH0 0101: Input from Parser1 CH1 0110: Input from Parser1 CH2 0111: Input from Parser1 CH3 1000: Input from Parser2 CH0 1001: Input from Parser2 CH1 1010: Input from Parser2 CH2 1011: Input from Parser2 CH3 1100: Input from Parser3 CH0 1101: Input from Parser3 CH1 1110: Input from Parser3 CH2 1111: Input from Parser3 CH3

16.1.9.24 0x0070 CSIC ISP Bridge Buffer Maxuse Counter Clear Register (Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: CSIC_ISP_BRG_BUF_MAXUSE_CNT_CLR_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	ISP0_BRG3_BUF_MAXUSE_CNT_CLR ISP0 Bridge3 Buffer Maxuse Count Clear 0: No effect 1: Clear
2	R/W	0x0	ISP0_BRG2_BUF_MAXUSE_CNT_CLR ISP0 Bridge2 Buffer Maxuse Count Clear 0: No effect 1: Clear
1	R/W	0x0	ISP0_BRG1_BUF_MAXUSE_CNT_CLR ISP0 Bridge1 Buffer Maxuse Count Clear 0: No effect 1: Clear

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0070			Register Name: CSIC_ISP_BRG_BUF_MAXUSE_CNT_CLR_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	ISP0_BRG0_BUF_MAXUSE_CNT_CLR ISP0 Bridge0 Buffer Maxuse Count Clear 0: No effect 1: Clear

16.1.9.25 0x0074 CSIC ISP0 Bridge01 Buffer Maxuse Counter Register (Default Value: 0x0000_0000)

Offset: 0x0074			Register Name: CSIC_ISP0_BRG01_BUF_MAXUSE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	ISP0_BRG1_BUF_MAXUSE_CNT ISP0 Bridge1 Buffer Maxuse Counter
15:0	R	0x0	ISP0_BRG0_BUF_MAXUSE_CNT ISP0 Bridge0 Buffer Maxuse Counter

16.1.9.26 0x0078 CSIC ISP0 Bridge23 Buffer Maxuse Counter Register (Default Value: 0x0000_0000)

Offset: 0x0078			Register Name: CSIC_ISP0_BRG23_BUF_MAXUSE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	ISP0_BRG3_BUF_MAXUSE_CNT ISP0 Bridge3 Buffer Maxuse Counter
15:0	R	0x0	ISP0_BRG2_BUF_MAXUSE_CNT ISP0 Bridge2 Buffer Maxuse Counter

16.1.9.27 0x0084 CSIC ISP0 Bridge Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: CSIC_ISP0_BRG_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R/W	0x0	ISP0_BRG3_S2F_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge3 Slow to Fast Side
26	R/W	0x0	ISP0_BRG2_S2F_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge2 Slow to Fast Side
25	R/W	0x0	ISP0_BRG1_S2F_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge1 Slow to Fast Side

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0084			Register Name: CSIC_ISP0_BRG_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
24	R/W	0x0	ISP0_BRG0_S2F_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge0 Slow to Fast Side
23:20	/	/	/
19	R/W	0x0	ISP0_BRG3_F2S_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge3 Fast to Slow Side
18	R/W	0x0	ISP0_BRG2_F2S_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge2 Fast to Slow Side
17	R/W	0x0	ISP0_BRG1_F2S_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge1 Fast to Slow Side
16	R/W	0x0	ISP0_BRG0_F2S_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge0 Fast to Slow Side
15:12	/	/	/
11	R/W	0x0	ISP0_BRG3_BUF_OV_INT_EN ISP0 Bridge3 Buffer overflow interrupt enable
10	R/W	0x0	ISP0_BRG2_BUF_OV_INT_EN ISP0 Bridge2 Buffer overflow interrupt enable
9	R/W	0x0	ISP0_BRG1_BUF_OV_INT_EN ISP0 Bridge1 Buffer overflow interrupt enable
8	R/W	0x0	ISP0_BRG0_BUF_OV_INT_EN ISP0 Bridge0 Buffer overflow interrupt enable
7:4	/	/	/
3	R/W	0x0	ISP0_BRG3_RS_INT_EN ISP0 Bridge3 Read clock too slow interrupt enable
2	R/W	0x0	ISP0_BRG2_RS_INT_EN ISP0 Bridge2 Read clock too slow interrupt enable
1	R/W	0x0	ISP0_BRG1_RS_INT_EN ISP0 Bridge1 Read clock too slow interrupt enable
0	R/W	0x0	ISP0_BRG0_RS_INT_EN ISP0 Bridge0 Read clock too slow interrupt enable

16.1.9.28 0x008C CSIC ISP0 Bridge Interrupt Pending Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: CSIC_ISP0_BRG_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x008C			Register Name: CSIC_ISP0_BRG_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
27	R/W1C	0x0	ISP0_BRG3_S2F_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge3 Slow to Fast Side
26	R/W1C	0x0	ISP0_BRG2_S2F_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge2 Slow to Fast Side
25	R/W1C	0x0	ISP0_BRG1_S2F_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge1 Slow to Fast Side
24	R/W1C	0x0	ISP0_BRG0_S2F_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge0 Slow to Fast Side
23:20	/	/	/
19	R/W1C	0x0	ISP0_BRG3_F2S_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge3 Fast to Slow Side
18	R/W1C	0x0	ISP0_BRG2_F2S_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge2 Fast to Slow Side
17	R/W1C	0x0	ISP0_BRG1_F2S_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge1 Fast to Slow Side
16	R/W1C	0x0	ISP0_BRG0_F2S_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge0 Fast to Slow Side
15:12	/	/	/
11	R/W1C	0x0	ISP0_BRG3_BUF_OV_INT_PD ISP0 Bridge3 Buffer overflow interrupt pending
10	R/W1C	0x0	ISP0_BRG2_BUF_OV_INT_PD ISP0 Bridge2 Buffer overflow interrupt pending
9	R/W1C	0x0	ISP0_BRG1_BUF_OV_INT_PD ISP0 Bridge1 Buffer overflow interrupt pending
8	R/W1C	0x0	ISP0_BRG0_BUF_OV_INT_PD ISP0 Bridge0 Buffer overflow interrupt pending
7:4	/	/	/
3	R/W1C	0x0	ISP0_BRG3_RS_INT_PD ISP0 Bridge3 Read clock too slow interrupt pending
2	R/W1C	0x0	ISP0_BRG2_RS_INT_PD ISP0 Bridge2 Read clock too slow interrupt pending
1	R/W1C	0x0	ISP0_BRG1_RS_INT_PD ISP0 Bridge1 Read clock too slow interrupt pending

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x008C			Register Name: CSIC_ISP0_BRG_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
0	R/W1C	0x0	ISP0_BRG0_RS_INT_PD ISP0 Bridge0 Read clock too slow interrupt pending

16.1.9.29 0x00A0 CSIC DMA0 Input Select Register (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: CSIC_DMA0_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	DMA0_INPUT_SEL DMA0 Input select 0000: Input from ISP0 CH0 0001: Input from ISP0 CH1 0010: Input from ISP0 CH2 0011: Input from ISP0 CH3 0100: Input from ISP1 CH0 0101: Input from ISP1 CH1 0110: Input from ISP1 CH2 0111: Input from ISP1 CH3 1000: Input from ISP2 CH0 1001: Input from ISP2 CH1 1010: Input from ISP2 CH2 1011: Input from ISP2 CH3 1100: Input from ISP3 CH0 1101: Input from ISP3 CH1 1110: Input from ISP3 CH2 1111: Input from ISP3 CH3 NOTE: no ISP1/2/3 exists, ISP1/2/3 is a virtual concept here and referring to a pass-through channel. Should be configured together with CSIC_ISP1/2/3_INPUT0/1/2/3_SEL_REG

16.1.9.30 0x00A4 CSIC DMA1 Input Select Register (Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: CSIC_DMA1_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00A4			Register Name: CSIC_DMA1_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	DMA1_INPUT_SEL DMA1 Input select 0000: Input from ISP0 CH0 0001: Input from ISP0 CH1 0010: Input from ISP0 CH2 0011: Input from ISP0 CH3 0100: Input from ISP1 CH0 0101: Input from ISP1 CH1 0110: Input from ISP1 CH2 0111: Input from ISP1 CH3 1000: Input from ISP2 CH0 1001: Input from ISP2 CH1 1010: Input from ISP2 CH2 1011: Input from ISP2 CH3 1100: Input from ISP3 CH0 1101: Input from ISP3 CH1 1110: Input from ISP3 CH2 1111: Input from ISP3 CH3 NOTE: no ISP1/2/3 exists, ISP1/2/3 is a virtual concept here and referring to a pass-through channel. Should be configured together with CSIC_ISP1/2/3_INPUT0/1/2/3_SEL_REG

16.1.9.31 0x00A8 CSIC DMA2 Input Select Register (Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: CSIC_DMA2_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00A8			Register Name: CSIC_DMA2_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	DMA2_INPUT_SEL DMA2 Input select 0000: Input from ISP0 CH0 0001: Input from ISP0 CH1 0010: Input from ISP0 CH2 0011: Input from ISP0 CH3 0100: Input from ISP1 CH0 0101: Input from ISP1 CH1 0110: Input from ISP1 CH2 0111: Input from ISP1 CH3 1000: Input from ISP2 CH0 1001: Input from ISP2 CH1 1010: Input from ISP2 CH2 1011: Input from ISP2 CH3 1100: Input from ISP3 CH0 1101: Input from ISP3 CH1 1110: Input from ISP3 CH2 1111: Input from ISP3 CH3 NOTE: no ISP1/2/3 exists, ISP1/2/3 is a virtual concept here and referring to a pass-through channel. Should be configured together with CSIC_ISP1/2/3_INPUT0/1/2/3_SEL_REG

16.1.9.32 0x00AC CSIC DMA3 Input Select Register (Default Value: 0x0000_0000)

Offset: 0x00AC			Register Name: CSIC_DMA3_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00AC			Register Name: CSIC_DMA3_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	DMA3_INPUT_SEL DMA3 Input select 0000: Input from ISP0 CH0 0001: Input from ISP0 CH1 0010: Input from ISP0 CH2 0011: Input from ISP0 CH3 0100: Input from ISP1 CH0 0101: Input from ISP1 CH1 0110: Input from ISP1 CH2 0111: Input from ISP1 CH3 1000: Input from ISP2 CH0 1001: Input from ISP2 CH1 1010: Input from ISP2 CH2 1011: Input from ISP2 CH3 1100: Input from ISP3 CH0 1101: Input from ISP3 CH1 1110: Input from ISP3 CH2 1111: Input from ISP3 CH3 NOTE: no ISP1/2/3 exists, ISP1/2/3 is a virtual concept here and referring to a pass-through channel. Should be configured together with CSIC_ISP1/2/3_INPUT0/1/2/3_SEL_REG

16.1.9.33 0x00B0 CSIC DMA4 Input Select Register (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: CSIC_DMA4_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00B0			Register Name: CSIC_DMA4_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	DMA4_INPUT_SEL DMA4 Input select 0000: Input from ISP0 CH0 0001: Input from ISP0 CH1 0010: Input from ISP0 CH2 0011: Input from ISP0 CH3 0100: Input from ISP1 CH0 0101: Input from ISP1 CH1 0110: Input from ISP1 CH2 0111: Input from ISP1 CH3 1000: Input from ISP2 CH0 1001: Input from ISP2 CH1 1010: Input from ISP2 CH2 1011: Input from ISP2 CH3 1100: Input from ISP3 CH0 1101: Input from ISP3 CH1 1110: Input from ISP3 CH2 1111: Input from ISP3 CH3 NOTE: no ISP1/2/3 exists, ISP1/2/3 is a virtual concept here and referring to a pass-through channel. Should be configured together with CSIC_ISP1/2/3_INPUT0/1/2/3_SEL_REG

16.1.9.34 0x00B4 CSIC DMA5 Input Select Register (Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: CSIC_DMA5_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00B4			Register Name: CSIC_DMA5_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	DMA5_INPUT_SEL DMA5 Input select 0000: Input from ISP0 CH0 0001: Input from ISP0 CH1 0010: Input from ISP0 CH2 0011: Input from ISP0 CH3 0100: Input from ISP1 CH0 0101: Input from ISP1 CH1 0110: Input from ISP1 CH2 0111: Input from ISP1 CH3 1000: Input from ISP2 CH0 1001: Input from ISP2 CH1 1010: Input from ISP2 CH2 1011: Input from ISP2 CH3 1100: Input from ISP3 CH0 1101: Input from ISP3 CH1 1110: Input from ISP3 CH2 1111: Input from ISP3 CH3 NOTE: no ISP1/2/3 exists, ISP1/2/3 is a virtual concept here and referring to a pass-through channel. Should be configured together with CSIC_ISP1/2/3_INPUT0/1/2/3_SEL_REG

16.1.9.35 0x00F0 CSIC MBUS REQ MAX Register (Default Value: 0x0f03_0f0f)

Offset: 0x00F0			Register Name: CSIC_MBUS_REQ_MAX_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0f	MISP_MEM_LNUM_REQ_MAX Maximum of request commands for the master granted in MISP_MEM_LNUM arbiter is N+1.
23:21	/	/	/
20:16	R/W	0x03	MISP_MEM_REQ_MAX Maximum of request commands for the master granted in MISP_MEM arbiter is N+1.
15:13	/	/	/
12:8	R/W	0x0f	MCSI_MEM_1_REQ_MAX Maximum of request commands for the master granted in MCSI_MEM_1 arbiter is N+1.
7:5	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00F0			Register Name: CSIC_MBUS_REQ_MAX_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x0f	MCSI_MEM_REQ_MAX Maximum of request commands for the master granted in MCSI_MEM arbiter is N+1.

16.1.9.36 0x00F8 CSIC MBUS WAIT MAX Register (Default Value: 0x0008_0000)

Offset: 0x00F8			Register Name: CSIC_MBUS_WAIT_MAX_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x08	MISP_MEM_WAIT_MAX Maximum of wait cycles for the master granted in MISP_MEM arbiter is N， when N is 0 it waits until a request accepted.
15:8	R/W	0x00	MCSI_MEM_1_WAIT_MAX Maximum of wait cycles for the master granted in MCSI_MEM_1 arbiter is N， when N is 0 it waits until a request accepted.
7:0	R/W	0x00	MCSI_MEM_WAIT_MAX Maximum of wait cycles for the master granted in MCSI_MEM arbiter is N， when N is 0 it waits until a request accepted.

16.1.9.37 0x0100 CSIC Multi-Frame Mode Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: CSIC_MULF_MOD_REG
Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	MULF_STATUS Multi-Frame Mode Status indicates each DMA in frame done pending or not
23:16	/	/	/
15:8	R/W	0x0	MULF_CS Chip Selection for Multi-Frame Mode indicates which DMA is in selected
7:1	/	/	/
0	R/W	0x0	MULF_EN Multi-Frame Mode Enable

16.1.9.38 0x0104 CSIC Multi-Frame Interrupt Register (Default Value: 0x0000_0000)

Offset: 0x0104	Register Name: CSIC_MULF_INT_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W1C	0x0	MULF_ERR_PD Multi-Frame Mode Frame Error Interrupt Pending
16	R/W1C	0x0	MULF_DONE_PD Multi-Frame Mode Frame Done Interrupt Pending
15:2	/	/	/
1	R/W	0x0	MULF_ERR_EN Multi-Frame Mode Frame Error Interrupt Enable
0	R/W	0x0	MULF_DONE_EN Multi-Frame Mode Frame Done Interrupt Enable

16.1.9.39 0x0108 CSIC Change Frequency Configuration 0 Register (Default Value: 0x0001_0000)

Offset: 0x0108			Register Name: CSIC_CHFREQ_CFG0_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0001	CHFREQ_PAR2ISP_SEL Chfreq_par2isp select. Each bit corresponds to one channel. When the channel has data stream passing through, the corresponding bit must be set to 1. [19:16]->par2isp0 ch3,ch2,ch1,ch0 [23:20]->par2isp1 ch3,ch2,ch1,ch0 [27:24]->par2isp2 ch3,ch2,ch1,ch0 [31:28]->par2isp3 ch3,ch2,ch1,ch0
15:6	/	/	/
5	R/W	0x0	CHFREQ_BK_DONE_SRC Chfreq_bk done source select. 0: Select bk_frm_end as source 1: Select bk_frm_done as source
4	R/W	0x0	CHFREQ_PULSE_CNT_SCLR_EN Chfreq_pulse cnt self clear en. 0: Disable pulse cnt self clear 1: Enable pulse cnt self clear
3	R/W	0x0	CHFREQ_RDY_MASK Chfreq Ready Mask 0: Unmask 1: Mask assert, keep chfreq_rdy output as 0
2	R/W	0x0	CHFREQ_SELECT Chfreq_rdy output source select. 0: new implementation 1: old implementation

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0108			Register Name: CSIC_CHFREQ_CFG0_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	CHFREQ_ALLOW Chfreq allow signal. (note: when CHFREQ_EN is asserted or all bk*_en, mvipp*_en&isp_en are set as 0,CHFREQ_ALLOW can't play a role) 0: keep chfreq_rdy output as 0 1: allow chfreq logic
0	R/W	0x0	CHFREQ_RST Soft reset for chfreq logic. 0: Assert 1: De-assert

16.1.9.40 0x010C CSIC Change Frequency Configuration 1 Register (Default Value: 0x0000_0064)

Offset: 0x010C			Register Name: CSIC_CHFREQ_CFG1_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x0000	CHFREQ_WAIT_DONE_TIME The time between hardware chfreq frm_done assert and mcsi chfrq_rdy assert. Take one chfreq_clk cycle as the unit, which by default is 1 us.
15:0	R/W	0x0064	CHFREQ_DDR_TIME The time for ddr to complete frequency change. Take one chfreq_clk cycle as the unit, which by default is 1 us.

16.1.9.41 0x0110 CSIC Change Frequency Observation Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: CSIC_CHFREQ_OBS_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0000	CHFREQ_FRM_DONE_TIME The time for frm done after frm_end, measured by hardware. Take one chfreq_clk cycle as the unit, which by default is 1 us.
15:0	R	0x0000	CHFREQ_VBLANK_LENGTH Vblank length measured by hardware. Take one chfreq_clk cycle as the unit, which by default is 1 us.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.9.42 0x0114 CSIC Change Frequency Interrupt Register (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: CSIC_CHFREQ_INT_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W1C	0x0	CHFREQ_FRM_DONE_NUM_ERR_PD Change Frequency Frame Done Number Error Interrupt Pending
17	R/W1C	0x0	CHFREQ_FRM_END_NUM_ERR_PD Change Frequency Frame End Number Error Interrupt Pending
16	R/W1C	0x0	CHFREQ_FRM_STR_NUM_ERR_PD Change Frequency Frame Start Number Error Interrupt Pending
15:3	/	/	/
2	R/W	0x0	CHFREQ_FRM_DONE_NUM_ERR_EN Change Frequency Frame Done Number Error Interrupt Enable
1	R/W	0x0	CHFREQ_FRM_END_NUM_ERR_EN Change Frequency Frame End Number Error Interrupt Enable
0	R/W	0x0	CHFREQ_FRM_STR_NUM_ERR_EN Change Frequency Frame Start Number Error Interrupt Enable

16.1.9.43 0x0118 CSIC Change Frequency Debug Observation Register (Default Value: 0x0000_2101)

Offset: 0x0118			Register Name: CSIC_CHFREQ_DBG_OBS_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R	0x0	CHFREQ_RSTN_T Chfreq Resetn
26	R	0x0	ISP_RSTN_T ISP Resetn
25	R	0x0	PAR_RSTN_T Parser Resetn
24	R	0x0	POST_RSTN_T Post Resetn
23	R	0x0	ISP_EN_POST_S ISP Enable Post
22:18	R	0x0	FRM_DONE_SRC_NUM Frm Done Source Number

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0118			Register Name: CSIC_CHFREQ_DBG_OBS_REG
Bit	Read/Write	Default/Hex	Description
17:13	R	0x1	FRM_STR_SRC_NUM Frm Start Source Number
12:8	R	0x1	FRM_END_SRC_NUM Frm End Source Number
7	R	0x0	POST_EN_S POST Enable After Sync
6	R	0x0	ISP_EN_S ISP Enable After Sync
5	R	0x0	CHFREQ_ALLOW_S Chfreq Allow After Sync
4	R	0x0	FIRST_FRM_END_RECEIVED First Frm End Received
3	R	0x0	VBLANK_LENTH_VALID Vblank Length Valid
2	R	0x0	IN_VBLANK In Vblank
1	R	0x0	FRM_DONE_TIME_VALID Frm Done Time Valid
0	R	0x1	CHFREQ_RDY Chfreq Rdy

16.1.9.44 0x0120 CSIC ISP Bypass Software Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: CSIC_ISP_BYP_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	MISP_BYP_EN ISP Bypass Enable 0: Disable 1: Enable
0	R/W	0x0	MISP_BYP_SEL Select the Way to Bypass ISP 0: Hardware 1: Software

16.1.9.45 0x0130 CSIC BK INTERRUPT Pool0 Configuration 0 Register (Default Value: 0xffff_0010)

Offset: 0x0130			Register Name: CSIC_BK_INTPOOL0_CFG0_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0130			Register Name: CSIC_BK_INTPOOL0_CFG0_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	SRC_MSK_BK3_CH3 Source mask bit for BK3 channel3. 0: Unmasked 1: Masked
30	R/W	0x1	SRC_MSK_BK3_CH2 Source mask bit for BK3 channel2. 0: Unmasked 1: Masked
29	R/W	0x1	SRC_MSK_BK3_CH1 Source mask bit for BK3 channel1. 0: Unmasked 1: Masked
28	R/W	0x1	SRC_MSK_BK3_CH0 Source mask bit for BK3 channel0. 0: Unmasked 1: Masked
27	R/W	0x1	SRC_MSK_BK2_CH3 Source mask bit for BK2 channel3. 0: Unmasked 1: Masked
26	R/W	0x1	SRC_MSK_BK2_CH2 Source mask bit for BK2 channel2. 0: Unmasked 1: Masked
25	R/W	0x1	SRC_MSK_BK2_CH1 Source mask bit for BK2 channel1. 0: Unmasked 1: Masked
24	R/W	0x1	SRC_MSK_BK2_CH0 Source mask bit for BK2 channel0. 0: Unmasked 1: Masked
23	R/W	0x1	SRC_MSK_BK1_CH3 Source mask bit for BK1 channel3. 0: Unmasked 1: Masked
22	R/W	0x1	SRC_MSK_BK1_CH2 Source mask bit for BK1 channel2. 0: Unmasked 1: Masked

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0130			Register Name: CSIC_BK_INTPOOL0_CFG0_REG
Bit	Read/Write	Default/Hex	Description
21	R/W	0x1	SRC_MSK_BK1_CH1 Source mask bit for BK1 channel1. 0: Unmasked 1: Masked
20	R/W	0x1	SRC_MSK_BK1_CH0 Source mask bit for BK1 channel0. 0: Unmasked 1: Masked
19	R/W	0x1	SRC_MSK_BK0_CH3 Source mask bit for BK0 channel3. 0: Unmasked 1: Masked
18	R/W	0x1	SRC_MSK_BK0_CH2 Source mask bit for BK0 channel2. 0: Unmasked 1: Masked
17	R/W	0x1	SRC_MSK_BK0_CH1 Source mask bit for BK0 channel1. 0: Unmasked 1: Masked
16	R/W	0x1	SRC_MSK_BK0_CH0 Source mask bit for BK0 channel0. 0: Unmasked 1: Masked
15:14	R/W	0x0	TRIG_CH Trigger Channel. When TRIG_MOD=1, this field decides the BK channel which the int fifo contains then fifo_avl int will happen. Can be set between ‘d0~‘d3 for BK0/1/6/7, and ‘d0 for the other BKs. Used together with TRIG_ID field.
13:10	R/W	0x0	TRIG_ID Trigger ID. When TRIG_MOD=1, this field decides the BK ID which the int fifo contains then fifo_avl int will happen. Can be set between ‘d0~‘d11. Used together with TRIG_CH field.
9:4	R/W	0x1	TRIG_LEVEL Trigger level. When TRIG_MOD=0, this field decides the fifo level at which the int fifo reaches then fifo_avl int will happen. Can be set between‘d1~‘d63.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0130			Register Name: CSIC_BK_INTPOOL0_CFG0_REG
Bit	Read/Write	Default/Hex	Description
3	/	/	/
2	R/W	0x0	TRIG_MOD Trigger mode for fifo_avl int generation. 0: fifo_level trigger mode 1: target trigger mode
1	R/W	0x0	INT_SRC_SEL Interrupt source select. 0: Select VS_INT as source 1: Select FD_INT as source
0	R/W	0x0	BK_INT_POOL_EN Soft reset for bk interrupt pool logic. 0: Assert 1: De-assert

16.1.9.46 0x0134 CSIC BK INTERRUPT Pool0 Configuration 1 Register (Default Value: 0xffff_ffff)

Offset: 0x0134			Register Name: CSIC_BK_INTPOOL0_CFG1_REG
Bit	Read/Write	Default/Hex	Description
31:5	R	0x7ff_ffff	RESERVED Reserved
4	R/W	0x1	SRC_MSK_BK5_CH0 Source mask bit for BK5 channel0. 0: Unmasked 1: Masked
3:1	R	0x7	RESERVED Reserved
0	R/W	0x1	SRC_MSK_BK4_CH0 Source mask bit for BK4 channel0. 0: Unmasked 1: Masked

16.1.9.47 0x0138 CSIC BK INTERRUPT FIFO0 Register (Default Value: 0x0000_0000)

Offset: 0x0138			Register Name: CSIC_BK_INT_FIFO0_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0138			Register Name: CSIC_BK_INT_FIFO0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_FIFO_DATA Interrupt FIFO data Host can get one interrupt event out of the interrupt fifo by reading this register. 32bit Interrupt FIFO data = {4'h0,Time Stamp Delta (20 bit),2'h0,Channel Number(2 bit),BK ID(4 bit)}

16.1.9.48 0x013C CSIC BK INTERRUPT Pool0 Observation 0 Register (Default Value: 0x0000_0000)

Offset: 0x013C			Register Name: CSIC_BK_INTPOOL0_OBS0_REG
Bit	Read/Write	Default/Hex	Description
31:23	/	/	/
22:16	R	0x0	TRIG_TGT_LEVEL Trigger target level. Indicates how many BK interrupt events of trigger target are currently stored in the interrupt FIFO.
15:7	/	/	/
6:0	R	0x0	FIFO_LEVEL FIFO level. Indicates how many BK interrupt events are currently stored in the interrupt FIFO.

16.1.9.49 0x0140 CSIC BK INTERRUPT Pool0 Observation 1 Register (Default Value: 0x0000_0000)

Offset: 0x0140			Register Name: CSIC_BK_INTPOOL0_OBS1_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	FULL_ACCESS_DELAY Full access delay. Indicates the delay for the last read-out BK interrupt event in one fifo_full interrupt handling event from when it is stored into the interrupt fifo to when it is read out. Take one bk_intpool_clk cycle as the unit, which by default is 1 us.
15:0	R	0x0	ACCESS_DELAY Access delay. Indicates the delay for the last read-out BK interrupt event in one fifo_avl interrupt handling event from when it is stored into the interrupt fifo to when it is read out. Take one bk_intpool_clk cycle as the unit, which by default is 1 us.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.9.50 0x0144 CSIC BK INTERRUPT Pool0 Interrupt Enable 0 Register (Default Value: 0x0000_0000)

Offset: 0x0144			Register Name: CSIC_BK_INTPOOL0_INT_EN0_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	BK3_CH3_INT_LOST_INT_EN BK3 channel3 interrupt lost interrupt enable Indicates some Interrupts of BK3 channel3 are lost 0: Disable 1: Enable
30	R/W	0x0	BK3_CH2_INT_LOST_INT_EN BK3 channel2 interrupt lost interrupt enable Indicates some Interrupts of BK3 channel2 are lost 0: Disable 1: Enable
29	R/W	0x0	BK3_CH1_INT_LOST_INT_EN BK3 channel1 interrupt lost interrupt enable Indicates some Interrupts of BK3 channel1 are lost 0: Disable 1: Enable
28	R/W	0x0	BK3_CH0_INT_LOST_INT_EN BK3 channel0 interrupt lost interrupt enable Indicates some Interrupts of BK3 channel0 are lost 0: Disable 1: Enable
27	R/W	0x0	BK2_CH3_INT_LOST_INT_EN BK2 channel3 interrupt lost interrupt enable Indicates some Interrupts of BK2 channel3 are lost 0: Disable 1: Enable
26	R/W	0x0	BK2_CH2_INT_LOST_INT_EN BK2 channel2 interrupt lost interrupt enable Indicates some Interrupts of BK2 channel2 are lost 0: Disable 1: Enable
25	R/W	0x0	BK2_CH1_INT_LOST_INT_EN BK2 channel1 interrupt lost interrupt enable Indicates some Interrupts of BK2 channel1 are lost 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0144			Register Name: CSIC_BK_INTPOOL0_INT_EN0_REG
Bit	Read/Write	Default/Hex	Description
24	R/W	0x0	BK2_CH0_INT_LOST_INT_EN BK2 channel0 interrupt lost interrupt enable Indicates some Interrupts of BK2 channel0 are lost 0: Disable 1: Enable
23	R/W	0x0	BK1_CH3_INT_LOST_INT_EN BK1 channel3 interrupt lost interrupt enable Indicates some Interrupts of BK1 channel3 are lost 0: Disable 1: Enable
22	R/W	0x0	BK1_CH2_INT_LOST_INT_EN BK1 channel2 interrupt lost interrupt enable Indicates some Interrupts of BK1 channel2 are lost 0: Disable 1: Enable
21	R/W	0x0	BK1_CH1_INT_LOST_INT_EN BK1 channel1 interrupt lost interrupt enable Indicates some Interrupts of BK1 channel1 are lost 0: Disable 1: Enable
20	R/W	0x0	BK1_CH0_INT_LOST_INT_EN BK1 channel0 interrupt lost interrupt enable Indicates some Interrupts of BK1 channel0 are lost 0: Disable 1: Enable
19	R/W	0x0	BK0_CH3_INT_LOST_INT_EN BK0 channel3 interrupt lost interrupt enable Indicates some Interrupts of BK0 channel3 are lost 0: Disable 1: Enable
18	R/W	0x0	BK0_CH2_INT_LOST_INT_EN BK0 channel2 interrupt lost interrupt enable Indicates some Interrupts of BK0 channel2 are lost 0: Disable 1: Enable
17	R/W	0x0	BK0_CH1_INT_LOST_INT_EN BK0 channel1 interrupt lost interrupt enable Indicates some Interrupts of BK0 channel1 are lost 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0144			Register Name: CSIC_BK_INTPOOL0_INT_EN0_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	BK0_CH0_INT_LOST_INT_EN BK0 channel0 interrupt lost interrupt enable Indicates some Interrupts of BK0 channel0 are lost 0: Disable 1: Enable
15:2	/	/	/
1	R/W	0x0	FIFO_FULL_INT_EN FIFO full interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	FIFO_AVL_INT_EN FIFO available interrupt Enable 0: Disable 1: Enable

16.1.9.51 0x0148 CSIC BK INTERRUPT Pool0 Interrupt Enable 1 Register (Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: CSIC_BK_INTPOOL0_INT_EN1_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W	0x0	BK5_CH0_INT_LOST_INT_EN BK5 channel0 interrupt lost interrupt enable Indicates some Interrupts of BK5 channel0 are lost 0: Disable 1: Enable
3:1	/	/	/
0	R/W	0x0	BK4_CH0_INT_LOST_INT_EN BK4 channel0 interrupt lost interrupt enable Indicates some Interrupts of BK4 channel0 are lost 0: Disable 1: Enable

16.1.9.52 0x014C CSIC BK INTERRUPT Pool0 Interrupt Status 0 Register (Default Value: 0x0000_0000)

Offset: 0x014C			Register Name: CSIC_BK_INTPOOL0_INT_STA0_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x014C			Register Name: CSIC_BK_INTPOOL0_INT_STA0_REG
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	BK3_CH3_INT_LOST_INT_PD BK3 channel3 interrupt lost interrupt pending Indicates some Interrupts of BK3 channel3 are lost Flag 1 when pending. Write 1 to clear.
30	R/W1C	0x0	BK3_CH2_INT_LOST_INT_PD BK3 channel2 interrupt lost interrupt pending Indicates some Interrupts of BK3 channel2 are lost Flag 1 when pending. Write 1 to clear.
29	R/W1C	0x0	BK3_CH1_INT_LOST_INT_PD BK3 channel1 interrupt lost interrupt pending Indicates some Interrupts of BK3 channel1 are lost Flag 1 when pending. Write 1 to clear.
28	R/W1C	0x0	BK3_CH0_INT_LOST_INT_PD BK3 channel0 interrupt lost interrupt pending Indicates some Interrupts of BK3 channel0 are lost Flag 1 when pending. Write 1 to clear.
27	R/W1C	0x0	BK2_CH3_INT_LOST_INT_PD BK2 channel3 interrupt lost interrupt pending Indicates some Interrupts of BK2 channel3 are lost Flag 1 when pending. Write 1 to clear.
26	R/W1C	0x0	BK2_CH2_INT_LOST_INT_PD BK2 channel2 interrupt lost interrupt pending Indicates some Interrupts of BK2 channel2 are lost Flag 1 when pending. Write 1 to clear.
25	R/W1C	0x0	BK2_CH1_INT_LOST_INT_PD BK2 channel1 interrupt lost interrupt pending Indicates some Interrupts of BK2 channel1 are lost Flag 1 when pending. Write 1 to clear.
24	R/W1C	0x0	BK2_CH0_INT_LOST_INT_PD BK2 channel0 interrupt lost interrupt pending Indicates some Interrupts of BK2 channel0 are lost Flag 1 when pending. Write 1 to clear.
23	R/W1C	0x0	BK1_CH3_INT_LOST_INT_PD BK1 channel3 interrupt lost interrupt pending Indicates some Interrupts of BK1 channel3 are lost Flag 1 when pending. Write 1 to clear.
22	R/W1C	0x0	BK1_CH2_INT_LOST_INT_PD BK1 channel2 interrupt lost interrupt pending Indicates some Interrupts of BK1 channel2 are lost Flag 1 when pending. Write 1 to clear.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x014C			Register Name: CSIC_BK_INTPOOL0_INT_STA0_REG
Bit	Read/Write	Default/Hex	Description
21	R/W1C	0x0	BK1_CH1_INT_LOST_INT_PD BK1 channel1 interrupt lost interrupt pending Indicates some Interrupts of BK1 channel1 are lost Flag 1 when pending. Write 1 to clear.
20	R/W1C	0x0	BK1_CH0_INT_LOST_INT_PD BK1 channel0 interrupt lost interrupt pending Indicates some Interrupts of BK1 channel0 are lost Flag 1 when pending. Write 1 to clear.
19	R/W1C	0x0	BK0_CH3_INT_LOST_INT_PD BK0 channel3 interrupt lost interrupt pending Indicates some Interrupts of BK0 channel3 are lost Flag 1 when pending. Write 1 to clear.
18	R/W1C	0x0	BK0_CH2_INT_LOST_INT_PD BK0 channel2 interrupt lost interrupt pending Indicates some Interrupts of BK0 channel2 are lost Flag 1 when pending. Write 1 to clear.
17	R/W1C	0x0	BK0_CH1_INT_LOST_INT_PD BK0 channel1 interrupt lost interrupt pending Indicates some Interrupts of BK0 channel1 are lost Flag 1 when pending. Write 1 to clear.
16	R/W1C	0x0	BK0_CH0_INT_LOST_INT_PD BK0 channel0 interrupt lost interrupt pending Indicates some Interrupts of BK0 channel0 are lost Flag 1 when pending. Write 1 to clear.
15:2	/	/	/
1	R/W1C	0x0	FIFO_FULL_INT_PD FIFO full interrupt pending Flag 1 when pending. Write 1 to clear.
0	R/W1C	0x0	FIFO_AVL_INT_PD FIFO available interrupt pending Flag 1 when pending. Write 1 to clear.

16.1.9.53 0x0150 CSIC BK INTERRUPT Pool0 Interrupt Status 1 Register (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: CSIC_BK_INTPOOL0_INT_STA1_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0150			Register Name: CSIC_BK_INTPOOL0_INT_STA1_REG
Bit	Read/Write	Default/Hex	Description
4	R/W1C	0x0	BK5_CH0_INT_LOST_INT_PD BK5 channel0 interrupt lost interrupt pending Indicates some Interrupts of BK5 channel0 are lost Flag 1 when pending. Write 1 to clear.
3:1	/	/	/
0	R/W1C	0x0	BK4_CH0_INT_LOST_INT_PD BK4 channel0 interrupt lost interrupt pending Indicates some Interrupts of BK4 channel0 are lost Flag 1 when pending. Write 1 to clear.

16.1.9.54 0x0160 CSIC BK INTERRUPT Pool1 Configuration 0 Register (Default Value: 0xffff_0010)

Offset: 0x0160			Register Name: CSIC_BK_INTPOOL1_CFG0_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	SRC_MSK_BK3_CH3 Source mask bit for BK3 channel3. 0: Unmasked 1: Masked
30	R/W	0x1	SRC_MSK_BK3_CH2 Source mask bit for BK3 channel2. 0: Unmasked 1: Masked
29	R/W	0x1	SRC_MSK_BK3_CH1 Source mask bit for BK3 channel1. 0: Unmasked 1: Masked
28	R/W	0x1	SRC_MSK_BK3_CH0 Source mask bit for BK3 channel0. 0: Unmasked 1: Masked
27	R/W	0x1	SRC_MSK_BK2_CH3 Source mask bit for BK2 channel3. 0: Unmasked 1: Masked
26	R/W	0x1	SRC_MSK_BK2_CH2 Source mask bit for BK2 channel2. 0: Unmasked 1: Masked

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0160			Register Name: CSIC_BK_INTPOOL1_CFG0_REG
Bit	Read/Write	Default/Hex	Description
25	R/W	0x1	SRC_MSK_BK2_CH1 Source mask bit for BK2 channel1. 0: Unmasked 1: Masked
24	R/W	0x1	SRC_MSK_BK2_CH0 Source mask bit for BK2 channel0. 0: Unmasked 1: Masked
23	R/W	0x1	SRC_MSK_BK1_CH3 Source mask bit for BK1 channel3. 0: Unmasked 1: Masked
22	R/W	0x1	SRC_MSK_BK1_CH2 Source mask bit for BK1 channel2. 0: Unmasked 1: Masked
21	R/W	0x1	SRC_MSK_BK1_CH1 Source mask bit for BK1 channel1. 0: Unmasked 1: Masked
20	R/W	0x1	SRC_MSK_BK1_CH0 Source mask bit for BK1 channel0. 0: Unmasked 1: Masked
19	R/W	0x1	SRC_MSK_BK0_CH3 Source mask bit for BK0 channel3. 0: Unmasked 1: Masked
18	R/W	0x1	SRC_MSK_BK0_CH2 Source mask bit for BK0 channel2. 0: Unmasked 1: Masked
17	R/W	0x1	SRC_MSK_BK0_CH1 Source mask bit for BK0 channel1. 0: Unmasked 1: Masked
16	R/W	0x1	SRC_MSK_BK0_CH0 Source mask bit for BK0 channel0. 0: Unmasked 1: Masked

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0160			Register Name: CSIC_BK_INTPOOL1_CFG0_REG
Bit	Read/Write	Default/Hex	Description
15:14	R/W	0x0	TRIG_CH Trigger Channel. When TRIG_MOD=1, this field decides the BK channel which the int fifo contains then fifo_avl int will happen. Can be set between ‘d0~‘d3 for BK0/1/6/7, and ‘d0 for the other BKs. Used together with TRIG_ID field.
13:10	R/W	0x0	TRIG_ID Trigger ID. When TRIG_MOD=1, this field decides the BK ID which the int fifo contains then fifo_avl int will happen. Can be set between ‘d0~‘d11. Used together with TRIG_CH field.
9:4	R/W	0x1	TRIG_LEVEL Trigger level. When TRIG_MOD=0, this field decides the fifo level at which the int fifo reaches then fifo_avl int will happen. Can be set between‘d1~‘d63.
3	/	/	/
2	R/W	0x0	TRIG_MOD Trigger mode for fifo_avl int generation. 0: fifo_level trigger mode 1: target trigger mode
1	R/W	0x0	INT_SRC_SEL Interrupt source select. 0: Select VS_INT as source 1: Select FD_INT as source
0	R/W	0x0	BK_INT_POOL_EN Soft reset for bk interrupt pool logic. 0: Assert 1: De-assert

16.1.9.55 0x0164 CSIC BK INTERRUPT Pool1 Configuration 1 Register (Default Value: 0xffff_ffff)

Offset: 0x0164			Register Name: CSIC_BK_INTPOOL1_CFG1_REG
Bit	Read/Write	Default/Hex	Description
31:5	R	0x7ff_ffff	RESERVED Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0164			Register Name: CSIC_BK_INTPOOL1_CFG1_REG
Bit	Read/Write	Default/Hex	Description
4	R/W	0x1	SRC_MSK_BK5_CH0 Source mask bit for BK5 channel0. 0: Unmasked 1: Masked
3:1	R	0x7	RESERVED Reserved
0	R/W	0x1	SRC_MSK_BK4_CH0 Source mask bit for BK4 channel0. 0: Unmasked 1: Masked

16.1.9.56 0x0168 CSIC BK INTERRUPT FIFO1 Register (Default Value: 0x0000_0000)

Offset: 0x0168			Register Name: CSIC_BK_INT_FIFO1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_FIFO_DATA Interrupt FIFO data Host can get one interrupt event out of the interrupt fifo by reading this register. 32bit Interrupt FIFO data = {4'h0,Time Stamp Delta (20 bit),2'h0,Channel Number(2 bit),BK ID(4 bit)}

16.1.9.57 0x016C CSIC BK INTERRUPT Pool1 Observation 0 Register (Default Value: 0x0000_0000)

Offset: 0x016C			Register Name: CSIC_BK_INTPOOL1_OBS0_REG
Bit	Read/Write	Default/Hex	Description
31:23	/	/	/
22:16	R	0x0	TRIG_TGT_LEVEL Trigger target level. Indicates how many BK interrupt events of trigger target are currently stored in the interrupt FIFO.
15:7	/	/	/
6:0	R	0x0	FIFO_LEVEL FIFO level. Indicates how many BK interrupt events are currently stored in the interrupt FIFO.

16.1.9.58 0x0170 CSIC BK INTERRUPT Pool1 Observation 1 Register (Default Value: 0x0000_0000)

Offset: 0x0170	Register Name: CSIC_BK_INTPOOL1_OBS1_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	FULL_ACCESS_DELAY Full access delay. Indicates the delay for the last read-out BK interrupt event in one fifo_full interrupt handling event from when it is stored into the interrupt fifo to when it is read out. Take one bk_intpool_clk cycle as the unit, which by default is 1 us.
15:0	R	0x0	ACCESS_DELAY Access delay. Indicates the delay for the last read-out BK interrupt event in one fifo_avl interrupt handling event from when it is stored into the interrupt fifo to when it is read out. Take one bk_intpool_clk cycle as the unit, which by default is 1 us.

16.1.9.59 0x0174 CSIC BK INTERRUPT Pool1 Interrupt Enable 0 Register (Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: CSIC_BK_INTPOOL1_INT_EN0_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R/W	0x0	BK3_CH0_INT_LOST_INT_EN BK3 channel0 interrupt lost interrupt enable Indicates some Interrupts of BK3 channel0 are lost 0: Disable 1: Enable
27	R/W	0x0	BK2_CH3_INT_LOST_INT_EN BK2 channel3 interrupt lost interrupt enable Indicates some Interrupts of BK2 channel3 are lost 0: Disable 1: Enable
26	R/W	0x0	BK2_CH2_INT_LOST_INT_EN BK2 channel2 interrupt lost interrupt enable Indicates some Interrupts of BK2 channel2 are lost 0: Disable 1: Enable
25	R/W	0x0	BK2_CH1_INT_LOST_INT_EN BK2 channel1 interrupt lost interrupt enable Indicates some Interrupts of BK2 channel1 are lost 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0174			Register Name: CSIC_BK_INTPOOL1_INT_EN0_REG
Bit	Read/Write	Default/Hex	Description
24	R/W	0x0	BK2_CH0_INT_LOST_INT_EN BK2 channel0 interrupt lost interrupt enable Indicates some Interrupts of BK2 channel0 are lost 0: Disable 1: Enable
23	R/W	0x0	BK1_CH3_INT_LOST_INT_EN BK1 channel3 interrupt lost interrupt enable Indicates some Interrupts of BK1 channel3 are lost 0: Disable 1: Enable
22	R/W	0x0	BK1_CH2_INT_LOST_INT_EN BK1 channel2 interrupt lost interrupt enable Indicates some Interrupts of BK1 channel2 are lost 0: Disable 1: Enable
21	R/W	0x0	BK1_CH1_INT_LOST_INT_EN BK1 channel1 interrupt lost interrupt enable Indicates some Interrupts of BK1 channel1 are lost 0: Disable 1: Enable
20	R/W	0x0	BK1_CH0_INT_LOST_INT_EN BK1 channel0 interrupt lost interrupt enable Indicates some Interrupts of BK1 channel0 are lost 0: Disable 1: Enable
19	R/W	0x0	BK0_CH3_INT_LOST_INT_EN BK0 channel3 interrupt lost interrupt enable Indicates some Interrupts of BK0 channel3 are lost 0: Disable 1: Enable
18	R/W	0x0	BK0_CH2_INT_LOST_INT_EN BK0 channel2 interrupt lost interrupt enable Indicates some Interrupts of BK0 channel2 are lost 0: Disable 1: Enable
17	R/W	0x0	BK0_CH1_INT_LOST_INT_EN BK0 channel1 interrupt lost interrupt enable Indicates some Interrupts of BK0 channel1 are lost 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0174			Register Name: CSIC_BK_INTPOOL1_INT_EN0_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	BK0_CH0_INT_LOST_INT_EN BK0 channel0 interrupt lost interrupt enable Indicates some Interrupts of BK0 channel0 are lost 0: Disable 1: Enable
15:2	/	/	/
1	R/W	0x0	FIFO_FULL_INT_EN FIFO full interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	FIFO_AVL_INT_EN FIFO available interrupt Enable 0: Disable 1: Enable

16.1.9.60 0x0178 CSIC BK INTERRUPT Pool1 Interrupt Enable 1 Register (Default Value: 0x0000_0000)

Offset: 0x0178			Register Name: CSIC_BK_INTPOOL1_INT_EN1_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W	0x0	BK5_CH0_INT_LOST_INT_EN BK5 channel0 interrupt lost interrupt enable Indicates some Interrupts of BK5 channel0 are lost 0: Disable 1: Enable
3:1	/	/	/
0	R/W	0x0	BK4_CH0_INT_LOST_INT_EN BK4 channel0 interrupt lost interrupt enable Indicates some Interrupts of BK4 channel0 are lost 0: Disable 1: Enable

16.1.9.61 0x017C CSIC BK INTERRUPT Pool1 Interrupt Status 0 Register (Default Value: 0x0000_0000)

Offset: 0x017C			Register Name: CSIC_BK_INTPOOL1_INT_STA0_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x017C			Register Name: CSIC_BK_INTPOOL1_INT_STA0_REG
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	BK3_CH3_INT_LOST_INT_PD BK3 channel3 interrupt lost interrupt pending Indicates some Interrupts of BK3 channel3 are lost Flag 1 when pending. Write 1 to clear.
30	R/W1C	0x0	BK3_CH2_INT_LOST_INT_PD BK3 channel2 interrupt lost interrupt pending Indicates some Interrupts of BK3 channel2 are lost Flag 1 when pending. Write 1 to clear.
29	R/W1C	0x0	BK3_CH1_INT_LOST_INT_PD BK3 channel1 interrupt lost interrupt pending Indicates some Interrupts of BK3 channel1 are lost Flag 1 when pending. Write 1 to clear.
28	R/W1C	0x0	BK3_CH0_INT_LOST_INT_PD BK3 channel0 interrupt lost interrupt pending Indicates some Interrupts of BK3 channel0 are lost Flag 1 when pending. Write 1 to clear.
27	R/W1C	0x0	BK2_CH3_INT_LOST_INT_PD BK2 channel3 interrupt lost interrupt pending Indicates some Interrupts of BK2 channel3 are lost Flag 1 when pending. Write 1 to clear.
26	R/W1C	0x0	BK2_CH2_INT_LOST_INT_PD BK2 channel2 interrupt lost interrupt pending Indicates some Interrupts of BK2 channel2 are lost Flag 1 when pending. Write 1 to clear.
25	R/W1C	0x0	BK2_CH1_INT_LOST_INT_PD BK2 channel1 interrupt lost interrupt pending Indicates some Interrupts of BK2 channel1 are lost Flag 1 when pending. Write 1 to clear.
24	R/W1C	0x0	BK2_CH0_INT_LOST_INT_PD BK2 channel0 interrupt lost interrupt pending Indicates some Interrupts of BK2 channel0 are lost Flag 1 when pending. Write 1 to clear.
23	R/W1C	0x0	BK1_CH3_INT_LOST_INT_PD BK1 channel3 interrupt lost interrupt pending Indicates some Interrupts of BK1 channel3 are lost Flag 1 when pending. Write 1 to clear.
22	R/W1C	0x0	BK1_CH2_INT_LOST_INT_PD BK1 channel2 interrupt lost interrupt pending Indicates some Interrupts of BK1 channel2 are lost Flag 1 when pending. Write 1 to clear.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x017C			Register Name: CSIC_BK_INTPOOL1_INT_STA0_REG
Bit	Read/Write	Default/Hex	Description
21	R/W1C	0x0	BK1_CH1_INT_LOST_INT_PD BK1 channel1 interrupt lost interrupt pending Indicates some Interrupts of BK1 channel1 are lost Flag 1 when pending. Write 1 to clear.
20	R/W1C	0x0	BK1_CH0_INT_LOST_INT_PD BK1 channel0 interrupt lost interrupt pending Indicates some Interrupts of BK1 channel0 are lost Flag 1 when pending. Write 1 to clear.
19	R/W1C	0x0	BK0_CH3_INT_LOST_INT_PD BK0 channel3 interrupt lost interrupt pending Indicates some Interrupts of BK0 channel3 are lost Flag 1 when pending. Write 1 to clear.
18	R/W1C	0x0	BK0_CH2_INT_LOST_INT_PD BK0 channel2 interrupt lost interrupt pending Indicates some Interrupts of BK0 channel2 are lost Flag 1 when pending. Write 1 to clear.
17	R/W1C	0x0	BK0_CH1_INT_LOST_INT_PD BK0 channel1 interrupt lost interrupt pending Indicates some Interrupts of BK0 channel1 are lost Flag 1 when pending. Write 1 to clear.
16	R/W1C	0x0	BK0_CH0_INT_LOST_INT_PD BK0 channel0 interrupt lost interrupt pending Indicates some Interrupts of BK0 channel0 are lost Flag 1 when pending. Write 1 to clear.
15:2	/	/	/
1	R/W1C	0x0	FIFO_FULL_INT_PD FIFO full interrupt pending Flag 1 when pending. Write 1 to clear.
0	R/W1C	0x0	FIFO_AVL_INT_PD FIFO available interrupt pending Flag 1 when pending. Write 1 to clear.

16.1.9.62 0x0180 CSIC BK INTERRUPT Pool1 Interrupt Status 1 Register (Default Value: 0x0000_0000)

Offset: 0x0180			Register Name: CSIC_BK_INTPOOL1_INT_STA1_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0180			Register Name: CSIC_BK_INTPOOL1_INT_STA1_REG
Bit	Read/Write	Default/Hex	Description
4	R/W1C	0x0	BK5_CH0_INT_LOST_INT_PD BK5 channel0 interrupt lost interrupt pending Indicates some Interrupts of BK5 channel0 are lost Flag 1 when pending. Write 1 to clear.
3:1	/	/	/
0	R/W1C	0x0	BK4_CH0_INT_LOST_INT_PD BK4 channel0 interrupt lost interrupt pending Indicates some Interrupts of BK4 channel0 are lost Flag 1 when pending. Write 1 to clear.

16.1.9.63 0x0190 CSIC BK INTERRUPT Pool2 Configuration 0 Register (Default Value: 0xffff_0010)

Offset: 0x0190			Register Name: CSIC_BK_INTPOOL2_CFG0_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	SRC_MSK_BK3_CH3 Source mask bit for BK3 channel3. 0: Unmasked 1: Masked
30	R/W	0x1	SRC_MSK_BK3_CH2 Source mask bit for BK3 channel2. 0: Unmasked 1: Masked
29	R/W	0x1	SRC_MSK_BK3_CH1 Source mask bit for BK3 channel1. 0: Unmasked 1: Masked
28	R/W	0x1	SRC_MSK_BK3_CH0 Source mask bit for BK3 channel0. 0: Unmasked 1: Masked
27	R/W	0x1	SRC_MSK_BK2_CH3 Source mask bit for BK2 channel3. 0: Unmasked 1: Masked
26	R/W	0x1	SRC_MSK_BK2_CH2 Source mask bit for BK2 channel2. 0: Unmasked 1: Masked

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0190			Register Name: CSIC_BK_INTPOOL2_CFG0_REG
Bit	Read/Write	Default/Hex	Description
25	R/W	0x1	SRC_MSK_BK2_CH1 Source mask bit for BK2 channel1. 0: Unmasked 1: Masked
24	R/W	0x1	SRC_MSK_BK2_CH0 Source mask bit for BK2 channel0. 0: Unmasked 1: Masked
23	R/W	0x1	SRC_MSK_BK1_CH3 Source mask bit for BK1 channel3. 0: Unmasked 1: Masked
22	R/W	0x1	SRC_MSK_BK1_CH2 Source mask bit for BK1 channel2. 0: Unmasked 1: Masked
21	R/W	0x1	SRC_MSK_BK1_CH1 Source mask bit for BK1 channel1. 0: Unmasked 1: Masked
20	R/W	0x1	SRC_MSK_BK1_CH0 Source mask bit for BK1 channel0. 0: Unmasked 1: Masked
19	R/W	0x1	SRC_MSK_BK0_CH3 Source mask bit for BK0 channel3. 0: Unmasked 1: Masked
18	R/W	0x1	SRC_MSK_BK0_CH2 Source mask bit for BK0 channel2. 0: Unmasked 1: Masked
17	R/W	0x1	SRC_MSK_BK0_CH1 Source mask bit for BK0 channel1. 0: Unmasked 1: Masked
16	R/W	0x1	SRC_MSK_BK0_CH0 Source mask bit for BK0 channel0. 0: Unmasked 1: Masked

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0190			Register Name: CSIC_BK_INTPOOL2_CFG0_REG
Bit	Read/Write	Default/Hex	Description
15:14	R/W	0x0	TRIG_CH Trigger Channel. When TRIG_MOD=1, this field decides the BK channel which the int fifo contains then fifo_avl int will happen. Can be set between ‘d0~‘d3 for BK0/1/6/7, and ‘d0 for the other BKs. Used together with TRIG_ID field.
13:10	R/W	0x0	TRIG_ID Trigger ID. When TRIG_MOD=1, this field decides the BK ID which the int fifo contains then fifo_avl int will happen. Can be set between ‘d0~‘d11. Used together with TRIG_CH field.
9:4	R/W	0x1	TRIG_LEVEL Trigger level. When TRIG_MOD=0, this field decides the fifo level at which the int fifo reaches then fifo_avl int will happen. Can be set between‘d1~‘d63.
3	/	/	/
2	R/W	0x0	TRIG_MOD Trigger mode for fifo_avl int generation. 0: fifo_level trigger mode 1: target trigger mode
1	R/W	0x0	INT_SRC_SEL Interrupt source select. 0: Select VS_INT as source 1: Select FD_INT as source
0	R/W	0x0	BK_INT_POOL_EN Soft reset for bk interrupt pool logic. 0: Assert 1: De-assert

16.1.9.64 0x0194 CSIC BK INTERRUPT Pool2 Configuration 1 Register (Default Value: 0xffff_ffff)

Offset: 0x0194			Register Name: CSIC_BK_INTPOOL2_CFG1_REG
Bit	Read/Write	Default/Hex	Description
31:5	R	0x7ff_ffff	RESERVED Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0194			Register Name: CSIC_BK_INTPOOL2_CFG1_REG
Bit	Read/Write	Default/Hex	Description
4	R/W	0x1	SRC_MSK_BK5_CH0 Source mask bit for BK5 channel0. 0: Unmasked 1: Masked
3:1	R	0x7	RESERVED Reserved
0	R/W	0x1	SRC_MSK_BK4_CH0 Source mask bit for BK4 channel0. 0: Unmasked 1: Masked

16.1.9.65 0x0198 CSIC BK INTERRUPT FIFO2 Register (Default Value: 0x0000_0000)

Offset: 0x0198			Register Name: CSIC_BK_INT_FIFO2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_FIFO_DATA Interrupt FIFO data Host can get one interrupt event out of the interrupt fifo by reading this register. 32bit Interrupt FIFO data = {4'h0,Time Stamp Delta (20 bit),2'h0,Channel Number(2 bit),BK ID(4 bit)}

16.1.9.66 0x019C CSIC BK INTERRUPT Pool2 Observation 0 Register (Default Value: 0x0000_0000)

Offset: 0x019C			Register Name: CSIC_BK_INTPOOL2_OBS0_REG
Bit	Read/Write	Default/Hex	Description
31:23	/	/	/
22:16	R	0x0	TRIG_TGT_LEVEL Trigger target level. Indicates how many BK interrupt events of trigger target are currently stored in the interrupt FIFO.
15:7	/	/	/
6:0	R	0x0	FIFO_LEVEL FIFO level. Indicates how many BK interrupt events are currently stored in the interrupt FIFO.

16.1.9.67 0x01A0 CSIC BK INTERRUPT Pool2 Observation 1 Register (Default Value: 0x0000_0000)

Offset: 0x01A0	Register Name: CSIC_BK_INTPOOL2_OBS1_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	FULL_ACCESS_DELAY Full access delay. Indicates the delay for the last read-out BK interrupt event in one fifo_full interrupt handling event from when it is stored into the interrupt fifo to when it is read out. Take one bk_intpool_clk cycle as the unit, which by default is 1 us.
15:0	R	0x0	ACCESS_DELAY Access delay. Indicates the delay for the last read-out BK interrupt event in one fifo_avl interrupt handling event from when it is stored into the interrupt fifo to when it is read out. Take one bk_intpool_clk cycle as the unit, which by default is 1 us.

16.1.9.68 0x01A4 CSIC BK INTERRUPT Pool2 Interrupt Enable 0 Register (Default Value: 0x0000_0000)

Offset: 0x01A4			Register Name: CSIC_BK_INTPOOL2_INT_EN0_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	BK3_CH3_INT_LOST_INT_EN BK3 channel3 interrupt lost interrupt enable Indicates some Interrupts of BK3 channel3 are lost 0: Disable 1: Enable
30	R/W	0x0	BK3_CH2_INT_LOST_INT_EN BK3 channel2 interrupt lost interrupt enable Indicates some Interrupts of BK3 channel2 are lost 0: Disable 1: Enable
29	R/W	0x0	BK3_CH1_INT_LOST_INT_EN BK3 channel1 interrupt lost interrupt enable Indicates some Interrupts of BK3 channel1 are lost 0: Disable 1: Enable
28	R/W	0x0	BK3_CH0_INT_LOST_INT_EN BK3 channel0 interrupt lost interrupt enable Indicates some Interrupts of BK3 channel0 are lost 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x01A4			Register Name: CSIC_BK_INTPOOL2_INT_EN0_REG
Bit	Read/Write	Default/Hex	Description
27	R/W	0x0	BK2_CH3_INT_LOST_INT_EN BK2 channel3 interrupt lost interrupt enable Indicates some Interrupts of BK2 channel3 are lost 0: Disable 1: Enable
26	R/W	0x0	BK2_CH2_INT_LOST_INT_EN BK2 channel2 interrupt lost interrupt enable Indicates some Interrupts of BK2 channel2 are lost 0: Disable 1: Enable
25	R/W	0x0	BK2_CH1_INT_LOST_INT_EN BK2 channel1 interrupt lost interrupt enable Indicates some Interrupts of BK2 channel1 are lost 0: Disable 1: Enable
24	R/W	0x0	BK2_CH0_INT_LOST_INT_EN BK2 channel0 interrupt lost interrupt enable Indicates some Interrupts of BK2 channel0 are lost 0: Disable 1: Enable
23	R/W	0x0	BK1_CH3_INT_LOST_INT_EN BK1 channel3 interrupt lost interrupt enable Indicates some Interrupts of BK1 channel3 are lost 0: Disable 1: Enable
22	R/W	0x0	BK1_CH2_INT_LOST_INT_EN BK1 channel2 interrupt lost interrupt enable Indicates some Interrupts of BK1 channel2 are lost 0: Disable 1: Enable
21	R/W	0x0	BK1_CH1_INT_LOST_INT_EN BK1 channel1 interrupt lost interrupt enable Indicates some Interrupts of BK1 channel1 are lost 0: Disable 1: Enable
20	R/W	0x0	BK1_CH0_INT_LOST_INT_EN BK1 channel0 interrupt lost interrupt enable Indicates some Interrupts of BK1 channel0 are lost 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x01A4			Register Name: CSIC_BK_INTPOOL2_INT_EN0_REG
Bit	Read/Write	Default/Hex	Description
19	R/W	0x0	BK0_CH3_INT_LOST_INT_EN BK0 channel3 interrupt lost interrupt enable Indicates some Interrupts of BK0 channel3 are lost 0: Disable 1: Enable
18	R/W	0x0	BK0_CH2_INT_LOST_INT_EN BK0 channel2 interrupt lost interrupt enable Indicates some Interrupts of BK0 channel2 are lost 0: Disable 1: Enable
17	R/W	0x0	BK0_CH1_INT_LOST_INT_EN BK0 channel1 interrupt lost interrupt enable Indicates some Interrupts of BK0 channel1 are lost 0: Disable 1: Enable
16	R/W	0x0	BK0_CH0_INT_LOST_INT_EN BK0 channel0 interrupt lost interrupt enable Indicates some Interrupts of BK0 channel0 are lost 0: Disable 1: Enable
15:2	/	/	/
1	R/W	0x0	FIFO_FULL_INT_EN FIFO full interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	FIFO_AVL_INT_EN FIFO available interrupt Enable 0: Disable 1: Enable

16.1.9.69 0x01A8 CSIC BK INTERRUPT Pool2 Interrupt Enable 1 Register (Default Value: 0x0000_0000)

Offset: 0x01A8			Register Name: CSIC_BK_INTPOOL2_INT_EN1_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W	0x0	BK5_CH0_INT_LOST_INT_EN BK5 channel0 interrupt lost interrupt enable Indicates some Interrupts of BK5 channel0 are lost 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x01A8			Register Name: CSIC_BK_INTPOOL2_INT_EN1_REG
Bit	Read/Write	Default/Hex	Description
3:1	/	/	/
0	R/W	0x0	BK4_CH0_INT_LOST_INT_EN BK4 channel0 interrupt lost interrupt enable Indicates some Interrupts of BK4 channel0 are lost 0: Disable 1: Enable

16.1.9.70 0x01AC CSIC BK INTERRUPT Pool2 Interrupt Status 0 Register (Default Value: 0x0000_0000)

Offset: 0x01AC			Register Name: CSIC_BK_INTPOOL2_INT_STA0_REG
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	BK3_CH3_INT_LOST_INT_PD BK3 channel3 interrupt lost interrupt pending Indicates some Interrupts of BK3 channel3 are lost Flag 1 when pending. Write 1 to clear.
30	R/W1C	0x0	BK3_CH2_INT_LOST_INT_PD BK3 channel2 interrupt lost interrupt pending Indicates some Interrupts of BK3 channel2 are lost Flag 1 when pending. Write 1 to clear.
29	R/W1C	0x0	BK3_CH1_INT_LOST_INT_PD BK3 channel1 interrupt lost interrupt pending Indicates some Interrupts of BK3 channel1 are lost Flag 1 when pending. Write 1 to clear.
28	R/W1C	0x0	BK3_CH0_INT_LOST_INT_PD BK3 channel0 interrupt lost interrupt pending Indicates some Interrupts of BK3 channel0 are lost Flag 1 when pending. Write 1 to clear.
27	R/W1C	0x0	BK2_CH3_INT_LOST_INT_PD BK2 channel3 interrupt lost interrupt pending Indicates some Interrupts of BK2 channel3 are lost Flag 1 when pending. Write 1 to clear.
26	R/W1C	0x0	BK2_CH2_INT_LOST_INT_PD BK2 channel2 interrupt lost interrupt pending Indicates some Interrupts of BK2 channel2 are lost Flag 1 when pending. Write 1 to clear.
25	R/W1C	0x0	BK2_CH1_INT_LOST_INT_PD BK2 channel1 interrupt lost interrupt pending Indicates some Interrupts of BK2 channel1 are lost Flag 1 when pending. Write 1 to clear.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x01AC			Register Name: CSIC_BK_INTPOOL2_INT_STA0_REG
Bit	Read/Write	Default/Hex	Description
24	R/W1C	0x0	BK2_CH0_INT_LOST_INT_PD BK2 channel0 interrupt lost interrupt pending Indicates some Interrupts of BK2 channel0 are lost Flag 1 when pending. Write 1 to clear.
23	R/W1C	0x0	BK1_CH3_INT_LOST_INT_PD BK1 channel3 interrupt lost interrupt pending Indicates some Interrupts of BK1 channel3 are lost Flag 1 when pending. Write 1 to clear.
22	R/W1C	0x0	BK1_CH2_INT_LOST_INT_PD BK1 channel2 interrupt lost interrupt pending Indicates some Interrupts of BK1 channel2 are lost Flag 1 when pending. Write 1 to clear.
21	R/W1C	0x0	BK1_CH1_INT_LOST_INT_PD BK1 channel1 interrupt lost interrupt pending Indicates some Interrupts of BK1 channel1 are lost Flag 1 when pending. Write 1 to clear.
20	R/W1C	0x0	BK1_CH0_INT_LOST_INT_PD BK1 channel0 interrupt lost interrupt pending Indicates some Interrupts of BK1 channel0 are lost Flag 1 when pending. Write 1 to clear.
19	R/W1C	0x0	BK0_CH3_INT_LOST_INT_PD BK0 channel3 interrupt lost interrupt pending Indicates some Interrupts of BK0 channel3 are lost Flag 1 when pending. Write 1 to clear.
18	R/W1C	0x0	BK0_CH2_INT_LOST_INT_PD BK0 channel2 interrupt lost interrupt pending Indicates some Interrupts of BK0 channel2 are lost Flag 1 when pending. Write 1 to clear.
17	R/W1C	0x0	BK0_CH1_INT_LOST_INT_PD BK0 channel1 interrupt lost interrupt pending Indicates some Interrupts of BK0 channel1 are lost Flag 1 when pending. Write 1 to clear.
16	R/W1C	0x0	BK0_CH0_INT_LOST_INT_PD BK0 channel0 interrupt lost interrupt pending Indicates some Interrupts of BK0 channel0 are lost Flag 1 when pending. Write 1 to clear.
15:2	/	/	/
1	R/W1C	0x0	FIFO_FULL_INT_PD FIFO full interrupt pending Flag 1 when pending. Write 1 to clear.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x01AC			Register Name: CSIC_BK_INTPOOL2_INT_STA0_REG
Bit	Read/Write	Default/Hex	Description
0	R/W1C	0x0	FIFO_AVL_INT_PD FIFO available interrupt pending Flag 1 when pending. Write 1 to clear.

16.1.9.71 0x01B0 CSIC BK INTERRUPT Pool2 Interrupt Status 1 Register (Default Value: 0x0000_0000)

Offset: 0x01B0			Register Name: CSIC_BK_INTPOOL2_INT_STA1_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W1C	0x0	BK5_CH0_INT_LOST_INT_PD BK5 channel0 interrupt lost interrupt pending Indicates some Interrupts of BK5 channel0 are lost Flag 1 when pending. Write 1 to clear.
3:1	/	/	/
0	R/W1C	0x0	BK4_CH0_INT_LOST_INT_PD BK4 channel0 interrupt lost interrupt pending Indicates some Interrupts of BK4 channel0 are lost Flag 1 when pending. Write 1 to clear.

16.1.10 PHY COMMON Register Description

16.1.10.1 0x0000 PHY Top Control Register (Default Value: 0x006_0500)

Offset: 0x0000			Register Name: PHY_TOP_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:29	R/W	0x0	PHY_LINK_MODE PHY Link Selection 00: 2 x4 -lane Links (phya+phyb) + 1 x 2-lane
28:27	/	/	/
26:24	R/W	0x0	PRBS_SEL PRBS Test Interface Selection 0x0: PHYA PRBS 0x1: PHYB PRBS 0x2: PHYC PRBS Other: Reserved
23:16	R	0x36	RESERVED_REG Reserved Register
15:13	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: PHY_TOP_CTL_REG
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	PHY_SEL_VREF_0P2 PHY 0.2V Terminal Resistor Reference Voltage Source Selection 0: The reference voltage comes from PHY. 1: The reference voltage comes from the external.
11:10	R/W	0x1	PHY_VREF_0P2 PHY 0.2V Terminal Resistor Reference Voltage Fine Trimming at a step of 25 mV.
9:8	R/W	0x1	PHY_VREF_0P9 PHY 0.9V LDO Reference Voltage Fine Trimming at a step of 50 mV.
7:4	/	/	/
3	R/W	0x0	PHY_LVLDO_EN PHY 0.9V LDO Enable (High Active)
2	R/W	0x0	PHY_VREF_EN PHY Reference Voltage Enable (High Active)
1	R/W	0x0	PHY_RSTN PHY Analog Layer Digital Circuit Reset (Low Active)
0	R/W	0x0	PHY_PWDNZ PHY Analog Layer Power Reset (Low Active)

16.1.10.2 0x0004 PHY Terminal Resistor Calibration Register (Default Value: 0x0000_00a5)

Offset: 0x0004			Register Name: PHY_TRESCAL_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R	0x0	PHY_TRESCAL_RESULT PHY Terminal Resistor Calibration Result In automatic calibration mode, the result is automatic calibration output value. In software calibration mode, the result is the value of PHYA_TRESCAL_SET bit.
15:9	/	/	/
8:4	R/W	0xa	PHY_TRESCAL_SET PHY Terminal Resistor Software Calibration Set Value

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: PHY_TRESCAL_REG
Bit	Read/Write	Default/Hex	Description
3	R	0x0	PHY_TRESCAL_FLAG PHY Terminal Resistor Calibration Flag In automatic calibration mode, when the value of this bit is 1, the automatic calibration is completed. This bit is fixed as 1 in software calibration mode.
2	R/W	0x1	PHY_TRESCAL_RESETN PHY Terminal Resistor Calibration Reset This bit is only valid for automatic calibration, low active.
1	R/W	0x0	PHY_TRESCAL_SOFT PHY Terminal Resistor Software Calibration Enable (High Active)
0	R/W	0x1	PHY_TRESCAL_AUTO PHY Terminal Resistor Automatic Calibration Enable (High Active)

16.1.11 CSIC_PHY DIGITAL LAYER Register Description

16.1.11.1 0x0000 PHY Control Register (Default Value: 0x0004_0000)

Offset: 0x0000			Register Name: PHY_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	PHY0_WORK_MODE 0: Every lane of PHY0 works in MIPI mode. Others: Reserved
27	/	/	/
26	R/W	0x0	PHY0_IBIAS_EN PHY0 Reference Current Enable (High Active)
25:20	/	/	/
19	R/W	0x0	PHY0_VCM PHY0 Common Voltage Selection 0: 200mV MIPI 1: Reserved
18:16	R/W	0x4	PHY0_HS_REFI You can obtain faster speed of every lane by adjusting PHY0 HSRX reference current. The larger the value of this bit, the faster the speed of every lane.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: PHY_CTL_REG
Bit	Read/Write	Default/Hex	Description
15:13	/	/	/
12	R/W	0x0	PHY0_LP_REFI You can adjust the threshold voltage window size by adjusting LPRX reference current to filter LP noise signals effectively.
11:9	/	/	/
8	R/W	0x0	PHY_LANECK_EN PHY Clock Lane Enable
7:4	R/W	0x0	PHY_LANEDT_EN PHY Data Lane0-3 Enable Bit4: Data Lane0 Enable Bit5: Data Lane1 Enable Bit6: Data Lane2 Enable Bit7: Data Lane3 Enable 0: Disable 1: Enable
3:1	/	/	/
0	R/W	0x0	PHY_EN PHY Digital Layer Enable (High Active)

16.1.11.2 0x0004 PHY Equalization Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: PHY_EQ_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x0	PHY_EQ_LANECK0 PHY clock lane0 comparator equalization compensation value
23:22	R/W	0x0	PHY_EQ_LANED3 PHY data lane3 comparator equalization compensation value
21:20	R/W	0x0	PHY_EQ_LANED2 PHY data lane2 comparator equalization compensation value
19:18	R/W	0x0	PHY_EQ_LANED1 PHYC data lane1 comparator equalization compensation value
17:16	R/W	0x0	PHY_EQ_LANED0 PHY data lane0 comparator equalization compensation value
15:5	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: PHY_EQ_REG
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	PHY_EQ_CK_EN PHY clock lane comparator equalization enable (High Active)
3:0	R/W	0x0	PHY_EQ_DT_EN PHY data lane0-3 comparator equalization enable (high active)

16.1.11.3 0x0008 PHY Offset Calibration Register0 (Default Value: 0x0010_0010)

Offset: 0x0008			Register Name: PHY_OFSCAL_REG0
Bit	Read/Write	Default/Hex	Description
31:39	/	/	/
28	R	0x0	PHY0_OFSCAL_FLAG PHY0 Offset Calibration Flag In automatic calibration mode, when the value of this bit is 1, the automatic calibration is completed. This bit is fixed as 1 in software calibration mode.
27:21	/	/	/
20	R/W	0x1	PHY0_OFSCAL_RESETN PHY0 Offset Calibration Reset The comparator offset of every lane restarts to calibrate after reset. Note: This bit is only valid for automatic calibration mode.
19:13	/	/	/
12	R/W	0x0	PHY0_OFSCAL_SOFT PHY0 offset software calibration enable (high active)
7:6	/	/	/
4	R/W	0x1	PHY_OFSCAL_AUTO PHY0 offset automatic calibration enable (high active)
3:0	/	/	/

16.1.11.4 0x000C PHY Offset Calibration Register1 (Default Value: 0x0120_0000)

Offset: 0x000C			Register Name: PHY_OFSCAL_REG1
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x000C			Register Name: PHY_OFSCAL_REG1
Bit	Read/Write	Default/Hex	Description
24:20	R/W	0x12	PHY0_OFSCAL_SET PHY0 offset software calibration set value
19:0	/	/	/

16.1.11.5 0x0010 PHY Offset Calibration Register2 (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: PHY_OFSCAL_REG2
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:20	R	0x0	PHY0_OFSCAL_RESULT PHY0 offset calibration result In automatic calibration mode, the result is automatic calibration output value. In software calibration mode, the result is the value of PHY0_OFSCAL_SET bit.
19:0	/	/	/

16.1.11.6 0x0014 PHY Deskew Register0 (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: PHY_DESKEW_REG0
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	PHY0_DESKEW_PERIOD_STEP PHY0 data lane period deskew step precision 0: Every step is 1. 1: Every step is 2.
11:10	/	/	/
9:8	R/W	0x0	PHY0_DESKEW_STEP PHY0 data lane initial deskew step precision 00: Every step is 1. 01: Every step is 2. 10: Every step is 4. 11: Reserved
7:4	R/W	0x0	PHY_DESKEW_PERIOD_EN PHY data lane0-3 period deskew automatic delay enable (high active) Note: When using deskew, sensors should comply with MIPI DPHY protocol. Specifically, send a synchronization header of 16 ones, followed by a skew calibration sequence.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: PHY_DESKEW_REG0
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	PHY_DESKEW_EN PHY data lane0-3 deskew automatic delay enable (high active) Note: When using deskew, sensors should comply with MIPI DPHY protocol. Specifically, send a synchronization header of 16 ones, followed by a skew calibration sequence.

16.1.11.7 0x0018 PHY Deskew Register1 (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: PHY_DESKEW_REG1
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:20	R/W	0x0	PHY_DESKEW_LANECK0_SET PHY clock lane0 delay
19:15	R/W	0x0	PHY_DESKEW_LANED3_SET PHY data lane3 delay This bit is valid when PHY_DESKEW_EN[3] =0.
14:10	R/W	0x0	PHY_DESKEW_LANED2_SET PHY data lane2 delay This bit is valid when PHY_DESKEW_EN[2] =0.
9:5	R/W	0x0	PHY_DESKEW_LANED1_SET PHY data lane1 delay This bit is valid when PHY_DESKEW_EN[1] =0.
4:0	R/W	0x0	PHY_DESKEW_LANED0_SET PHY data lane0 delay This bit is valid when PHY_DESKEW_EN[0] =0.

16.1.11.8 0x001C PHY Deskew Register2 (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: PHY_DESKEW_REG2
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
24:20	R	0x0	PHY_DESKEW_LANECK0_RESULT PHY clock lane0 deskew delay result The value of this bit is equal to the value of PHY_DESKEW_LANECK0_SET bit.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x001C			Register Name: PHY_DESKEW_REG2
Bit	Read/Write	Default/Hex	Description
19:15	R	0x0	PHY_DESKEW_LANED3_RESULT PHY data lane3 deskew delay result The value of this bit is equal to the value of PHY_DESKEW_LANECK3_SET bit, when PHY_DESKEW_EN[3] =0.
14:10	R	0x0	PHY_DESKEW_LANED2_RESULT PHY data lane2 deskew delay result The value of this bit is equal to the value of PHY_DESKEW_LANECK2_SET bit, when PHY_DESKEW_EN[2] =0.
9:5	R	0x0	PHY_DESKEW_LANED1_RESULT PHY data lane1 deskew delay result The value of this bit is equal to the value of PHY_DESKEW_LANECK1_SET bit, when PHY_DESKEW_EN[1] =0.
4:0	R	0x0	PHY_DESKEW_LANED0_RESULT PHY data lane0 deskew delay result The value of this bit is equal to the value of PHY_DESKEW_LANECK0_SET bit, when PHY_DESKEW_EN[0] =0.

16.1.11.9 0x0020 PHY Terminal Control Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: PHY_TERM_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	PHY0_TERM_EN_DLY These bits are to set the delay of every clock lane and data lane from high-speed RX (LP11-LP01-LP00) request is received to the terminal resistor is enabled in hardware auto-enable mode. These bits are only valid for MIPI CSI. The unit is cmb_clk cycle.
15:5	/	/	/
4	R/W	0x0	PHY_TERMCK_EN PHY Clock Lane Terminal Resistor Software Enable 0: Hardware auto-enable 1: Software enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0020			Register Name: PHY_TERM_CTL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	PHY_TERMDT_EN PHY Data Lane 0-3 Terminal Resistor Software Enable 0: Hardware auto-enable 1: Software enable

16.1.11.10 0x0024 PHY High Speed Control Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: PHY_HS_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	PHY0_HS_DLY These bits are to set the delay of every clock lane and data lane from high-speed RX (LP11-LP01-LP00) request is received to the high-speed comparator is enabled in hardware auto-enable mode. These bits are only valid for MIPI CSI. The unit is cmb_clk cycle.
15:13	/	/	/
12	R/W	0x0	PHY_HSCK_POLAR PHY Clock Lane HSRX Signal Inversion 0: HSRX Signal is not inverse. 1: HSRX Signal is inverse.
11:8	R/W	0x0	PHY_HSDT_POLAR PHY Data Lane0-3 HSRX Signal Inversion 0: HSRX Signal is not inverse. 1: HSRX Signal is inverse.
7:5	/	/	/
4	R/W	0x0	PHY_HSCK_EN PHY Clock Lane High-Speed Mode Software Enable (High Active) 0: Hardware auto-enable 1: Software enable
3:0	R/W	0x0	PHY_HSDT_EN PHY Data Lane0-3 High-Speed Mode Software Enable (High Active) 0: Hardware auto-enable 1: Software enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.11.11 0x0028 PHY Serial to Parallel Control Register (Default Value: 0x0000_0A00)

Offset: 0x0028			Register Name: PHY_S2P_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	PHY0_S2P_DLY These bits are to set the delay of every data lane from high-speed RX request is received to the S2P circuit is enabled in hardware auto-enable mode (HS_Settle). These bits are only valid for MIPI CSI. The unit is cmb_clk cycle.
15:12	/	/	/
11:10	R	0x2	Reserved
9:8	R/W	0x2	PHY0_S2P_WIDTH PHY0 S2P Circuit Output Width 00: 2 bits 01: 4 bits 1X: 8 bits
7:4	/	/	/
3:0	R/W	0x0	PHY_S2P_EN PHY Data Lane0-3 S2P Circuit Software Enable 0: Hardware auto-enable 1: Software enable

16.1.11.12 0x002C PHY MIPIRX Control Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: PHY_MIPIRX_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	PHY0_MIPILP_DBC_EN PHY0 LPRX Debounce Circuit Enable (High Active)
15:13	/	/	/
12	R/W	0x0	PHY_MIPI_LPCK_EN PHY Clock Lane LPRX Enable 0: Disable LPRX 1: Enable LPRX
11:8	R/W	0x0	PHY_MIPI_LPDT_EN PHY Data Lane 0-3 LPRX Enable 0: Disable LPRX 1: Enable LPRX
7:5	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x002C			Register Name: PHY_MIPIRX_CTL_REG
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	PHY0_MIPIHS_8B9B 0: No 8B9B decoding when receiving bytes in PHY0 MIPI high-speed mode. 1: 8B9B decoding when receiving bytes in PHY0 MIPI high-speed mode.
3	/	/	/
2	R/W	0x0	PHY0_MIPIHS_SYNC_MODE 0: The Sync-Sequence must be 0xb8 in PHY0 MIPI high-speed mode. 1: The Sync-Sequence allows 1-bit difference from 0xb8 in PHY0 MIPI high-speed mode.
1	/	/	/
0	R/W	0x0	PHY0_MIPIHS_ENDIAN This bit is to set which one of the big-endian and little-endian to receive data in PHY0 MIPI high-speed mode. 0: LSB First 1: MSB First

16.1.11.13 0x0030 PHY MIPIRX Synchronization Timeout Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: PHY_MIPIRX_SYNC_TIMEOUT_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	PHY0_MIPIHS_SYNC_TOSET The PHY_NOSYNC_ERR_D0_PD bit and PHY_NOSYNC_ERR_D1_PD bit will generate interrupt when the Sync-Sequence (0xb8) is unable to be detected after PHY0 data lane switching from LP mode to HS mode for a period of time configured by this bit. The unit is 16 byte_clk cycles.
15:1	/	/	/
0	R/W	0x0	PHY0_MIPIHS_SYNC_TOEN PHY0 data lane HS Sync-Sequence Detection Time Out Enable (High Active)

16.1.11.14 0x0034 PHY Frequency Counter Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: PHY_FREQ_CNT_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0034			Register Name: PHY_FREQ_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	PHY_FREQ_CNT The value of these bits is the number of cmb_clk cycle during 1000 PHY byte clk cycles, which is used for byte clk frequency conversion of PHY0 or PHY1. The unit is cmb_clk cycle.
15:1	/	/	/
0	R/W	0x0	PHY0_FREQ_EN PHY0 byte_clk frequency detection enable (high active)

16.1.11.15 0x0038 PHY MIPI LP Timeout Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: PHY_MIPI_LP_TIMEOUT_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	PHY0_MIPI_LP_TIMEOUT_SET By default, the LP value will be refreshed when PHY0 MIPI LP signal bounce occurs. After enabling PHY0_MIPI_LP_TIMEOUT_EN bit, even if the signal bounce does not occur, the LP value will be refreshed after the time set by this bit. The unit is cmb_clk cycle.
15:1	/	/	/
0	R/W	0x0	PHY0_MIPI_LP_TIMEOUT_EN By default, the LP value will be refreshed when PHY0 MIPI LP signal bounce occurs. After enabling this bit, even if the signal bounce does not occur, the LP value will be refreshed after the time set by the PHY0_MIPI_LP_TIMEOUT_SET bit.

16.1.11.16 0x0040 PHY MIPI ULPSEXIT Register0 (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: PHY_MIPI_ULPSEXIT_REG0
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PHY0_MIPI_ULPS_EN Enter ULPS status after the ULPS instruction is detected by PHY0 lane.
30:20	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0040			Register Name: PHY_MIPI_ULPSEXIT_REG0
Bit	Read/Write	Default/Hex	Description
19:0	R/W	0x0	PHY0_MIPI_ULPSEXIT PHY0 lane needs to keep detecting Mark 1 signal for a certain period of time before exiting ULPS status. The unit is cmb_clk cycle.

16.1.11.17 0x0080 PHY Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: PHY_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	PHY_LP_CK0_CMD_EN PHY clock lane0 interrupt generation enable after receiving recognizable LP commands.
15	R/W	0x0	PHY_LP_D3_CMD_EN PHY data lane3 interrupt generation enable after receiving recognizable LP commands.
14	R/W	0x0	PHY_LP_D2_CMD_EN PHY data lane2 interrupt generation enable after receiving recognizable LP commands.
13	R/W	0x0	PHY_LP_D1_CMD_EN PHY data lane1 interrupt generation enable after receiving recognizable LP commands.
12	R/W	0x0	PHY_LP_D0_CMD_EN PHY data lane0 interrupt generation enable after receiving recognizable LP commands.
11	R/W	0x0	PHY_NOSYNC_ERR_D3_EN PHY Sync-Sequence Error Interrupt Generation Enable This bit is to enable the interrupt generation when the Sync-Sequence is unable to be detected after data lane3 switching from LP mode to HS mode for a period of time.
10	R/W	0x0	PHY_NOSYNC_ERR_D2_EN PHY Sync-Sequence Error Interrupt Generation Enable This bit is to enable the interrupt generation when the Sync-Sequence is unable to be detected after data lane2 switching from LP mode to HS mode for a period of time.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0080			Register Name: PHY_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
9	R/W	0x0	PHY_NOSYNC_ERR_D1_EN PHY Sync-Sequence Error Interrupt Generation Enable This bit is to enable the interrupt generation when the Sync-Sequence is unable to be detected after data lane1 switching from LP mode to HS mode for a period of time.
8	R/W	0x0	PHY_NOSYNC_ERR_D0_EN PHY Sync-Sequence Error Interrupt Generation Enable This bit is to enable the interrupt generation when the Sync-Sequence is unable to be detected after data lane0 switching from LP mode to HS mode for a period of time.
7	R/W	0x0	PHY_SYNC_ERR_D3_EN This bit is to enable the interrupt generation when 1-bit error is detected in the data lane3 Sync-Sequence.
6	R/W	0x0	PHY_SYNC_ERR_D2_EN This bit is to enable the interrupt generation when 1-bit error is detected in the data lane2 Sync-Sequence.
5	R/W	0x0	PHY_SYNC_ERR_D1_EN This bit is to enable the interrupt generation when 1-bit error is detected in the data lane1 Sync-Sequence.
4	R/W	0x0	PHY_SYNC_ERR_D0_EN This bit is to enable the interrupt generation when 1-bit error is detected in the data lane0 Sync-Sequence.
3	R/W	0x0	PHY_SOTDET_D3_EN Data lane3 generates an interrupt after detecting the Sync-Sequence.
2	R/W	0x0	PHY_SOTDET_D2_EN Data lane2 generates an interrupt after detecting the Sync-Sequence.
1	R/W	0x0	PHY_SOTDET_D1_EN Data lane1 generates an interrupt after detecting the Sync-Sequence.
0	R/W	0x0	PHY_SOTDET_D0_EN Data lane0 generates an interrupt after detecting the Sync-Sequence.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.11.18 0x0084 PHY Interrupt Pending Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: PHY_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W1C	0x0	PHY_LP_CK0_CMD_PD PHY clock lane0 generates an interrupt after receiving recognizable LP commands.
15	R/W1C	0x0	PHY_LP_D3_CMD_PD PHY data lane3 generates an interrupt after receiving recognizable LP commands.
14	R/W1C	0x0	PHY_LP_D2_CMD_PD PHY data lane2 generates an interrupt after receiving recognizable LP commands.
13	R/W1C	0x0	PHY_LP_D1_CMD_PD PHY data lane1 generates an interrupt after receiving recognizable LP commands.
12	R/W1C	0x0	PHY_LP_D0_CMD_PD PHY data lane0 generates an interrupt after receiving recognizable LP commands.
11	R/W1C	0x0	PHY_NOSYNC_ERR_D3_PD Generate an interrupt when the Sync-Sequence is unable to be detected after data lane3 switching from LP mode to HS mode for a period of time.
10	R/W1C	0x0	PHY_NOSYNC_ERR_D2_PD Generate an interrupt when the Sync-Sequence is unable to be detected after data lane2 switching from LP mode to HS mode for a period of time.
9	R/W1C	0x0	PHY_NOSYNC_ERR_D1_PD Generate an interrupt when the Sync-Sequence is unable to be detected after data lane1 switching from LP mode to HS mode for a period of time.
8	R/W1C	0x0	PHY_NOSYNC_ERR_D0_PD Generate an interrupt when the Sync-Sequence is unable to be detected after data lane0 switching from LP mode to HS mode for a period of time.
7	R/W1C	0x0	PHY_SYNC_ERR_D3_PD Generate an interrupt when 1-bit error is detected in the data lane3 Sync-Sequence.
6	R/W1C	0x0	PHY_SYNC_ERR_D2_PD Generate an interrupt when 1-bit error is detected in the data lane2 Sync-Sequence.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0084			Register Name: PHY_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
5	R/W1C	0x0	PHY_SYNC_ERR_D1_PD Generate an interrupt when 1-bit error is detected in the data lane1 Sync-Sequence.
4	R/W1C	0x0	PHY_SYNC_ERR_D0_PD Generate an interrupt when 1-bit error is detected in the data lane0 Sync-Sequence.
3	R/W1C	0x0	PHY_SOTDET_D3_PD Data lane3 generates an interrupt after detecting the Sync-Sequence.
2	R/W1C	0x0	PHY_SOTDET_D2_PD Data lane2 generates an interrupt after detecting the Sync-Sequence.
1	R/W1C	0x0	PHY_SOTDET_D1_PD Data lane1 generates an interrupt after detecting the Sync-Sequence.
0	R/W1C	0x0	PHY_SOTDET_D0_PD Data lane0 generates an interrupt after detecting the Sync-Sequence.

16.1.11.19 0x00E0 PHY Deskew Register3 (Default Value: 0x0000_0000)

Offset: 0x00E0			Register Name: PHY_DESKEW_REG3
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:24	R	0x0	PHY_LANE3_DLY_MATCH_LEN PHY lane3 auto deskew result, which is a consecutive length of available delay step. The final selection is the midpoint of this segment length. For example, a delay step of 3-15 is available; then, the length is 12 and the result chosen is 9.
23:22	/	/	/
21:16	R	0x0	PHY_LANE2_DLY_MATCH_LEN PHY lane2 auto deskew result, which is a consecutive length of available delay step.
15:14	/	/	/
13:8	R	0x0	PHY_LANE1_DLY_MATCH_LEN PHY lane1 auto deskew result, which is a consecutive length of available delay step.
7:6	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00E0			Register Name: PHY_DESKEW_REG3
Bit	Read/Write	Default/Hex	Description
5:0	R	0x0	PHY_LANE0_DLY_MATCH_LEN PHY lane0 auto deskew result, which is a consecutive length of available delay step.

16.1.12 CSIC_PHY PORT PAYLOAD LAYER Register Description

16.1.12.1 0x0000 PORT Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: PORT_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PORT_OUT_NUM Port Out Number 0: Output 1 data every valid 1: Output 2 data every valid
30:18	/	/	/
17:16	R/W	0x0	PORT_CHANNEL_NUM Port Channel Number 0: 1 channel 1: 2 channels 2: 3 channels 3: 4 channels
15:12	/	/	/
11:8	R/W	0x0	PORT_LANE_NUM Port Lane Number MIPI: 1-4 PORT0 and PORT1 support 4 lanes. PORT2 supports 2 lanes.
7:6	/	/	/
5:4	R/W	0x0	PORT_WORK_MODE 00: PORT channels work in MIPI mode.
3:1	/	/	/
0	R/W	0x0	PORT_EN PORT Channel Enable (High Active)

16.1.12.2 0x0004 PORT Lane Mapping Register0 (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: PORT_LANE_MAP_REG0
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: PORT_LANE_MAP_REG0
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	PORT_LANE3_ID Port Lane3 ID 0x0: Set lane0 (PHYA lane0) as PORT LANE3 0x1: Set lane1 (PHYA lane1) as PORT LANE3 0x2: Set lane2 (PHYA lane2) as PORT LANE3 0x3: Set lane3 (PHYA lane3) as PORT LANE3 0x4: Set lane4 (PHYB lane0) as PORT LANE3 0x5: Set lane5 (PHYB lane1) as PORT LANE3 0x6: Set lane6 (PHYB lane2) as PORT LANE3 0x7: Set lane7 (PHYB lane3) as PORT LANE3 0x8: Set lane8 (PHYC lane0) as PORT LANE3 0x9: Set lane9 (PHYC lane1) as PORT LANE3
11:8	R/W	0x0	PORT_LANE2_ID Port Lane2 ID 0x0: Set lane0 (PHYA lane0) as PORT LANE2 0x1: Set lane1 (PHYA lane1) as PORT LANE2 0x2: Set lane2 (PHYA lane2) as PORT LANE2 0x3: Set lane3 (PHYA lane3) as PORT LANE2 0x4: Set lane4 (PHYB lane0) as PORT LANE2 0x5: Set lane5 (PHYB lane1) as PORT LANE2 0x6: Set lane6 (PHYB lane2) as PORT LANE2 0x7: Set lane7 (PHYB lane3) as PORT LANE2 0x8: Set lane8 (PHYC lane0) as PORT LANE2 0x9: Set lane9 (PHYC lane1) as PORT LANE2
7:4	R/W	0x0	PORT_LANE1_ID Port Lane1 ID 0x0: Set lane0 (PHYA lane0) as PORT LANE1 0x1: Set lane1 (PHYA lane1) as PORT LANE1 0x2: Set lane2 (PHYA lane2) as PORT LANE1 0x3: Set lane3 (PHYA lane3) as PORT LANE1 0x4: Set lane4 (PHYB lane0) as PORT LANE1 0x5: Set lane5 (PHYB lane1) as PORT LANE1 0x6: Set lane6 (PHYB lane2) as PORT LANE1 0x7: Set lane7 (PHYB lane3) as PORT LANE1 0x8: Set lane8 (PHYC lane0) as PORT LANE1 0x9: Set lane9 (PHYC lane1) as PORT LANE1

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: PORT_LANE_MAP_REG0
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	PORT_LANE0_ID Port Lane1 ID 0x0: Set lane0 (PHYA lane0) as PORT LANE0 0x1: Set lane1 (PHYA lane1) as PORT LANE0 0x2: Set lane2 (PHYA lane2) as PORT LANE0 0x3: Set lane3 (PHYA lane3) as PORT LANE0 0x4: Set lane4 (PHYB lane0) as PORT LANE0 0x5: Set lane5 (PHYB lane1) as PORT LANE0 0x6: Set lane6 (PHYB lane2) as PORT LANE0 0x7: Set lane7 (PHYB lane3) as PORT LANE0 0x8: Set lane8 (PHYC lane0) as PORT LANE0 0x9: Set lane9 (PHYC lane1) as PORT LANE0

16.1.12.3 0x000C PORT WDR Mode Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: PORT_WDR_MODE_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	PORT_WDR_MODE Port WDR Mode 0x0: Normal mode, No WDR, MIPI VC, or MIPIDT. 0x2: Pixel data mode, distinguish the multi-channel WDR/HR images through the first pixel data of each line. others: Reserved

16.1.12.4 0x0010 PORT Frame ID Select Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: PORT_FID_SEL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PORT_FID_MODE 0: Identify the Frame in bit cs mode. For example, identify Frame0 when FID [0] =1, identify Frame1 when FID [1] =1. 1: Identify the Frame in bit value mode. For example, identify Frame0 when FID [0] =0, identify Frame1 when FID [0] =1.
30:20	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0010			Register Name: PORT_FID_SEL_REG
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0x0	PORT_FID_MAP_EN FID Mapping Enable Bit19: FID3_MAP_EN Bit18: FID2_MAP_EN Bit17: FID1_MAP_EN Bit16: FID0_MAP_EN
15:12	R/W	0x0	PORT_FID3_MAP These bits indicate the bit position with a 16-bit high-order aligned address for FID3 in the first pixel data of every line.
11:8	R/W	0x0	PORT_FID2_MAP These bits indicate the bit position with a 16-bit high-order aligned address for FID2 in the first pixel data of every line.
7:4	R/W	0x0	PORT_FID1_MAP These bits indicate the bit position with a 16-bit high-order aligned address for FID1 in the first pixel data of every line.
3:0	R/W	0x0	PORT_FID0_MAP These bits indicate the bit position with a 16-bit high-order aligned address for FID0 in the first pixel data of every line.

16.1.12.5 0x0100 PORT MIPI Configuration Register (Default Value: 0x4920_0000)

Offset: 0x0100			Register Name: PORT_MIPI_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:26	R/W	0x12	MIPI_REAR_EMB_DTYPE MIPI Rear Embedded Data Type Value
25:20	R/W	0x12	MIPI_FRONT_EMB_DTYPE MIPI Front Embedded Data Type Value
19	R/W	0x0	MIPI_EMB_MAP The MIPI received embedded data is output in a certain format. 0: Output in the pixel format of the corresponding channel. 1: Output in RAW8 format.
18	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0100			Register Name: PORT_MIPI_CFG_REG
Bit	Read/Write	Default/Hex	Description
17:16	R/W	0x0	MIPI_YUV_SEQ MIPI YUV Format Transmission Sequence 00: YUYV 01: YVYU 10: UYVY 11: VYUY
15:10	/	/	/
9	R/W	0x0	MIPI_FRAME_SYNC_ONLY_FS MIPI Frame Synchronization only for Frame Start 0: No support 1: Support
8	R/W	0x0	MIPI_LINE_SYNC_EN MIPI Line Synchronization Enable 0: Generate line sync signals based on long packets 1: Generate line sync signals based on short packets
7	R/W	0x0	MIPI_PL_BITORD MIPI RX Payload Bit Sequence 0: LSb First 1: MSb First
6	R/W	0x0	MIPI_PH_BITORD MIPI Packet Header Bit Sequence (for ECC checksum) 0: LSb First, for example, {WC[15:8],WC[7:0], DI[7:0]} 1: MSb First, for example,{WC[8:15],WC[0:7], DI[0:7]}
5:4	R/W	0x0	MIPI_PH_BYTEORD MIPI Packet Header Byte Sequence (for ECC check) 0: {WCH, WCL, DI} 1: {DI, WCH, WCL} 2: {WCL, WCH, DI} 3: {DI,WCL,WCH}
3	R/W	0x0	MIPI_USER_DEF_EN MIPI USER Define Data Type Enable
2	R/W	0x0	EMBED_EN embed data receiving enable and output in the pixel format of the corresponding channel.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0100			Register Name: PORT_MIPI_CFG_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	MIPI_NO_UNPACK_ALL **MIPI_UNPACK_EN=0**: Receive data directly without unpacking. **MIPI_NO_UNPACK_ALL=0**: Only receive effective high-speed data without unpacking and output them from PORT Channel0 in RAW8 format. **MIPI_NO_UNPACK_ALL =1**: Receive rxhs_active, rxhs_valid, and rxhs_data[7:0] simultaneously as RX data and output them from PORT Channel0 in {2 h0, rxhs_active, rxhs_valid, rxhs_data[7:0]} sequence in RAW12 format.
0	R/W	0x0	MIPI_UNPACK_EN MIPI CSI2 Protocol Unpack Enable

16.1.12.6 0x0104 PORT MIPI No Unpacket Number Register (Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: PORT_MIPI_NO_UNPAK_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:00	R/W	0x0	MIPI_NO_UNPAK_NUM_REG This bit indicates the number of received raw data. The unit is pixel component.

16.1.12.7 0x0108 PORT MIPI Data Identity Register (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: PORT_MIPI_DI_REG
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	MIPI_CH3_VC MIPI Channel3 VC Number Set
29:24	R/W	0x0	MIPI_CH3_DT MIPI Channel3 Data Type Set
23:22	R/W	0x0	MIPI_CH2_VC MIPI channel2 VC Number Set
21:16	R/W	0x0	MIPI_CH2_DT MIPI Channel2 Data Type Set
15:14	R/W	0x0	MIPI_CH1_VC MIPI Channel1 VC Number Set
13:8	R/W	0x0	MIPI_CH1_DT MIPI Channel1 Data Type Set

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0108			Register Name: PORT_MIPI_DI_REG
Bit	Read/Write	Default/Hex	Description
7:6	R/W	0x0	MIPI_CH0_VC MIPI channel0 VC Number Set
5:0	R/W	0x0	MIPI_CH0_DT MIPI Channel0 Data Type Set/Real Mapping of USER Define Data Type

16.1.12.8 0x010C PORT MIPI User Data Type Register (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: PORT_MIPI_USER_DT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MIPI_USER3_DT_EN Channel3 MIPI USER Define Data Type Enable
30	/	/	/
29:24	R/W	0x0	MIPI_USER3_DT Channel3 MIPI USER Define Data Type This bit is to identify the data belonging to channel3, which is unpacked into the data type set by the MIPI_CH3_DT bit following CSI2 protocol.
23	R/W	0x0	MIPI_USER2_DT_EN Channel2 MIPI USER Define Data Type Enable
22	/	/	/
21:16	R/W	0x0	MIPI_USER2_DT Channel2 MIPI USER Define Data Type This bit is to identify the data belonging to channel2, which is unpacked into the data type set by the MIPI_CH2_DT bit following CSI2 protocol.
15	R/W	0x0	MIPI_USER1_DT_EN Channel1 MIPI USER Define Data Type Enable
14	/	/	/
13:8	R/W	0x0	MIPI_USER1_DT Channel1 MIPI USER Define Data Type This bit is to identify the data belonging to channel1, which is unpacked into the data type set by the MIPI_CH1_DT bit following CSI2 protocol.
7	R/W	0x0	MIPI_USER0_DT_EN Channel0 MIPI USER Define Data Type
6	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x010C			Register Name: PORT_MIPI_USER_DT_REG
Bit	Read/Write	Default/Hex	Description
5:0	R/W	0x0	MIPI_USER0_DT Channel0 MIPI USER Define Data Type This bit is to identify the data belonging to channel0, which is unpacked into the data type set by the MIPI_CH0_DT bit following CSI2 protocol.

16.1.12.9 0x0110 PORT MIPI Channel0 Data Type Trigger Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: PORT_MIPI_CH0_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MIPI_FIELD_REV Field Polarity 0: Positive (frm num [0] =1 indicate odd, =0 indicate even) 1: Negative (frm num [0] =0 indicate odd, =1 indicate even) This bit is only valid when MIPI_SRC_IS_FIELD = 1.
30	R/W	0x0	MIPI_SRC_IS_FIELD 0: The MIPI input is progressive data. 1: The MIPI input is interlaced data.
29	R/W	0x0	MIPI_RAW_EXTEND Data Type RAW24/20/16 to RAW12/10/8 0: Masked 1: Enable
28:20	/	/	/
19	R/W	0x0	RAW RAW Long Packet Data Type 0x28 to 0x2F Trigger Enable: 0: Masked 1: Enabled
18	R/W	0x0	RGB RGB Long Packet Data Type 0x20 to 0x27 Trigger Enable: 0: Masked 1: Enabled
17	R/W	0x0	YUV YUV Long Packet Data Type 0x18 to 0x1F Trigger Enable: 0: Masked 1: Enabled

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0110			Register Name: PORT_MIPI_CH0_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	GL Generic 8bit Long Packet Data Type 0x10 to 0x17 Trigger Enable: 0: Masked 1: Enabled
15	R/W	0x0	GS7 Generic 8bit Short Packet Data Type 0x0F Trigger Enable: 0: Masked 1: Enabled
14	R/W	0x0	GS6 Generic Short Packet Data Type 0x0E Trigger Enable: 0: Masked 1: Enabled
13	R/W	0x0	GS5 Generic Short Packet Data Type 0x0D Trigger Enable: 0: Masked 1: Enabled
12	R/W	0x0	GS4 Generic Short Packet Data Type 0x0C Trigger Enable: 0: Masked 1: Enabled
11	R/W	0x0	GS3 Generic Short Packet Data Type 0x0B Trigger Enable: 0: Masked 1: Enabled
10	R/W	0x0	GS2 Generic Short Packet Data Type 0x0A Trigger Enable: 0: Masked 1: Enabled
9	R/W	0x0	GS1 Generic Short Packet Data Type 0x09 Trigger Enable: 0: Masked 1: Enabled
8	R/W	0x0	GS0 Generic Short Packet Data Type 0x08 Trigger Enable: 0: Masked 1: Enabled
7:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0110			Register Name: PORT_MIPI_CH0_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	LE Data Type 0x03 Trigger Enable: 0: Masked 1: Enabled
2	R/W	0x0	LS Data Type 0x02 Trigger Enable: 0: Masked 1: Enabled
1	R/W	0x0	FE Data Type 0x01 Trigger Enable: 0: Masked 1: Enabled
0	R/W	0x0	FS Data Type 0x00 Trigger Enable: 0: Masked 1: Enabled

16.1.12.10 0x0114 PORT MIPI Channel0 Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: PORT_MIPI_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	EOT_ERR_INT_EN EOT error interrupt enable
11	R/W	0x0	CHKSUM_ERR_INT_EN Checksum error interrupt enable
10	R/W	0x0	ECC_ERR_INT_EN ECC error interrupt enable
9	R/W	0x0	ECC_WRN_INT_EN ECC warning interrupt enable
8	R/W	0x0	LINE_SYNC_ERR_INT_EN Line synchronization error interrupt enable
7	R/W	0x0	FRAME_SYNC_ERR_INT_EN Frame synchronization error interrupt enable
6	R/W	0x0	EMBED_SYNC_INT_EN Embedded data interrupt enable
5	R/W	0x0	LINE_END_SYNC_INT_EN LE synchronization interrupt enable
4	R/W	0x0	LINE_START_SYNC_INT_EN LS synchronization interrupt enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0114			Register Name: PORT_MIPI_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	FRAME_END_SYNC_INT_EN FE synchronization interrupt enable
2	R/W	0x0	FRAME_START_SYNC_INT_EN FS synchronization interrupt enable 0: Disable 1: Enable
1	R/W	0x0	PF_SYNC_INT_EN Packet Footer detected interrupt enable 0: Disable 1: Enable
0	R/W	0x0	PH_SYNC_INT_EN Packet Header update interrupt enable 0: Disable 1: Enable

16.1.12.11 0x0118 PORT MIPI Channel0 Interrupt Pending Register (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: PORT_MIPI_CH0_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W1C	0x0	EOT_ERR_INT_PD EOT error interrupt
11	R/W1C	0x0	CHKSUM_ERR_INT_PD Checksum error interrupt
10	R/W1C	0x0	ECC_ERR_INT_PD ECC error interrupt
9	R/W1C	0x0	ECC_WRN_INT_PD ECC warning interrupt
8	R/W1C	0x0	LINE_SYNC_ERR_INT_PD Line synchronization error interrupt
7	R/W1C	0x0	FRAME_SYNC_ERR_INT_PD Frame synchronization error interrupt
6	R/W1C	0x0	EMBED_SYNC_INT_PD Embedded data interrupt
5	R/W1C	0x0	LINE_END_SYNC_INT_PD LE synchronization interrupt
4	R/W1C	0x0	LINE_START_SYNC_INT_PD LS synchronization interrupt
3	R/W1C	0x0	FRAME_END_SYNC_INT_PD FE synchronization interrupt

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0118			Register Name: PORT_MIPI_CH0_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
2	R/W1C	0x0	FRAME_START_SYNC_INT_PD FS synchronization interrupt
1	R/W1C	0x0	PF_SYNC_INT_PD Packet Footer detected interrupt
0	R/W1C	0x0	PH_SYNC_INT_PD Packet Header update interrupt

16.1.12.12 0x011C PORT MIPI Channel0 Packet Header Register (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: PORT_MIPI_CH0_PH_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	MIPI_CUR_WC MIPI current Word Counter
15:8	/	/	/
7:6	R	0x0	MIPI_CUR_VC MIPI current Virtual Channel
5:0	R	0x0	PORT_MIPI_CUR_DT MIPI current Data Type

16.1.12.13 0x0120 PORT MIPI Channel0 ECC Register (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: PORT_MIPI_CH0_ECC_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R	0x0	MIPI_CAL_ECC MIPI calculated ECC
15:8	/	/	/
7:0	R	0x0	MIPI_RXD_ECC MIPI received ECC

16.1.12.14 0x0124 PORT MIPI Channel0 Checksum Register (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: PORT_MIPI_CH0_CKSUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	MIPI_CAL_CKSUM MIPI calculated Checksum
15:0	R	0x0	MIPI_RXD_CKSUM MIPI received Checksum

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.12.15 0x0128 PORT MIPI Channel0 Frame Number Register (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: PORT_MIPI_CH0_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	FRAME_NUM Update when FRAME_START_SYNC_INT_PD and FRAME_END_SYNC_INT_PD comes

16.1.12.16 0x012C PORT MIPI Channel0 Line Number Register (Default Value: 0x0000_0000)

Offset: 0x012C			Register Name: PORT_MIPI_CH0_LINE_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	LINE_NUM Update when LINE_START_SYNC_INT_PD and LINE_END_SYNC_INT_PD comes

16.1.12.17 0x0130 PORT MIPI Channel1 Data Type Trigger Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: PORT_MIPI_CH1_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MIPI_FIELD_REV Field Polarity 0: Positive (frm num [0] =1 indicate odd, =0 indicate even) 1: Negative (frm num [0] =0 indicate odd, =1 indicate even) This bit is only valid when MIPI_SRC_IS_FIELD = 1.
30	R/W	0x0	MIPI_SRC_IS_FIELD 0: The MIPI input is progressive data. 1: The MIPI input is interlaced data.
29	R/W	0x0	MIPI_RAW_EXTEND Data Type RAW24/20/16 to RAW12/10/8 0: Masked 1: Enable
28:20	/	/	/
19	R/W	0x0	RAW RAW Long Packet Data Type 0x28 to 0x2F Trigger Enable: 0: Masked 1: Enabled

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0130			Register Name: PORT_MIPI_CH1_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
18	R/W	0x0	RGB RGB Long Packet Data Type 0x20 to 0x27 Trigger Enable: 0: Masked 1: Enabled
17	R/W	0x0	YUV YUV Long Packet Data Type 0x18 to 0x1F Trigger Enable: 0: Masked 1: Enabled
16	R/W	0x0	GL Generic 8bit Long Packet Data Type 0x10 to 0x17 Trigger Enable: 0: Masked 1: Enabled
15	R/W	0x0	GS7 Generic 8bit Short Packet Data Type 0x0F Trigger Enable: 0: Masked 1: Enabled
14	R/W	0x0	GS6 Generic Short Packet Data Type 0x0E Trigger Enable: 0: Masked 1: Enabled
13	R/W	0x0	GS5 Generic Short Packet Data Type 0x0D Trigger Enable: 0: Masked 1: Enabled
12	R/W	0x0	GS4 Generic Short Packet Data Type 0x0C Trigger Enable: 0: Masked 1: Enabled
11	R/W	0x0	GS3 Generic Short Packet Data Type 0x0B Trigger Enable: 0: Masked 1: Enabled
10	R/W	0x0	GS2 Generic Short Packet Data Type 0x0A Trigger Enable: 0: Masked 1: Enabled

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0130			Register Name: PORT_MIPI_CH1_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
9	R/W	0x0	GS1 Generic Short Packet Data Type 0x09 Trigger Enable: 0: Masked 1: Enabled
8	R/W	0x0	GS0 Generic Short Packet Data Type 0x08 Trigger Enable: 0: Masked 1: Enabled
7:4	/	/	/
3	R/W	0x0	LE Data Type 0x03 Trigger Enable: 0: Masked 1: Enabled
2	R/W	0x0	LS Data Type 0x02 Trigger Enable: 0: Masked 1: Enabled
1	R/W	0x0	FE Data Type 0x01 Trigger Enable: 0: Masked 1: Enabled
0	R/W	0x0	FS Data Type 0x00 Trigger Enable: 0: Masked 1: Enabled

16.1.12.18 0x0134 PORT MIPI Channel1 Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: PORT_MIPI_CH1_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	EOT_ERR_INT_EN EOT error interrupt enable
11	R/W	0x0	CHKSUM_ERR_INT_EN Checksum error interrupt enable
10	R/W	0x0	ECC_ERR_INT_EN ECC error interrupt enable
9	R/W	0x0	ECC_WRN_INT_EN ECC warning interrupt enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0134			Register Name: PORT_MIPI_CH1_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
8	R/W	0x0	LINE_SYNC_ERR_INT_EN Line synchronization error interrupt enable
7	R/W	0x0	FRAME_SYNC_ERR_INT_EN Frame synchronization error interrupt enable
6	R/W	0x0	EMBED_SYNC_INT_EN Embedded data interrupt enable
5	R/W	0x0	LINE_END_SYNC_INT_EN LE synchronization interrupt enable
4	R/W	0x0	LINE_START_SYNC_INT_EN LS synchronization interrupt enable
3	R/W	0x0	FRAME_END_SYNC_INT_EN FE synchronization interrupt enable
2	R/W	0x0	FRAME_START_SYNC_INT_EN FS synchronization interrupt enable 0: Disable 1: Enable
1	R/W	0x0	PF_SYNC_INT_EN Packet Footer detected interrupt enable 0: Disable 1: Enable
0	R/W	0x0	PH_SYNC_INT_EN Packet Header update interrupt enable 0: Disable 1: Enable

16.1.12.19 0x0138 PORT MIPI Channel1 Interrupt Pending Register (Default Value: 0x0000_0000)

Offset: 0x0138			Register Name: PORT_MIPI_CH1_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W1C	0x0	EOT_ERR_INT_PD EOT error interrupt
11	R/W1C	0x0	CHKSUM_ERR_INT_PD Checksum error interrupt
10	R/W1C	0x0	ECC_ERR_INT_PD ECC error interrupt
9	R/W1C	0x0	ECC_WRN_INT_PD ECC warning interrupt
8	R/W1C	0x0	LINE_SYNC_ERR_INT_PD Line synchronization error interrupt

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0138			Register Name: PORT_MIPI_CH1_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
7	R/W1C	0x0	FRAME_SYNC_ERR_INT_PD Frame synchronization error interrupt
6	R/W1C	0x0	EMBED_SYNC_INT_PD Embedded data interrupt
5	R/W1C	0x0	LINE_END_SYNC_INT_PD LE synchronization interrupt
4	R/W1C	0x0	LINE_START_SYNC_INT_PD LS synchronization interrupt
3	R/W1C	0x0	FRAME_END_SYNC_INT_PD FE synchronization interrupt
2	R/W1C	0x0	FRAME_START_SYNC_INT_PD FS synchronization interrupt
1	R/W1C	0x0	PF_SYNC_INT_PD Packet Footer detected interrupt
0	R/W1C	0x0	PH_SYNC_INT_PD Packet Header update interrupt

16.1.12.20 0x013C PORT MIPI Channel1 Packet Header Register (Default Value: 0x0000_0000)

Offset: 0x013C			Register Name: PORT_MIPI_CH1_PH_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	MIPI_CUR_WC MIPI current Word Counter
15:8	/	/	/
7:6	R	0x0	MIPI_CUR_VC MIPI current Virtual Channel
5:0	R	0x0	PORT_MIPI_CUR_DT MIPI current Data Type

16.1.12.21 0x0140 PORT MIPI Channel1 ECC Register (Default Value: 0x0000_0000)

Offset: 0x0140			Register Name: PORT_MIPI_CH1_ECC_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R	0x0	MIPI_CAL_ECC MIPI calculated ECC
15:8	/	/	/
7:0	R	0x0	MIPI_RXD_ECC MIPI received ECC

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.12.22 0x0144 PORT MIPI Channel1 Checksum Register (Default Value: 0x0000_0000)

Offset: 0x0144			Register Name: PORT_MIPI_CH1_CKSUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	MIPI_CAL_CKSUM MIPI calculated Checksum
15:0	R	0x0	MIPI_RXD_CKSUM MIPI received Checksum

16.1.12.23 0x0148 PORT MIPI Channel1 Frame Number Register (Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: PORT_MIPI_CH1_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	FRAME_NUM Update when FRAME_START_SYNC_INT_PD and FRAME_END_SYNC_INT_PD comes

16.1.12.24 0x014C PORT MIPI Channel1 Line Number Register (Default Value: 0x0000_0000)

Offset: 0x014C			Register Name: PORT_MIPI_CH1_LINE_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	LINE_NUM Update when LINE_START_SYNC_INT_PD and LINE_END_SYNC_INT_PD comes

16.1.12.25 0x0150 PORT MIPI Channel2 Data Type Trigger Register (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: PORT_MIPI_CH2_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MIPI_FIELD_REV Field Polarity 0: Positive (frm num [0] =1 indicate odd, =0 indicate even) 1: Negative (frm num [0] =0 indicate odd, =1 indicate even) This bit is only valid when MIPI_SRC_IS_FIELD = 1.
30	R/W	0x0	MIPI_SRC_IS_FIELD 0: The MIPI input is progressive data. 1: The MIPI input is interlaced data.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0150			Register Name: PORT_MIPI_CH2_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
29	R/W	0x0	MIPI_RAW_EXTEND Data Type RAW24/20/16 to RAW12/10/8 0: Masked 1: Enable
28:20	/	/	/
19	R/W	0x0	RAW RAW Long Packet Data Type 0x28 to 0x2F Trigger Enable: 0: Masked 1: Enabled
18	R/W	0x0	RGB RGB Long Packet Data Type 0x20 to 0x27 Trigger Enable: 0: Masked 1: Enabled
17	R/W	0x0	YUV YUV Long Packet Data Type 0x18 to 0x1F Trigger Enable: 0: Masked 1: Enabled
16	R/W	0x0	GL Generic 8bit Long Packet Data Type 0x10 to 0x17 Trigger Enable: 0: Masked 1: Enabled
15	R/W	0x0	GS7 Generic 8bit Short Packet Data Type 0x0F Trigger Enable: 0: Masked 1: Enabled
14	R/W	0x0	GS6 Generic Short Packet Data Type 0x0E Trigger Enable: 0: Masked 1: Enabled
13	R/W	0x0	GS5 Generic Short Packet Data Type 0x0D Trigger Enable: 0: Masked 1: Enabled

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0150			Register Name: PORT_MIPI_CH2_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	GS4 Generic Short Packet Data Type 0x0C Trigger Enable: 0: Masked 1: Enabled
11	R/W	0x0	GS3 Generic Short Packet Data Type 0x0B Trigger Enable: 0: Masked 1: Enabled
10	R/W	0x0	GS2 Generic Short Packet Data Type 0x0A Trigger Enable: 0: Masked 1: Enabled
9	R/W	0x0	GS1 Generic Short Packet Data Type 0x09 Trigger Enable: 0: Masked 1: Enabled
8	R/W	0x0	GS0 Generic Short Packet Data Type 0x08 Trigger Enable: 0: Masked 1: Enabled
7:4	/	/	/
3	R/W	0x0	LE Data Type 0x03 Trigger Enable: 0: Masked 1: Enabled
2	R/W	0x0	LS Data Type 0x02 Trigger Enable: 0: Masked 1: Enabled
1	R/W	0x0	FE Data Type 0x01 Trigger Enable: 0: Masked 1: Enabled
0	R/W	0x0	FS Data Type 0x00 Trigger Enable: 0: Masked 1: Enabled

16.1.12.26 0x0154 PORT MIPI Channel2 Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0154	Register Name: PORT_MIPI_CH2_INT_EN_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	EOT_ERR_INT_EN EOT error interrupt enable
11	R/W	0x0	CHKSUM_ERR_INT_EN Checksum error interrupt enable
10	R/W	0x0	ECC_ERR_INT_EN ECC error interrupt enable
9	R/W	0x0	ECC_WRN_INT_EN ECC warning interrupt enable
8	R/W	0x0	LINE_SYNC_ERR_INT_EN Line synchronization error interrupt enable
7	R/W	0x0	FRAME_SYNC_ERR_INT_EN Frame synchronization error interrupt enable
6	R/W	0x0	EMBED_SYNC_INT_EN Embedded data interrupt enable
5	R/W	0x0	LINE_END_SYNC_INT_EN LE synchronization interrupt enable
4	R/W	0x0	LINE_START_SYNC_INT_EN LS synchronization interrupt enable
3	R/W	0x0	FRAME_END_SYNC_INT_EN FE synchronization interrupt enable
2	R/W	0x0	FRAME_START_SYNC_INT_EN FS synchronization interrupt enable 0: Disable 1: Enable
1	R/W	0x0	PF_SYNC_INT_EN Packet Footer detected interrupt enable 0: Disable 1: Enable
0	R/W	0x0	PH_SYNC_INT_EN Packet Header update interrupt enable 0: Disable 1: Enable

16.1.12.27 0x0158 PORT MIPI Channel2 Interrupt Pending Register (Default Value: 0x0000_0000)

Offset: 0x0158			Register Name: PORT_MIPI_CH2_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W1C	0x0	EOT_ERR_INT_PD EOT error interrupt

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0158			Register Name: PORT_MIPI_CH2_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
11	R/W1C	0x0	CHKSUM_ERR_INT_PD Checksum error interrupt
10	R/W1C	0x0	ECC_ERR_INT_PD ECC error interrupt
9	R/W1C	0x0	ECC_WRN_INT_PD ECC warning interrupt
8	R/W1C	0x0	LINE_SYNC_ERR_INT_PD Line synchronization error interrupt
7	R/W1C	0x0	FRAME_SYNC_ERR_INT_PD Frame synchronization error interrupt
6	R/W1C	0x0	EMBED_SYNC_INT_PD Embedded data interrupt
5	R/W1C	0x0	LINE_END_SYNC_INT_PD LE synchronization interrupt
4	R/W1C	0x0	LINE_START_SYNC_INT_PD LS synchronization interrupt
3	R/W1C	0x0	FRAME_END_SYNC_INT_PD FE synchronization interrupt
2	R/W1C	0x0	FRAME_START_SYNC_INT_PD FS synchronization interrupt
1	R/W1C	0x0	PF_SYNC_INT_PD Packet Footer detected interrupt
0	R/W1C	0x0	PH_SYNC_INT_PD Packet Header update interrupt

16.1.12.28 0x015C PORT MIPI Channel2 Packet Header Register (Default Value: 0x0000_0000)

Offset: 0x015C			Register Name: PORT_MIPI_CH2_PH_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	MIPI_CUR_WC MIPI current Word Counter
15:8	/	/	/
7:6	R	0x0	MIPI_CUR_VC MIPI current Virtual Channel
5:0	R	0x0	PORT_MIPI_CUR_DT MIPI current Data Type

16.1.12.29 0x0160 PORT MIPI Channel2 ECC Register (Default Value: 0x0000_0000)

Offset: 0x0160	Register Name: PORT_MIPI_CH2_ECC_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R	0x0	MIPI_CAL_ECC MIPI calculated ECC
15:8	/	/	/
7:0	R	0x0	MIPI_RXD_ECC MIPI received ECC

16.1.12.30 0x0164 PORT MIPI Channel2 Checksum Register (Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: PORT_MIPI_CH2_CKSUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	MIPI_CAL_CKSUM MIPI calculated Checksum
15:0	R	0x0	MIPI_RXD_CKSUM MIPI received Checksum

16.1.12.31 0x0168 PORT MIPI Channel2 Frame Number Register (Default Value: 0x0000_0000)

Offset: 0x0168			Register Name: PORT_MIPI_CH2_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	FRAME_NUM Update when FRAME_START_SYNC_INT_PD and FRAME_END_SYNC_INT_PD comes

16.1.12.32 0x016C PORT MIPI Channel2 Line Number Register (Default Value: 0x0000_0000)

Offset: 0x016C			Register Name: PORT_MIPI_CH2_LINE_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	LINE_NUM Update when LINE_START_SYNC_INT_PD and LINE_END_SYNC_INT_PD comes

16.1.12.33 0x0170 PORT MIPI Channel3 Data Type Trigger Register (Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: PORT_MIPI_CH3_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0170			Register Name: PORT_MIPI_CH3_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MIPI_FIELD_REV Field polarity 0: Positive (frm num [0] =1 indicate odd, =0 indicate even) 1: Negative (frm num [0] =0 indicate odd, =1 indicate even) This bit is only valid when MIPI_SRC_IS_FIELD = 1.
30	R/W	0x0	MIPI_SRC_IS_FIELD 0: The MIPI input is progressive data. 1: The MIPI input is interlaced data.
29	R/W	0x0	MIPI_RAW_EXTEND Data Type RAW24/20/16 to RAW12/10/8 0: Masked 1: Enable
28:20	/	/	/
19	R/W	0x0	RAW RAW Long Packet Data Type 0x28 to 0x2F Trigger Enable: 0: Masked 1: Enabled
18	R/W	0x0	RGB RGB Long Packet Data Type 0x20 to 0x27 Trigger Enable: 0: Masked 1: Enabled
17	R/W	0x0	YUV YUV Long Packet Data Type 0x18 to 0x1F Trigger Enable: 0: Masked 1: Enabled
16	R/W	0x0	GL Generic 8bit Long Packet Data Type 0x10 to 0x17 Trigger Enable: 0: Masked 1: Enabled
15	R/W	0x0	GS7 Generic 8bit Short Packet Data Type 0x0F Trigger Enable: 0: Masked 1: Enabled

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0170			Register Name: PORT_MIPI_CH3_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
14	R/W	0x0	GS6 Generic Short Packet Data Type 0x0E Trigger Enable: 0: Masked 1: Enabled
13	R/W	0x0	GS5 Generic Short Packet Data Type 0x0D Trigger Enable: 0: Masked 1: Enabled
12	R/W	0x0	GS4 Generic Short Packet Data Type 0x0C Trigger Enable: 0: Masked 1: Enabled
11	R/W	0x0	GS3 Generic Short Packet Data Type 0x0B Trigger Enable: 0: Masked 1: Enabled
10	R/W	0x0	GS2 Generic Short Packet Data Type 0x0A Trigger Enable: 0: Masked 1: Enabled
9	R/W	0x0	GS1 Generic Short Packet Data Type 0x09 Trigger Enable: 0: Masked 1: Enabled
8	R/W	0x0	GS0 Generic Short Packet Data Type 0x08 Trigger Enable: 0: Masked 1: Enabled
7:4	/	/	/
3	R/W	0x0	LE Data Type 0x03 Trigger Enable: 0: Masked 1: Enabled
2	R/W	0x0	LS Data Type 0x02 Trigger Enable: 0: Masked 1: Enabled
1	R/W	0x0	FE Data Type 0x01 Trigger Enable: 0: Masked 1: Enabled

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0170			Register Name: PORT_MIPI_CH3_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	FS Data Type 0x00 Trigger Enable: 0: Masked 1: Enabled

16.1.12.34 0x0174 PORT MIPI Channel3 Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: PORT_MIPI_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	EOT_ERR_INT_EN EOT error interrupt enable
11	R/W	0x0	CHKSUM_ERR_INT_EN Checksum error interrupt enable
10	R/W	0x0	ECC_ERR_INT_EN ECC error interrupt enable
9	R/W	0x0	ECC_WRN_INT_EN ECC warning interrupt enable
8	R/W	0x0	LINE_SYNC_ERR_INT_EN Line synchronization error interrupt enable
7	R/W	0x0	FRAME_SYNC_ERR_INT_EN Frame synchronization error interrupt enable
6	R/W	0x0	EMBED_SYNC_INT_EN Embedded data interrupt enable
5	R/W	0x0	LINE_END_SYNC_INT_EN LE synchronization interrupt enable
4	R/W	0x0	LINE_START_SYNC_INT_EN LS synchronization interrupt enable
3	R/W	0x0	FRAME_END_SYNC_INT_EN FE synchronization interrupt enable
2	R/W	0x0	FRAME_START_SYNC_INT_EN FS synchronization interrupt enable 0: Disable 1: Enable
1	R/W	0x0	PF_SYNC_INT_EN Packet Footer detected interrupt enable 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0174			Register Name: PORT_MIPI_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	PH_SYNC_INT_EN Packet Header update interrupt enable 0: Disable 1: Enable

16.1.12.35 0x0178 PORT MIPI Channel3 Interrupt Pending Register (Default Value: 0x0000_0000)

Offset: 0x0178			Register Name: PORT_MIPI_CH3_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W1C	0x0	EOT_ERR_INT_PD EOT error interrupt
11	R/W1C	0x0	CHKSUM_ERR_INT_PD Checksum error interrupt
10	R/W1C	0x0	ECC_ERR_INT_PD ECC error interrupt
9	R/W1C	0x0	ECC_WRN_INT_PD ECC warning interrupt
8	R/W1C	0x0	LINE_SYNC_ERR_INT_PD Line synchronization error interrupt
7	R/W1C	0x0	FRAME_SYNC_ERR_INT_PD Frame synchronization error interrupt
6	R/W1C	0x0	EMBED_SYNC_INT_PD Embedded data interrupt
5	R/W1C	0x0	LINE_END_SYNC_INT_PD LE synchronization interrupt
4	R/W1C	0x0	LINE_START_SYNC_INT_PD LS synchronization interrupt
3	R/W1C	0x0	FRAME_END_SYNC_INT_PD FE synchronization interrupt
2	R/W1C	0x0	FRAME_START_SYNC_INT_PD FS synchronization interrupt
1	R/W1C	0x0	PF_SYNC_INT_PD Packet Footer detected interrupt
0	R/W1C	0x0	PH_SYNC_INT_PD Packet Header update interrupt

16.1.12.36 0x017C PORT MIPI Channel3 Packet Header Register (Default Value: 0x0000_0000)

Offset: 0x017C	Register Name: PORT_MIPI_CH3_PH_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	MIPI_CUR_WC MIPI current Word Counter
15:8	/	/	/
7:6	R	0x0	MIPI_CUR_VC MIPI current Virtual Channel
5:0	R	0x0	PORT_MIPI_CUR_DT MIPI current Data Type

16.1.12.37 0x0180 PORT MIPI Channel3 ECC Register (Default Value: 0x0000_0000)

Offset: 0x0180			Register Name: PORT_MIPI_CH3_ECC_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R	0x0	MIPI_CAL_ECC MIPI calculated ECC
15:8	/	/	/
7:0	R	0x0	MIPI_RXD_ECC MIPI received ECC

16.1.12.38 0x0184 PORT MIPI Channel3 Checksum Register (Default Value: 0x0000_0000)

Offset: 0x0184			Register Name: PORT_MIPI_CH3_CKSUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	MIPI_CAL_CKSUM MIPI calculated Checksum
15:0	R	0x0	MIPI_RXD_CKSUM MIPI received Checksum

16.1.12.39 0x0188 PORT MIPI Channel3 Frame Number Register (Default Value: 0x0000_0000)

Offset: 0x0188			Register Name: PORT_MIPI_CH3_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	FRAME_NUM Update when FRAME_START_SYNC_INT_PD and FRAME_END_SYNC_INT_PD comes

16.1.12.40 0x018C PORT MIPI Channel3 Line Number Register (Default Value: 0x0000_0000)

Offset: 0x018C	Register Name: PORT_MIPI_CH3_LINE_NUM_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	LINE_NUM Update when LINE_START_SYNC_INT_PD and LINE_END_SYNC_INT_PD comes

16.1.12.41 0x01F0 PORT MIPI Lane Error Interrupt Register (Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: PORT_MIPI_LANE_ERR_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:4	R/W	0x0	MIPI_LANE_ACT_NO_VLD_INT_EN Data lane0-3 receive no valid data when act high interrupt enable
3:0	R/W	0x0	MIPI_LANE_FIFO_OVERFLOW_INT_EN Data lane0-3 FIFO overflow interrupt enable

16.1.12.42 0x01F4 PORT MIPI Lane Error Interrupt Pending Register (Default Value: 0x0000_0000)

Offset: 0x01F4			Register Name: PORT_MIPI_LANE_ERR_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:4	R/W1C	0x0	MIPI_LANE_ACT_NO_VLD_INT_PD Data lane0-3 receive no valid data when act high interrupt
3:0	R/W1C	0x0	MIPI_LANE_FIFO_OVERFLOW_INT_PD Data lane0-3 FIFO overflow interrupt

16.1.13 CSIC Parser0 Register Description

16.1.13.1 0x0000 CSIC Parser Enable Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CSIC_PRS_EN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MCSIC_EN MCSIC Enable 0: Reset and disable the MCSIC module 1: Enable the MCSIC module
30:17	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: CSIC_PRS_EN_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	NCSIC_EN NCSI Controller Enable 0: Reset and disable the NCSIC module 1: Enable the NCSIC module
15	R/W	0x0	PCLK_EN NCSI Pixel Clock Ge pclk input 1: Enable pclk input
14:4	/	/	/
3:2	R/W	0x0	PRS_CH_MODE Parser channel mode 00: Parser output channel 0~3 corresponding from input channel 0~3 01: Parser output channel 0~3 all from input channel 0 10: Parser output channel0 and 2 from input channel 0, output channel1 and 3 from input channel 1 11: Reserved
1	R/W	0x0	PRS_MODE Parser Mode 0: NCSI 1: MCSI
0	R/W	0x0	PRS_EN Parser Enable 0: Reset and disable the parser module 1: Enable the parser module

16.1.13.2 0x0004 CSIC Parser NCSIC Interface Configuration Register (Default Value: 0x0105_0080)

Offset: 0x0004			Register Name: CSIC_PRS_NCSIC_IF_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	YUV420_LINE_ORDER YUV420 Input Line Order 0: YUV420 input in Y-YC-Y-YC Line Order 1: YUV420 input in YC-Y-YC-Y Line Order
30	R/W	0x0	ONLY_ACT_CARE Only Care V Active 1:only care V active period
29	R/W	0x0	YUV422_SEP When input format is YUV422 16bit or Bt1120, set this bit to transfer YU,YV(2 components for each clock cycle) to Y,U,Y,V(1 component for each clock cycle)
28	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: CSIC_PRS_NCSIC_IF_CFG_REG
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0x1	FIELD_DT_PCLK_SHIFT Only for vsync detected field mode, the odd field permitted pclk shift = 4* FIELD_DT_PCLK_SHIFT
23:20	R/W	0x0	SRC_TYPE Bit 20~23 corresponding to the Source types for channel0~3 0: Progressed 1: Interlaced
19	R/W	0x0	FIELD For YUV HV timing, Field polarity 0: Negative (field=0 indicate odd, field=1 indicate even) 1: Positive (field=1 indicate odd, field=0 indicate even) For BT656 timing, Field sequence 0: Normal sequence (field 0 first) 1: Inverse sequence (field 1 first)
18	R/W	0x1	VREF_POL Vref polarity 0: Negative 1: Positive This register is not apply to CCIR656 interface.
17	R/W	0x0	HERF_POL Href polarity 0: Negative 1: Positive This register is not apply to CCIR656 interface.
16	R/W	0x1	CLK_POL Data clock type 0: Active in rising edge 1: Active in falling edge
15:14	R/W	0x0	Field_DT_MODE only valid when CSI_IF is YUV and source type is interlaced 00: by both field and vsync 01: by field 10: by vsync 11: Reserved
13	R/W	0x0	DDR_SAMPLE_MODE_EN Dual Data Rate Sample Mode Enable 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: CSIC_PRS_NCSIC_IF_CFG_REG
Bit	Read/Write	Default/Hex	Description
12:11	R/W	0x0	SEQ_8PLUS2 When select IF_DATA_WIDTH to be 8+2bit, odd/even pixel byte at CSI-D [11:4] will be rearranged to D [11:2] +2'b0 at the actual CSI data bus according to these sequences: 00: 6'bx+D[9:8], D[7:0] 01: D[9:2], 6'bx+D[1:0] 10: D[7:0], D[9:8]+6'bx 11: D[7:0], 6'bx+D[9:8]
10:8	R/W	0x0	IF_DATA_WIDTH Input Data Width 000: 8 bit data bus 001: 10 bit data bus 010: 12 bit data bus 011: 8+2bit data bus 100: 2x8/16bit data bus 101: 14 bit data bus 110: 20 bit data bus, only for packet generator 111:24 bit data bus, only for packet generator
7:6	R/W	0x2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU
5	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: CSIC_PRS_NCSIC_IF_CFG_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x0	CSI_IF YUV (separate syncs): 0x0: YUYV422/YUV420 or RAW (All data in one data bus) 0x1: 2x8 bit YUYV422 0x2: Reserved 0x3: Reserved CCIR656(embedded syncs): 0x4: BT656 1 channel 0x5: 16bit BT656(BT1120 like) 1 channel 0x6: Reserved 0x7: Reserved 0x8: BT656 2 channels (All data interleaved in one data bus) 0x9: 16bit BT656(BT1120 like) 2 channels (All data interleaved in one data bus) 0xE: BT656 4 channels (All data interleaved in one data bus) 0XF:16bit BT656(BT1120 like) 4 channels (All data interleaved in one data bus) Others: Reserved

16.1.13.3 0x0008 CSIC Parser MCSIC Interface Configuration Register (Default Value: 0x0000_0080)

Offset: 0x0008			Register Name: CSIC_PRS_MCSI_IF_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	YUV420_LINE_ORDER YUV420 Line Order 0: YUV420 input in Y-YC-Y-YC Line Order 1: YUV420 input in YC-Y-YC-Y Line Order
30:8	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: CSIC_PRS_MCSI_IF_CFG_REG
Bit	Read/Write	Default/Hex	Description
7:6	R/W	0x2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU
5:0	/	/	/

16.1.13.4 0x000C CSIC Parser Capture Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: CSIC_PRS_CAP_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:26	R/W	0x0	CH3_FPS_DS_PRD Fps down sample period 0x0: period is 1 frames 0x1: period is 2 frames 0x2: period is 3 frames 0x3: period is 4 frames 0x4: period is 5 frames (p)(p) 0xF: period is 16 frames Note: CH3_FPS_DS_PRD should be used together with CSIC_PRS_CAP_FRM_MSK_1_REG bit[31:16]. Show an example as following. When CH3_FPS_DS_PRD is configured as 4'd6, CSIC_PRS_CAP_FRM_MSK_1_REG bit[22:16] will take effect and bit[31:23] will be ignored. If CSIC_PRS_CAP_FRM_MSK_1_REG bit[22:16] is configured as 7'b1011011, frame 0,frame 1, frame 3,frame 4, frame 6, frame 7,frame 8, frame 10,frame 11, frame 13...will be dropped.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x000C			Register Name: CSIC_PRS_CAP_REG
Bit	Read/Write	Default/Hex	Description
25	R/W	0x0	CH3_VCAP_ON Video capture control: Capture the video image data stream on channel 3. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
24	R/WAC	0x0	CH3_SCAP_ON Still capture control: Capture a single still image frame on channel 3. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared.
23:22	/	/	/
21:18	R/W	0x0	CH2_FPS_DS_PRD Fps down sample period 0x0: period is 1 frames 0x1: period is 2 frames 0x2: period is 3 frames 0x3: period is 4 frames 0x4: period is 5 frames (p)(p) 0xF: period is 16 frames Note: CH2_FPS_DS_PRD should be used together with CSIC_PRS_CAP_FRM_MSK_1_REG bit[15:0]. Show an example as following. When CH2_FPS_DS_PRD is configured as 4'd6, CSIC_PRS_CAP_FRM_MSK_1_REG bit[6:0] will take effect and bit[15:7] will be ignored. If CSIC_PRS_CAP_FRM_MSK_1_REG bit[6:0] is configured as 7'b1011011, frame 0,frame 1, frame 3,frame 4, frame 6, frame 7,frame 8, frame 10,frame 11, frame 13...will be dropped.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x000C			Register Name: CSIC_PRS_CAP_REG
Bit	Read/Write	Default/Hex	Description
17	R/W	0x0	CH2_VCAP_ON Video capture control: Capture the video image data stream on channel 2. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
16	R/WAC	0x0	CH2_SCAP_ON Still capture control: Capture a single still image frame on channel 2. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared.
15:14	/	/	/
13:10	R/W	0x0	CH1_FPS_DS_PRD Fps down sample period 0x0: period is 1 frames 0x1: period is 2 frames 0x2: period is 3 frames 0x3: period is 4 frames 0x4: period is 5 frames (p)(p) 0xF: period is 16 frames Note: CH1_FPS_DS_PRD should be used together with CSIC_PRS_CAP_FRM_MSK_0_REG bit[31:16]. Show an example as following. When CH1_FPS_DS_PRD is configured as 4'd6, CSIC_PRS_CAP_FRM_MSK_0_REG bit[22:16] will take effect and bit[31:23] will be ignored. If CSIC_PRS_CAP_FRM_MSK_0_REG bit[22:16] is configured as 7'b1011011, frame 0,frame 1, frame 3,frame 4, frame 6, frame 7,frame 8, frame 10,frame 11, frame 13...will be dropped.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x000C			Register Name: CSIC_PRS_CAP_REG
Bit	Read/Write	Default/Hex	Description
9	R/W	0x0	CH1_VCAP_ON Video capture control: Capture the video image data stream on channel 1. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
8	R/WAC	0x0	CH1_SCAP_ON Still capture control: Capture a single still image frame on channel 1. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared.
7:6	/	/	/
5:2	R/W	0x0	CH0_FPS_DS_PRD Fps down sample period 0x0: period is 1 frames 0x1: period is 2 frames 0x2: period is 3 frames 0x3: period is 4 frames 0x4: period is 5 frames (p)(p) 0xF: period is 16 frames Note: CH0_FPS_DS_PRD should be used together with CSIC_PRS_CAP_FRM_MSK_0_REG bit[15:0]. Show an example as following. When CH0_FPS_DS_PRD is configured as 4'd6, CSIC_PRS_CAP_FRM_MSK_0_REG bit[6:0] will take effect and bit[15:7] will be ignored. If CSIC_PRS_CAP_FRM_MSK_0_REG bit[6:0] is configured as 7'b1011011, frame 0,frame 1, frame 3,frame 4, frame 6, frame 7,frame 8, frame 10,frame 11, frame 13...will be dropped.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x000C			Register Name: CSIC_PRS_CAP_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	CH0_VCAP_ON Video capture control: Capture the video image data stream on channel 0. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
0	R/WAC	0x0	CH0_SCAP_ON Still capture control: Capture a single still image frame on channel 0. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared.

16.1.13.5 0x0010 CSIC Parser Signal Status Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CSIC_PRS_SIGNAL_STA_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	FIFO_FULL Indicates the NCSI IN Async FIFO FULL 0: Not Full 1: Full
30:28	R	0x0	PCLK_CNT Indicates the NCSI Pclk is toggle or not
27	R	0x0	VSYNC_STA Indicates the NCSI Vsync Signal status 0: Low 1: High
26	R	0x0	HSYNC_STA Indicates the NCSI Hsync Signal status 0: Low 1: High
25	R	0x0	FIELD_STA Indicates the NCSI Field Signal status 0: Low 1: High

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0010			Register Name: CSIC_PRS_SIGNAL_STA_REG
Bit	Read/Write	Default/Hex	Description
24	R	0x0	DATA_VALID_STA Indicates the NCSI Data Valid Signal status(n=0~15), MSB for D15, LSB for D0 0: Low 1: High
23:0	R	0x0	DATA_STA Indicates the NCSI Data Signal status(n=0~15), MSB for D15, LSB for D0 0: Low 1: High

16.1.13.6 0x0014 CSIC Parser NCSIC BT656 Header Configuration Register (Default Value: 0x0302_0100)

Offset: 0x0014			Register Name: CSIC_PRS_NCSIC_BT656_HEAD_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0x3	CH3_ID (no use actually) The low 4bit of BT656 header for channel 3 Only valid in BT656 multi-channel mode
23:20	/	/	/
19:16	R/W	0x2	CH2_ID (no use actually) The low 4bit of BT656 header for channel 2 Only valid in BT656 multi-channel mode
15:12	/	/	/
11:8	R/W	0x1	CH1_ID (no use actually) The low 4bit of BT656 header for channel 1 Only valid in BT656 multi-channel mode
7:4	/	/	/
3:0	R/W	0x0	CH0_ID (no use actually) The low 4bit of BT656 header for channel 0 Only valid in BT656 multi-channel mode

16.1.13.7 0x0018 CSIC Parser Capture Frame Mask 0 Register (Default Value: 0x0000_0000)

Offset: 0x0018	Register Name: CSIC_PRS_CAP_FRM_MSK_0_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	CH1_FRAME_DATA_MASK Only [CH1_FPS_DS_PRD+16:16] are valid
15:0	R/W	0x0	CH0_FRAME_DATA_MASK Only [CH0_FPS_DS_PRD:0] are valid

16.1.13.8 0x001C CSIC Parser Capture Frame Mask 1 Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: CSIC_PRS_CAP_FRM_MSK_1_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	CH3_FRAME_DATA_MASK Only [CH3_FPS_DS_PRD+16:16] are valid
15:0	R/W	0x0	CH2_FRAME_DATA_MASK Only [CH2_FPS_DS_PRD:0] are valid

16.1.13.9 0x0020 CSIC Parser Channel_0 Input Dmask Setting Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: CSIC_PRS_CH0_IN_DMSK_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	IN_DMSK_PERIOD Input dmask period 0000: 1 0001: 2 0010: 3 ... 1111: 16 Note: CH0 IN_DMSK_PERIOD should be used together with CSIC_PRS_CH0_INFMT_REG bit[31:16]. Show an example as following. When IN_DMSK_PERIOD is configured as 4'd6, CSIC_PRS_CH0_INFMT_REG bit[22:16] will take effect and bit[31:23] will be ignored. If CSIC_PRS_CH0_INFMT_REG bit[22:16] is configured as 7'b1011011, dvld high cycle 0, 1, 3, 4, 6, 7, 8, 10, 11, 13...will be dropped. Depending on AIDB btype bit[8], one dvld high cycle may transfer one pixel or two pixels.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.13.10 0x0024 CSIC Parser Channel_0 Input Format Register (Default Value: 0x0000_0003)

Offset: 0x0024			Register Name: CSIC_PRS_CH0_INFMT_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PIXEL_DATA_MASK Only [IN_DMSK_PERIOD+16:16] are valid pixel data masks for every (IN_DMSK_PERIOD+1) dvld high cycles of one line
15:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: Reserved 0010: Reserved 0011: YUV422 0100: YUV420 Others: reserved

16.1.13.11 0x0028 CSIC Parser Channel_0 Output Horizontal Size Register (Default Value: 0x0500_0000)

Offset: 0x0028			Register Name: CSIC_PRS_CH0_OUTPUT_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HOR_MASK_MODE Horizontal Mask Mode 0: The Area defined by HOR_START and HOR_LEN is not Masked 1: The Area defined by HOR_START and HOR_LEN is Masked
30	/	/	/
29:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

16.1.13.12 0x002C CSIC Parser Channel_0 Output Vertical Size Register (Default Value: 0x02d0_0000)

Offset: 0x002C			Register Name: CSIC_PRS_CH0_OUTPUT_VSIZE_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x002C			Register Name: CSIC_PRS_CH0_OUTPUT_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VER_MASK_MODE Vertical Mask Mode 0: The Area defined by VER_START and VER_LEN is not Masked 1: The Area defined by VER_START and VER_LEN is Masked
30	/	/	/
29:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

16.1.13.13 0x0030 CSIC Parser Channel_0 Input Parameter0 Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: CSIC_PRS_CH0_INPUT_PARA0_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE Actual Input Source Type of Channel 0 0: Progress 1: Interlace

16.1.13.14 0x0034 CSIC Parser Channel_0 Input Parameter1 Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: CSIC_PRS_CH0_INPUT_PARA1_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VT Input Frame Vertical Total INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT Input Frame Horizontal Total INPUT_HT = INPUT_HB+INPUT_X

16.1.13.15 0x0038 CSIC Parser Channel_0 Input Parameter2 Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: CSIC_PRS_CH0_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0038			Register Name: CSIC_PRS_CH0_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VB Input Frame Vertical Blanking
15:14	/	/	/
13:0	R	0x0	INPUT_HB Input Frame Horizontal Blanking

16.1.13.16 0x003C CSIC Parser Channel_0 Input Parameter3 Register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: CSIC_PRS_CH0_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_Y Input Frame Vertical Size
15:14	/	/	/
13:0	R	0x0	INPUT_X Input Frame Horizontal Size

16.1.13.17 0x0040 CSIC Parser Channel_0 Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: CSIC_PRS_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x0	IN_VB_CHG_INT_EN In Vblanking Change Interrupt Enable
5	R/W	0x0	IN_Y_CHG_INT_EN In Y Change Interrupt Enable
4	R/W	0x0	IN_HB_CHG_INT_EN In Hblanking Change Interrupt Enable
3	R/W	0x0	IN_X_CHG_INT_EN In X Change Interrupt Enable
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN Input Parameter1 update interrupt Enable 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0040			Register Name: CSIC_PRS_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	INPUT_PARA0_INT_EN Input Parameter0 update interrupt Enable 0: Disable 1: Enable

16.1.13.18 0x0044 CSIC Parser Channel_0 Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: CSIC_PRS_CH0_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W1C	0x0	IN_VB_CHG_PD In Vblanking Change Interrupt
5	R/W1C	0x0	IN_Y_CHG_PD In Y Change Interrupt
4	R/W1C	0x0	IN_HB_CHG_PD In Hblanking Change Interrupt
3	R/W1C	0x0	IN_X_CHG_PD In X Change Interrupt
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update, this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register, parser input parameter2 register or parser input parameter3 register update, this flag set to 1. Write 1 to clear.

16.1.13.19 0x0048 CSIC Parser Channel_0 Line Time Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: CSIC_PRS_CH0_LINE_TIME_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	PRS_CH0_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	R	0x0	PRS_CH0_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.13.20 0x004C CSIC Parser Channel_0 Frame Pre Mask Setting Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: CSIC_PRS_CH0_FRM_PRE_MSK_REG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:4	R/W	0x0	FRM_PRE_MSK_NUM Frame Pre Mask Number 0x0: 0 0x1: 1 0x2: 2 ... 0xFF: 255
3:1	/	/	/
0	R/W	0x0	FRM_PRE_MSK_EN Should be set after configuration FRM_PRE_MSK_NUM 0: Disable frame pre mask 1: Enable frame pre mask

16.1.13.21 0x0120 CSIC Parser Channel_1 Input Dmask Setting Register (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: CSIC_PRS_CH1_IN_DMSK_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	IN_DMSK_PERIOD Input dmask period 0000: 1 0001: 2 0010: 3 ... 1111: 16 Note: CH1 IN_DMSK_PERIOD should be used together with CSIC_PRS_CH1_INFMT_REG bit[31:16]. Show an example as following. When IN_DMSK_PERIOD is configured as 4'd6, CSIC_PRS_CH1_INFMT_REG bit[22:16] will take effect and bit[31:23] will be ignored. If CSIC_PRS_CH1_INFMT_REG bit[22:16] is configured as 7'b1011011, dvld high cycle 0, 1, 3, 4, 6, 7, 8, 10, 11, 13...will be dropped. Depending on AIDB btype bit[8], one dvld high cycle may transfer one pixel or two pixels.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.13.22 0x0124 CSIC Parser Channel_1 Input Format Register (Default Value: 0x0000_0003)

Offset: 0x0124			Register Name: CSIC_PRS_CH1_INFMT_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PIXEL_DATA_MASK Only [IN_DMSK_PERIOD+16:16] are valid pixel data masks for every (IN_DMSK_PERIOD+1) dvld high cycles of one line
15:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: Reserved 0010: Reserved 0011: YUV422 0100: YUV420 Others: reserved

16.1.13.23 0x0128 CSIC Parser Channel_1 Output Horizontal Size Register (Default Value: 0x0500_0000)

Offset: 0x0128			Register Name: CSIC_PRS_CH1_OUTPUT_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HOR_MASK_MODE Horizontal Mask Mode 0: The Area defined by HOR_START and HOR_LEN is not Masked 1: The Area defined by HOR_START and HOR_LEN is Masked
30	/	/	/
29:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

16.1.13.24 0x012C CSIC Parser Channel_1 Output Vertical Size Register (Default Value: 0x02d0_0000)

Offset: 0x012C			Register Name: CSIC_PRS_CH1_OUTPUT_VSIZE_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x012C			Register Name: CSIC_PRS_CH1_OUTPUT_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VER_MASK_MODE Vertical Mask Mode 0: The Area defined by VER_START and VER_LEN is not Masked 1: The Area defined by VER_START and VER_LEN is Masked
30	/	/	/
29:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

16.1.13.25 0x0130 CSIC Parser Channel_1 Input Parameter0 Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: CSIC_PRS_CH1_INPUT_PARA0_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE Actual Input Source Type of Channel 1 0: Progress 1: Interlace

16.1.13.26 0x0134 CSIC Parser Channel_1 Input Parameter1 Register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: CSIC_PRS_CH1_INPUT_PARA1_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VT Input Frame Vertical Total INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT Input Frame Horizontal Total INPUT_HT = INPUT_HB+INPUT_X

16.1.13.27 0x0138 CSIC Parser Channel_1 Input Parameter2 Register (Default Value: 0x0000_0000)

Offset: 0x0138			Register Name: CSIC_PRS_CH1_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0138			Register Name: CSIC_PRS_CH1_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VB Input Frame Vertical Blanking
15:14	/	/	/
13:0	R	0x0	INPUT_HB Input Frame Horizontal Blanking

16.1.13.28 0x013C CSIC Parser Channel_1 Input Parameter3 Register (Default Value: 0x0000_0000)

Offset: 0x013C			Register Name: CSIC_PRS_CH1_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_Y Input Frame Vertical Size
15:14	/	/	/
13:0	R	0x0	INPUT_X Input Frame Horizontal Size

16.1.13.29 0x0140 CSIC Parser Channel_1 Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0140			Register Name: CSIC_PRS_CH1_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x0	IN_VB_CHG_INT_EN In Vblanking Change Interrupt Enable
5	R/W	0x0	IN_Y_CHG_INT_EN In Y Change Interrupt Enable
4	R/W	0x0	IN_HB_CHG_INT_EN In Hblanking Change Interrupt Enable
3	R/W	0x0	IN_X_CHG_INT_EN In X Change Interrupt Enable
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN Input Parameter1 update interrupt Enable 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0140			Register Name: CSIC_PRS_CH1_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	INPUT_PARA0_INT_EN Input Parameter0 update interrupt Enable 0: Disable 1: Enable

16.1.13.30 0x0144 CSIC Parser Channel_1 Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0144			Register Name: CSIC_PRS_CH1_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W1C	0x0	IN_VB_CHG_PD In Vblanking Change Interrupt
5	R/W1C	0x0	IN_Y_CHG_PD In Y Change Interrupt
4	R/W1C	0x0	IN_HB_CHG_PD In Hblanking Change Interrupt
3	R/W1C	0x0	IN_X_CHG_PD In X Change Interrupt
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update, this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register, parser input parameter2 register or parser input parameter3 register update, this flag set to 1. Write 1 to clear.

16.1.13.31 0x0148 CSIC Parser Channel_1 Line Time Register (Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: CSIC_PRS_CH1_LINE_TIME_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	PRS_CH1_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	R	0x0	PRS_CH1_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.13.32 0x014C CSIC Parser Channel_1 Frame Pre Mask Setting Register (Default Value: 0x0000_0000)

Offset: 0x014C			Register Name: CSIC_PRS_CH1_FRM_PRE_MSK_REG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:4	R/W	0x0	FRM_PRE_MSK_NUM Frame Pre Mask Number 0x0: 0 0x1: 1 0x2: 2 ... 0xff: 255
3:1	/	/	/
0	R/W	0x0	FRM_PRE_MSK_EN Should be set after configuration FRM_PRE_MSK_NUM 0: Disable frame pre mask 1: Enable frame pre mask

16.1.13.33 0x0220 CSIC Parser Channel_2 Input Dmask Setting Register (Default Value: 0x0000_0000)

Offset: 0x0220			Register Name: CSIC_PRS_CH2_IN_DMSK_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	IN_DMSK_PERIOD Input dmask period 0000: 1 0001: 2 0010: 3 ... 1111: 16 Note: CH2 IN_DMSK_PERIOD should be used together with CSIC_PRS_CH2_INFMT_REG bit[31:16]. Show an example as following. When IN_DMSK_PERIOD is configured as 4'd6, CSIC_PRS_CH2_INFMT_REG bit[22:16] will take effect and bit[31:23] will be ignored. If CSIC_PRS_CH2_INFMT_REG bit[22:16] is configured as 7'b1011011, dvld high cycle 0, 1, 3, 4, 6, 7, 8, 10, 11, 13...will be dropped. Depending on AIDB btype bit[8], one dvld high cycle may transfer one pixel or two pixels.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.13.34 0x0224 CSIC Parser Channel_2 Input Format Register (Default Value: 0x0000_0003)

Offset: 0x0224			Register Name: CSIC_PRS_CH2_INFMT_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PIXEL_DATA_MASK Only [IN_DMSK_PERIOD+16:16] are valid pixel data masks for every (IN_DMSK_PERIOD+1) dvld high cycles of one line
15:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: Reserved 0010: Reserved 0011: YUV422 0100: YUV420 Others: reserved

16.1.13.35 0x0228 CSIC Parser Channel_2 Output Horizontal Size Register (Default Value: 0x0500_0000)

Offset: 0x0228			Register Name: CSIC_PRS_CH2_OUTPUT_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HOR_MASK_MODE Horizontal Mask Mode 0: The Area defined by HOR_START and HOR_LEN is not Masked 1: The Area defined by HOR_START and HOR_LEN is Masked
30	/	/	/
29:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

16.1.13.36 0x022C CSIC Parser Channel_2 Output Vertical Size Register (Default Value: 0x02d0_0000)

Offset: 0x022C			Register Name: CSIC_PRS_CH2_OUTPUT_VSIZE_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x022C			Register Name: CSIC_PRS_CH2_OUTPUT_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VER_MASK_MODE Vertical Mask Mode 0: The Area defined by VER_START and VER_LEN is not Masked 1: The Area defined by VER_START and VER_LEN is Masked
30	/	/	/
29:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

16.1.13.37 0x0230 CSIC Parser Channel_2 Input Parameter0 Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: CSIC_PRS_CH2_INPUT_PARA0_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE Actual Input Source Type of Channel 2 0: Progress 1: Interlace

16.1.13.38 0x0234 CSIC Parser Channel_2 Input Parameter1 Register (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: CSIC_PRS_CH2_INPUT_PARA1_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VT Input Frame Vertical Total INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT Input Frame Horizontal Total INPUT_HT = INPUT_HB+INPUT_X

16.1.13.39 0x0238 CSIC Parser Channel_2 Input Parameter2 Register (Default Value: 0x0000_0000)

Offset: 0x0238			Register Name: CSIC_PRS_CH2_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0238			Register Name: CSIC_PRS_CH2_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VB Input Frame Vertical Blanking
15:14	/	/	/
13:0	R	0x0	INPUT_HB Input Frame Horizontal Blanking

16.1.13.40 0x023C CSIC Parser Channel_2 Input Parameter3 Register (Default Value: 0x0000_0000)

Offset: 0x023C			Register Name: CSIC_PRS_CH2_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_Y Input Frame Vertical Size
15:14	/	/	/
13:0	R	0x0	INPUT_X Input Frame Horizontal Size

16.1.13.41 0x0240 CSIC Parser Channel_2 Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0240			Register Name: CSIC_PRS_CH2_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x0	IN_VB_CHG_INT_EN In Vblanking Change Interrupt Enable
5	R/W	0x0	IN_Y_CHG_INT_EN In Y Change Interrupt Enable
4	R/W	0x0	IN_HB_CHG_INT_EN In Hblanking Change Interrupt Enable
3	R/W	0x0	IN_X_CHG_INT_EN In X Change Interrupt Enable
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN Input Parameter1 update interrupt Enable 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0240			Register Name: CSIC_PRS_CH2_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	INPUT_PARA0_INT_EN Input Parameter0 update interrupt Enable 0: Disable 1: Enable

16.1.13.42 0x0244 CSIC Parser Channel_2 Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0244			Register Name: CSIC_PRS_CH2_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W1C	0x0	IN_VB_CHG_PD In Vblanking Change Interrupt
5	R/W1C	0x0	IN_Y_CHG_PD In Y Change Interrupt
4	R/W1C	0x0	IN_HB_CHG_PD In Hblanking Change Interrupt
3	R/W1C	0x0	IN_X_CHG_PD In X Change Interrupt
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update, this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register, parser input parameter2 register or parser input parameter3 register update, this flag set to 1. Write 1 to clear.

16.1.13.43 0x0248 CSIC Parser Channel_2 Line Time Register (Default Value: 0x0000_0000)

Offset: 0x0248			Register Name: CSIC_PRS_CH2_LINE_TIME_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	PRS_CH2_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	R	0x0	PRS_CH2_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.13.44 0x024C CSIC Parser Channel_2 Frame Pre Mask Setting Register (Default Value: 0x0000_0000)

Offset: 0x024C			Register Name: CSIC_PRS_CH2_FRM_PRE_MSK_REG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:4	R/W	0x0	FRM_PRE_MSK_NUM Frame Pre Mask Number 0x0: 0 0x1: 1 0x2: 2 ... 0xff: 255
3:1	/	/	/
0	R/W	0x0	FRM_PRE_MSK_EN Should be set after configuration FRM_PRE_MSK_NUM 0: Disable frame pre mask 1: Enable frame pre mask

16.1.13.45 0x0320 CSIC Parser Channel_3 Input Dmask Setting Register (Default Value: 0x0000_0000)

Offset: 0x0320			Register Name: CSIC_PRS_CH3_IN_DMSK_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	IN_DMSK_PERIOD Input dmask period 0000: 1 0001: 2 0010: 3 ... 1111: 16 Note: CH3 IN_DMSK_PERIOD should be used together with CSIC_PRS_CH3_INFMT_REG bit[31:16]. Show an example as following. When IN_DMSK_PERIOD is configured as 4'd6, CSIC_PRS_CH3_INFMT_REG bit[22:16] will take effect and bit[31:23] will be ignored. If CSIC_PRS_CH3_INFMT_REG bit[22:16] is configured as 7'b1011011, dvld high cycle 0, 1, 3, 4, 6, 7, 8, 10, 11, 13...will be dropped. Depending on AIDB btype bit[8], one dvld high cycle may transfer one pixel or two pixels.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.13.46 0x0324 CSIC Parser Channel_3 Input Format Register (Default Value: 0x0000_0003)

Offset: 0x0324			Register Name: CSIC_PRS_CH3_INFMT_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PIXEL_DATA_MASK Only [IN_DMSK_PERIOD+16:16] are valid pixel data masks for every (IN_DMSK_PERIOD+1) dvld high cycles of one line
15:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: Reserved 0010: Reserved 0011: YUV422 0100: YUV420 Others: reserved

16.1.13.47 0x0328 CSIC Parser Channel_3 Output Horizontal Size Register (Default Value: 0x0500_0000)

Offset: 0x0328			Register Name: CSIC_PRS_CH3_OUTPUT_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HOR_MASK_MODE Horizontal Mask Mode 0: The Area defined by HOR_START and HOR_LEN is not Masked 1: The Area defined by HOR_START and HOR_LEN is Masked
30	/	/	/
29:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

16.1.13.48 0x032C CSIC Parser Channel_3 Output Vertical Size Register (Default Value: 0x02d0_0000)

Offset: 0x032C			Register Name: CSIC_PRS_CH3_OUTPUT_VSIZE_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x032C			Register Name: CSIC_PRS_CH3_OUTPUT_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VER_MASK_MODE Vertical Mask Mode 0: The Area defined by VER_START and VER_LEN is not Masked 1: The Area defined by VER_START and VER_LEN is Masked
30	/	/	/
29:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

16.1.13.49 0x0330 CSIC Parser Channel_3 Input Parameter0 Register (Default Value: 0x0000_0000)

Offset: 0x0330			Register Name: CSIC_PRS_CH3_INPUT_PARA0_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE Actual Input Source Type of Channel 3 0: Progress 1: Interlace

16.1.13.50 0x0334 CSIC Parser Channel_3 Input Parameter1 Register (Default Value: 0x0000_0000)

Offset: 0x0334			Register Name: CSIC_PRS_CH3_INPUT_PARA1_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VT Input Frame Vertical Total INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT Input Frame Horizontal Total INPUT_HT = INPUT_HB+INPUT_X

16.1.13.51 0x0338 CSIC Parser Channel_3 Input Parameter2 Register (Default Value: 0x0000_0000)

Offset: 0x0338			Register Name: CSIC_PRS_CH3_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0338			Register Name: CSIC_PRS_CH3_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VB Input Frame Vertical Blanking
15:14	/	/	/
13:0	R	0x0	INPUT_HB Input Frame Horizontal Blanking

16.1.13.52 0x033C CSIC Parser Channel_3 Input Parameter3 Register (Default Value: 0x0000_0000)

Offset: 0x033C			Register Name: CSIC_PRS_CH3_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_Y Input Frame Vertical Size
15:14	/	/	/
13:0	R	0x0	INPUT_X Input Frame Horizontal Size

16.1.13.53 0x0340 CSIC Parser Channel_3 Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: CSIC_PRS_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x0	IN_VB_CHG_INT_EN In Vblanking Change Interrupt Enable
5	R/W	0x0	IN_Y_CHG_INT_EN In Y Change Interrupt Enable
4	R/W	0x0	IN_HB_CHG_INT_EN In Hblanking Change Interrupt Enable
3	R/W	0x0	IN_X_CHG_INT_EN In X Change Interrupt Enable
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN Input Parameter1 update interrupt Enable 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0340			Register Name: CSIC_PRS_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	INPUT_PARA0_INT_EN Input Parameter0 update interrupt Enable 0: Disable 1: Enable

16.1.13.54 0x0344 CSIC Parser Channel_3 Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0344			Register Name: CSIC_PRS_CH3_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W1C	0x0	IN_VB_CHG_PD In Vblanking Change Interrupt
5	R/W1C	0x0	IN_Y_CHG_PD In Y Change Interrupt
4	R/W1C	0x0	IN_HB_CHG_PD In Hblanking Change Interrupt
3	R/W1C	0x0	IN_X_CHG_PD In X Change Interrupt
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update, this flag is set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register, parser input parameter2 register or parser input parameter3 register update, this flag set to 1. Write 1 to clear.

16.1.13.55 0x0348 CSIC Parser Channel_3 Line Time Register (Default Value: 0x0000_0000)

Offset: 0x0348			Register Name: CSIC_PRS_CH3_LINE_TIME_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	PRS_CH3_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	R	0x0	PRS_CH3_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.13.56 0x034C CSIC Parser Channel_3 Frame Pre Mask Setting Register (Default Value: 0x0000_0000)

Offset: 0x034C			Register Name: CSIC_PRS_CH3_FRM_PRE_MSK_REG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:4	R/W	0x0	FRM_PRE_MSK_NUM Frame Pre Mask Number 0x0: 0 0x1: 1 0x2: 2 ... 0xff: 255
3:1	/	/	/
0	R/W	0x0	FRM_PRE_MSK_EN Should be set after configuration FRM_PRE_MSK_NUM 0: Disable frame pre mask 1: Enable frame pre mask

16.1.13.57 0x0500 CSIC Parser NCSIC RX Signal0 Delay Adjust Register (Default Value: 0x0000_0000)

Offset: 0x0500			Register Name: CSIC_PRS_NCSIC_RX_SIGNAL0_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	FILED_DLY Filed dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	VSYNC_DLY Vsync dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	HSYNC_DLY Hsync dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	PCLK_DLY Pclk dly 32 Step for adjust, 1 step = 0.2ns

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.13.58 0x050C CSIC Parser NCSIC RX Signal3 Delay Adjust Register (Default Value: 0x0000_0000)

Offset: 0x050C			Register Name: CSIC_PRS_NCSIC_RX_SIGNAL3_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	D15_DLY D15 dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D14_DLY D14 dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D13_DLY D13 dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D12_DLY D12 dly 32 Step for adjust, 1 step = 0.2ns

16.1.13.59 0x0510 CSIC Parser NCSIC RX Signal4 Delay Adjust Register (Default Value: 0x0000_0000)

Offset: 0x0510			Register Name: CSIC_PRS_NCSIC_RX_SIGNAL4_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	D11_DLY D11 dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D10_DLY D10 dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D9_DLY D9 dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D8_DLY D8 dly 32 Step for adjust, 1 step = 0.2ns

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.13.60 0x0514 CSIC Parser NCSIC RX Signal5 Delay Adjust Register (Default Value: 0x0000_0000)

Offset: 0x0514			Register Name: CSIC_PRS_NCSIC_RX_SIGNAL5_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	D7_DLY D7 dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D6_DLY D6 dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D5_DLY D5 dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D4_DLY D4 dly 32 Step for adjust, 1 step = 0.2ns

16.1.13.61 0x0518 CSIC Parser NCSIC RX Signal6 Delay Adjust Register (Default Value: 0x0000_0000)

Offset: 0x0518			Register Name: CSIC_PRS_NCSIC_RX_SIGNAL6_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	D3_DLY D3 dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D2_DLY D2 dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D1_DLY D1 dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D0_DLY D0 dly 32 Step for adjust, 1 step = 0.2ns

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.13.62 0x0520 CSIC Parser SYNC EN Register (Default Value: 0x0000_0000)

Offset: 0x0520			Register Name: CSIC_PRS_SYNC_EN_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
19:16	R/W	0x0	VSYNC_MODE Input vsync signal Source select 0x0: Vsync signals all from 1 parser 0x1: Vsync signals from 2 parser 0x2: Vsync signals from 4 parser others: Reserved
15:12	/	/	/
11:8	R/W	0x0	VSYNC_SEL Generate sync signal Benchmark select Bit8: USE VSYNC_Input0 Bit9: USE VSYNC_Input1 Bit10: USE VSYNC_Input2 Bit11: USE VSYNC_Input3 Set 1,Use input
7:4	R/W	0x0	VSYNC_USED Parser input vsync signal enable in sync mode Bit4: VSYNC_Input0 Bit5: VSYNC_Input1 Bit6: VSYNC_Input2 Bit7: VSYNC_Input3 Set 1,enable input
3	/	/	/
2	R/W	0x0	FSYNC_OUT_SEL Parser sent sync signal via by 0: FSYNC0 1: FSYNC1
1	R/W	0x0	FSYNC_MODE Parser sync signal source select 0: From outside 1: Generate by self
0	R/W	0x0	FSYNC_FUN_EN Enable Parser sent sync signal 0: Disable 1: Enable

16.1.13.63 0x0524 CSIC Parser SYNC CFG Register (Default Value: 0x0000_0000)

Offset: 0x0524	Register Name: CSIC_PRS_SYNC_CFG_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	FSYNC_PUL_WID Sync signal pulse width $N*T_{24M}$, $N*T_{24M}$ 4*Tpclk
15:0	R/W	0x0	FYSNC_DISTANCE The interval of two sync signal

16.1.13.64 0x0528 CSIC Parser VS WAIT N Register (Default Value: 0x0000_0000)

Offset: 0x0528			Register Name: CSIC_PRS_VS_WAIT_N_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VS_WAIT_N When multi-channel vsync all come, the max wait time.

16.1.13.65 0x052C CSIC Parser VS WAIT M Register (Default Value: 0x0000_0000)

Offset: 0x052C			Register Name: CSIC_PRS_VS_WAIT_M_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VS_WAIT_M When in multi-channel mode, vsync comes at the different time. These bits indicate the max wait time.

16.1.13.66 0x0540 CSIC Parser XSYNC ENABLE Register (Default Value: 0x0000_0000)

Offset: 0x0540			Register Name: CSIC_PRS_XSYNC_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:8	R/W	0x0	XVS_TO_XHS_T The period of XHS delay to XVS, ${XVS_TO_XHS_T}+1 master clock cycles, no more than XHS_LEN
7:5	/	/	/
4	R/W	0x0	XVS_XHS_OUT_SEL When sensor works in slave mode, this bit select XVS and XHS to output. 0: XHS0, XVS0 1: XHS1, XVS1

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0540			Register Name: CSIC_PRS_XSYNC_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	XVS_POL When sensor works in slave mode, this bit set polarity of XVS. 0: Negative 1: Positive
2	R/W	0x0	XHS_POL When sensor works in slave mode, this bit set polarity of XHS. 0: Negative 1: Positive
1	R/W	0x0	XVS_OUT_EN When sensor works in slave mode, this bit enable output XVS to sensor 0: Disable 1: Enable
0	R/W	0x0	XHS_OUT_EN When sensor works in slave mode, this bit enables output XHS to sensor 0: Disable 1: Enable

16.1.13.67 0x0544 CSIC Parser XVS Period Register (Default Value: 0x0000_0000)

Offset: 0x0544			Register Name: CSIC_PRS_XVS_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	XVS_T The period of XVS signal, ${XVS_T}+2 master clock cycles

16.1.13.68 0x0548 CSIC Parser XHS Period Register (Default Value: 0x0000_0000)

Offset: 0x0548			Register Name: CSIC_PRS_XHS_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	XHS_T The period of XHS signal, ${XHS_T}+2 master clock cycles

16.1.13.69 0x054C CSIC Parser XVS LENGTH Register (Default Value: 0x0000_0000)

Offset: 0x054C	Register Name: CSIC_PRS_XVS_LENGTH_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	XVS_LEN The valid length of XVS signal, ${XVS_LEN}+1 master clock cycles

16.1.13.70 0x0550 CSIC Parser XHS LENGTH Register (Default Value: 0x0000_0000)

Offset: 0x0550			Register Name: CSIC_PRS_XHS_LENGTH_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	XHS_LEN The valid length of XHS signal, ${XHS_LEN}+1 master clock cycles

16.1.13.71 0x0554 CSIC Parser SYNC DELAY Register (Default Value: 0x0000_0000)

Offset: 0x0554			Register Name: CSIC_PRS_SYNC_DLY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	SYNC_DLY The XHS/XVS will sent after, ${SYNC_DLY}+1 master clock cycles, no more than XVS_LEN

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.14 CSIC DMA0 Register Description

16.1.14.1 0x0000 CSIC DMA TOP Register (Default Value: 0x7000_0000)

Offset: 0x0000			Register Name: CSIC_DMA_TOP_REG
Bit	Read/Write	Default/Hex	Description
31	N/A	N/A	/
30	R/W	0x1	VFLIP_BUF_ADDR_CFG_MODE Vflip buffer address set by software or calculated by hardware 0: Hardware 1: Software
29	R/W	0x1	BUF_LENGTH_CFG_MODE buffer length set by software or calculated by hardware 0: Hardware 1: Software
28	R/W	0x1	FLIP_SIZE_CFG_MODE FLIP SIZE set by software or calculated by hardware 0: Hardware 1: Software
27:17	/	/	/
16	R/W	0x0	FRM_END_SEL Frame End Select 0:Sel mcsi_bk_frm_end_in External input AIDB frm_end 1:Sel dma_frm_end Vsyn negedge after bk pre-process
15	/	/	/
14:13	R/W	0x0	VE_ONLINE_CH_SEL Select BK Channel for VE Online handshake
12	R/W	0x0	VE_ONLINE_HANDSHAKE_EN Set this bit to Enable frame and line counter for VE online handshake
11:10	/	/	/
9:8	R/W	0x0	MIN_SDR_WR_SIZE Minimum size of SDRAM block write 00: 256 bytes (if hflip is enable, always select 256 bytes) 01: 512 bytes 10: 1k bytes (not support For DMA4/5) 11: 2k bytes (not support For DMA4/5)
7	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: CSIC_DMA_TOP_REG
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	VI_TO_CNT_EN Enable Video Input Timeout counter, add 1 when there is no effective video input in a 12M clock, clear to 0 when detecting effective video input. 0: Disable 1: Enable
5	R/W	0x0	FS_FRM_CNT_EN When BK_TOP_EN is enabled, this bit will be set to 1, indicating the Frame counter start to add. 0: Disable 1: Enable
4:3	/	/	/
2	R/W	0x0	FRM_RATE_CNT_SPL Sampling time for clk counter per frame 0: Sampling clock counter every frame done 1: Sampling clock counter every vsync
1	R/W	0x0	FRM_RATE_CNT_EN clk count per frame enable
0	R/W	0x0	BK_TOP_EN Module Enable 0: Disable 1: Enable

16.1.14.2 0x0004 CSIC DMA Multi-Channel Configuration Register (Default Value: 0x0001_1000)

Offset: 0x0004			Register Name: CSIC_DMA_MUL_CH_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R	0x0	CSTATE Debug Info.BK write ddr block FSM state.
27:24	R	0x0	LSTATE Debug Info.BK write ddr line FSM state.
23:22	/	/	/
21:20	R	0x0	FSTATE Debug Info.BK write ddr frame FSM state.
19:16	R	0x1	TR_VLD_ST Debug Info.BK transport FSM state.
15:12	R	0x1	IN_ST Debug Info.BK capture FSM state.
11:10	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: CSIC_DMA_MUL_CH_CFG_REG
Bit	Read/Write	Default/Hex	Description
9:8	R	0x0	CUR_OUT_CH When Multi-Channel enable, this field indicates the Current Output Channel ID
7:6	/	/	/
5:4	R	0x0	CUR_IN_CH When Multi-Channel enable, this field indicates the Current Input Channel ID
3:1	/	/	/
0	R/W	0x0	MUL_CH_EN DMA off-line multi-channel enable 0: Disable 1: Enable

16.1.14.3 0x0008 CSIC DMA FIFO Pointer Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CSIC_DMA_FIFO_POINTER_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	FIFO_RPT Debug Info.BK data fifo read pointer.
15:14	/	/	/
13:0	R	0x0	FIFO_WPT Debug Info.BK data fifo write pointer.

16.1.14.4 0x000C CSIC DMA Write Counter Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: CSIC_DMA_WRITE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:16	R	0x0	BCNT Debug Info.BK received brdy number.
15:11	/	/	/
10:0	R	0x0	FCNT Debug Info.BK send valid req number.

16.1.14.5 0x0010 CSIC DMA Frame Rate Clock Counter Register (Default Value: 0x0000_0000)

Offset: 0x0010	Register Name: CSIC_DMA_FRM_CLK_CNT_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R	0x0	FRM_RATE_CLK_CNT Counter value between every frame. For instant hardware frame rate statics. The internal counter is added by one every 12MHz clock cycle. When frame done or vsync comes, the internal counter value is sampled to FRM_CLK_CNT, and cleared to 0.

16.1.14.6 0x0014 CSIC DMA Accumulated and Internal Clock Counter Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: CSIC_DMA_ACC_ITNL_CLK_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/WC	0x0	ACC_CLK_CNT The accumulated value of FRM_CLK_CNT for software frame rate statics. Every interrupt of frame done, the software checks this accumulated value and clear it to 0. If the ACC_CLK_CNT is larger than 1, the software has lost frame. When frame done or vsync comes, ACC_CLK_CNT = ACC_CLK_CNT + 1, and cleared to 0 when writing this register.
23:0	R	0x0	ITNL_CLK_CNT The instant value of internal frame clock counter. When frame done interrupt comes, the software can query this counter for judging whether it is the time for updating the double buffer address registers.

16.1.14.7 0x0020 CSIC DMA Fsync Frame Counter Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: CSIC_DMA_FS_FRM_CNT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	FS_FRM_CNT_CLR When the bit set to 1,Frame cnt clear to 0
30:16	R/W	0x0	FS_FRM_CNT_CLR_DISTANCE Frame cnt clear cycle $N*T_{SYNC}$
15	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0020			Register Name: CSIC_DMA_FS_FRM_CNT_REG
Bit	Read/Write	Default/Hex	Description
14:0	R	0x0	FS_FRM_CNT Counter value of frame. When frame done comes, the internal counter value adds 1; when the reg is full, it is cleared to 0. When parser sends a sync signal, it is cleared to 0.

16.1.14.8 0x0040 CSIC DMA Video Input Timeout Threshold0 Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: CSIC_DMA_VI_TO_TH0_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	VI_TO_TH0 Video Input Timeout Threshold0 Set VIDEO_INPUT_TO_INT_PD when VI Counter reaches TH0 after VI_TO_CNT_EN is set. Time Unit is a 12M clock period.

16.1.14.9 0x0044 CSIC DMA Video Input Timeout Threshold1 Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: CSIC_DMA_VI_TO_TH1_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	VI_TO_TH1 Video Input Timeout Threshold1 Set VIDEO_INPUT_TO_INT_PD when VI Counter reaches TH1 after getting the first frame has been input, Time Unit is a 12M clock period.

16.1.14.10 0x0048 CSIC DMA Video Input Timeout Counter Value Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: CSIC_DMA_VI_TO_CNT_VAL_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R	0x0	VI_TCNT_VAL Video Input Timeout Counter Value Indicate the current value of Video Input Timeout Counter

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.14.11 0x0050 CSIC DMA VE Frame Counter Value Register (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: CSIC_DMA_VE_FRM_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R	0x0	FRM_DONE_CNT Indicates How Many Frame which Stored in DDR
15:8	/	/	/
7:0	R	0x0	FRM_ST_CNT Indicates the Frame Number which is Storing

16.1.14.12 0x0054 CSIC DMA VE Line Counter Value Register (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: CSIC_DMA_VE_LINE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	LINE_DONE_CNT Indicates How Many Line which Stored in DDR
15:14	/	/	/
13:0	R	0x0	LINE_ST_CNT Indicates the Line Number which is Storing

16.1.14.13 0x0058 CSIC DMA VE Current Frame Address Register (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: CSIC_DMA_VE_CUR_FRM_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CUR_FRM_ADDR Indicates the FIFO0 Address Which Current Frame is Storing

16.1.14.14 0x005C CSIC DMA VE Last Frame Address Register (Default Value: 0x0000_0000)

Offset: 0x005C			Register Name: CSIC_DMA_VE_LAST_FRM_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	LAST_FRM_ADDR Indicates the FIFO0 Address Which Last Frame is Stored

16.1.14.15 0x0080 CSIC DMA FIFO Statistic Register (Default Value: 0x0000_0000)

Offset: 0x0080	Register Name: CSIC_DMA_FIFO_STAT_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R	0x0	FIFO_FRM_MAX Indicates the maximum depth of FIFO being occupied for whole frame. Update at every vsync or framedone. Unit is byte.

16.1.14.16 0x0084 CSIC DMA FIFO Threshold Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: CSIC_DMA_FIFO_THRS_REG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x0	FIFO_THRS When FIFO occupied memory exceed the threshold, dram frequency cannot change. Unit is byte.

16.1.14.17 0x0100 CSIC DMA TOP Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: CSIC_DMA_TOP_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	VIDEO_INPUT_TO_INT_EN Set an INT when no video input exceeds the setting threshold time
1	R/W	0x0	CLR_FS_FRM_CNT_INT_EN Set a INT When Clear FS Frame cnt.
0	R/W	0x0	FS_PUL_INT_EN Set an INT when a Fsync signal received

16.1.14.18 0x0104 CSIC DMA TOP Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: CSIC_DMA_TOP_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	VIDEO_INPUT_TO_INT_PD Set an INT Pending when no video input exceeds the setting threshold time
1	R/W1C	0x0	CLR_FRAME_CNT_INT_PD Set a INT When Clear FS Frame cnt.
0	R/W1C	0x0	FS_PUL_INT_PD Set an INT when a Fsync signal received

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.14.19 0x01F4 CSIC DMA Feature List Register (Default Value: 0x0000_0040)

Offset: 0x01F4			Register Name: CSIC_DMA_FEATURE_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R	0x4	DMA0_CHNUM Channel numbers (note: DMA0/1/2/3_CHNUM=4; for other DMAs, DMA*_CHNUM=1)
3:2	/	/	/
1	R	0x0	DMA0_EMBEDDED_LBC LBC Feature Existence 0: No Embedded LBC 1: Embedded LBC
0	R	0x0	DMA0_EMBEDDED_FBC FBC Feature Existence 0: No Embedded FBC 1: Embedded FBC

16.1.14.20 0x0200 CSIC DMA Channel0 Enable Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: CSIC_DMA_CH0_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	FRM_DROP_EN Drop Frame when vsync comes but buffer address is not ready 0: Not Drop 1: Drop
7	R/W	0x0	BUF_ADDR_MODE Frame buffer Address configuration mode 0: Buffer Address Register Mode 1: Buffer Address FIFO Mode
6:1	/	/	/
0	R/W	0x0	CAP_EN Video In Capture Enable 0: Disable 1: Enable

16.1.14.21 0x0204 CSIC DMA Channel0 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0204	Register Name: CSIC_DMA_CH0_CFG_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00~0xff
23:22	/	/	/
21	R/W	0x0	YUV10to8_EN YUV 10bit input cut to 8bit 0: Disable 1: Enable
20	R/W	0x0	YUV10_STO_FMT YUV 10bit store configure 0: YUV 10bit Stored in low 10bit of a 16bit-word 1: YUV 10bit Stored in high 10bit of a 16bit-word
19:16	R/W	0x0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: raw-8 0001: raw-10 0010: raw-12 0011: raw-14 0100: raw-16 0101: raw-20 0110: raw-24 0111: Reserved 1000: rgb565 1001: rgb888 1010: prgb888 others: Reserved When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined (UV sequence) 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined (UV sequence) 0111: frame planar YCbCr 422 UV combined (UV sequence) 1000: filed planar YCbCr 422 UV combined (VU sequence)

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1001: field planar YCbCr 420 UV combined (VU sequence) 1010: frame planar YCbCr 420 UV combined (VU sequence) 1011: frame planar YCbCr 422 UV combined (VU sequence) 1100: Reserved 1101: field YCbCr 400 1110: Reserved 1111: frame YCbCr 400 When the input format is set YUV420 0000: LBC Mode Output 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: Reserved 0100: Reserved 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined (UV sequence) 0111~1000: Reserved 1001: field planar YCbCr 420 UV combined (VU sequence) 1010: frame planar YCbCr 420 UV combined (VU sequence) 1011~1100: Reserved 1101: field YCbCr 400 1110: Reserved 1111: frame YCbCr 400
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0: Disable 1: Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11:10	R/W	0x0	FIELD_SEL Field selection. 00: capturing with field 0. 01: capturing with field 1. 10: capturing with either field. 11: Reserved
9:6	R/W	0x0	FPS_DS_PRD Fps down sample period 0: 1 frames 1: 2 frames 2: 3 frames 3: 4 frames 4: 5 frames (p)(p) 15: 16 frames Note: CH0 FPS_DS_PRD should be used together with CSIC_DMA_CH0_FRM_MSK_CFG_REG bit[15:0]. Show an example as following. When CH0 FPS_DS_PRD is configured as 4'd6, CSIC_DMA_CH0_FRM_MSK_CFG_REG bit[6:0] will take effect and bit[15:7] will be ignored. If CSIC_DMA_CH0_FRM_MSK_CFG_REG bit[6:0] is configured as 7'b1011011, frame 0,frame 1, frame 3,frame 4, frame 6, frame 7,frame 8, frame 10,frame 11, frame 13...will be dropped.
5:2	R/W	0x0	CAP_FRONT_MASK_NUM Indicates the frame number masked after CAP_EN set.
1:0	/	/	/

16.1.14.22 0x0208 CSIC DMA Channel0 Frame Lost Counter Register (Default Value: 0x0000_0000)

Offset: 0x0208			Register Name: CSIC_DMA_CH0_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	FRM_LOST_CNT_EN When set 1, FRM_LOST_CNT is enable; when set 0, FRM_LOST_CNT is cleared
30:8	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0208			Register Name: CSIC_DMA_CH0_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description
7:0	R	0x0	FRM_LOST_CNT Once a new frame comes when the buffer address not ready and FRM_DROP_EN set, or when the last frame still processing, the new frame is dropped and the FRM_LOST_CNT increases when FRM_LOST_CNT_EN set.

16.1.14.23 0x020C CSIC DMA Channel0 Frame Mask Configuration Register (Default Value: 0x0000_0000)

Offset: 0x020C			Register Name: CSIC_DMA_CH0_FRM_MSK_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	FRAME_DATA_MASK Only [FPS_DS_PRD:0] are valid

16.1.14.24 0x0210 CSIC DMA Channel0 Horizontal Size Register (Default Value: 0x0500_0000)

Offset: 0x0210			Register Name: CSIC_DMA_CH0_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x500	HOR_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Horizontal pixel unit length. Valid pixel of a line in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

16.1.14.25 0x0214 CSIC DMA Channel0 Vertical Size Register (Default Value: 0x02d0_0000)

Offset: 0x0214			Register Name: CSIC_DMA_CH0_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x2d0	VER_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Valid line number of a frame in DMA mode.
15:14	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0214			Register Name: CSIC_DMA_CH0_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

16.1.14.26 0x0218 CSIC DMA Channel0 Vertical Crop Mode Register (Default Value: 0x0000_0000)

Offset: 0x0218			Register Name: CSIC_DMA_CH0_VCROP_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	FLD_FRM_VCROP_EN Field Frame Vcrop Enable 0: Disable field frame vcrop 1: Enable field frame vcrop When input frame is of field type and V crop wants to be implemented, this bit should be configured as 1. (note: only even lines crop is supported for field input V crop)

16.1.14.27 0x0220 CSIC DMA Channel0 FIFO 0 Output Buffer-A Address Register (Default Value: 0x0000_0000)

Offset: 0x0220			Register Name: CSIC_DMA_CH0_F0_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F0_BUFA When LBC_EN disable, these bits indicate FIFO 0 output buffer-A address in DMA mode. When LBC_EN enable, these bits indicate the output buffer address in LBC mode.

16.1.14.28 0x0224 CSIC DMA Channel0 FIFO 0 Output Buffer-A Address Result Register (Default Value: 0x0000_0000)

Offset: 0x0224			Register Name: CSIC_DMA_CH0_F0_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F0_BUFA_RESULT Indicate the final F0_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.14.29 0x0228 CSIC DMA Channel0 FIFO 1 Output Buffer-A Address Register (Default Value: 0x0000_0000)

Offset: 0x0228			Register Name: CSIC_DMA_CH0_F1_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F1_BUFA FIFO 1 output buffer-A address.

16.1.14.30 0x022C CSIC DMA Channel0 FIFO 1 Output Buffer-A Address Result Register (Default Value: 0x0000_0000)

Offset: 0x022C			Register Name: CSIC_DMA_CH0_F1_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F1_BUFA_RESULT Indicate the final F1_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

16.1.14.31 0x0230 CSIC DMA Channel0 FIFO 2 Output Buffer-A Address Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: CSIC_DMA_CH0_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address

16.1.14.32 0x0234 CSIC DMA Channel0 FIFO 2 Output Buffer-A Address Result Register (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: CSIC_DMA_CH0_F2_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F2_BUFA_RESULT Indicate the final F2_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.14.33 0x0238 CSIC DMA Channel0 Buffer Length Register (Default Value: 0x0280_0500)

Offset: 0x0238			Register Name: CSIC_DMA_CH0_BUF_LEN_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x280	BUF_LEN_C DMA_MODE: Buffer length of chroma C in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y in ONLY Y line. Unit is byte.
15:0	R/W	0x500	BUF_LEN DMA_MODE: Buffer length of luminance Y in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y and chroma C in YC line. Unit is byte.

16.1.14.34 0x023C CSIC DMA Channel0 Flip Size Register (Default Value: 0x02d0_0500)

Offset: 0x023C			Register Name: CSIC_DMA_CH0_FLIP_SIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x2d0	VER_LEN Vertical line number when in VFLIP mode. Unit is line. Only Readable when FLIP_SIZE_CFG_MODE set 0
15	/	/	/
14:0	R/W	0x500	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel component. Only Readable when FLIP_SIZE_CFG_MODE set 0

16.1.14.35 0x024C CSIC DMA Channel0 Capture Status Register (Default Value: 0x0000_0000)

Offset: 0x024C			Register Name: CSIC_DMA_CH0_CAP_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R	0x0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x024C			Register Name: CSIC_DMA_CH0_CAP_STA_REG
Bit	Read/Write	Default/Hex	Description
0	R	0x0	CAP_STA capture in progress Indicates the CSI is capturing image data. The bit is set at the start of the first frame after enabling frame capture.

16.1.14.36 0x0250 CSIC DMA Channel0 Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0250			Register Name: CSIC_DMA_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	LACK_HBLANK_INT_EN Set an INT when trying filling dummy for missed pixels at the end of the line but hblank is too short.
22	R/W	0x0	LINE_REDUNDANT_INT_EN Set an INT when the amount of lines in one frame is more than expected.
21	R/W	0x0	LINE_MISS_INT_EN Set an INT when the amount of lines in one frame is less than expected.
20	R/W	0x0	PIXEL_REDUNDANT_INT_EN Set an INT when the amount of pixels in one line is more than expected.
19	R/W	0x0	PIXEL_MISS_INT_EN Set an INT when the amount of pixels in one line is less than expected.
18	R/W	0x0	BUF_ADDR_OVERFLOW_INT_EN Set an INT when buffer address is overwrite before used
17	R/W	0x0	BUF_ADDR_UNDERFLOW_INT_EN Set an INT when new frame comes but buffer address is not ready
16	R/W	0x0	LBC_HBLKMIN_INT_EN Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W	0x0	FRM_LOST_INT_EN Set an INT once frame is in when last frame processing

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0250			Register Name: CSIC_DMA_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
14	R/W	0x0	STORED_FRM_CNT_INT_EN Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD , only use in BUF Address FIFO MODE
13	R/W	0x0	BUF_ADDR_FIFO_INT_EN Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
6	R/W	0x0	LI_OF_INT_EN Line information FIFO(16 lines) overflow.
5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every frame. The line number is set in the line counter register.
4:3	/	/	/
2	R/W	0x0	FIFO_OF_INT_EN FIFO overflow The bit is set when the FIFO become overflow.
1	R/W	0x0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0250			Register Name: CSIC_DMA_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been written to buffer. For video capture, the bit is set when the last frame has been written to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

16.1.14.37 0x0254 CSIC DMA Channel0 Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0254			Register Name: CSIC_DMA_CH0_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W1C	0x0	LACK_HBLANK_INT_PD Set an INT when trying filling dummy for missed pixels at the end of the line but hblank is too short.
22	R/W1C	0x0	LINE_REDUNDANT_INT_PD Set an INT when the amount of lines in one frame is more than expected.
21	R/W1C	0x0	LINE_MISS_INT_PD Set an INT when the amount of lines in one frame is less than expected.
20	R/W1C	0x0	PIXEL_REDUNDANT_INT_PD Set an INT when the amount of pixels in one line is more than expected.
19	R/W1C	0x0	PIXEL_MISS_INT_PD Set an INT when the amount of pixels in one line is less than expected.
18	R/W1C	0x0	BUF_ADDR_OVERFLOW_INT_PD Set an INT when buffer address is overwrite before used
17	R/W1C	0x0	BUF_ADDR_UNDERFLOW_INT_PD Set an INT when new frame comes but buffer address is not ready

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0254			Register Name: CSIC_DMA_CH0_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
16	R/W1C	0x0	LBC_HBLKMIN_INT_PD Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W1C	0x0	FRM_LOST_INT_PD Set an INT once frame is in when last frame processing
14	R/W1C	0x0	STORED_FRM_CNT_INT_PD Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE
13	R/W1C	0x0	BUF_ADDR_FIFO_INT_PD Set an INT when content in BUF Address FIFO no more than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	LI_OF_PD Line information FIFO(16 lines) overflow
5	R/W1C	0x0	LC_PD Line counter flag
4:3	/	/	/
2	R/W1C	0x0	FIFO_OF_PD FIFO 0 overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

16.1.14.38 0x0258 CSIC DMA Channel0 Line Counter Register (Default Value: 0x0000_0000)

Offset: 0x0258			Register Name: CSIC_DMA_CH0_LINE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM value is set by users. When internal line counter reach the set value, the LC_PD will set.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.14.39 0x0268 CSIC DMA Channel0 Line Statistic Register (Default Value: 0x0000_0000)

Offset: 0x0268			Register Name: CSIC_DMA_CH0_LINE_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	LINE_INDEX Indicates the line index in current hsync.
15:0	/	/	/

16.1.14.40 0x0270 CSIC DMA Channel0 PCLK Statistic Register (Default Value: 0x0000_0000)

Offset: 0x0270			Register Name: CSIC_DMA_CH0_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.
15	/	/	/
14:0	R	0x0	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

16.1.14.41 0x0280 CSIC DMA Channel0 BUF Address FIFO0 Entry Register (Default Value: 0x0000_0000)

Offset: 0x0280			Register Name: CSIC_DMA_CH0_BUF_ADDR_FIFO0_ENTRY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO0_ENTRY FIFO Entry of Buffer Address FIFO0 for input frames to be stored, only used in Buffer Addr FIFO Mode

16.1.14.42 0x0284 CSIC DMA Channel0 BUF Address FIFO1 Entry Register (Default Value: 0x0000_0000)

Offset: 0x0284			Register Name: CSIC_DMA_CH0_BUF_ADDR_FIFO1_ENTRY_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0284			Register Name: CSIC_DMA_CH0_BUF_ADDR_FIFO1_ENTRY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO1_ENTRY FIFO Entry of Buffer Address FIFO1 for input frames to be stored, only used in Buffer Addr FIFO Mode

16.1.14.43 0x0288 CSIC DMA Channel0 BUF Address FIFO2 Entry Register (Default Value: 0x0000_0000)

Offset: 0x0288			Register Name: CSIC_DMA_CH0_BUF_ADDR_FIFO2_ENTRY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO2_ENTRY FIFO Entry of Buffer Address FIFO2 for input frames to be stored, only used in Buffer Addr FIFO Mode

16.1.14.44 0x028C CSIC DMA Channel0 BUF Threshold Register (Default Value: 0x0020_0000)

Offset: 0x028C			Register Name: CSIC_DMA_CH0_BUF_TH_REG
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:16	R/W	0x20	CSIC_DMA_STORED_FRM_THRESHOLD when stored frame counter value reaches the threshold , counter is cleared to 0 , only used in Buffer Addr FIFO Mode
15:6	/	/	/
5:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO_THRESHOLD when content in Buffer Address FIFO no more than the threshold, an interrupt is set, only used in Buffer Addr FIFO Mode

16.1.14.45 0x0290 CSIC DMA Channel0 BUF Address FIFO Content Register (Default Value: 0x0000_0000)

Offset: 0x0290			Register Name: CSIC_DMA_CH0_BUF_ADDR_FIFO_CON_REG
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:16	R	0x0	CSIC_DMA_BUF_ADDR_FIFO2_CONTENT FIFO Content of address buffered in Buffer Address FIFO2, only used in Buffer Addr FIFO Mode

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0290			Register Name: CSIC_DMA_CH0_BUF_ADDR_FIFO_CON_REG
Bit	Read/Write	Default/Hex	Description
15:14	/	/	/
13:8	R	0x0	CSIC_DMA_BUF_ADDR_FIFO1_CONTENT FIFO Content of address buffered in Buffer Address FIFO1, only used in Buffer Addr FIFO Mode
7:6	/	/	/
5:0	R	0x0	CSIC_DMA_BUF_ADDR_FIFO0_CONTENT FIFO Content of address buffered in Buffer Address FIFO0, only used in Buffer Addr FIFO Mode

16.1.14.46 0x0294 CSIC DMA Channel0 Stored Frame Counter Register (Default Value: 0x0000_0000)

Offset: 0x0294			Register Name: CSIC_DMA_CH0_STORED_FRM_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	CSIC_DMA_STORED_FRM_CNT Indicates value of stored frames counter, when counter value reaches CSIC_DMA_STORED_FRM_THRESHOLD, counter is cleared to 0, only used in Buffer Addr FIFO Mode

16.1.14.47 0x0298 CSIC DMA Channel0 Abnormal Mask Register (Default Value: 0x0000_0000)

Offset: 0x0298			Register Name: CSIC_DMA_CH0_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	FRM_DONE_INT_MSK_EN Decide whether the FD_INT of this frame will be masked or not once any abnormal condition happens during this frame. 0: Disable MSK 1: Enable MSK
4	R/W	0x0	LINE_REDUNDANT_MSK_EN Decide whether the remaining data in this frame will be dropped or not once line redundant error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0298			Register Name: CSIC_DMA_CH0_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	LINE_MISS_MSK_EN Decide whether the remaining data in this frame will be dropped or not once line miss error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
2	R/W	0x0	PIXEL_REDUNDANT_MSK_EN Decide whether the remaining data in this frame will be dropped or not once pixel redundant error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
1	R/W	0x0	PIXEL_MISS_MSK_EN Decide whether the remaining data in this frame will be dropped or not once pixel miss error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0298			Register Name: CSIC_DMA_CH0_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	VSYN_ABN_MSK_EN Decide whether the remaining data in this frame will be dropped or not once abnormal happens in this frame. 0: Disable MSK 1: Enable MSK Note: When VSYN_ABN_MSK_EN is set as 1 and one of the following conditions happens, the remaining data in this frame will be dropped. And the next frame will be received as normal. a. When trying to fill dummy for pixel miss and LACK_HBLANK happens. b. When PIXEL_REDUNDANT happens and PIXEL_REDUNDANT_MSK_EN is set as 1. c. When PIXEL_MISS happens, LACK_HBLANK no happen and PIXEL_MISS_MSK_EN is set as 1. d. When LINE_REDUNDANT happens and LINE_REDUNDANT_MSK_EN is set as 1. e. When LINE_MISS happens and LINE_MISS_MSK_EN is set as 1.

16.1.14.48 0x029C CSIC DMA Channel0 Pixels Add Enable Register (Default Value: 0x0000_0000)

Offset: 0x029C			Register Name: CSIC_DMA_CH0_PIXELS_ADD_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	PIXELS_ADD_EN Decide whether dummy pixels will be added at the end of the line or not once pixels miss error happens. 0: Disable ADD 1: Enable ADD

16.1.14.49 0x02A0 CSIC DMA Channel0 Pixels Add Value Register (Default Value: 0x0000_0000)

Offset: 0x02A0			Register Name: CSIC_DMA_CH0_PIXELS_ADD_VAL_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x02A0			Register Name: CSIC_DMA_CH0_PIXELS_ADD_VAL_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PIXELS_ADD_VALUE Decide the value of dummy pixels when PIXELS_ADD_EN is set as 1

16.1.14.50 0x0400 CSIC DMA Channel1 Enable Register (Default Value: 0x0000_0000)

Offset: 0x0400			Register Name: CSIC_DMA_CH1_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	FRM_DROP_EN Drop Frame when vsync comes but buffer address is not ready 0: Not Drop 1: Drop
7	R/W	0x0	BUF_ADDR_MODE Frame buffer Address configuration mode 0: Buffer Address Register Mode 1: Buffer Address FIFO Mode
6:1	/	/	/
0	R/W	0x0	CAP_EN Video In Capture Enable 0: Disable 1: Enable

16.1.14.51 0x0404 CSIC DMA Channel1 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0404			Register Name: CSIC_DMA_CH1_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00~0xff
23:22	/	/	/
21	R/W	0x0	YUV10to8_EN YUV 10bit input cut to 8bit 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0404			Register Name: CSIC_DMA_CH1_CFG_REG
Bit	Read/Write	Default/Hex	Description
20	R/W	0x0	YUV10_STO_FMT YUV 10bit store configure 0: YUV 10bit Stored in low 10bit of a 16bit-word 1: YUV 10bit Stored in high 10bit of a 16bit-word
19:16	R/W	0x0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: raw-8 0001: raw-10 0010: raw-12 0011: raw-14 0100: raw-16 0101: raw-20 0110: raw-24 0111: Reserved 1000: rgb565 1001: rgb888 1010: prgb888 others: Reserved When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined (UV sequence) 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined (UV sequence) 0111: frame planar YCbCr 422 UV combined (UV sequence) 1000: filed planar YCbCr 422 UV combined (VU sequence) 1001: field planar YCbCr 420 UV combined (VU sequence) 1010: frame planar YCbCr 420 UV combined (VU sequence) 1011: frame planar YCbCr 422 UV combined (VU sequence) 1100: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0404			Register Name: CSIC_DMA_CH1_CFG_REG
Bit	Read/Write	Default/Hex	Description
			1101: field YCbCr 400 1110: Reserved 1111: frame YCbCr 400 When the input format is set to YUV420. 0000: LBC Mode Output 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: Reserved 0100: Reserved 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined (UV sequence) 0111~1000: Reserved 1001: field planar YCbCr 420 UV combined (VU sequence) 1010: frame planar YCbCr 420 UV combined (VU sequence) 1011~1100: Reserved 1101: field YCbCr 400 1110: Reserved 1111: frame YCbCr 400
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0: Disable 1: Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0: Disable 1: Enable
11:10	R/W	0x0	FIELD_SEL Field selection. 00: Capturing with field 0. 01: Capturing with field 1. 10: Capturing with either field. 11: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0404			Register Name: CSIC_DMA_CH1_CFG_REG
Bit	Read/Write	Default/Hex	Description
9:6	R/W	0x0	FPS_DS_PRD Fps down sample period 0: 1 frames 1: 2 frames 2: 3 frames 3: 4 frames 4: 5 frames (p)(p) 15: 16 frames Note: CH1 FPS_DS_PRD should be used together with CSIC_DMA_CH1_FRM_MSK_CFG_REG bit[15:0]. Show an example as following. When CH1 FPS_DS_PRD is configured as 4'd6, CSIC_DMA_CH1_FRM_MSK_CFG_REG bit[6:0] will take effect and bit[15:7] will be ignored. If CSIC_DMA_CH1_FRM_MSK_CFG_REG bit[6:0] is configured as 7'b1011011, frame 0,frame 1, frame 3,frame 4, frame 6, frame 7,frame 8, frame 10,frame 11, frame 13...will be dropped.
5:2	R/W	0x0	CAP_FRONT_MASK_NUM Indicates the frame number masked after CAP_EN set.
1:0	/	/	/

16.1.14.52 0x0408 CSIC DMA Channel1 Frame Lost Counter Register (Default Value: 0x0000_0000)

Offset: 0x0408			Register Name: CSIC_DMA_CH1_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	FRM_LOST_CNT_EN When set 1, FRM_LOST_CNT is enable; when set 0, FRM_LOST_CNT is cleared
30:8	/	/	/
7:0	R	0x0	FRM_LOST_CNT Once a new frame comes when the buffer address not ready and FRM_DROP_EN set, or when the last frame still processing, the new frame is dropped and the FRM_LOST_CNT increases when FRM_LOST_CNT_EN set.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.14.53 0x040C CSIC DMA Channel1 Frame Mask Configuration Register (Default Value: 0x0000_0000)

Offset: 0x040C			Register Name: CSIC_DMA_CH1_FRM_MSK_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	FRAME_DATA_MASK Only [FPS_DS_PRD:0] are valid

16.1.14.54 0x0410 CSIC DMA Channel1 Horizontal Size Register (Default Value: 0x0500_0000)

Offset: 0x0410			Register Name: CSIC_DMA_CH1_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x500	HOR_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Horizontal pixel unit length. Valid pixel of a line in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

16.1.14.55 0x0414 CSIC DMA Channel1 Vertical Size Register (Default Value: 0x02d0_0000)

Offset: 0x0414			Register Name: CSIC_DMA_CH1_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x2d0	VER_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Valid line number of a frame in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

16.1.14.56 0x0418 CSIC DMA Channel1 Vertical Crop Mode Register (Default Value: 0x0000_0000)

Offset: 0x0418			Register Name: CSIC_DMA_CH1_VCROP_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0418			Register Name: CSIC_DMA_CH1_VCROP_CFG_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	FLD_FRM_VCROP_EN Field Frame Vcrop Enable 0: Disable field frame vcrop 1: Enable field frame vcrop When input frame is of field type and V crop wants to be implemented, this bit should be configured as 1. (note: only even lines crop is supported for field input V crop)

16.1.14.57 0x0420 CSIC DMA Channel1 FIFO 0 Output Buffer-A Address Register (Default Value: 0x0000_0000)

Offset: 0x0420			Register Name: CSIC_DMA_CH1_F0_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F0_BUFA When LBC_EN disable, these bits indicate FIFO 0 output buffer-A address in DMA mode. When LBC_EN enable, these bits indicate the output buffer address in LBC mode.

16.1.14.58 0x0424 CSIC DMA Channel1 FIFO 0 Output Buffer-A Address Result Register (Default Value: 0x0000_0000)

Offset: 0x0424			Register Name: CSIC_DMA_CH1_F0_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F0_BUFA_RESULT Indicate the final F0_BUFA address used for DMA or FBC after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

16.1.14.59 0x0428 CSIC DMA Channel1 FIFO 1 Output Buffer-A Address Register (Default Value: 0x0000_0000)

Offset: 0x0428			Register Name: CSIC_DMA_CH1_F1_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F1_BUFA FIFO 1 output buffer-A address.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.14.60 0x042C CSIC DMA Channel1 FIFO 1 Output Buffer-A Address Result Register (Default Value: 0x0000_0000)

Offset: 0x042C			Register Name: CSIC_DMA_CH1_F1_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F1_BUFA_RESULT Indicate the final F1_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

16.1.14.61 0x0430 CSIC DMA Channel1 FIFO 2 Output Buffer-A Address Register (Default Value: 0x0000_0000)

Offset: 0x0430			Register Name: CSIC_DMA_CH1_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address

16.1.14.62 0x0434 CSIC DMA Channel1 FIFO 2 Output Buffer-A Address Result Register (Default Value: 0x0000_0000)

Offset: 0x0434			Register Name: CSIC_DMA_CH1_F2_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F2_BUFA_RESULT Indicate the final F2_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

16.1.14.63 0x0438 CSIC DMA Channel1 Buffer Length Register (Default Value: 0x0280_0500)

Offset: 0x0438			Register Name: CSIC_DMA_CH1_BUF_LEN_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x280	BUF_LEN_C DMA_MODE: Buffer length of chroma C in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y in ONLY Y line. Unit is byte.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0438			Register Name: CSIC_DMA_CH1_BUF_LEN_REG
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x500	BUF_LEN DMA_MODE: Buffer length of luminance Y in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y and chroma C in YC line. Unit is byte.

16.1.14.64 0x043C CSIC DMA Channel1 Flip Size Register (Default Value: 0x02d0_0500)

Offset: 0x043C			Register Name: CSIC_DMA_CH1_FLIP_SIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x2d0	VER_LEN Vertical line number when in VFLIP mode. Unit is line. Only Readable when FLIP_SIZE_CFG_MODE set 0
15	/	/	/
14:0	R/W	0x500	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel component. Only Readable when FLIP_SIZE_CFG_MODE set 0

16.1.14.65 0x044C CSIC DMA Channel1 Capture Status Register (Default Value: 0x0000_0000)

Offset: 0x044C			Register Name: CSIC_DMA_CH1_CAP_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R	0x0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
1	/	/	/
0	R	0x0	CAP_STA capture in progress Indicates the CSI is capturing image data. The bit is set at the start of the first frame after enabling frame capture.

16.1.14.66 0x0450 CSIC DMA Channel1 Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0450	Register Name: CSIC_DMA_CH1_INT_EN_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	LACK_HBLANK_INT_EN Set an INT when trying filling dummy for missed pixels at the end of the line but hblank is too short.
22	R/W	0x0	LINE_REDUNDANT_INT_EN Set an INT when the amount of lines in one frame is more than expected.
21	R/W	0x0	LINE_MISS_INT_EN Set an INT when the amount of lines in one frame is less than expected.
20	R/W	0x0	PIXEL_REDUNDANT_INT_EN Set an INT when the amount of pixels in one line is more than expected.
19	R/W	0x0	PIXEL_MISS_INT_EN Set an INT when the amount of pixels in one line is less than expected.
18	R/W	0x0	BUF_ADDR_OVERFLOW_INT_EN Set an INT when buffer address is overwrite before used
17	R/W	0x0	BUF_ADDR_UNDERFLOW_INT_EN Set an INT when new frame comes but buffer address is not ready
16	R/W	0x0	LBC_HBLKMIN_INT_EN Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W	0x0	FRM_LOST_INT_EN Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W	0x0	STORED_FRM_CNT_INT_EN Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD , only use in BUF Address FIFO MODE
13	R/W	0x0	BUF_ADDR_FIFO_INT_EN Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
6	R/W	0x0	LI_OF_INT_EN Line information FIFO(16 lines) overflow.
5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every frame. The line number is set in the line counter register.
4:3	/	/	/
2	R/W	0x0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
1	R/W	0x0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been written to buffer. For video capture, the bit is set when the last frame has been written to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

16.1.14.67 0x0454 CSIC DMA Channel1 Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0454			Register Name: CSIC_DMA_CH1_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W1C	0x0	LACK_HBLANK_INT_PD Set an INT when trying filling dummy for missed pixels at the end of the line but hblank is too short.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0454			Register Name: CSIC_DMA_CH1_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
22	R/W1C	0x0	LINE_REDUNDANT_INT_PD Set an INT when the amount of lines in one frame is more than expected.
21	R/W1C	0x0	LINE_MISS_INT_PD Set an INT when the amount of lines in one frame is less than expected.
20	R/W1C	0x0	PIXEL_REDUNDANT_INT_PD Set an INT when the amount of pixels in one line is more than expected.
19	R/W1C	0x0	PIXEL_MISS_INT_PD Set an INT when the amount of pixels in one line is less than expected.
18	R/W1C	0x0	BUF_ADDR_OVERFLOW_INT_PD Set an INT when buffer address is overwrite before used
17	R/W1C	0x0	BUF_ADDR_UNDERFLOW_INT_PD Set an INT when new frame comes but buffer address is not ready
16	R/W1C	0x0	LBC_HBLKMIN_INT_PD Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W1C	0x0	FRM_LOST_INT_PD Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W1C	0x0	STORED_FRM_CNT_INT_PD Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE
13	R/W1C	0x0	BUF_ADDR_FIFO_INT_PD Set an INT when content in BUF Address FIFO no more than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	LI_OF_PD Line information FIFO(16 lines) overflow
5	R/W1C	0x0	LC_PD Line counter flag
4:3	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0454			Register Name: CSIC_DMA_CH1_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
2	R/W1C	0x0	FIFO0_OF_PD FIFO 0 overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

16.1.14.68 0x0458 CSIC DMA Channel1 Line Counter Register (Default Value: 0x0000_0000)

Offset: 0x0458			Register Name: CSIC_DMA_CH1_LINE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM value is set by users. When internal line counter reach the set value, the LC_PD will be set.

16.1.14.69 0x0468 CSIC DMA Channel1 Line Statistic Register (Default Value: 0x0000_0000)

Offset: 0x0468			Register Name: CSIC_DMA_CH1_LINE_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	LINE_INDEX Indicates the line index in current vsync.
15:0	/	/	/

16.1.14.70 0x0470 CSIC DMA Channel1 PCLK Statistic Register (Default Value: 0x0000_0000)

Offset: 0x0470			Register Name: CSIC_DMA_CH1_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.
15	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0470			Register Name: CSIC_DMA_CH1_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
14:0	R	0x0	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

16.1.14.71 0x0480 CSIC DMA Channel1 BUF Address FIFO0 Entry Register (Default Value: 0x0000_0000)

Offset: 0x0480			Register Name: CSIC_DMA_CH1_BUF_ADDR_FIFO0_ENTRY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO0_ENTRY FIFO Entry of Buffer Address FIFO0 for input frames to be stored, only used in Buffer Addr FIFO Mode

16.1.14.72 0x0484 CSIC DMA Channel1 BUF Address FIFO1 Entry Register (Default Value: 0x0000_0000)

Offset: 0x0484			Register Name: CSIC_DMA_CH1_BUF_ADDR_FIFO1_ENTRY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO1_ENTRY FIFO Entry of Buffer Address FIFO1 for input frames to be stored, only used in Buffer Addr FIFO Mode

16.1.14.73 0x0488 CSIC DMA Channel1 BUF Address FIFO2 Entry Register (Default Value: 0x0000_0000)

Offset: 0x0488			Register Name: CSIC_DMA_CH1_BUF_ADDR_FIFO2_ENTRY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO2_ENTRY FIFO Entry of Buffer Address FIFO2 for input frames to be stored, only used in Buffer Addr FIFO Mode

16.1.14.74 0x048C CSIC DMA Channel1 BUF Threshold Register (Default Value: 0x0020_0000)

Offset: 0x048C			Register Name: CSIC_DMA_CH1_BUF_TH_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x048C			Register Name: CSIC_DMA_CH1_BUF_TH_REG
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:16	R/W	0x20	CSIC_DMA_STORED_FRM_THRESHOLD when stored frame counter value reaches the threshold , counter is cleared to 0 , only used in Buffer Addr FIFO Mode
15:6	/	/	/
5:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO_THRESHOLD when content in Buffer Address FIFO no more than the threshold, an interrupt is set, only used in Buffer Addr FIFO Mode

16.1.14.75 0x0490 CSIC DMA Channel1 BUF Address FIFO Content Register (Default Value: 0x0000_0000)

Offset: 0x0490			Register Name: CSIC_DMA_CH1_BUF_ADDR_FIFO_CON_REG
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:16	R	0x0	CSIC_DMA_BUF_ADDR_FIFO2_CONTENT FIFO Content of address buffered in Buffer Address FIFO2, only used in Buffer Addr FIFO Mode
15:14	/	/	/
13:8	R	0x0	CSIC_DMA_BUF_ADDR_FIFO1_CONTENT FIFO Content of address buffered in Buffer Address FIFO1, only used in Buffer Addr FIFO Mode
7:6	/	/	/
5:0	R	0x0	CSIC_DMA_BUF_ADDR_FIFO0_CONTENT FIFO Content of address buffered in Buffer Address FIFO0, only used in Buffer Addr FIFO Mode

16.1.14.76 0x0494 CSIC DMA Channel1 Stored Frame Counter Register (Default Value: 0x0000_0000)

Offset: 0x0494			Register Name: CSIC_DMA_CH1_STORED_FRM_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0494			Register Name: CSIC_DMA_CH1_STORED_FRM_CNT_REG
Bit	Read/Write	Default/Hex	Description
7:0	R	0x0	CSIC_DMA_STORED_FRM_CNT Indicates value of stored frames counter, when counter value reaches CSIC_DMA_STORED_FRM_THRESHOLD, counter is cleared to 0, only used in Buffer Addr FIFO Mode

16.1.14.77 0x0498 CSIC DMA Channel1 Abnormal Mask Register (Default Value: 0x0000_0000)

Offset: 0x0498			Register Name: CSIC_DMA_CH1_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	FRM_DONE_INT_MSK_EN Decide whether the FD_INT of this frame will be masked or not once any abnormal condition happens during this frame. 0: Disable MSK 1: Enable MSK
4	R/W	0x0	LINE_REDUNDANT_MSK_EN Decide whether the remaining data in this frame will be dropped or not once line redundant error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
3	R/W	0x0	LINE_MISS_MSK_EN Decide whether the remaining data in this frame will be dropped or not once line miss error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0498			Register Name: CSIC_DMA_CH1_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	PIXEL_REDUNDANT_MSK_EN Decide whether the remaining data in this frame will be dropped or not once pixel redundant error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
1	R/W	0x0	PIXEL_MISS_MSK_EN Decide whether the remaining data in this frame will be dropped or not once pixel miss error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
0	R/W	0x0	VSYN_ABN_MSK_EN Decide whether the remaining data in this frame will be dropped or not once abnormal happens in this frame. 0: Disable MSK 1: Enable MSK Note: When VSYN_ABN_MSK_EN is set as 1 and one of the following conditions happens, the remaining data in this frame will be dropped. And the next frame will be received as normal. a. When trying to fill dummy for pixel miss and LACK_HBLANK happens. b. When PIXEL_REDUNDANT happens and PIXEL_REDUNDANT_MSK_EN is set as 1. c. When PIXEL_MISS happens, LACK_HBLANK no happen and PIXEL_MISS_MSK_EN is set as 1. d. When LINE_REDUNDANT happens and LINE_REDUNDANT_MSK_EN is set as 1. e. When LINE_MISS happens and LINE_MISS_MSK_EN is set as 1.

16.1.14.78 0x049C CSIC DMA Channel1 Pixels Add Enable Register (Default Value: 0x0000_0000)

Offset: 0x049C	Register Name: CSIC_DMA_CH1_PIXELS_ADD_EN_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	PIXELS_ADD_EN Decide whether dummy pixels will be added in the end of the line or not once pixels miss error happens. 0: Disable ADD 1: Enable ADD

16.1.14.79 0x04A0 CSIC DMA Channel1 Pixels Add Value Register (Default Value: 0x0000_0000)

Offset: 0x04A0			Register Name: CSIC_DMA_CH1_PIXELS_ADD_VAL_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PIXELS_ADD_VALUE Decide the value of dummy pixels when PIXELS_ADD_EN is set as 1

16.1.14.80 0x0600 CSIC DMA Channel2 Enable Register (Default Value: 0x0000_0000)

Offset: 0x0600			Register Name: CSIC_DMA_CH2_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	FRM_DROP_EN Drop Frame when vsync comes but buffer address is not ready 0: Not Drop 1: Drop
7	R/W	0x0	BUF_ADDR_MODE Frame buffer Address configuration mode 0: Buffer Address Register Mode 1: Buffer Address FIFO Mode
6:1	/	/	/
0	R/W	0x0	CAP_EN Video In Capture Enable 0: Disable 1: Enable

16.1.14.81 0x0604 CSIC DMA Channel2 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0604			Register Name: CSIC_DMA_CH2_CFG_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0604			Register Name: CSIC_DMA_CH2_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00~0xff
23:22	/	/	/
21	R/W	0x0	YUV10to8_EN YUV 10bit input cut to 8bit 0: Disable 1: Enable
20	R/W	0x0	YUV10_STO_FMT YUV 10bit store configure 0: YUV 10bit Stored in low 10bit of a 16bit-word 1: YUV 10bit Stored in high 10bit of a 16bit-word
19:16	R/W	0x0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: raw-8 0001: raw-10 0010: raw-12 0011: raw-14 0100: raw-16 0101: raw-20 0110: raw-24 0111: Reserved 1000: rgb565 1001: rgb888 1010: prgb888 others: Reserved When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined (UV sequence) 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined (UV sequence) 0111: frame planar YCbCr 422 UV combined (UV sequence) 1000: filed planar YCbCr 422 UV combined (VU

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0604			Register Name: CSIC_DMA_CH2_CFG_REG
Bit	Read/Write	Default/Hex	Description
			sequence) 1001: field planar YCbCr 420 UV combined (VU sequence) 1010: frame planar YCbCr 420 UV combined (VU sequence) 1011: frame planar YCbCr 422 UV combined (VU sequence) 1100: Reserved 1101: field YCbCr 400 1110: Reserved 1111: frame YCbCr 400 When the input format is set YUV420 0000: LBC Mode Output 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: Reserved 0100: Reserved 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined (UV sequence) 0111~1000: Reserved 1001: field planar YCbCr 420 UV combined (VU sequence) 1010: frame planar YCbCr 420 UV combined (VU sequence) 1011~1100: Reserved 1101: field YCbCr 400 1110: Reserved 1111: frame YCbCr 400
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0604			Register Name: CSIC_DMA_CH2_CFG_REG
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0: Disable 1: Enable
11:10	R/W	0x0	FIELD_SEL Field selection. 00: capturing with field 0. 01: capturing with field 1. 10: capturing with either field. 11: Reserved
9:6	R/W	0x0	FPS_DS_PRD Fps down sample period 0x0: 1 frames 0x1: 2 frames 0x2: 3 frames 0x3: 4 frames 0x4: 5 frames (p)(p) 0xF: 16 frames Note: CH2 FPS_DS_PRD should be used together with CSIC_DMA_CH2_FRM_MSK_CFG_REG bit[15:0]. Show an example as following. When CH2 FPS_DS_PRD is configured as 4'd6, CSIC_DMA_CH2_FRM_MSK_CFG_REG bit[6:0] will take effect and bit[15:7] will be ignored. If CSIC_DMA_CH2_FRM_MSK_CFG_REG bit[6:0] is configured as 7'b1011011, frame 0,frame 1, frame 3,frame 4, frame 6, frame 7,frame 8, frame 10,frame 11, frame 13...will be dropped.
5:2	R/W	0x0	CAP_FRONT_MASK_NUM Indicates the frame number masked after CAP_EN set.
1:0	/	/	/

16.1.14.82 0x0608 CSIC DMA Channel2 Frame Lost Counter Register (Default Value: 0x0000_0000)

Offset: 0x0608			Register Name: CSIC_DMA_CH2_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0608			Register Name: CSIC_DMA_CH2_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	FRM_LOST_CNT_EN When set 1, FRM_LOST_CNT is enable; when set 0, FRM_LOST_CNT is cleared
30:8	/	/	/
7:0	R	0x0	FRM_LOST_CNT Once a new frame comes when the buffer address not ready and FRM_DROP_EN set, or when the last frame still processing, the new frame is dropped and the FRM_LOST_CNT increases when FRM_LOST_CNT_EN set.

16.1.14.83 0x060C CSIC DMA Channel2 Frame Mask Configuration Register (Default Value: 0x0000_0000)

Offset: 0x060C			Register Name: CSIC_DMA_CH2_FRM_MSK_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	FRAME_DATA_MASK Only [FPS_DS_PRD:0] are valid

16.1.14.84 0x0610 CSIC DMA Channel2 Horizontal Size Register (Default Value: 0x0500_0000)

Offset: 0x0610			Register Name: CSIC_DMA_CH2_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x500	HOR_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Horizontal pixel unit length. Valid pixel of a line in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

16.1.14.85 0x0614 CSIC DMA Channel2 Vertical Size Register (Default Value: 0x02d0_0000)

Offset: 0x0614			Register Name: CSIC_DMA_CH2_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0614			Register Name: CSIC_DMA_CH2_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
29:16	R/W	0x2d0	VER_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Valid line number of a frame in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

16.1.14.86 0x0618 CSIC DMA Channel2 Vertical Crop Mode Register (Default Value: 0x0000_0000)

Offset: 0x0618			Register Name: CSIC_DMA_CH2_VCROP_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	FLD_FRM_VCROP_EN Field Frame Vcrop Enable 0: Disable field frame vcrop 1: Enable field frame vcrop When input frame is of field type and V crop wants to be implemented, this bit should be configured as 1. (note: only even lines crop is supported for field input V crop)

16.1.14.87 0x0620 CSIC DMA Channel2 FIFO 0 Output Buffer-A Address Register (Default Value: 0x0000_0000)

Offset: 0x0620			Register Name: CSIC_DMA_CH2_F0_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F0_BUFA When LBC_EN disable, these bits indicate FIFO 0 output buffer-A address in DMA mode. When LBC_EN enable, these bits indicate the output buffer address in LBC mode.

16.1.14.88 0x0624 CSIC DMA Channel2 FIFO 0 Output Buffer-A Address Result Register (Default Value: 0x0000_0000)

Offset: 0x0624			Register Name: CSIC_DMA_CH2_F0_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0624			Register Name: CSIC_DMA_CH2_F0_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F0_BUFA_RESULT Indicate the final F0_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

16.1.14.89 0x0628 CSIC DMA Channel2 FIFO 1 Output Buffer-A Address Register (Default Value: 0x0000_0000)

Offset: 0x0628			Register Name: CSIC_DMA_CH2_F1_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F1_BUFA FIFO 1 output buffer-A address.

16.1.14.90 0x062C CSIC DMA Channel2 FIFO 1 Output Buffer-A Address Result Register (Default Value: 0x0000_0000)

Offset: 0x062C			Register Name: CSIC_DMA_CH2_F1_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F1_BUFA_RESULT Indicate the final F1_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

16.1.14.91 0x0630 CSIC DMA Channel2 FIFO 2 Output Buffer-A Address Register (Default Value: 0x0000_0000)

Offset: 0x0630			Register Name: CSIC_DMA_CH2_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.14.92 0x0634 CSIC DMA Channel2 FIFO 2 Output Buffer-A Address Result Register (Default Value: 0x0000_0000)

Offset: 0x0634			Register Name: CSIC_DMA_CH2_F2_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F2_BUFA_RESULT Indicate the final F2_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

16.1.14.93 0x0638 CSIC DMA Channel2 Buffer Length Register (Default Value: 0x0280_0500)

Offset: 0x0638			Register Name: CSIC_DMA_CH2_BUF_LEN_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x280	BUF_LEN_C DMA_MODE: Buffer length of chroma C in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y in ONLY Y line. Unit is byte.
15:0	R/W	0x500	BUF_LEN DMA_MODE: Buffer length of luminance Y in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y and chroma C in YC line. Unit is byte.

16.1.14.94 0x063C CSIC DMA Channel2 Flip Size Register (Default Value: 0x02d0_0500)

Offset: 0x063C			Register Name: CSIC_DMA_CH2_FLIP_SIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x2d0	VER_LEN Vertical line number when in VFLIP mode. Unit is line. Only Readable when FLIP_SIZE_CFG_MODE set 0
15	/	/	/
14:0	R/W	0x500	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel component. Only Readable when FLIP_SIZE_CFG_MODE set 0

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.14.95 0x064C CSIC DMA Channel2 Capture Status Register (Default Value: 0x0000_0000)

Offset: 0x064C			Register Name: CSIC_DMA_CH2_CAP_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R	0x0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
1	/	/	/
0	R	0x0	CAP_STA capture in progress Indicates the CSI is capturing image data. The bit is set at the start of the first frame after enabling frame capture.

16.1.14.96 0x0650 CSIC DMA Channel2 Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0650			Register Name: CSIC_DMA_CH2_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	LACK_HBLANK_INT_EN Set an INT when trying filling dummy for missed pixels at the end of the line but hblank is too short.
22	R/W	0x0	LINE_REDUNDANT_INT_EN Set an INT when the amount of lines in one frame is more than expected.
21	R/W	0x0	LINE_MISS_INT_EN Set an INT when the amount of lines in one frame is less than expected.
20	R/W	0x0	PIXEL_REDUNDANT_INT_EN Set an INT when the amount of pixels in one line is more than expected.
19	R/W	0x0	PIXEL_MISS_INT_EN Set an INT when the amount of pixels in one line is less than expected.
18	R/W	0x0	BUF_ADDR_OVERFLOW_INT_EN Set an INT when buffer address is overwrite before used
17	R/W	0x0	BUF_ADDR_UNDERFLOW_INT_EN Set an INT when new frame comes but buffer address is not ready

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0650			Register Name: CSIC_DMA_CH2_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	LBC_HBLKMIN_INT_EN Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W	0x0	FRM_LOST_INT_EN Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W	0x0	STORED_FRM_CNT_INT_EN Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD , only use in BUF Address FIFO MODE
13	R/W	0x0	BUF_ADDR_FIFO_INT_EN Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
6	R/W	0x0	LI_OF_INT_EN Line information FIFO(16 lines) overflow.
5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every frame. The line number is set in the line counter register.
4:3	/	/	/
2	R/W	0x0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
1	R/W	0x0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0650			Register Name: CSIC_DMA_CH2_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been written to buffer. For video capture, the bit is set when the last frame has been written to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

16.1.14.97 0x0654 CSIC DMA Channel2 Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0654			Register Name: CSIC_DMA_CH2_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W1C	0x0	LACK_HBLANK_INT_PD Set an INT when trying filling dummy for missed pixels at the end of the line but hblank is too short.
22	R/W1C	0x0	LINE_REDUNDANT_INT_PD Set an INT when the amount of lines in one frame is more than expected.
21	R/W1C	0x0	LINE_MISS_INT_PD Set an INT when the amount of lines in one frame is less than expected.
20	R/W1C	0x0	PIXEL_REDUNDANT_INT_PD Set an INT when the amount of pixels in one line is more than expected.
19	R/W1C	0x0	PIXEL_MISS_INT_PD Set an INT when the amount of pixels in one line is less than expected.
18	R/W1C	0x0	BUF_ADDR_OVERFLOW_INT_PD Set an INT when buffer address is overwrite before used
17	R/W1C	0x0	BUF_ADDR_UNDERFLOW_INT_PD Set an INT when new frame comes but buffer address is not ready

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0654			Register Name: CSIC_DMA_CH2_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
16	R/W1C	0x0	LBC_HBLKMIN_INT_PD Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W1C	0x0	FRM_LOST_INT_PD Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W1C	0x0	STORED_FRM_CNT_INT_PD Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE
13	R/W1C	0x0	BUF_ADDR_FIFO_INT_PD Set an INT when content in BUF Address FIFO no more than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	LI_OF_PD Line information FIFO(16 lines) overflow
5	R/W1C	0x0	LC_PD Line counter flag
4:3	/	/	/
2	R/W1C	0x0	FIFO0_OF_PD FIFO 0 overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

16.1.14.98 0x0658 CSIC DMA Channel2 Line Counter Register (Default Value: 0x0000_0000)

Offset: 0x0658			Register Name: CSIC_DMA_CH2_LINE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM value is set by user, when internal line counter reach the set value, the LC_PD will set.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.14.99 0x0668 CSIC DMA Channel2 Line Statistic Register (Default Value: 0x0000_0000)

Offset: 0x0668			Register Name: CSIC_DMA_CH2_LINE_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	LINE_INDEX Indicates the line index in current vsync.
15:0	/	/	/

16.1.14.100 0x0670 CSIC DMA Channel2 PCLK Statistic Register (Default Value: 0x0000_0000)

Offset: 0x0670			Register Name: CSIC_DMA_CH2_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.
15	/	/	/
14:0	R	0x0	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

16.1.14.101 0x0680 CSIC DMA Channel2 BUF Address FIFO0 Entry Register (Default Value: 0x0000_0000)

Offset: 0x0680			Register Name: CSIC_DMA_CH2_BUF_ADDR_FIFO0_ENTRY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO0_ENTRY FIFO Entry of Buffer Address FIFO0 for input frames to be stored, only used in Buffer Addr FIFO Mode

16.1.14.102 0x0684 CSIC DMA Channel2 BUF Address FIFO1 Entry Register (Default Value: 0x0000_0000)

Offset: 0x0684			Register Name: CSIC_DMA_CH2_BUF_ADDR_FIFO1_ENTRY_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0684			Register Name: CSIC_DMA_CH2_BUF_ADDR_FIFO1_ENTRY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO1_ENTRY FIFO Entry of Buffer Address FIFO1 for input frames to be stored, only used in Buffer Addr FIFO Mode

16.1.14.103 0x0688 CSIC DMA Channel2 BUF Address FIFO2 Entry Register (Default Value: 0x0000_0000)

Offset: 0x0688			Register Name: CSIC_DMA_CH2_BUF_ADDR_FIFO2_ENTRY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO2_ENTRY FIFO Entry of Buffer Address FIFO2 for input frames to be stored, only used in Buffer Addr FIFO Mode

16.1.14.104 0x068C CSIC DMA Channel2 BUF Threshold Register (Default Value: 0x0020_0000)

Offset: 0x068C			Register Name: CSIC_DMA_CH2_BUF_TH_REG
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:16	R/W	0x20	CSIC_DMA_STORED_FRM_THRESHOLD when stored frame counter value reaches the threshold , counter is cleared to 0 , only used in Buffer Addr FIFO Mode
15:6	/	/	/
5:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO_THRESHOLD when content in Buffer Address FIFO no more than the threshold, an interrupt is set, only used in Buffer Addr FIFO Mode

16.1.14.105 0x0690 CSIC DMA Channel2 BUF Address FIFO Content Register (Default Value: 0x0000_0000)

Offset: 0x0690			Register Name: CSIC_DMA_CH2_BUF_ADDR_FIFO_CON_REG
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:16	R	0x0	CSIC_DMA_BUF_ADDR_FIFO2_CONTENT FIFO Content of address buffered in Buffer Address FIFO2, only used in Buffer Addr FIFO Mode

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0690			Register Name: CSIC_DMA_CH2_BUF_ADDR_FIFO_CON_REG
Bit	Read/Write	Default/Hex	Description
15:14	/	/	/
13:8	R	0x0	CSIC_DMA_BUF_ADDR_FIFO1_CONTENT FIFO Content of address buffered in Buffer Address FIFO1, only used in Buffer Addr FIFO Mode
7:6	/	/	/
5:0	R	0x0	CSIC_DMA_BUF_ADDR_FIFO0_CONTENT FIFO Content of address buffered in Buffer Address FIFO0, only used in Buffer Addr FIFO Mode

16.1.14.106 0x0694 CSIC DMA Channel2 Stored Frame Counter Register (Default Value: 0x0000_0000)

Offset: 0x0694			Register Name: CSIC_DMA_CH2_STORED_FRM_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	CSIC_DMA_STORED_FRM_CNT Indicates value of stored frames counter, when counter value reaches CSIC_DMA_STORED_FRM_THRESHOLD, counter is cleared to 0, only used in Buffer Addr FIFO Mode

16.1.14.107 0x0698 CSIC DMA Channel2 Abnormal Mask Register (Default Value: 0x0000_0000)

Offset: 0x0698			Register Name: CSIC_DMA_CH2_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	FRM_DONE_INT_MSK_EN Decide whether the FD_INT of this frame will be masked or not once any abnormal condition happens during this frame. 0: Disable MSK 1: Enable MSK
4	R/W	0x0	LINE_REDUNDANT_MSK_EN Decide whether the remaining data in this frame will be dropped or not once line redundant error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0698			Register Name: CSIC_DMA_CH2_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	LINE_MISS_MSK_EN Decide whether the remaining data in this frame will be dropped or not once line miss error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
2	R/W	0x0	PIXEL_REDUNDANT_MSK_EN Decide whether the remaining data in this frame will be dropped or not once pixel redundant error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
1	R/W	0x0	PIXEL_MISS_MSK_EN Decide whether the remaining data in this frame will be dropped or not once pixel miss error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0698			Register Name: CSIC_DMA_CH2_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	VSYN_ABN_MSK_EN Decide whether the remaining data in this frame will be dropped or not once abnormal happens in this frame. 0: Disable MSK 1: Enable MSK Note: When VSYN_ABN_MSK_EN is set as 1 and one of the following conditions happens, the remaining data in this frame will be dropped. And the next frame will be received as normal. a. When trying to fill dummy for pixel miss and LACK_HBLANK happens. b. When PIXEL_REDUNDANT happens and PIXEL_REDUNDANT_MSK_EN is set as 1. c. When PIXEL_MISS happens, LACK_HBLANK no happen and PIXEL_MISS_MSK_EN is set as 1. d. When LINE_REDUNDANT happens and LINE_REDUNDANT_MSK_EN is set as 1. e. When LINE_MISS happens and LINE_MISS_MSK_EN is set as 1.

16.1.14.108 0x069C CSIC DMA Channel2 Pixels Add Enable Register (Default Value: 0x0000_0000)

Offset: 0x069C			Register Name: CSIC_DMA_CH2_PIXELS_ADD_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	PIXELS_ADD_EN Decide whether dummy pixels will be added in the end of the line or not once pixels miss error happens. 0: Disable ADD 1: Enable ADD

16.1.14.109 0x06A0 CSIC DMA Channel2 Pixels Add Value Register (Default Value: 0x0000_0000)

Offset: 0x06A0			Register Name: CSIC_DMA_CH2_PIXELS_ADD_VAL_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x06A0			Register Name: CSIC_DMA_CH2_PIXELS_ADD_VAL_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PIXELS_ADD_VALUE Decide the value of dummy pixels when PIXELS_ADD_EN is set as 1

16.1.14.110 0x0800 CSIC DMA Channel3 Enable Register (Default Value: 0x0000_0000)

Offset: 0x0800			Register Name: CSIC_DMA_CH3_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	FRM_DROP_EN Drop Frame when vsync comes but buffer address is not ready 0: Not Drop 1: Drop
7	R/W	0x0	BUF_ADDR_MODE Frame buffer Address configuration mode 0: Buffer Address Register Mode 1: Buffer Address FIFO Mode
6:2	/	/	/
1	R/W	0x0	LBC_EN LBC Function Enable 0: Disable 1: Enable
0	R/W	0x0	CAP_EN Video In Capture Enable 0: Disable 1: Enable

16.1.14.111 0x0804 CSIC DMA Channel3 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0804			Register Name: CSIC_DMA_CH3_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00~0xff
23:22	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0804			Register Name: CSIC_DMA_CH3_CFG_REG
Bit	Read/Write	Default/Hex	Description
21	R/W	0x0	YUV10to8_EN YUV 10bit input cut to 8bit 0: Disable 1: Enable
20	R/W	0x0	YUV10_STO_FMT YUV 10bit store configure 0: YUV 10bit Stored in low 10bit of a 16bit-word 1: YUV 10bit Stored in high 10bit of a 16bit-word
19:16	R/W	0x0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: raw-8 0001: raw-10 0010: raw-12 0011: raw-14 0100: raw-16 0101: raw-20 0110: raw-24 0111: Reserved 1000: rgb565 1001: rgb888 1010: prgb888 others: Reserved When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined (UV sequence) 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined (UV sequence) 0111: frame planar YCbCr 422 UV combined (UV sequence) 1000: filed planar YCbCr 422 UV combined (VU sequence) 1001: field planar YCbCr 420 UV combined (VU sequence) 1010: frame planar YCbCr 420 UV combined (VU

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0804			Register Name: CSIC_DMA_CH3_CFG_REG
Bit	Read/Write	Default/Hex	Description
			sequence) 1011: frame planar YCbCr 422 UV combined (VU sequence) 1100: Reserved 1101: field YCbCr 400 1110: Reserved 1111: frame YCbCr 400 When the input format is set YUV420 0000: LBC Mode Output 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: Reserved 0100: Reserved 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined (UV sequence) 0111~1000: Reserved 1001: field planar YCbCr 420 UV combined (VU sequence) 1010: frame planar YCbCr 420 UV combined (VU sequence) 1011~1100: Reserved 1101: field YCbCr 400 1110: Reserved 1111: frame YCbCr 400
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0: Disable 1: Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0804			Register Name: CSIC_DMA_CH3_CFG_REG
Bit	Read/Write	Default/Hex	Description
11:10	R/W	0x0	FIELD_SEL Field selection. 00: capturing with field 0. 01: capturing with field 1. 10: capturing with either field. 11: Reserved
9:6	R/W	0x0	FPS_DS_PRD Fps down sample period 0x0: 1 frames 0x1: 2 frames 0x2: 3 frames 0x3: 4 frames 0x4: 5 frames (p)(p) 0xf: 16 frames Note: CH3 FPS_DS_PRD should be used together with CSIC_DMA_CH3_FRM_MSK_CFG_REG bit[15:0]. Show an example as following. When CH3 FPS_DS_PRD is configured as 4'd6, CSIC_DMA_CH3_FRM_MSK_CFG_REG bit[6:0] will take effect and bit[15:7] will be ignored. If CSIC_DMA_CH3_FRM_MSK_CFG_REG bit[6:0] is configured as 7'b1011011, frame 0,frame 1, frame 3,frame 4, frame 6, frame 7,frame 8, frame 10,frame 11, frame 13...will be dropped.
5:2	R/W	0x0	CAP_FRONT_MASK_NUM Indicates the frame number masked after CAP_EN set.
1:0	/	/	/

16.1.14.112 0x0808 CSIC DMA Channel3 Frame Lost Counter Register (Default Value: 0x0000_0000)

Offset: 0x0808			Register Name: CSIC_DMA_CH3_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	FRM_LOST_CNT_EN When set 1, FRM_LOST_CNT is enable; when set 0, FRM_LOST_CNT is cleared
30:8	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0808			Register Name: CSIC_DMA_CH3_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description
7:0	R	0x0	FRM_LOST_CNT Once a new frame comes when the buffer address not ready and FRM_DROP_EN set, or when the last frame still processing, the new frame is dropped and the FRM_LOST_CNT increases when FRM_LOST_CNT_EN set.

16.1.14.113 0x080C CSIC DMA Channel3 Frame Mask Configuration Register (Default Value: 0x0000_0000)

Offset: 0x080C			Register Name: CSIC_DMA_CH3_FRM_MSK_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	FRAME_DATA_MASK Only [FPS_DS_PRD:0] are valid

16.1.14.114 0x0810 CSIC DMA Channel3 Horizontal Size Register (Default Value: 0x0500_0000)

Offset: 0x0810			Register Name: CSIC_DMA_CH3_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x500	HOR_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Horizontal pixel unit length. Valid pixel of a line in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

16.1.14.115 0x0814 CSIC DMA Channel3 Vertical Size Register (Default Value: 0x02d0_0000)

Offset: 0x0814			Register Name: CSIC_DMA_CH3_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x2d0	VER_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Valid line number of a frame in DMA mode.
15:14	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0814			Register Name: CSIC_DMA_CH3_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

16.1.14.116 0x0818 CSIC DMA Channel3 Vertical Crop Mode Register (Default Value: 0x0000_0000)

Offset: 0x0818			Register Name: CSIC_DMA_CH3_VCROP_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	FLD_FRM_VCROP_EN Field Frame Vcrop Enable 0: Disable field frame vcrop 1: Enable field frame vcrop When input frame is of field type and V crop wants to be implemented, this bit should be configured as 1. (note: only even lines crop is supported for field input V crop)

16.1.14.117 0x0820 CSIC DMA Channel3 FIFO 0 Output Buffer-A Address Register (Default Value: 0x0000_0000)

Offset: 0x0820			Register Name: CSIC_DMA_CH3_F0_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F0_BUFA When LBC_EN disable, these bits indicate FIFO 0 output buffer-A address in DMA mode. When LBC_EN enable, these bits indicate the output buffer address in LBC mode.

16.1.14.118 0x0824 CSIC DMA Channel3 FIFO 0 Output Buffer-A Address Result Register (Default Value: 0x0000_0000)

Offset: 0x0824			Register Name: CSIC_DMA_CH3_F0_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F0_BUFA_RESULT Indicate the final F0_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.14.119 0x0828 CSIC DMA Channel3 FIFO 1 Output Buffer-A Address Register (Default Value: 0x0000_0000)

Offset: 0x0828			Register Name: CSIC_DMA_CH3_F1_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F1_BUFA FIFO 1 output buffer-A address in DMA mode.

16.1.14.120 0x082C CSIC DMA Channel3 FIFO 1 Output Buffer-A Address Result Register (Default Value: 0x0000_0000)

Offset: 0x082C			Register Name: CSIC_DMA_CH3_F1_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F1_BUFA_RESULT Indicate the final F1_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

16.1.14.121 0x0830 CSIC DMA Channel3 FIFO 2 Output Buffer-A Address Register (Default Value: 0x0000_0000)

Offset: 0x0830			Register Name: CSIC_DMA_CH3_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address

16.1.14.122 0x0834 CSIC DMA Channel3 FIFO 2 Output Buffer-A Address Result Register (Default Value: 0x0000_0000)

Offset: 0x0834			Register Name: CSIC_DMA_CH3_F2_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F2_BUFA_RESULT Indicate the final F2_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.14.123 0x0838 CSIC DMA Channel3 Buffer Length Register (Default Value: 0x0280_0500)

Offset: 0x0838			Register Name: CSIC_DMA_CH3_BUF_LEN_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x280	BUF_LEN_C DMA_MODE: Buffer length of chroma C in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y in ONLY Y line. Unit is byte.
15:0	R/W	0x500	BUF_LEN DMA_MODE: Buffer length of luminance Y in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y and chroma C in YC line. Unit is byte.

16.1.14.124 0x083C CSIC DMA Channel3 Flip Size Register (Default Value: 0x02d0_0500)

Offset: 0x083C			Register Name: CSIC_DMA_CH3_FLIP_SIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x2d0	VER_LEN Vertical line number when in VFLIP mode. Unit is line. Only Readable when FLIP_SIZE_CFG_MODE set 0
15	/	/	/
14:0	R/W	0x500	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel component. Only Readable when FLIP_SIZE_CFG_MODE set 0

16.1.14.125 0x084C CSIC DMA Channel3 Capture Status Register (Default Value: 0x0000_0000)

Offset: 0x084C			Register Name: CSIC_DMA_CH3_CAP_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R	0x0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x084C			Register Name: CSIC_DMA_CH3_CAP_STA_REG
Bit	Read/Write	Default/Hex	Description
0	R	0x0	CAP_STA capture in progress Indicates the CSI is capturing image data. The bit is set at the start of the first frame after enabling frame capture.

16.1.14.126 0x0850 CSIC DMA Channel3 Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0850			Register Name: CSIC_DMA_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	LACK_HBLANK_INT_EN Set an INT when trying filling dummy for missed pixels at the end of the line but hblank is too short.
22	R/W	0x0	LINE_REDUNDANT_INT_EN Set an INT when the amount of lines in one frame is more than expected.
21	R/W	0x0	LINE_MISS_INT_EN Set an INT when the amount of lines in one frame is less than expected.
20	R/W	0x0	PIXEL_REDUNDANT_INT_EN Set an INT when the amount of pixels in one line is more than expected.
19	R/W	0x0	PIXEL_MISS_INT_EN Set an INT when the amount of pixels in one line is less than expected.
18	R/W	0x0	BUF_ADDR_OVERFLOW_INT_EN Set an INT when buffer address is overwrite before used
17	R/W	0x0	BUF_ADDR_UNDERFLOW_INT_EN Set an INT when new frame comes but buffer address is not ready
16	R/W	0x0	LBC_HBLKMIN_INT_EN Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W	0x0	FRM_LOST_INT_EN Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0850			Register Name: CSIC_DMA_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
14	R/W	0x0	STORED_FRM_CNT_INT_EN Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD , only use in BUF Address FIFO MODE
13	R/W	0x0	BUF_ADDR_FIFO_INT_EN Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
6	R/W	0x0	LI_OF_INT_EN Line information FIFO(16 lines) overflow.
5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every frame. The line number is set in the line counter register.
4:3	/	/	/
2	R/W	0x0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
1	R/W	0x0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0850			Register Name: CSIC_DMA_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been written to buffer. For video capture, the bit is set when the last frame has been written to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

16.1.14.127 0x0854 CSIC DMA Channel3 Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0854			Register Name: CSIC_DMA_CH3_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W1C	0x0	LACK_HBLANK_INT_PD Set an INT when trying filling dummy for missed pixels at the end of the line but hblank is too short.
22	R/W1C	0x0	LINE_REDUNDANT_INT_PD Set an INT when the amount of lines in one frame is more than expected.
21	R/W1C	0x0	LINE_MISS_INT_PD Set an INT when the amount of lines in one frame is less than expected.
20	R/W1C	0x0	PIXEL_REDUNDANT_INT_PD Set an INT when the amount of pixels in one line is more than expected.
19	R/W1C	0x0	PIXEL_MISS_INT_PD Set an INT when the amount of pixels in one line is less than expected.
18	R/W1C	0x0	BUF_ADDR_OVERFLOW_INT_PD Set an INT when buffer address is overwrite before used
17	R/W1C	0x0	BUF_ADDR_UNDERFLOW_INT_PD Set an INT when new frame comes but buffer address is not ready

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0854			Register Name: CSIC_DMA_CH3_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
16	R/W1C	0x0	LBC_HBLKMIN_INT_PD Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W1C	0x0	FRM_LOST_INT_PD Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W1C	0x0	STORED_FRM_CNT_INT_PD Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE
13	R/W1C	0x0	BUF_ADDR_FIFO_INT_PD Set an INT when content in BUF Address FIFO no more than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	LI_OF_PD Line information FIFO(16 lines) overflow
5	R/W1C	0x0	LC_PD Line counter flag
4:3	/	/	/
2	R/W1C	0x0	FIFO0_OF_PD FIFO 0 overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

16.1.14.128 0x0858 CSIC DMA Channel3 Line Counter Register (Default Value: 0x0000_0000)

Offset: 0x0858			Register Name: CSIC_DMA_CH3_LINE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM value is set by user, when internal line counter reach the set value, the LC_PD will set.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

16.1.14.129 0x0868 CSIC DMA Channel3 Line Statistic Register (Default Value: 0x0000_0000)

Offset: 0x0868			Register Name: CSIC_DMA_CH3_LINE_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	LINE_INDEX Indicates the line index in current vsync.
15:0	/	/	/

16.1.14.130 0x0870 CSIC DMA Channel3 PCLK Statistic Register (Default Value: 0x0000_0000)

Offset: 0x0870			Register Name: CSIC_DMA_CH3_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.
15	/	/	/
14:0	R	0x0	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

16.1.14.131 0x0880 CSIC DMA Channel3 BUF Address FIFO0 Entry Register (Default Value: 0x0000_0000)

Offset: 0x0880			Register Name: CSIC_DMA_CH3_BUF_ADDR_FIFO0_ENTRY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO0_ENTRY FIFO Entry of Buffer Address FIFO0 for input frames to be stored, only used in Buffer Addr FIFO Mode

16.1.14.132 0x0884 CSIC DMA Channel3 BUF Address FIFO1 Entry Register (Default Value: 0x0000_0000)

Offset: 0x0884			Register Name: CSIC_DMA_CH3_BUF_ADDR_FIFO1_ENTRY_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0884			Register Name: CSIC_DMA_CH3_BUF_ADDR_FIFO1_ENTRY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO1_ENTRY FIFO Entry of Buffer Address FIFO1 for input frames to be stored, only used in Buffer Addr FIFO Mode

16.1.14.133 0x0888 CSIC DMA Channel3 BUF Address FIFO2 Entry Register (Default Value: 0x0000_0000)

Offset: 0x0888			Register Name: CSIC_DMA_CH3_BUF_ADDR_FIFO2_ENTRY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO2_ENTRY FIFO Entry of Buffer Address FIFO2 for input frames to be stored, only used in Buffer Addr FIFO Mode

16.1.14.134 0x088C CSIC DMA Channel3 BUF Threshold Register (Default Value: 0x0020_0000)

Offset: 0x088C			Register Name: CSIC_DMA_CH3_BUF_TH_REG
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:16	R/W	0x20	CSIC_DMA_STORED_FRM_THRESHOLD when stored frame counter value reaches the threshold , counter is cleared to 0 , only used in Buffer Addr FIFO Mode
15:6	/	/	/
5:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO_THRESHOLD when content in Buffer Address FIFO no more than the threshold, an interrupt is set, only used in Buffer Addr FIFO Mode

16.1.14.135 0x0890 CSIC DMA Channel3 BUF Address FIFO Content Register (Default Value: 0x0000_0000)

Offset: 0x0890			Register Name: CSIC_DMA_CH3_BUF_ADDR_FIFO_CON_REG
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:16	R	0x0	CSIC_DMA_BUF_ADDR_FIFO2_CONTENT FIFO Content of address buffered in Buffer Address FIFO2, only used in Buffer Addr FIFO Mode

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0890			Register Name: CSIC_DMA_CH3_BUF_ADDR_FIFO_CON_REG
Bit	Read/Write	Default/Hex	Description
15:14	/	/	/
13:8	R	0x0	CSIC_DMA_BUF_ADDR_FIFO1_CONTENT FIFO Content of address buffered in Buffer Address FIFO1, only used in Buffer Addr FIFO Mode
7:6	/	/	/
5:0	R	0x0	CSIC_DMA_BUF_ADDR_FIFO0_CONTENT FIFO Content of address buffered in Buffer Address FIFO0, only used in Buffer Addr FIFO Mode

16.1.14.136 0x0894 CSIC DMA Channel3 Stored Frame Counter Register (Default Value: 0x0000_0000)

Offset: 0x0894			Register Name: CSIC_DMA_CH3_STORED_FRM_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	CSIC_DMA_STORED_FRM_CNT Indicates value of stored frames counter, when counter value reaches CSIC_DMA_STORED_FRM_THRESHOLD, counter is cleared to 0, only used in Buffer Addr FIFO Mode

16.1.14.137 0x0898 CSIC DMA Channel3 Abnormal Mask Register (Default Value: 0x0000_0000)

Offset: 0x0898			Register Name: CSIC_DMA_CH3_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	FRM_DONE_INT_MSK_EN Decide whether the FD_INT of this frame will be masked or not once any abnormal condition happens during this frame. 0: Disable MSK 1: Enable MSK
4	R/W	0x0	LINE_REDUNDANT_MSK_EN Decide whether the remaining data in this frame will be dropped or not once line redundant error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0898			Register Name: CSIC_DMA_CH3_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	LINE_MISS_MSK_EN Decide whether the remaining data in this frame will be dropped or not once line miss error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
2	R/W	0x0	PIXEL_REDUNDANT_MSK_EN Decide whether the remaining data in this frame will be dropped or not once pixel redundant error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
1	R/W	0x0	PIXEL_MISS_MSK_EN Decide whether the remaining data in this frame will be dropped or not once pixel miss error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0898			Register Name: CSIC_DMA_CH3_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	VSYN_ABN_MSK_EN Decide whether the remaining data in this frame will be dropped or not once abnormal happens in this frame. 0: Disable MSK 1: Enable MSK Note: When VSYN_ABN_MSK_EN is set as 1 and one of the following conditions happens, the remaining data in this frame will be dropped. And the next frame will be received as normal. a. when trying to fill dummy for pixel miss and LACK_HBLANK happens. b. when PIXEL_REDUNDANT happens and PIXEL_REDUNDANT_MSK_EN is set as 1. c. when PIXEL_MISS happens, LACK_HBLANK no happen and PIXEL_MISS_MSK_EN is set as 1. d. when LINE_REDUNDANT happens and LINE_REDUNDANT_MSK_EN is set as 1. e. when LINE_MISS happens and LINE_MISS_MSK_EN is set as 1.

16.1.14.138 0x089C CSIC DMA Channel3 Pixels Add Enable Register (Default Value: 0x0000_0000)

Offset: 0x089C			Register Name: CSIC_DMA_CH3_PIXELS_ADD_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	PIXELS_ADD_EN Decide whether dummy pixels will be added in the end of the line or not once pixels miss error happens. 0: Disable ADD 1: Enable ADD

16.1.14.139 0x08A0 CSIC DMA Channel3 Pixels Add Value Register (Default Value: 0x0000_0000)

Offset: 0x08A0			Register Name: CSIC_DMA_CH3_PIXELS_ADD_VAL_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x08A0			Register Name: CSIC_DMA_CH3_PIXELS_ADD_VAL_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PIXELS_ADD_VALUE Decide the value of dummy pixels when PIXELS_ADD_EN is set as 1.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

17 Audio

17.1 I2S/PCM

17.1.1 Overview

The I2S/PCM controller is designed to transfer streaming audio data between the system memory and the codec chip. The controller supports standard I2S format, Left-justified mode format, Right-justified mode format, PCM mode format, and TDM mode format.

The I2S/PCM controller includes the following features:

- 5x I2S/PCM (I2S0-4)
  - 4-lane I2S0 is used for digital amplifier.
  - 2-lane I2S1 is used for Bluetooth audio call.
  - 4-lane I2S2 is used for digital amplifier and supports ASRC.
  - 4-lane I2S3 is used for HDMI or eDP.
  - 2-lane I2S4 is used for Bluetooth audio call or multiplexed to eDP.
- Compliant with standard Philips Inter-IC sound (I2S) bus specification
  - Left-justified, Right-justified, PCM mode, and Time Division Multiplexing (TDM) format
  - Programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- FIFOs for transmitting and receiving data
  - Programmable FIFO thresholds
  - 128 depth x 32-bit width TXFIFO and 64 depth x 32-bit width RXFIFO
- Supports multiple function clocks
  - Clock up to 24.576 MHz Data Output of I2S/PCM in Master mode (Only if the IO PAD and Peripheral I2S/PCM satisfy Timing Parameters)
  - Clock up to 12.288 MHz Data Input of I2S/PCM in Master mode (Only if the IO PAD and Peripheral I2S/PCM satisfy Timing Parameters)
- Supports TX/RX DMA slave interface
- Supports multiple application scenarios
  - Up to 16 channels (fs = 48 kHz) which has adjustable width from 8-bit to 32-bit
  - Sample rate from 8 kHz to 384 kHz (sample rate*channels*slot width 24.567 MHz)
  - 8-bit u-law and 8-bit A-law companded sample

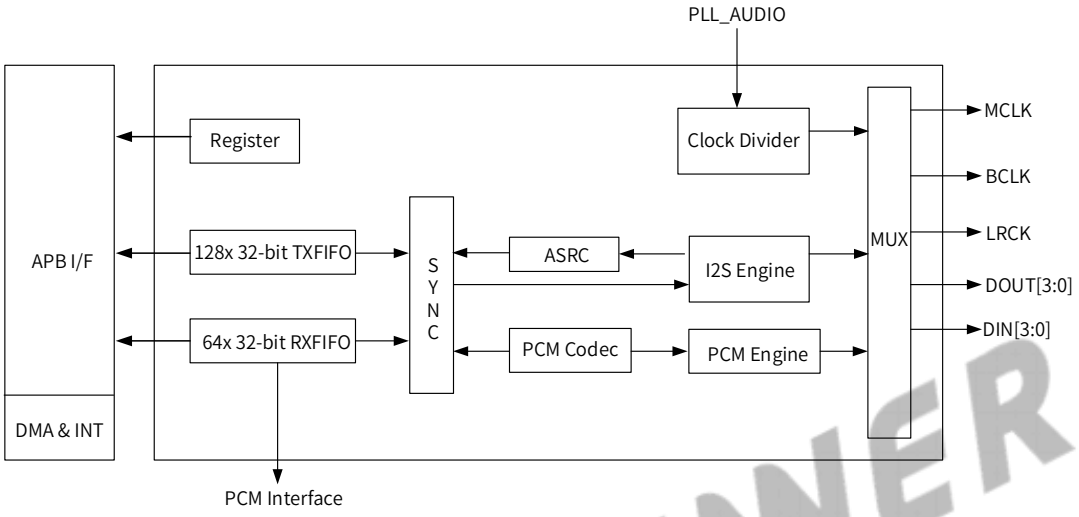
Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- Supports master/slave mode

17.1.2 Block Diagram

The following figure shows the functional block diagram of the I2S/PCM interface.

Figure 17-1 I2S/PCM Interface System Block Diagram



17.1.3 Clock Sources

The following table describes the clock sources of I2S/PCM. For clock setting, configurations, and gating information, refer to the section Clock Controller Unit (CCU).

Module	Clock Sources	Description
I2S/PCM 0/1/2/3/4	AUDIO0PLL4X	Its frequency is 24.5714*4 MHz by default.
	AUDIO1PLL_DIV2	Its frequency is 1536 MHz by default.
	AUDIO1PLL_DIV5	Its frequency is 614.4 MHz by default.
	PERI0_200M	Its frequency is 200 MHz by default.

17.1.4 External Signals

The following table describes the external signals of the I2S/PCM interface.

LRCK and BCLK are bidirectional I/O. When the I2S/PCM interface works in the Master mode, LRCK and BCLK are output pins. When the I2S/PCM interface works in the Slave mode, LRCK and BCLK are input pins.

MCLK is an output pin for external devices. DOUT is the serial data output pin, and DIN is the serial data input pin. For details about General Purpose I/O port, refer to the section GPIO.

Table 17-1 I2S/PCM External Signals

Signal Name	Description	Type
I2S0-MCLK	I2S0 Master Clock	O
I2S0-BCLK	I2S0/PCM0 Bit Rate Clock	I/O

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Signal Name	Description	Type
I2S0-LRCK	I2S0/PCM0 Sample Rate Clock/Sync	I/O
I2S0-DOUT[3:0]	I2S0/PCM0 Serial Data Output Channel [3:0]	O
I2S0-DIN[3:0]	I2S0/PCM0 Serial Data Input Channel [3:0]	I
I2S1-MCLK	I2S1 Master Clock	O
I2S1-BCLK	I2S1/PCM1 Bit Rate Clock	I/O
I2S1-LRCK	I2S1/PCM01Sample Rate Clock/Sync	I/O
I2S1-DOUT[1:0]	I2S1/PCM1 Serial Data Output Channel [1:0]	O
I2S1-DIN[1:0]	I2S1/PCM1 Serial Data Input Channel [1:0]	I
I2S2-MCLK	I2S2 Master Clock	O
I2S2-BCLK	I2S2/PCM2 Bit Rate Clock	I/O
I2S2-LRCK	I2S2/PCM2 Sample Rate Clock/Sync	I/O
I2S2-DOUT[3:0]	I2S2/PCM2 Serial Data Output Channel [3:0]	O
I2S2-DIN[3:0]	I2S2/PCM2 Serial Data Input Channel [3:0]	I
I2S3-MCLK<MUX-HDMI-EDP>	I2S3 Master Clock	O
I2S3-BCLK<MUX-HDMI-EDP>	I2S3/PCM3 Bit Rate Clock	I/O
I2S3-LRCK<MUX-HDMI-EDP>	I2S3/PCM3 Sample Rate Clock/Sync	I/O
I2S3-DIN[3:0]<MUX-HDMI-EDP>	I2S3/PCM3 Serial Data Output Channel [3:0]	O
I2S3-DOUT[3:0]<MUX-HDMI-EDP>	I2S3/PCM3 Serial Data Input Channel [3:0]	I
I2S4-MCLK<MUX-EDP>	I2S4 Master Clock	O
I2S4-BCLK<MUX-EDP>	I2S4/PCM4 Bit Rate Clock	I/O
I2S4-LRCK<MUX-EDP>	I2S4/PCM4 Sample Rate Clock/Sync	I/O
I2S4-DIN[1:0]<MUX-EDP>	I2S4/PCM4 Serial Data Output Channel [1:0]	O
I2S4-DOUT[1:0]<MUX-EDP>	I2S4/PCM4 Serial Data Input Channel [1:0]	I

17.1.5 Functional Description

17.1.5.1 I2S/PCM Transmit Modes

The I2S/PCM supports standard I2S mode, Left-justified I2S mode, Right-justified I2S mode, PCM mode, and TDM mode. The software can select the modes by setting I2S/PCM_CTL. The following figures describe the waveforms for SYNC, BCLK, DOUT, and DIN in different modes.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 17-2 I2S Standard Mode Timing

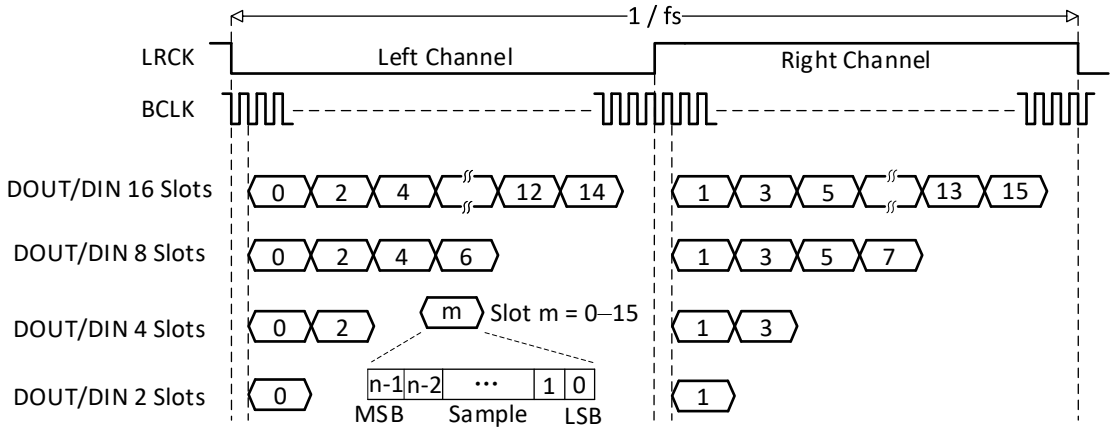


Figure 17-3 Left-Justified Mode Timing

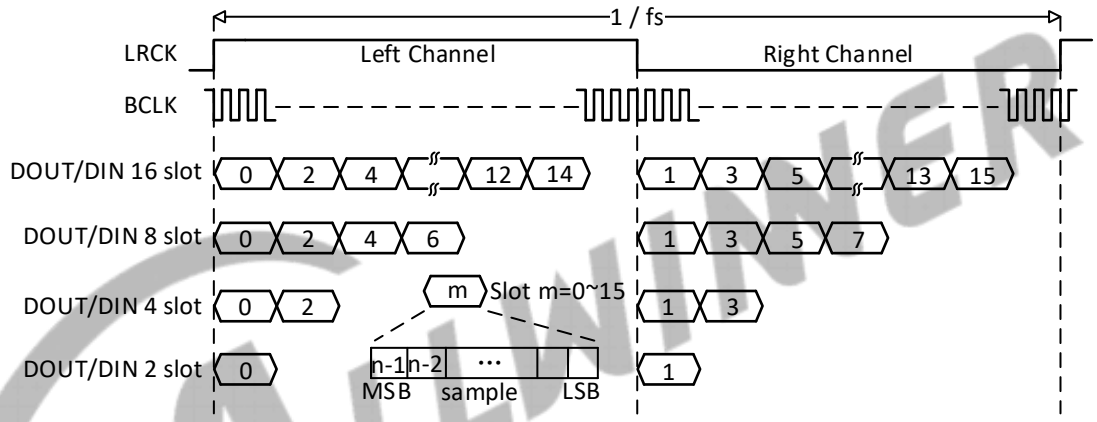
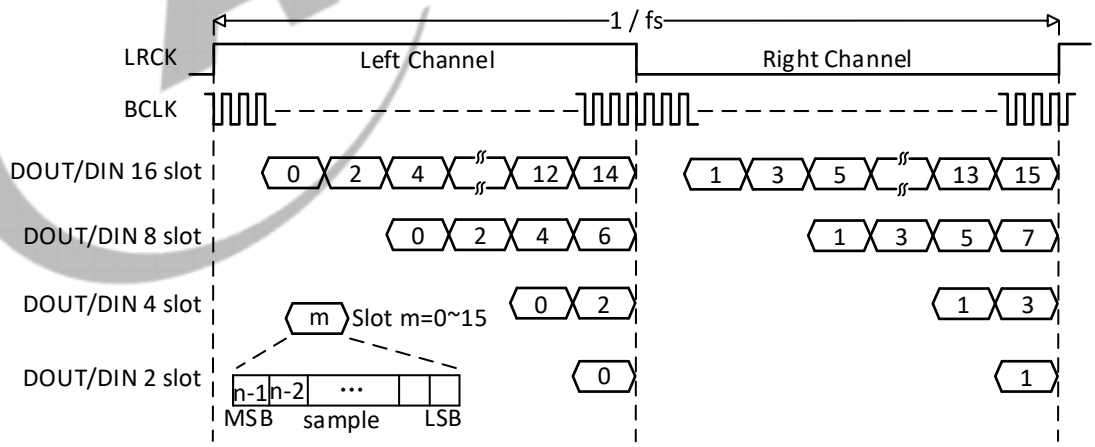


Figure 17-4 Right-Justified Mode Timing



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 17-5 PCM Long Frame Mode Timing

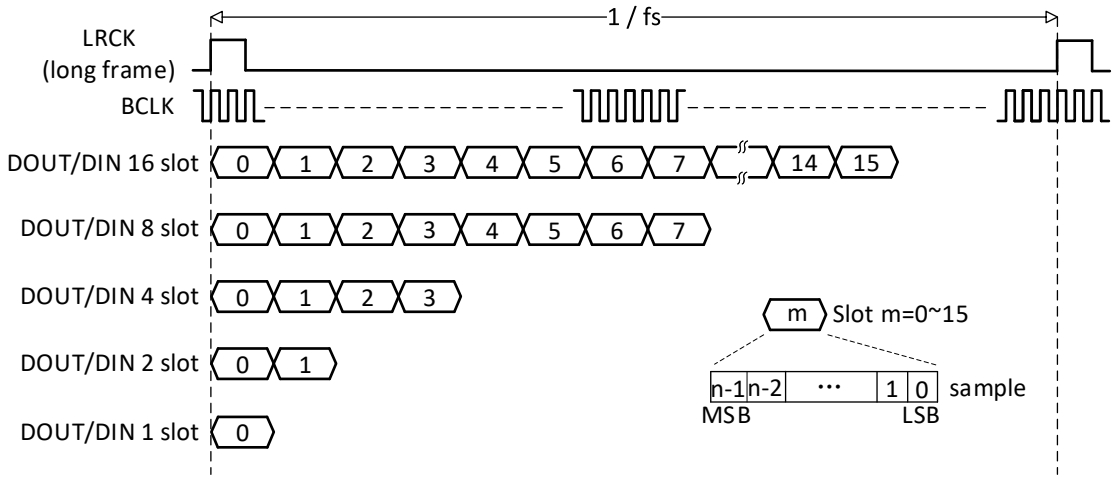
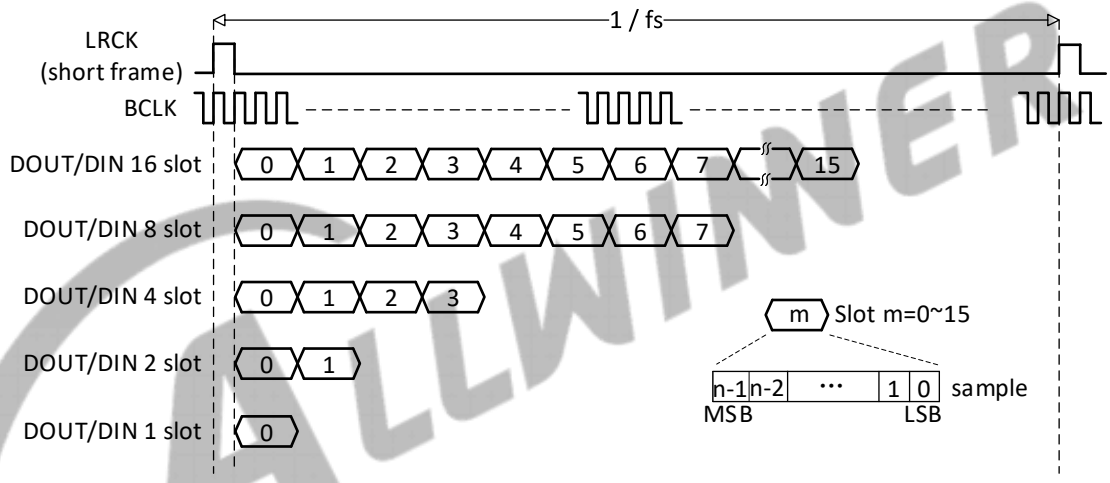


Figure 17-6 PCM Short Frame Mode Timing



17.1.5.2 Asynchronous Sample Rate Converter

The Asynchronous Sample Rate Converter (ASRC) module supports sampling rate conversion between the up-sampling and down-sampling. The ASRC also supports sampling rate conversion between dual-channel audio data, and the size of the sampling data is up to 24 bits.

The ASRC module has the following features:

- Typical THD + N: -130 dB (Range: -125 dB to -139 dB)
- Supports sampling rate conversion between the up-sampling and down-sampling to implement the sampling rate conversion for stereo data
  - The up-sampling ratio ranges from 1 to 7.5x
  - The down-sampling ratio ranges from 8 to 1x
- Supports sampling rate conversion between two identical frequencies
- Sampling rate for both the input and output range is from 8 kHz to 192 kHz and can be decimal

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- Sampling rate can be configured manually or via adaptive generation
- The ASRC input is connected to I2S RX_FIFO_WDATA [31:8], and the input data is 24-bit MSB big-endian. For the input data that is less than 24 bits, use zeros to pad out the values at the low bits instead of high bits
- The ASRC needs some time to calculate the result. The output outsample a/b will keep 0 during the calculation, and then change to the valid value when the result comes out

Calculating the ASRC Latency

Calculate the ASRC up-sampling and down-sampling latency according to the following formulas.

$$\text{Upsampling Latency} = \text{Phase Delay} + \text{FIFO Delay} = 32 + 16 = 48 \text{ Input Sample Periods}$$

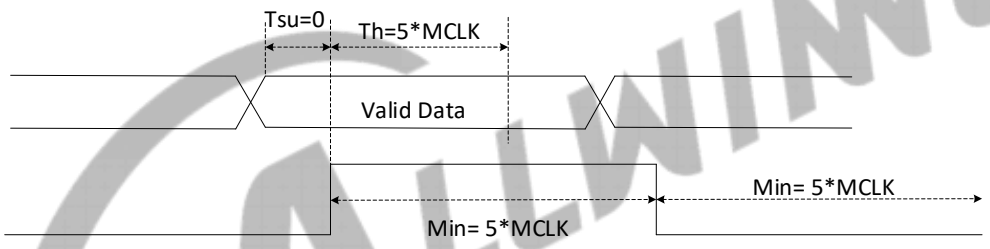
$$\text{Downsampling Latency} = \text{PhaseDelay} + \text{FIFODelay} = (32 * f_{sout}/f_{sin}) + 16 \text{ InputSample Periods}$$

ASRC Timing

The MCLK samples the input clock CLKIN to generate pulse signals.

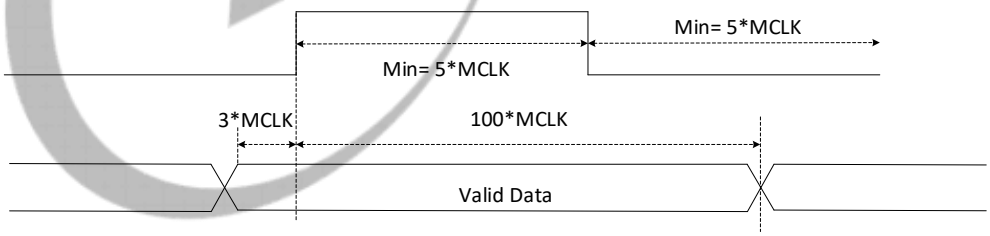
The following figure shows the timing requirements for the inputs.

Figure 17-7 Timing Requirements for Inputs



The following figure shows the timing requirements for the outputs.

Figure 17-8 Timing Requirements for Outputs



For the up-sampling, $F_{MCLK} = F_{sout} * 1350$

For the down-sampling, $F_{MCLK} = F_{sin} * 0.30 + F_{sout} * 295$

The following table provides the proper values of MCLK in MHz with different Fsin and Fsout in kHz.

Table 17-2 Proper MCLK Values with Different Fsin and Fsout

Fsin \ Fsout	32	44.1	48	88.2	96	144	192
32	45	60	65	120	130	195	260
44.1	55	60	65	120	130	195	260

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Fsin \ Fsout	32	44.1	48	88.2	96	144	192
48	60	65	65	120	130	195	260
88.2	105	105	110	120	130	195	260
96	110	115	115	125	130	195	260
144	160	165	165	175	180	195	260
192	210	215	215	225	230	245	260

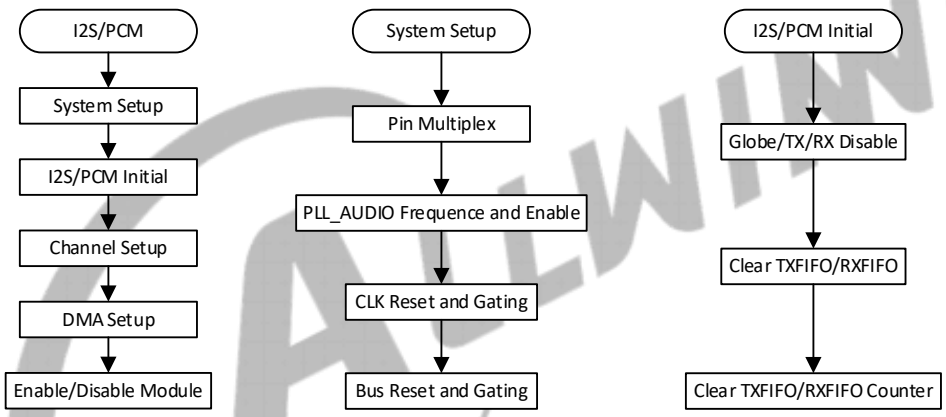
NOTE

The units for Fsin and Fsout are kHz and MCLK is MHz.

The software operation of the I2S/PCM is divided into five steps: system setup, I2S/PCM initialization, the channel setup, DMA setup, and Enable/Disable module.

The following figure shows the whole operation flow of I2S/PCM.

Figure 17-9 I2S/PCM Operation Flow



17.1.6 Programming Guidelines

17.1.6.1 System Setup and I2S/PCM Initialization

The first step in the system setup is properly programming the GPIO because the I2S/PCM port is a multiplex pin. For functions of the multiplex pins, refer to the section GPIO.

For the system setup, perform the following steps to set clock source.

Step 1 Disable the PLL_AUDIO through PLL_AUDIOx Control Register[PLL_ENABLE] in the CCU.

Step 2 Set up the frequency of the PLL_AUDIO in the PLL_AUDIOx Control Register.

Step 3 Enable the I2S/PCM gating through the I2S/PCMx_CLK_REG when you check out that the PLL_AUDIOx Control Register[LOCK] becomes to 1.

Step 4 Reset and enable the I2S/PCM bus gating by setting I2S_BGR_REG.

After the system setup, the register of I2S/PCM can be setup.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 5 Initialize the I2S/PCM. You should close the Globe Enable bit (I2S/PCM_CTL[0]), Transmitter Block Enable bit (I2S/PCM_CTL[2]), and Receiver Block Enable bit (I2S/PCM_CTL[1]) by writing 0.

Step 6 Clear the TX/RX FIFO by writing 0 to the bit[25:24] of I2S/PCM_FCTL.

Step 7 Clear the TX FIFO and RX FIFO counter by writing 0 to I2S/PCM_TXCNT and I2S/PCM_RXCNT.

17.1.6.2 Channel Setup and DMA Setup

Step 1 Set up the I2S/PCM of master and slave. The configuration can be referred to the protocol of I2S/PCM.

Step 2 Set up the translation mode, the sample resolution, the wide of the slot, the channel slot number, and the trigger level, and so on. The setup of the register can be found in the specification.

Step 3 The I2S/PCM supports two methods to transfer the data. The most common way is DMA, the setup of DMA can be found in the section DMA. In this module, you just enable the DRQ.

17.1.6.3 Enable and Disable I2S/PCM

Step 1 Enable TX/RX by writing I2S/PCM_CTL[TXEN]/I2S/PCM_CTL[RXEN].

Step 2 Enable I2S/PCM by writing 1 to I2S/PCM_CTL[Globe Enable].

Step 3 Write 0 to the Globe Enable bit to disable I2S/PCM.

17.1.6.4 Process ASRC Input and Output Data

The following example shows a typical application of ASRC: the input data is 24-bit valid, and the output data is a 32-bit data whose highest 24 bits are valid output and the lowest eight bits are padded out with zeros.

To implement the application, configure the sample resolution and slot width as 32 bits. Follow the steps below:

Step 1 For the input register: 0x04 [6:4] sample_res = 3`h7, 0x04 [2:0] slot_width = 3`h7. The format of the input data: 32 hXXXXXXXX, where, bit [31] is the MSB and X is the valid data bit.

Step 2 For the output register: 0x04 [6:4] sample_res = 3`h7, 0x04 [2:0] slot_width = 3`h7. The format of the output data: 32 hXXXXXX00, where, bit [31] is the MSB, X is the valid data bit, and bit [7:0] are the padded zeros.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

17.1.6.5 Convert the Sampling Rate with ASRC

Converting a 48 kHz sampling rate to 16 kHz is the most common scenario in actual applications. Follow the steps below to convert the sampling rate from 48 kHz to 16 kHz for the 32-bit data.

Step 1 Configure the PLL_AUDIO Register

a) Configure PLL_AUDIO_CTRL_REG[31:0] as 0x8814AB01. That is, PLL_AUDIO = 24*(171+1)/(1+1)/(1+0)/(1+20) = 98.286 MHz. According to the relationship among the Fsin, Fsout, and MCLK, the MCLK should be greater than 60 MHz. In the simulation phase, the SYS_CLK24M frequency is 24 MHz, so the output frequency of PLL_AUDIO should be 25*(171+1)/(1+1)/(1+0)/(1+20) = 102.381 MHz. In the IC test phase, configure the frequency of PLL_AUDIO according to its actual output frequency.

b) It is suggested that you configure the ASRC MCLK as an equal-duty-cycle signal. You can specify an odd number for bit[21:16] (PLL_POST_DIV_P) of PLL_AUDIO_CTRL_REG to get an equal-duty-cycle output clock of PLL_AUDIO.

c) Configure bit[25:24] of I2S3_ASRC_CLK_REG as 0x00 to select the PLL_AUDIO(4X).

Step 2 Configure the I2S Registers

a) Configure bit[7:4] (BCLKDIV) of I2S/PCM_CLKD as 4`h9, that is, the frequency of BCLK will be 98.286 MHz/32 = 3.072 MHz.

b) Configure bit[17:8] (LRCK_PERIOD) of I2S/PCM_FMT0 as 10`h1F. That is, the LRCK_PERIOD width is configured as 32 BLCKs and can generate the ASRC CLKIN with a 48 kHz sampling rate. ($\frac{3.072\text{MHz}}{32*2}=48\text{kHz}$)

c) Configure bit[6:4] (Sample Resolution bits) of I2S/PCM_FMT0 as 3`h7 to specify the sample resolution as 32-bit.

d) Configure bit[2:0] (Slot Width bits) of I2S/PCM_FMT0 as 3`h7 to specify the slot width as 32-bit.

Step 3 Configure the ASRC Registers

a) Configure bit[16] (clock gate) of MCLKCFG as 1`h1 to open the clock gating.

b) Configure bit[3:0] (division factor) of MCLKCFG as 1`h1 to specify the division factor as 1.

c) Configure bit[20] (clock gate) of FsoutCFG as 1`h1 to open the clock gating.

d) Configure bit[19:16] (clock select) of FsoutCFG as 4`h0 to select I2S0_ASRC_CLK as the clock source.

e) Configure bit[7:4] (the first division factor) of FsoutCFG as 16`h13 to configure the first division factor as 128.

f) Configure bit[3:0] (the second division factor) of FsoutCFG as 16`h10 to configure the second division factor as 48.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

g) Configure the ASRC ratio.

To configure the ASRC ratio manually, configure bit[31] (Manual Configuration of ASRC Ratio Enable) of ASRCMANCFG as 1`h1 to enable the manual configuration of ASRC ratio. Configure bit[25:0] of ASRCMANCFG as 26`h155555 to specify the ratio value as 0x155555. The calculation formula for the ratio value: Dec2Hex (Fsout/Fsin) *222). In this example, Fsout/Fsin = 16 kHz/48 kHz =1/3, then the ratio is 0x155555.

To configure the ASRC ratio automatically, configure bit[31] (Manual Configuration of ASRC Ratio Enable) of ASRCMANCFG as 1`h0 to enable the automatic configuration of ASRC ratio. Then the system will automatically calculate the ratio value based on the MCLK, Fsout, and Fsin.

17.1.7 Register List

Module Name	Base Address
I2S/PCM0	0x02532000
I2S/PCM1	0x02533000
I2S/PCM2	0x02534000
I2S/PCM3	0x02535000
I2S/PCM4	0x02536000

Register Name	Offset	Description
I2S/PCM_CTL	0x0000	I2S/PCM Control Register
I2S/PCM_FMT0	0x0004	I2S/PCM Format Register 0
I2S/PCM_FMT1	0x0008	I2S/PCM Format Register 1
I2S/PCM_ISTA	0x000C	I2S/PCM Interrupt Status Register
I2S/PCM_RXFIFO	0x0010	I2S/PCM RXFIFO Register
I2S/PCM_FCTL	0x0014	I2S/PCM FIFO Control Register
I2S/PCM_FSTA	0x0018	I2S/PCM FIFO Status Register
I2S/PCM_INT	0x001C	I2S/PCM DMA and Interrupt Control Register
I2S/PCM_TXFIFO	0x0020	I2S/PCM TXFIFO Register
I2S/PCM_CLKD	0x0024	I2S/PCM Clock Divide Register
I2S/PCM_TXCNT	0x0028	I2S/PCM TX Sample Counter Register
I2S/PCM_RXCNT	0x002C	I2S/PCM RX Sample Counter Register
I2S/PCM_CHCFG	0x0030	I2S/PCM Channel Configuration Register
I2S/PCM_TX0CHSEL	0x0034	I2S/PCM TX0 Channel Select Register
I2S/PCM_TX1CHSEL	0x0038	I2S/PCM TX1 Channel Select Register
I2S/PCM_TX2CHSEL	0x003C	I2S/PCM TX2 Channel Select Register
I2S/PCM_TX3CHSEL	0x0040	I2S/PCM TX3 Channel Select Register
I2S/PCM_TX0CHMAP0	0x0044	I2S/PCM TX0 Channel Mapping Register0
I2S/PCM_TX0CHMAP1	0x0048	I2S/PCM TX0 Channel Mapping Register1
I2S/PCM_TX1CHMAP0	0x004C	I2S/PCM TX1 Channel Mapping Register0
I2S/PCM_TX1CHMAP1	0x0050	I2S/PCM TX1 Channel Mapping Register1

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
I2S/PCM_TX2CHMAP0	0x0054	I2S/PCM TX2 Channel Mapping Register0
I2S/PCM_TX2CHMAP1	0x0058	I2S/PCM TX2 Channel Mapping Register1
I2S/PCM_TX3CHMAP0	0x005C	I2S/PCM TX3 Channel Mapping Register0
I2S/PCM_TX3CHMAP1	0x0060	I2S/PCM TX3 Channel Mapping Register1
I2S/PCM_RXCHSEL	0x0064	I2S/PCM RX Channel Select Register
I2S/PCM_RXCHMAP0	0x0068	I2S/PCM RX Channel Mapping Register0
I2S/PCM_RXCHMAP1	0x006C	I2S/PCM RX Channel Mapping Register1
I2S/PCM_RXCHMAP2	0x0070	I2S/PCM RX Channel Mapping Register2
I2S/PCM_RXCHMAP3	0x0074	I2S/PCM RX Channel Mapping Register3
MCLKCFG	0x0080	I2S/PCM ASRC MCLK Configure Register
FsoutCFG	0x0084	I2S/PCM ASRC Out Sample Configure Register
FsinEXTCFG	0x0088	I2S/PCM In Sample Pluse Extend Configure Register
ASRCEN	0x008C	I2S/PCM ASRC Enable Configure Register
ASRCMANCFG	0x0090	I2S/PCM ASRC Manual Configure Register
ASRCRATIOSTAT	0x0094	I2S/PCM ASRC Ratio State Configure Register
ASRCFIFOSTAT	0x0098	I2S/PCM ASRC FIFO State Configure Register
ASRCMBISTCFG	0x009C	I2S/PCM ASRC MBIST Test Configure Register
ASRCMBISTSTA	0x00A0	I2S/PCM ASRC MBIST Test State Configure Register

17.1.8 Register Description

17.1.8.1 0x0000 I2S/PCM Control Register (Default Value: 0x0006_0000)

Offset: 0x0000			Register Name: I2S/PCM_CTL
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21	R/W	0x0	RX_SYNC_EN_START Only if RX_SYNC_EN is set 1, RX_SYNC_EN_START can take effect. I2S0/I2S1/I2S2/I2S3/I2S4/DMIC/OWA RX Synchronize Enable Start. 0: Disable 1: Enable
20	R/W	0x0	RX_SYNC_EN I2S RX Synchronize Enable 0: Disable 1: Enable
19	/	/	/
18	R/W	0x1	BCLK_OUT Bit Clock Direction Select 0: Input 1: Output

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: I2S/PCM_CTL
Bit	Read/Write	Default/Hex	Description
17	R/W	0x1	LRCK_OUT LR Clock Direction Select 0: Input 1: Output
16:12	/	/	/
11	R/W	0x0	DOUT3_EN Data3 Output Enable 0: Disable, Hi-Z State 1: Enable
10	R/W	0x0	DOUT2_EN Data2 Output Enable 0: Disable, Hi-Z State 1: Enable
9	R/W	0x0	DOUT1_EN Data1 Output Enable 0: Disable, Hi-Z State 1: Enable
8	R/W	0x0	DOUT0_EN Data0 Output Enable 0: Disable, Hi-Z State 1: Enable
7	/	/	/
6	R/W	0x0	DOUT_MUTE_EN Data Output Mute Enable 0: Normal Transfer 1: Force DOUT to Output 0
5:4	R/W	0x0	MODE_SEL Mode Selection 00: PCM Mode offset 0: Long Frame offset 1: Short Frame 01: Left Mode offset 0: LJ Mode offset 1: I2S Mode 10: Right-Justified Mode 11: Reserved
3	R/W	0x0	LOOP Loop Back Test 0: Normal Mode 1: Loop Back Test When Set 1 , Connecting the DOUT with the DIN.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: I2S/PCM_CTL
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	TXEN Transmitter Block Enable 0: Disable 1: Enable
1	R/W	0x0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0x0	GEN Globe Enable A disable on this bit overrides any other block or channel enables. 0: Disable 1: Enable

17.1.8.2 0x0004 I2S/PCM Format Register 0 (Default Value: 0x0000_0033)

Offset: 0x0004			Register Name: I2S/PCM_FMT0
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R/W	0x0	LRCK_WIDTH (Only Apply in PCM Mode) LRCK Width 0: LRCK = 1 BCLK Width (Short Frame) 1: LRCK = 2 BCLK Width (Long Frame)
29:20	/	/	/
19	R/W	0x0	LRCK_POLARITY When Apply in I2S/Left-Justified/Right-Justified Mode: 0: Left Channel When LRCK is Low 1: Left Channel When LRCK is High When Apply in PCM Mode: 0: PCM LRCK Asserted at the Negative Edge 1: PCM LRCK Asserted at the Positive Edge
18	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: I2S/PCM_FMT0
Bit	Read/Write	Default/Hex	Description
17:8	R/W	0x0	LRCK_PERIOD It is used to program the number of BCLKs per channel of sample frame. This value is interpreted as follow: PCM Mode: Number of BCLKs within (Left + Right) channel width. I2S/Left-Justified/Right-Justified Mode: Number of BCLKs within each individual channel width (Left or Right). N+1 For example: N = 7: 8 BCLKs width (p) N = 1023: 1024 BCLKs width
7	R/W	0x0	BCLK_POLARITY BCLK Polarity Select 0: Normal Mode. DOUT Drive Data at Negative Edge 1: Invert Mode. DOUT Drive Data at Positive Edge
6:4	R/W	0x3	SR Sample Resolution 000: Reserved 001: 8-bit 010: 12-bit 011: 16-bit 100: 20-bit 101: 24-bit 110: 28-bit 111: 32-bit
3	R/W	0x0	EDGE_TRANSFER Edge Transfer 0: DOUT Drive Data and DIN Sample Data at the Different BCLK Edge 1: DOUT Drive Data and DIN Sample Data at the Same BCLK Edge BCLK_POLARITY = 0, EDGE_TRANSFER = 0, DIN Sample Data at Positive Edge; BCLK_POLARITY = 0, EDGE_TRANSFER = 1, DIN Sample Data at Negative Edge; BCLK_POLARITY = 1, EDGE_TRANSFER = 0, DIN Sample Data at Negative Edge; BCLK_POLARITY = 1, EDGE_TRANSFER = 1, DIN Sample Data at Positive Edge.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: I2S/PCM_FMT0
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x3	SW Slot Width Select 000: Reserved 001: 8-bit 010: 12-bit 011: 16-bit 100: 20-bit 101: 24-bit 110: 28-bit 111: 32-bit

17.1.8.3 0x0008 I2S/PCM Format Register 1 (Default Value: 0x0000_0030)

Offset: 0x0008			Register Name: I2S/PCM_FMT1
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	RX_MLS MSB / LSB First Select 0: MSB First 1: LSB First
6	R/W	0x0	TX_MLS MSB / LSB First Select 0: MSB First 1: LSB First
5:4	R/W	0x3	SEXT Sign Extend in Slot [Sample Resolution < Slot Width] 00: Zeros or Audio Gain Padding at LSB Position 01: Sign Extension at MSB Position 10: Reserved 11: Transfer 0 after each Sample in each Slot
3:2	R/W	0x0	RX_PDM PCM Data Mode 00: Linear PCM 01: Reserved 10: 8-bits U-law 11: 8-bits A-law

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: I2S/PCM_FMT1
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x0	TX_PDM PCM Data Mode 00: Linear PCM 01: Reserved 10: 8-bits U-law 11: 8-bits A-law

17.1.8.4 0x000C I2S/PCM Interrupt Status Register (Default Value: 0x0000_0010)

Offset: 0x000C			Register Name: I2S/PCM_ISTA
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W1C	0x0	TXU_INT TXFIFO Underrun Pending Interrupt 0: No Pending Interrupt 1: TXFIFO Underrun Pending Interrupt Write 1 to clear this interrupt.
5	R/W1C	0x0	TXO_INT TXFIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: TXFIFO Overrun Pending Interrupt Write 1 to clear this interrupt.
4	R	0x1	TXE_INT TXFIFO Empty Pending Interrupt 0: No Pending IRQ 1: TXFIFO Empty Pending Interrupt When Data in TXFIFO are Less than TX Trigger Level
3	/	/	/
2	R/W1C	0x0	RXU_INT RXFIFO Underrun Pending Interrupt 0: No Pending Interrupt 1: RXFIFO Underrun Pending Interrupt Write 1 to clear this interrupt.
1	R/W1C	0x0	RXO_INT RXFIFO Overrun Pending Interrupt 0: No Pending IRQ 1: RXFIFO Overrun Pending IRQ Write 1 to clear this interrupt.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x000C			Register Name: I2S/PCM_ISTA
Bit	Read/Write	Default/Hex	Description
0	R	0x0	RXA_INT RXFIFO Data Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ When Data in RXFIFO are More than RX Trigger Level

17.1.8.5 0x0010 I2S/PCM RXFIFO Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: I2S/PCM_RXFIFO
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RX_DATA RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

17.1.8.6 0x0014 I2S/PCM FIFO Control Register (Default Value: 0x0004_00F0)

Offset: 0x0014			Register Name: I2S/PCM_FCTL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HUB_EN Audio Hub Enable Only if TXEN set 1, HUB_EN can take effect. I2S0/I2S1/I2S2/I2S3/I2S4/OWA TXFIFO Hub Enable. 0: Disable 1: Enable
30:26	/	/	/
25	R/WAC	0x0	FTX Flush TX FIFO Write 1 to flush TXFIFO, self-clear to 0 .
24	R/WAC	0x0	FRX Flush RX FIFO Write 1 to flush RXFIFO, self-clear to 0 .
23:19	/	/	/
18:12	R/W	0x40	TXTL TXFIFO Empty Trigger Level Interrupt and DMA request trigger level for TXFIFO normal condition. Trigger Level = TXTL
11:10	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: I2S/PCM_FCTL
Bit	Read/Write	Default/Hex	Description
9:4	R/W	0xF	RXTL RXFIFO Trigger Level Interrupt and DMA request trigger level for RXFIFO normal condition. Trigger Level = RXTL + 1
3	/	/	/
2	R/W	0x0	TXIM TXFIFO Input Mode (Mode 0, 1) 0: Valid Data at the MSB of TXFIFO Register 1: Valid Data at the LSB of TXFIFO Register Example for 20-bits Transmitted Audio Sample: Mode 0: TXFIFO [31:0] = {APB_WDATA [31:12], 12 h0} Mode 1: TXFIFO[31:0] = {APB_WDATA[19:0], 12 h0}
1:0	R/W	0x0	RXOM RXFIFO Output Mode (Mode 0, 1, 2, 3) 00: Expanding 0 at LSB of RXFIFO Register 01: Expanding Received Sample Sign Bit at MSB of RXFIFO Register 10: Truncating Received Samples at High Half-word of RXFIFO Register and Low Half-word of RXFIFO Register is Filled by 0 11: Truncating Received Samples at Low Half-word of RXFIFO Register and High Half-word of RXFIFO Register is Expanded by Its Sign Bit Example for 20-bits Received Audio Sample: Mode 0: APB_RDATA [31:0] = {RXFIFO [31:12], 12 h0} Mode 1: APB_RDATA [31:0] = {12{RXFIFO [31]}, RXFIFO [31:12]} Mode 2: APB_RDATA [31:0] = {RXFIFO [31:16], 16 h0} Mode 3: APB_RDATA[31:0] = {16{RXFIFO[31], RXFIFO[31:16]}}

17.1.8.7 0x0018 I2S/PCM FIFO Status Register (Default Value: 0x1080_0080)

Offset: 0x0018			Register Name: I2S/PCM_FSTA
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0018			Register Name: I2S/PCM_FSTA
Bit	Read/Write	Default/Hex	Description
28	R	0x1	TXE TXFIFO Empty 0: No Room for New Sample in TXFIFO 1: More than One Room for New Sample in TXFIFO (>= 1 Word)
27:24	/	/	/
23:16	R	0x80	TXE_CNT TXFIFO Empty Space Word Counter
15:9	/	/	/
8	R	0x0	RXA RXFIFO Available 0: No Available Data in RXFIFO 1: More than One Sample in RXFIFO (>= 1 Word)
7	R	0x1	PLACE_HOLDER NO Meaning
6:0	R	0x0	RXA_CNT RXFIFO Available Sample Word Counter

17.1.8.8 0x001C I2S/PCM DMA and Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: I2S/PCM_INT
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TX_DRQ TXFIFO Empty DRQ Enable 0: Disable 1: Enable
6	R/W	0x0	TXUI_EN TXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TXOI_EN TXFIFO Overrun Interrupt Enable 0: Disable 1: Enable When set to 1 , an interrupt happens when writing new audio data if TXFIFO is full.
4	R/W	0x0	TXEI_EN TXFIFO Empty Interrupt Enable 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x001C			Register Name: I2S/PCM_INT
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	RX_DRQ RXFIFO Data Available DRQ Enable 0: Disable 1: Enable When set to 1 , RXFIFO DMA request line is asserted if data is available in RXFIFO.
2	R/W	0x0	RXUI_EN RXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RXOI_EN RXFIFO Overrun Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RXAI_EN RXFIFO Data Available Interrupt Enable 0: Disable 1: Enable

17.1.8.9 0x0020 I2S/PCM TXFIFO Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: I2S/PCM_TXFIFO
Bit	Read/Write	Default/Hex	Description
31:0	W	0x0	TX_DATA TX Sample Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

17.1.8.10 0x0024 I2S/PCM Clock Divide Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: I2S/PCM_CLKD
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	MCLKO_EN MCLK Out Enable 0: Disable MCLK Output 1: Enable MCLK Output Notes: Whether in Slave or Master mode, when this bit is set to 1 , MCLK should be output.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0024			Register Name: I2S/PCM_CLKD
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0x0	BCLKDIV BCLK Divide Ratio from PLL_AUDIO 0000: Reserved 0001: Divide by 1 0010: Divide by 2 0011: Divide by 4 0100: Divide by 6 0101: Divide by 8 0110: Divide by 12 0111: Divide by 16 1000: Divide by 24 1001: Divide by 32 1010: Divide by 48 1011: Divide by 64 1100: Divide by 96 1101: Divide by 128 1110: Divide by 176 1111: Divide by 192
3:0	R/W	0x0	MCLKDIV MCLK Divide Ratio from PLL_AUDIO 0000: Reserved 0001: Divide by 1 0010: Divide by 2 0011: Divide by 4 0100: Divide by 6 0101: Divide by 8 0110: Divide by 12 0111: Divide by 16 1000: Divide by 24 1001: Divide by 32 1010: Divide by 48 1011: Divide by 64 1100: Divide by 96 1101: Divide by 128 1110: Divide by 176 1111: Divide by 192

17.1.8.11 0x0028 I2S/PCM TX Sample Counter Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: I2S/PCM_TXCNT
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0028			Register Name: I2S/PCM_TXCNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial value at any time. After being updated by the initial value, the counter register should count on base of this initial value.

17.1.8.12 0x002C I2S/PCM RX Sample Counter Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: I2S/PCM_RXCNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this initial value.

17.1.8.13 0x0030 I2S/PCM Channel Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: I2S/PCM_CHCFG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9	R/W	0x0	TX_SLOT_HIZ TX Slot Value in Half Cycle of BCLK 0: Normal Mode for the Last Half Cycle of BCLK in the Slot 1: Turn to Hi-Z State for the Last Half Cycle of BCLK in the Slot
8	R/W	0x0	TX_STATE The state of transmission line When there is No Transmission 0: Transfer Level 0 When not Transferring Slot 1: Turn to Hi-Z State (TDM) When not Transferring Slot

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0030			Register Name: I2S/PCM_CHCFG
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0x0	RX_SLOT_NUM RX Channel/Slot Number between CPU/DMA and RXFIFO 0: 1 Channel or Slot ... 7: 8 Channels or Slots 8: 9 Channels or Slots ... 15:16 Channels or Slots
3:0	R/W	0x0	TX_SLOT_NUM TX Channel/Slot Number Which between CPU/DMA and TXFIFO 0: 1 Channel or Slot ... 7: 8 Channels or Slots 8: 9 Channels or Slots ... 15:16 Channels or Slots

17.1.8.14 0x0034 I2S/PCM TX0 Channel Select Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: I2S/PCM_TX0CHSEL
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:20	R/W	0x0	TX0_OFFSET TX0 offset Tune, TX0 Data offset to LRCK 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	TX0_CHSEL TX0 Channel (Slot) Number Select for each Output 0:1 Channel / Slot (p) 7:8 Channels / Slots 8:9 Channels / Slots ... 15:16 Channels / Slots

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0034			Register Name: I2S/PCM_TX0CHSEL
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x0	TX0_CHEN TX0 Channel (Slot) Enable, bit [15:0] Refer to Slot [15:0]. When One or More Slot(s) is disabled, the Affected Slot(s) is set to disable State. 0: Disable 1: Enable

17.1.8.15 0x0038 I2S/PCM TX1 Channel Select Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: I2S/PCM_TX1CHSEL
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:20	R/W	0x0	TX1_OFFSET TX1 offset Tune, TX1 Data offset to LRCK 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	TX1_CHSEL TX1 Channel (Slot) Number Select for each Output 0: 1 Channel/Slot (p) 7: 8 Channels/Slots 8: 9 Channels/Slots ... 15: 16 Channels/Slots
15:0	R/W	0x0	TX1_CHEN TX1 Channel (Slot) Enable, bit [15:0] Refer to Slot [15:0]. When One or More Slot(s) is disabled, the Affected Slot(s) is set to Disable State. 0: Disable 1: Enable

17.1.8.16 0x003C I2S/PCM TX2 Channel Select Register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: I2S/PCM_TX2CHSEL
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:20	R/W	0x0	TX2_OFFSET TX2 offset Tune, TX2 Data offset to LRCK 0: No offset n: Data is offset by n BCLKs to LRCK

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x003C			Register Name: I2S/PCM_TX2CHSEL
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0x0	TX2_CHSEL TX2 Channel (Slot) Number Select for each Output 0: 1 Channel/Slot (p) 7: 8 Channels/Slots 8: 9 Channels/Slots ... 15: 16 Channels/Slots
15:0	R/W	0x0	TX2_CHEN TX2 Channel (Slot) Enable, bit [15:0] Refer to Slot [15:0]. When One or More Slot(s) is(are) Disabled, the Affected Slot(s) is(are) Set to Disable State. 0: Disable 1: Enable

17.1.8.17 0x0040 I2S/PCM TX3 Channel Select Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: I2S/PCM_TX3CHSEL
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:20	R/W	0x0	TX3_OFFSET TX3 offset Tune, TX Data offset to LRCK 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	TX3_CHSEL TX3 Channel (Slot) Number Select for each Output 0:1 Channel / Slot (p) 7:8 Channels / Slots 8:9 Channels / Slots ... 15:16 Channels / Slots
15:0	R/W	0x0	TX3_CHEN TX3 Channel (Slot) Enable, bit [15:0] Refer to Slot [15:0]. When One or More Slot(s) is disabled, the Affected Slot(s) is set to Disable State. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

17.1.8.18 0x0044 I2S/PCM TX0 Channel Mapping Register0 (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: I2S/PCM_TX0CHMAP0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TX0_CH15_MAP TX0 Channel 15 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
27:24	R/W	0x0	TX0_CH14_MAP TX0 Channel 14 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th sample
23:20	R/W	0x0	TX0_CH13_MAP TX0 Channel 13 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
19:16	R/W	0x0	TX0_CH12_MAP TX0 Channel 12 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:12	R/W	0x0	TX0_CH11_MAP TX0 Channel 11 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th sample

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0044			Register Name: I2S/PCM_TX0CHMAP0
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0x0	TX0_CH10_MAP TX0 Channel 10 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:4	R/W	0x0	TX0_CH9_MAP TX0 Channel 9 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
3:0	R/W	0x0	TX0_CH8_MAP TX0 Channel 8 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

17.1.8.19 0x0048 I2S/PCM TX0 Channel Mapping Register1 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: I2S/PCM_TX0CHMAP1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TX0_CH7_MAP TX0 Channel 7 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0048			Register Name: I2S/PCM_TX0CHMAP1
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0x0	TX0_CH6_MAP TX0 Channel 6 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
23:20	R/W	0x0	TX0_CH5_MAP TX0 Channel 5 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
19:16	R/W	0x0	TX0_CH4_MAP TX0 Channel 4 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:12	R/W	0x0	TX0_CH3_MAP TX0 Channel 3 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
11:8	R/W	0x0	TX0_CH2_MAP TX0 Channel 2 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0048			Register Name: I2S/PCM_TX0CHMAP1
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0x0	TX0_CH1_MAP TX0 Channel 1 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
3:0	R/W	0x0	TX0_CH0_MAP TX0 Channel 0 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

17.1.8.20 0x004C I2S/PCM TX1 Channel Mapping Register0 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: I2S/PCM_TX1CHMAP0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TX1_CH15_MAP TX1 Channel 15 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
27:24	R/W	0x0	TX1_CH14_MAP TX1 Channel 14 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th sample

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x004C			Register Name: I2S/PCM_TX1CHMAP0
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0x0	TX1_CH13_MAP TX1 Channel 13 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
19:16	R/W	0x0	TX1_CH12_MAP TX1 Channel 12 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:12	R/W	0x0	TX1_CH11_MAP TX1 Channel 11 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th sample
11:8	R/W	0x0	TX1_CH10_MAP TX1 Channel 10 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:4	R/W	0x0	TX1_CH9_MAP TX1 Channel 9 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x004C			Register Name: I2S/PCM_TX1CHMAP0
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	TX1_CH8_MAP TX1 Channel 8 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

17.1.8.21 0x0050 I2S/PCM TX1 Channel Mapping Register1 (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: I2S/PCM_TX1CHMAP1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TX1_CH7_MAP TX1 Channel 7 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
27:24	R/W	0x0	TX1_CH6_MAP TX1 Channel 6 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
23:20	R/W	0x0	TX1_CH5_MAP TX1 Channel 5 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0050			Register Name: I2S/PCM_TX1CHMAP1
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0x0	TX1_CH4_MAP TX1 Channel 4 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:12	R/W	0x0	TX1_CH3_MAP TX1 Channel 3 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
11:8	R/W	0x0	TX1_CH2_MAP TX1 Channel 2 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:4	R/W	0x0	TX1_CH1_MAP TX1 Channel 1 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
3:0	R/W	0x0	TX1_CH0_MAP TX1 Channel 0 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

17.1.8.22 0x0054 I2S/PCM TX2 Channel Mapping Register0 (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: I2S/PCM_TX2CHMAP0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TX2_CH15_MAP TX2 Channel 15 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
27:24	R/W	0x0	TX2_CH14_MAP TX2 Channel 14 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th sample
23:20	R/W	0x0	TX2_CH13_MAP TX2 Channel 13 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
19:16	R/W	0x0	TX2_CH12_MAP TX2 Channel 12 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:12	R/W	0x0	TX2_CH11_MAP TX2 Channel 11 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th sample

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0054			Register Name: I2S/PCM_TX2CHMAP0
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0x0	TX2_CH10_MAP TX2 Channel 10 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:4	R/W	0x0	TX2_CH9_MAP TX2 Channel 9 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
3:0	R/W	0x0	TX2_CH8_MAP TX2 Channel 8 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

17.1.8.23 0x0058 I2S/PCM TX2 Channel Mapping Register1 (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: I2S/PCM_TX2CHMAP1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TX2_CH7_MAP TX2 Channel 7 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0058			Register Name: I2S/PCM_TX2CHMAP1
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0x0	TX2_CH6_MAP TX2 Channel 6 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
23:20	R/W	0x0	TX2_CH5_MAP TX2 Channel 5 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
19:16	R/W	0x0	TX2_CH4_MAP TX2 Channel 4 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:12	R/W	0x0	TX2_CH3_MAP TX2 Channel 3 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
11:8	R/W	0x0	TX2_CH2_MAP TX2 Channel 2 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0058			Register Name: I2S/PCM_TX2CHMAP1
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0x0	TX2_CH1_MAP TX2 Channel 1 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
3:0	R/W	0x0	TX2_CH0_MAP TX2 Channel 0 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

17.1.8.24 0x005C I2S/PCM TX3 Channel Mapping Register0 (Default Value: 0x0000_0000)

Offset: 0x005C			Register Name: I2S/PCM_TX3CHMAP0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TX3_CH15_MAP TX3 Channel 15 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
27:24	R/W	0x0	TX3_CH14_MAP TX3 Channel 14 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th sample

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x005C			Register Name: I2S/PCM_TX3CHMAP0
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0x0	TX3_CH13_MAP TX3 Channel 13 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
19:16	R/W	0x0	TX3_CH12_MAP TX3 Channel 12 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:12	R/W	0x0	TX3_CH11_MAP TX3 Channel 11 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th sample
11:8	R/W	0x0	TX3_CH10_MAP TX3 Channel 10 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:4	R/W	0x0	TX3_CH9_MAP TX3 Channel 9 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x005C			Register Name: I2S/PCM_TX3CHMAP0
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	TX3_CH8_MAP TX3 Channel 8 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

17.1.8.25 0x0060 I2S/PCM TX3 Channel Mapping Register1 (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: I2S/PCM_TX3CHMAP1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TX3_CH7_MAP TX3 Channel 7 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
27:24	R/W	0x0	TX3_CH6_MAP TX3 Channel 6 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
23:20	R/W	0x0	TX3_CH5_MAP TX3 Channel 5 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0060			Register Name: I2S/PCM_TX3CHMAP1
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0x0	TX3_CH4_MAP TX3 Channel 4 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:12	R/W	0x0	TX3_CH3_MAP TX3 Channel 3 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
11:8	R/W	0x0	TX3_CH2_MAP TX3 Channel 2 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:4	R/W	0x0	TX3_CH1_MAP TX3 Channel 1 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
3:0	R/W	0x0	TX3_CH0_MAP TX3 Channel 0 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

17.1.8.26 0x0064 I2S/PCM RX Channel Select Register (Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: I2S/PCM_RXCHSEL
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:20	R/W	0x0	RX_OFFSET RX offset Tune, RX Data offset to LRCK 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	RX_CHSEL RX Channel (Slot) Number Select for Input 0: 1 Channel / Slot (p) 7: 8 Channels / Slots 8: 9 Channels / Slots ... 15: 16 Channels / Slots
15:0	/	/	/

17.1.8.27 0x0068 I2S/PCM RX Channel Mapping Register0 (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: I2S/PCM_RXCHMAP0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	RX_CH15_SELECT Rx channel 15 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
27:24	R/W	0x0	RX_CH15_MAP RX Channel 15 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
23:22	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0068			Register Name: I2S/PCM_RXCHMAP0
Bit	Read/Write	Default/Hex	Description
21:20	R/W	0x0	RX_CH14_SELECT Rx channel 14 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
19:16	R/W	0x0	RX_CH14_MAP RX Channel 14 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:14	/	/	/
13:12	R/W	0x0	RX_CH13_SELECT Rx channel 13 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
11:8	R/W	0x0	RX_CH13_MAP RX Channel 13 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:6	/	/	/
5:4	R/W	0x0	RX_CH12_SELECT Rx channel 12 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0068			Register Name: I2S/PCM_RXCHMAP0
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	RX_CH12_MAP RX Channel 12 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

17.1.8.28 0x006C I2S/PCM RX Channel Mapping Register1 (Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: I2S/PCM_RXCHMAP1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	RX_CH11_SELECT Rx channel 11 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
27:24	R/W	0x0	RX_CH11_MAP RX Channel 11 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
23:22	/	/	/
21:20	R/W	0x0	RX_CH10_SELECT Rx channel 10 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x006C			Register Name: I2S/PCM_RXCHMAP1
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0x0	RX_CH10_MAP RX Channel 10 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:14	/	/	/
13:12	R/W	0x0	RX_CH9_SELECT Rx channel 9 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
11:8	R/W	0x0	RX_CH9_MAP RX Channel 9 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:6	/	/	/
5:4	R/W	0x0	RX_CH8_SELECT Rx channel 8 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
3:0	R/W	0x0	RX_CH8_MAP RX Channel 8 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

17.1.8.29 0x0070 I2S/PCM RX Channel Mapping Register2 (Default Value: 0x0000_0000)

Offset: 0x0070	Register Name: I2S/PCM_RXCHMAP2

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	RX_CH7_SELECT Rx channel 7 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
27:24	R/W	0x0	RX_CH7_MAP RX Channel 7 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
23:22	/	/	/
21:20	R/W	0x0	RX_CH6_SELECT Rx channel 6 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
19:16	R/W	0x0	RX_CH6_MAP RX Channel 6 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:14	/	/	/
13:12	R/W	0x0	RX_CH5_SELECT Rx channel 5 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

11: 8	R/W	0x0	RX_CH5_MAP RX Channel 5 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:6	/	/	/
5:4	R/W	0x0	RX_CH4_SELECT Rx channel 4 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
3:0	R/W	0x0	RX_CH4_MAP RX Channel 4 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

17.1.8.30 0x0074 I2S/PCM RX Channel Mapping Register3 (Default Value: 0x0000_0000)

Offset: 0x0074			Register Name: I2S/PCM_RXCHMAP3
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	RX_CH3_SELECT Rx channel 4 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
27:24	R/W	0x0	RX_CH3_MAP RX Channel 3 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
23:22	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0074			Register Name: I2S/PCM_RXCHMAP3
Bit	Read/Write	Default/Hex	Description
21:20	R/W	0x0	RX_CH2_SELECT Rx channel 2 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
19:16	R/W	0x0	RX_CH2_MAP RX Channel 2 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:14	/	/	/
13:12	R/W	0x0	RX_CH1_SELECT Rx channel 1 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
11:8	R/W	0x0	RX_CH1_MAP RX Channel 1 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:6	/	/	/
5:4	R/W	0x0	RX_CH0_SELECT Rx channel 0 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0074			Register Name: I2S/PCM_RXCHMAP3
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	RX_CH0_MAP RX Channel 0 Mapping 0: 1st Sample (p) 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

17.1.8.31 0x0080 I2S/PCM ASRC MCLK Configure Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: MCLKCFG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	ASRC_MCLK_GATE ASRC Clock Gate Enable 0: Gated 1: Not gated
15:4	/	/	/
3:0	R/W	0x0	ASRC_MCLK_FREQ_DIV_COE Frequency Division Coefficient 0000 = Reserved (no output) 0001 = 1x 0010 = 1/2x 0011 = 1/4x 0100 = 1/6x 0101 = 1/8x 0110 = 1/12x 0111 = 1/16x 1000 = 1/24x 1001 = 1/32x 1010 = 1/48 1011 = 1/64x 1100 = 1/96x 1101 = 1/128x 1110= 1/176x 1111= 1/192x

17.1.8.32 0x0084 I2S/PCM ASRC Out Sample Configure Register (Default Value: 0x0000_0000)

Offset: 0x0084	Register Name: F_{SOUT}CFG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20	R/W	0x0	FSOUT_GATE Fsout Clock Gate Enable Control 0: Gated 1: Not gated
19:16	R/W	0x0	FSOUT_CLK_SRC_SEL Fsout Clock Source Select 00: I2S0_ASRC_CLK 01: ACLK 10: ACLKM 11: BCLK Others: Reserved
15:8	/	/	/
7:4	R/W	0x0	FSOUT_CLK_FREQ_DIV_COE1 Fsout Frequency Division Coefficient 1 The First Division Factor It has two levels of frequency division, the first level is bit [7:4], the second level is bit [3:0], and the frequency division factors are multiplied by the two division factors, the division relationship of the two divisions are the same. 0000 = Res (no output) 0001 = 1x 0010 = 1/2x 0011 = 1/4x 0100 = 1/6x 0101 = 1/8x 0100 = 1/12x 0110 = 1/16x 0111 = 1/24x 1000 = 1/32x 1001 = 1/48 1010 = 1/64x 1011 = 1/96x 1100 = 1/128x 1101 = 1/176x 1111 = 1/192x

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

3:0	R/W	0x0	FSOUT_CLK_FREQ_DIV_COE2 Fsout Frequency Division Coefficient 2 The Second Division Factor It has two levels of frequency division, the first level is bit [7:4], the second level is bit [3:0], and the frequency division factors are multiplied by the two division factors, the division relationship of the two divisions are the same. 0000 = Res (no output) 0001 = 1x 0010 = 1/2x 0011 = 1/4x 0100 = 1/6x 0101 = 1/8x 0110 = 1/12x 0111 = 1/16x 1000 = 1/24x 1001 = 1/32x 1010 = 1/48 1011 = 1/64x 1100 = 1/96x 1101 = 1/128x 1110 = 1/176x 1111 = 1/192x

17.1.8.33 0x0088 I2S/PCM In Sample Pulse Extend Configure Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: FsinEXTCFG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	EXTEND_EN Extend Enable 0: Disabled 1: Enabled Enable the bit when using ASRC.
15:0	R/W	0x0	EXTEND_VALUE Extend value The Cycle Number of Pulse Extend The cycle is BCLK clock and is 1 at least.

17.1.8.34 0x008C I2S/PCM ASRC Enable Configure Register (Default Value: 0x0000_0000)

Offset: 0x008C	Register Name: ASRCEN

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	ASRC_EN ASRC Function Enable 0: Disabled 1: Enabled

17.1.8.35 0x0090 I2S/PCM ASRC Manual Configure Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: ASRCMANCFG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	ASRC_RATIO_MANUAL_EN Manual Configuration of ASRC Ratio Enable 0: Disabled 1: Enabled
30:26	/	/	/
25:0	R/W	0x0	ASRC_RATIO_VALUE_MANUAL_CFG ASRC Ratio Value Manual Configuration The ratio value is an unsigned 26-bit number in the format of 4.22 data. The higher 4 bits are integer, and the lower 22 bits are decimal.

17.1.8.36 0x0094 I2S/PCM ASRC Ratio State Configure Register (Default Value: 0x0040_0000)

Offset: 0x0094			Register Name: ASRCRATIOSTAT
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R	0x0	ASRC_BUF_OVERFLOW_STA ASRC Receive Data Buffer Overflow State It can control the mute with lock. 0: No overflow 1: Overflow
28	R	0x0	ADAPT_COMPUT_LOCK Adaptive Ratio Computational Lock 0: Unlocked 1: Locked
27:26	/	/	/
25:0	R	0x400000	ADAPT_COMPUT_VALUE Adaptive Ratio Computational Value

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

17.1.8.37 0x0098 I2S/PCM ASRC FIFO State Configure Register (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: ASRCFIFOSTAT
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:0	R	0x0	ASRC_RX_FIFO_FULL_LEVAL ASRC RXFIFO Full Level The FIFO fill level for the ratio value of the received data.

17.1.8.38 0x009C I2S/PCM ASRC MBIST Test Configure Register (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: ASRCMBISTCFG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	ASRC_RAM_BIST_EN ASRC RAM BIST Enable Enable the RAM BIST.
7:1	/	/	/
0	R/W	0x0	ASRC_ROM_BIST_EN ASRC ROM BIST Enable Enable the ROM BIST.

17.1.8.39 0x00A0 I2S/PCM ASRC MBIST Test State Configure Register (Default Value: 0x0000_0002)

Offset: 0x00A0			Register Name: ASRCMBISTSTA
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R	0x0	ROM_BIST_ERROR_XOR ROM Bist Error Xor
17	R	0x0	ROM_BIST_ERROR_SUM ROM Bist Error Sum
16	R	0x0	ROM_BUSY_STATUS ROM Busy Status 1: ROM busy 0: ROM IDLE
15:8	/	/	/
7	R	0x0	RAM_BIST_ERR_STATUS RAM Bist Error Status 1: Error 0: No Effect

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00A0			Register Name: ASRCMBISTSTA
Bit	Read/Write	Default/Hex	Description
6:4	R	0x0	RAM_BIST_ERROR_PATTERN. RAM Bist Error Pattern.
3:2	R	0x0	RAM_BIST_ERROR_CYCLE RAM Bist Error Cycle.
1	R	0x1	RAM_STOP_STATUS RAM Stop Status 1: Stop 0: Running
0	R	0x0	RAM_BUSY_STATUS RAM Busy Status 1: RAM busy 0: RAM IDLE.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

17.2 DMIC

17.2.1 Overview

The Digital MIC controller supports one 8-channel digital microphone interface and can output 128 fs or 64 fs (fs = ADC sample rate).

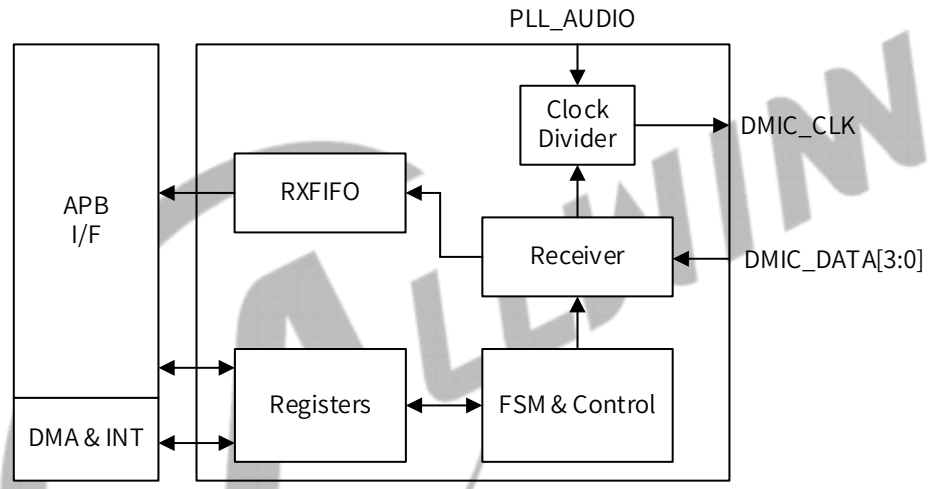
The DMIC controller includes the following features:

- Supports up to 8 channels
- Sample rate from 8 kHz to 48 kHz

17.2.2 Block Diagram

The following figure shows a block diagram of the DMIC.

Figure 17-10 DMIC Block Diagram



17.2.3 Clock Sources

The following table describes the clock sources of DMIC. For clock setting, configurations, and gating information, refer to the section CCU.

Module	Clock Sources	Description
DMIC	AUDIO0PLL4X	Its frequency is 24.5714*4 MHz by default.
	AUDIO1PLL_DIV2	Its frequency is 1536 MHz by default.
	AUDIO1PLL_DIV5	Its frequency is 614.4 MHz by default.

17.2.4 External Signals

The following table describes the external signals of DMIC.

Table 17-3 DMIC External Signals

Signal Name	Description	Type
DMIC-CLK	Digital Microphone Clock Output	O

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

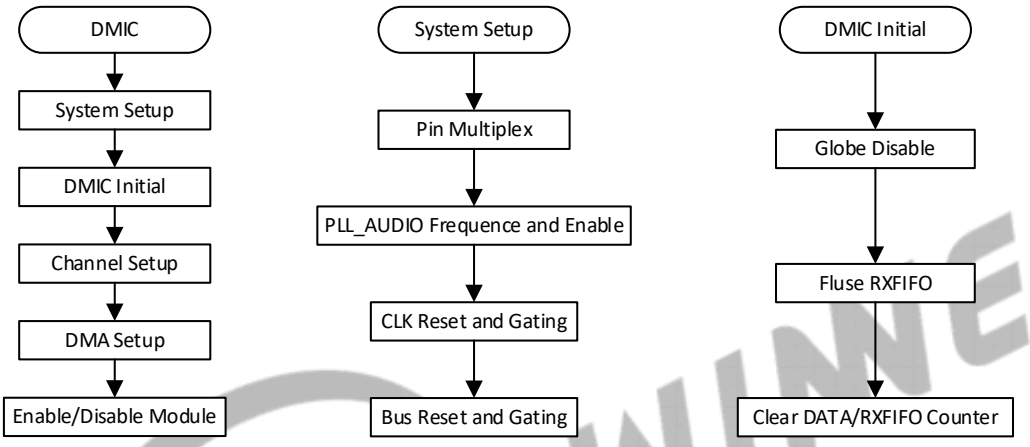
Signal Name	Description	Type
DMIC-DATA[3:0]	Digital Microphone Data Input	I

17.2.5 Programming Guidelines

The software operation of the DMIC is divided into five steps: system setup, DMIC initialization, channel setup, DMA setup, and Enable/Disable module.

The following figure shows the flow chart of the whole operation, the system setup, and the DMIC initialization.

Figure 17-11 DMIC Operation Mode



17.2.5.1 System Setup and DMIC Initialization

The first step in the system setup is properly programming the GPIO because the DMIC port is a multiplex pin. For functions of the multiplex pins, refer to the section GPIO.

For the system setup, perform the following steps to set clock source.

Step 1 Disable the PLL_AUDIO through PLL_AUDIOx Control Register[PLL_ENABLE].

Step 2 Set up the frequency of the PLL_AUDIO in PLL_AUDIOx Control Register. Then enable PLL_AUDIO.

Step 3 Enable the DMIC gating through DMIC_CLK_REG when you check out that the LOCK bit of PLL_AUDIOx Control Register becomes 1.

Step 4 Reset and enable the DMIC bus gating by DMIC_BGR_REG.

After the system setup, the register of DMIC can be setup.

Step 5 Initialize the DMIC. You should close the globe enable bit (DMIC_EN[8]), data channel enable bit (DMIC_EN[7:0]) by writing 0 to it.

Step 6 Flush the RXFIFO by writing 1 to DMIC_RXFIFO_CTR[31].

Step 7 Clear the Data/RXFIFO counter by writing 1 to DMIC_RXFIFO_STA, DMIC_CNT.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

17.2.5.2 Channel Setup and DMA Setup

You can set up the sample rate, the sample resolution, the over-sample rate, the channel number, the RXFIFO output mode, the RXFIFO trigger level, and so on. The setup of the register can be found in the specification.

The DMIC supports two methods to transfer the data. The most common way is DMA; the setup of DMA can be found in section DMAC. In this module, you just enable the DRQ.

17.2.5.3 Enable and Disable DMIC

Step 1 Enable the data channel enable bit (DMIC_EN[7:0]) by writing 1 to it.

Step 2 Enable DMIC by writing 1 to the Globe Enable bit (DMIC_EN[8]).

Step 3 Write 0 to DMIC_EN[8] to disable DMIC.

17.2.6 Register List

Module Name	Base Address
DMIC	0x02531000

Register Name	Offset	Description
DMIC_EN	0x0000	DMIC Enable Control Register
DMIC_SR	0x0004	DMIC Sample Rate Register
DMIC_CTR	0x0008	DMIC Control Register
DMIC_DATA	0x0010	DMIC DATA Register
DMIC_INTC	0x0014	DMIC Interrupt Control Register
DMIC_INTS	0x0018	DMIC Interrupt Status Register
DMIC_RXFIFO_CTR	0x001C	DMIC RXFIFO Control Register
DMIC_RXFIFO_STA	0x0020	DMIC RXFIFO Status Register
DMIC_CH_NUM	0x0024	DMIC Channel Number Register
DMIC_CH_MAP	0x0028	DMIC Channel Mapping Register
DMIC_CNT	0x002C	DMIC Counter Register
DATA0_DATA1_VOL_CTR	0x0030	DATA0 And DATA1 Volume Control Register
DATA2_DATA3_VOL_CTR	0x0034	DATA2 And DATA3 Volume Control Register
HPF_EN_CTR	0x0038	High Pass Filter Enable Control Register
HPF_COEF_REG	0x003C	High Pass Filter Coef Register
HPF_GAIN_REG	0x0040	High Pass Filter Gain Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

17.2.7 Register Description

17.2.7.1 0x0000 DMIC Enable Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: DMIC_EN
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R/W	0x0	RX_SYNC_EN_START Audio Subsys RX Synchronize Enable Start Includes I2S0/I2S1/I2S2/I2S3/I2S4/DMIC/OWA. The bit will take effect only when RX_SYNC_EN is set to 1. 0: Disable 1: Enable
28	R/W	0x0	RX_SYNC_EN DMIC RX Synchronize Enable 0: Disable 1: Enable
27:9	/	/	/
8	R/W	0x0	GLOBE_EN DMIC Globe Enable 0: Disable 1: Enable
7	R/W	0x0	DATA3_CHR_EN DATA3 Right Channel Enable 0: Disable 1: Enable
6	R/W	0x0	DATA3_CHL_EN DATA3 Left Channel Enable 0: Disable 1: Enable
5	R/W	0x0	DATA2_CHR_EN DATA2 Right Channel Enable 0: Disable 1: Enable
4	R/W	0x0	DATA2_CHL_EN DATA2 Left Channel Enable 0: Disable 1: Enable
3	R/W	0x0	DATA1_CHR_EN DATA1 Right Channel Enable 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: DMIC_EN
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	DATA1_CHL_EN DATA1 Left Channel Enable 0: Disable 1: Enable
1	R/W	0x0	DATA0_CHR_EN DATA0 Right Channel Enable 0: Disable 1: Enable
0	R/W	0x0	DATA0_CHL_EN DATA0 Left Channel Enable 0: Disable 1: Enable

17.2.7.2 0x0004 DMIC Sample Rate Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: DMIC_SR
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	R/W	0x0	DMIC_SR Sample Rate of DMIC 000: 48 kHz 010: 24 kHz 100: 12 kHz 110: Reserved 001: 32 kHz 011: 16 kHz 101: 8 kHz 111: Reserved 44.1 kHz/22.05 kHz/11.025 kHz can be supported by Audio PLL Configure Bit.

17.2.7.3 0x0008 DMIC Control Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: DMIC_CTR
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: DMIC_CTR
Bit	Read/Write	Default/Hex	Description
10:9	R/W	0x0	DMICFDT DMIC RXFIFO Delay Time for Writing Data after GLOBE_EN 00: 5 ms 01: 10 ms 10: 20 ms 11: 30 ms
8	R/W	0x0	DMICDFEN DMIC RXFIFO Delay Function for Writing Data after GLOBE_EN 0: Disable 1: Enable
7	R/W	0x0	DATA3_LR_SWAP_EN DATA3 Left Data and Right Data Swap Enable 0: Disable 1: Enable
6	R/W	0x0	DATA2_LR_SWAP_EN DATA2 Left Data and Right Data Swap Enable 0: Disable 1: Enable
5	R/W	0x0	DATA1_LR_SWAP_EN DATA1 Left Data and Right Data Swap Enable 0: Disable 1: Enable
4	R/W	0x0	DATA0_LR_SWAP_EN DATA0 Left Data and Right Data Swap Enable 0: Disable 1: Enable
3:1	/	/	/
0	R/W	0x0	DMIC_OS_Rate DMIC Oversample Rate 0: 128 (Supports 8 kHz to 24 kHz) 1: 64 (Supports 16 kHz to 48 kHz)

17.2.7.4 0x0010 DMIC DATA Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: DMIC_DATA
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DMIC_DATA

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

17.2.7.5 0x0014 DMIC Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: DMIC_INTC
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	RXFIFO_DRQ_EN DMIC RXFIFO Data Available DRQ Enable 0: Disable 1: Enable
1	R/W	0x0	RXFIFO_OVERRUN_IRQ_EN DMIC RXFIFO Overrun IRQ Enable 0: Disable 1: Enable
0	R/W	0x0	DATA_IRQ_EN DMIC RXFIFO Data Available IRQ Enable 0: Disable 1: Enable

17.2.7.6 0x0018 DMIC Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: DMIC_INTS
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W1C	0x0	RXFIFO_OVERRUN_IRQ_PENDING DMIC RXFIFO Overrun Pending Interrupt 0: No pending IRQ 1: RXFIFO overrun pending IRQ Writing 1 to clear this interrupt.
0	R/ W1C	0x0	RXFIFO_DATA_IRQ_PENDING DMIC RXFIFO Data Available Pending Interrupt 0: No pending IRQ 1: Data available pending IRQ Writing 1 to clear this interrupt or automatically clear if fifodeep >= rftlvl (RXFIFO Trigger Level).

17.2.7.7 0x001C DMIC RXFIFO Control Register (Default Value: 0x0000_0040)

Offset: 0x001C			Register Name: DMIC_RXFIFO_CTR
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	DMIC_RXFIFO_FLUSH DMIC RXFIFO Flush Writing 1 to flush RXFIFO, self-clear to 0

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x001C			Register Name: DMIC_RXFIFO_CTR
Bit	Read/Write	Default/Hex	Description
30:10	/	/	/
9	R/W	0x0	RXFIFO_MODE RXFIFO Output Mode (Mode 0, 1) 0: Expanding 0 at LSB of RXFIFO register 1: Expanding received sample sign bit at MSB of RXFIFO register For 24-bit received audio sample: Mode 0: APB_RDATA[31:0] = {RXFIFO[20:0],11 h0} Mode 1: APB_RDATA[31:0] = {8{RXFIFO[20]}, RXFIFO[20:0],3 h0} For 16-bit received audio sample: Mode 0: APB_RDATA[31:0] = {RXFIFO[20:5], 16 h0} Mode 1: APB_RDATA[31:0] = {16{RXFIFO[20]}, RXFIFO[20:5]}
8	R/W	0x0	Sample Resolution 0: 16-bit 1: 24- bit
7:0	R/W	0x40	RXFIFO_TRG_LEVEL RXFIFO Trigger Level (TRLV [7:0]) Interrupt and DMA request trigger level for DMIC RXFIFO normal condition IRQ/DRQ Generated when WLEVEL > TRLV [7:0]) Note: WLEVEL represents the number of valid samples in the DMIC RXFIFO

17.2.7.8 0x0020 DMIC RXFIFO Status Register (Default Value: 0x0000_0100)

Offset: 0x0020			Register Name: DMIC_RXFIFO_STA
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	/	/	Reserved
7:0	R/W	0x0	DMIC_DATA_CNT DMIC RXFIFO Available Sample Word Counter

17.2.7.9 0x0024 DMIC Channel Number Register (Default Value: 0x0000_0001)

Offset: 0x0024			Register Name: DMIC_CH_NUM
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	R/W	0x1	DMIC_CH_NUM DMIC enable channel numbers are (N + 1).

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

17.2.7.10 0x0028 DMIC Channel Mapping Register (Default Value: 0x7654_3210)

Offset: 0x0028			Register Name: DMIC_CH_MAP
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x7	DMIC_CH7_MAP DMIC Channel 7 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
27:24	R/W	0x6	DMIC_CH6_MAP DMIC Channel 6 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
23:20	R/W	0x5	DMIC_CH5_MAP DMIC Channel 5 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
19:16	R/W	0x4	DMIC_CH4_MAP DMIC Channel 4 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0028			Register Name: DMIC_CH_MAP
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x3	DMIC_CH3_MAP DMIC Channel 3 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
11:8	R/W	0x2	DMIC_CH2_MAP DMIC Channel 2 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
7:4	R/W	0x1	DMIC_CH1_MAP DMIC Channel 1 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
3:0	R/W	0x0	DMIC_CH0_MAP DMIC Channel0 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

17.2.7.11 0x002C DMIC Counter Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: DMIC_CNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	DMIC_CNT RX Sample Counter The audio sample number of reading from RXFIFO. When one sample is read by DMA or by host IO(such as MAD), the RX sample counter register increases by one. The RX sample counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this initial value. Note: It is used for Audio/Video Synchronization.

17.2.7.12 0x0030 DATA0 and DATA1 Volume Control Register (Default Value: 0xA0A0_A0A0)

Offset: 0x0030			Register Name: DATA0_DATA1_VOL_CTR
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0xA0	DATA1L_VOL Data1 Left Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB
23:16	R/W	0xA0	DATA1R_VOL Data1 Right Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0030			Register Name: DATA0_DATA1_VOL_CTR
Bit	Read/Write	Default/Hex	Description
15:8	R/W	0xA0	DATA0L_VOL Data0 Left Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB
7:0	R/W	0xA0	DATA0R_VOL Data0 Right Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB

17.2.7.13 0x0034 DATA2 and DATA3 Volume Control Register (Default Value: 0xA0A0_A0A0)

Offset: 0x0034			Register Name: DATA2_DATA3_VOL_CTR
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0xA0	DATA3L_VOL Data3 Light Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0034			Register Name: DATA2_DATA3_VOL_CTR
Bit	Read/Write	Default/Hex	Description
23:16	R/W	0xA0	DATA3R_VOL Data3 Right Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB
15:8	R/W	0xA0	DATA2L_VOL Data2 Light Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB
7:0	R/W	0xA0	DATA2R_VOL Data2 Right Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB

17.2.7.14 0x0038 High Pass Filter Enable Control Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: HPF_EN_CTR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0038			Register Name: HPF_EN_CTR
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	HPF_DATA3_CHR_EN High Pass Filter DATA3 Right Channel Enable 0: Disable 1: Enable
6	R/W	0x0	HPF_DATA3_CHL_EN High Pass Filter DATA3 Left Channel Enable 0: Disable 1: Enable
5	R/W	0x0	HPF_DATA2_CHR_EN High Pass Filter DATA2 Right Channel Enable 0: Disable 1: Enable
4	R/W	0x0	HPF_DATA2_CHL_EN High Pass Filter DATA2 Left Channel Enable 0: Disable 1: Enable
3	R/W	0x0	HPF_DATA1_CHR_EN High Pass Filter DATA1 Right Channel Enable 0: Disable 1: Enable
2	R/W	0x0	HPF_DATA1_CHL_EN High Pass Filter DATA1 Left Channel Enable 0: Disable 1: Enable
1	R/W	0x0	HPF_DATA0_CHR_EN High Pass Filter DATA0 Right Channel Enable 0: Disable 1: Enable
0	R/W	0x0	HPF_DATA0_CHL_EN High Pass Filter DATA0 Left Channel Enable 0: Disable 1: Enable

17.2.7.15 0x003C High Pass Filter Coefficient Register (Default Value: 0x00FF_AA45)

Offset: 0x003C			Register Name: HPF_COEF_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00FFAA45	HPF_COE High Pass Filter Coefficient

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

17.2.7.16 0x0040 High Pass Filter Gain Register (Default Value: 0x00FF_D522)

Offset: 0x0040			Register Name: HPF_GAIN_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00FFD522	HPF_GAIN High Pass Filter Gain

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

17.3 One Wire Audio (OWA)

17.3.1 Overview

The One Wire Audio (OWA) provides a serial bus interface for audio data. This interface is widely used for consumer audio connection.

The OWA includes the following features:

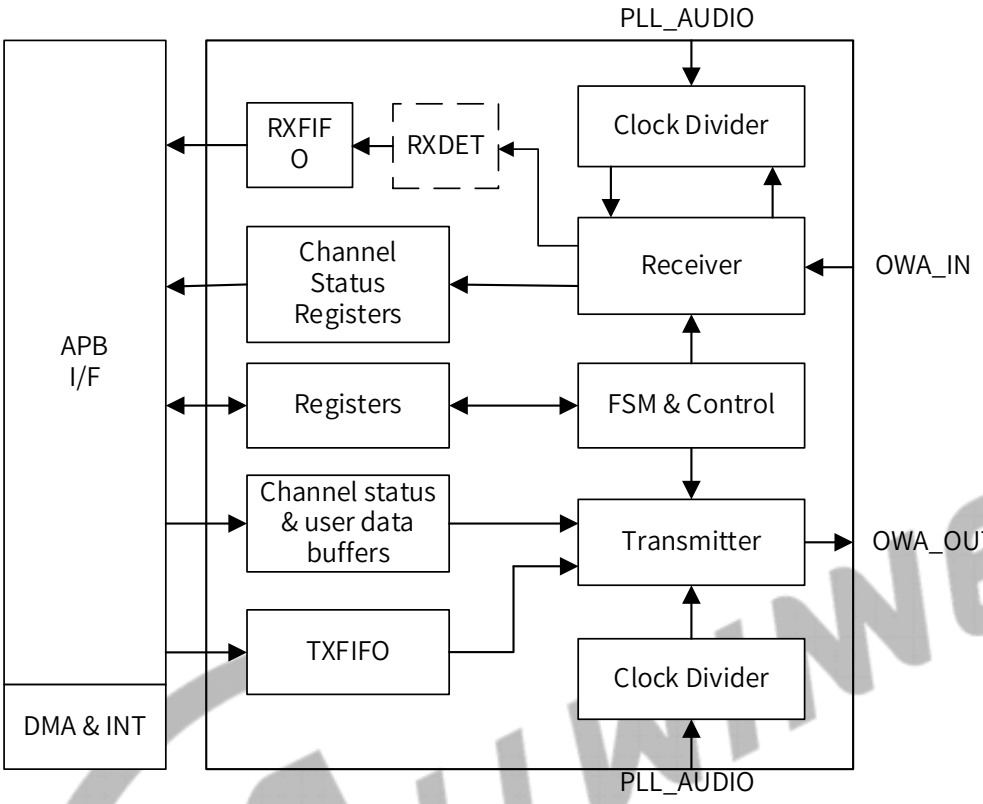
- One OWA TX and One OWA RX
- Compliance with S/PDIF interface
- Compatible with standard IEC-60958 and IEC-61937
- IEC-60958 supports data formats: 16 bits, 20 bits, and 24 bits
- TXFIFO and RXFIFO
  - One 128×24bits TXFIFO and one 64×24bits RXFIFO for audio data transfer
  - Programmable FIFO thresholds
- Supports TX/RX DMA slave interface
- Multiple function clock
  - Separate clock for OWA TX and OWA RX
  - OWA TX function clock includes a series of 24.576MHz/49.152MHz and 22.579MHz frequency (TX function clock 49.152MHz support ample rate 384KHz)
  - OWA RX function clock includes a series of 400MHz frequency (RX function clock 400MHz support CDR of sample rate from 8KHz to 384KHz)
- Supports hardware parity on TX/RX
  - Hardware parity generation on the transmitter
  - Hardware parity checking on the receiver
- Supports channel status capture on the receiver
- Supports channel sample rate capture on the receiver
- Supports insertion detection for the receiver
- Supports channel status insertion for the transmitter

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

17.3.2 Block Diagram

The following figure shows the OWA block diagram.

Figure 17-12 OWA Block Diagram



17.3.3 Clock Sources

The following table describes the clock sources of OWA. For clock setting, configurations, and gating information, refer to the section CCU.

Module	Clock Sources	Description
OWA_TX	AUDIO0PLL4X	Its frequency is 24.5714*4 MHz by default.
	AUDIO1PLL_DIV2	Its frequency is 1536 MHz by default.
	AUDIO1PLL_DIV5	Its frequency is 614.4 MHz by default.
OWA_RX	PERI0_400M	Its frequency is 400 MHz by default.

17.3.4 External Signals

The OWA is a Biphasic-Mark Encoding Digital Audio Transfer protocol. In this protocol, the CLK signal and data signal are transferred in the same line. The following table describes the external signals of OWA. OWA-OUT is the output pin for the output CLK and DATA, and OWA-IN is the input pin for the input CLK and DATA.

Table 17-4 OWA External Signals

Signal Name	Description	Type
OWA0-IN	One Wire Audio Input	I

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Signal Name	Description	Type
OWA0-OUT	One Wire Audio Output	O

17.3.5 Functional Description

17.3.5.1 Biphase-Mark Code (BMC)

In the OWA format, the digital signal is coded using the biphase-mark code (BMC). The clock, frame, and data are embedded in only one signal(c)the data pin. In the BMC system, each data bit is encoded into two logical states (00, 01, 10, or 11) at the pin. The following figure and table show how data is encoded to the BMC format.

The frequency of the clock is twice the data bit rate, as shown in the following figure. Also, the clock is always programmed to 128 x fs, where fs is the sample rate. The device receiving in the OWA format can recover the clock and frame information from the BMC signal.

Figure 17-13 OWA Biphase-Mark Code

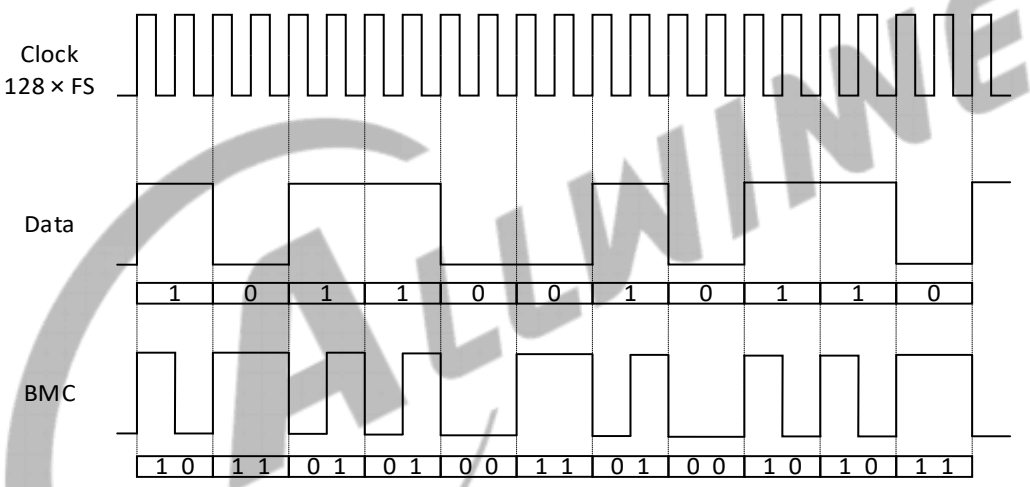


Table 17-5 Biphase-Mark Encoder

Data	Previous State	BMC
0	0	11
0	1	00
1	0	10
1	1	01

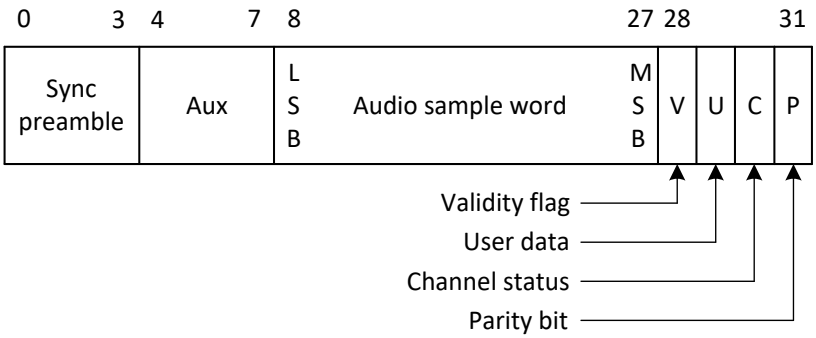
17.3.5.2 IEC60958 Transmit Format

The OWA supports digital audio data transfer and receive. It also supports full-duplex synchronous work mode. The software can set the work mode by the OWA Control Register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Every audio sample transmitted in a sub-frame consists of 32-bit, numbered from 0 to 31. The following figure shows a sub-frame.

Figure 17-14 OWA Sub-Frame Format



Bits 0-3 carry one of the four permitted preambles to signify the type of audio sample in the current sub-frame. The preamble is not encoded in BMC format, and therefore the preamble code can contain more than two consecutive 0 or 1 logical states in a row.

Bits 4-27 carry the audio sample word in linear 2s-complement representation. The most-significant bit (MSB) is carried by bit 27. When a 24-bit coding range is used, the least-significant bit (LSB) is in bit 4. When a 20-bit coding range is used, bit [8:27] carry the audio sample word with the LSB in bit 8. Bit [4:7] may be used for other applications and are designated auxiliary sample bits.

If the source provides fewer bits than the interface allows (either 20 or 24), the unused LSBs are set to logical 0. For a nonlinear PCM audio application or a data application, the main data field may carry any other information.

Bit 28 carries the validity bit (V) associated with the main data field in the sub-frame.

Bit 29 carries the user data channel (U) associated with the main data field in the sub-frame.

Bit 30 carries the channel status information (C) associated with the main data field in the sub-frame. The channel status indicates if the data in the sub-frame is a digital audio or some other type of data.

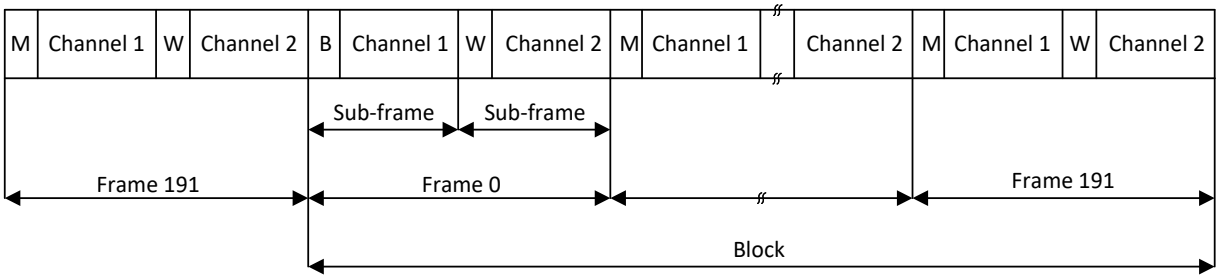
Bit 31 carries a parity bit (P) such that bit 4-31 carry an even number of 1s and an even number of 0s (even parity). As shown in the following table, the preambles (bit 0-3) are also defined with even parity.

Table 17-6 Preamble Codes

Preamble Code	Previous Logical State	Logical State	Description
B (or Z)	0	1110 1000	Start of a block and sub-frame 1
M (or X)	0	1110 0010	Sub-frame 1
W (or Y)	0	1110 0100	Sub-frame 2

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 17-15 OWA Frame/Block Format



17.3.5.3 IEC61937 Transmit Format

IEC 61937 applies to the digital audio interface by using the IEC 60958 series for the conveying of non-linear PCM encoded audio bitstreams. The non-linear PCM encoded audio bitstream is transferred by using the basic 16-bit data area of the IEC 60958 subframes, i.e. in time-slots 12 to 27. Because the non-linear PCM encoded audio bitstream to be transported is at a lower data rate than that supported by the IEC 60958 interface, the audio bitstream is broken into a sequence of discrete data-bursts, and stuffing between the data-bursts is necessary.

IEC 60958 Data Burst

The method of placing the data into the IEC 60958 bitstream is to format the data to be transmitted into data-bursts and to send each data-burst in a continuous sequence of IEC 60958 frames.

Table 17-7 Bit Allocation of Data-Burst in IEC 60958 Subframes

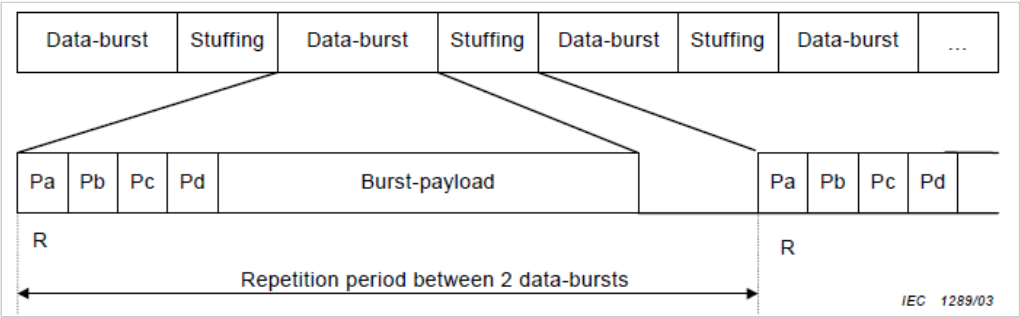
Subframe	Bit of subframes				
	MSB b27	b26	b25 ..... b14	b13	LSB b12
Frame 0; subframe B or M	0	1		14	15
Frame 0; subframe W	16	17		30	31
Frame 1; subframe B or M	32	33		46	47
Frame 1; subframe W	48	49		62	63
Frame 2; subframe B or M	64	65		78	79
----------			----------		
Last subframe B or M of data-burst	n-32	n-31		n-18	n-17
Last subframe W of data-burst	n-16	n-15		n-2	n-1

Data Burst Format

Each data-burst contains a burst-preamble consisting of four 16-bit words (Pa, Pb, Pc and Pd) followed by the burst-payload which contains data of an encoded audio frame.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

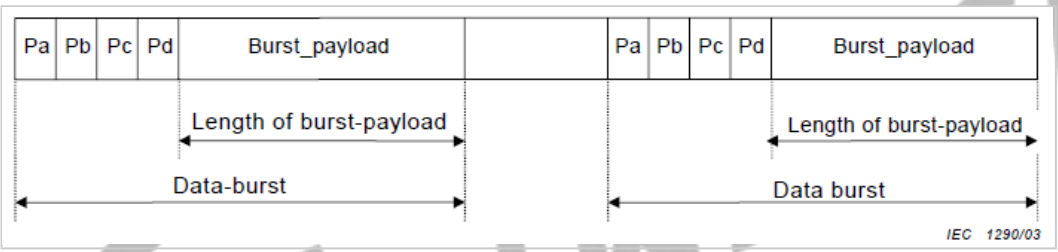
Figure 17-16 Data-Burst Format



- Burst-preamble

The burst-preamble consists of four mandatory fields. Pa and Pb represent a synchronization word. Pc gives information about the type of data, and some information/control for the receiver. Pd gives the length of the burst-payload, and is limited to 65535 bits in the case of Pd represent bits length, or is limited to 65535 bytes in the case of Pd represent bytes length.

Figure 17-17 Data-burst Preamble



The four preamble words are contained in two sequential IEC 60958 frames. The frame beginning the data-burst contains preamble word Pa in subframe 1, and Pb in subframe 2. The next frame contains Pc in subframe 1 and Pd in subframe 2. When placed into an IEC 60958 subframe, the MSB of a 16-bit burst-preamble word is placed into time-slot 27 and the LSB is placed into time-slot 12.

Figure 17-18 Data-burst Preamble words

Preamble word	Length of field	Contents	Value MSB..LSB
Pa	16-bit	Sync word 1	F872h
Pb	16-bit	Sync word 2	4E1Fh
Pc	16-bit	Burst-info	Table 5
Pd	16-bit	Length-code	Number of bits or number of bytes according to data-type

- Burst-information

The 16-bit burst-information contains information about the data which will be found in the data-burst.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 17-19 Fields of Burst-information

Bits of Pc	Value	Contents	Remark
0 – 6		Data-type	See IEC 61937-2
7	0	Error-flag indicating a valid burst-payload	
	1	Error-flag indicating that the burst-payload may contain errors	
8 – 12		Data-type-dependent info	
13 – 15	0	Bitstream-number	
NOTE The repetition period of pause data-bursts depends on the application in which IEC 60958 is used to convey encoded audio bitstreams.			

The 7-bit data-type is defined in bits 0-6 of the burst-preamble Pc, the bit 6 is the MSB. This data-type field indicates the format of the burst-payload, which will be conveyed in the data-burst. Typical properties of a data-type are the reference point and repetition period of the burst, which is the number of sampling periods of the audio between the reference point of the current data-burst and the reference point of the next data-burst. The reference point is inherently defined for each data-type.

The error-flag bit is available to indicate if the contents of the data-burst contain data errors. If a data-burst is thought to be error-free, or if the data source does not know if the data contains errors, then the value of this bit is set to a 0 . If the data source does know that a particular data-burst contains some errors this bit may be set to a 1 . The usage of this bit by receiver is optional.

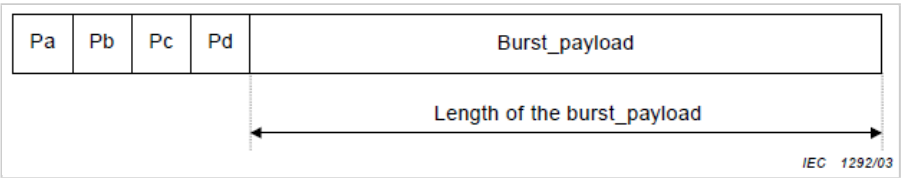
The meaning of the 5-bit data-type-dependent info depends on the value of the data-type.

The 3-bit bitstream-number indicates to which bitstream the data-burst belongs. Eight codes (0-7) are available so that up to eight independent bitstreams may be multiplexed in one bitstream in a time multiplex. Each independent bitstream shall use a unique bit-stream number.

- Length-code

The length-code indicates the number of bits or bytes according to data-type within the data burst, from 0 to 65535. The size of the Pa, Pb, Pc and Pd is not counted in the value of the length-code. In other words, the length-code indicates the number of bits of the burst-payload in bits, plus the conditional length of Pe and Pf, or the number of bytes of the burst-payload in bytes, plus the conditional length of Pe and Pf if exists.

Figure 17-20 Length of the Burst-Payload Specified by Pd



17.3.5.4 Audio Sample Ratio Detection

The sampling rate is calculated according to the data pulse back-stepping method. In the first phase lock of the CDR, find the period of 1 Frame. Then count by using the high-speed sampling

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

clock and read the counting value of the pulse width of Period Max, then the sampling rate can be calculated.

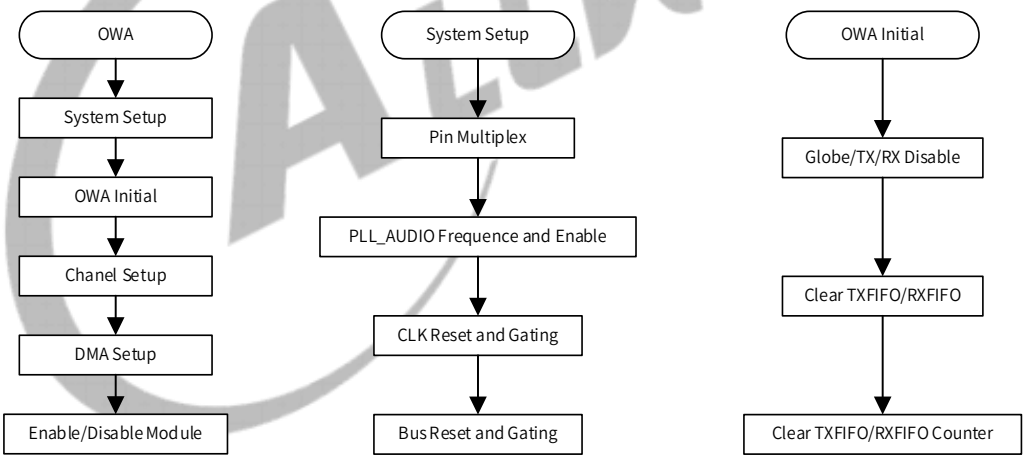
Table 17-8 The Relation between Different System Clock and Sample Ratio

	Sample Clock Cycles			
TX Sample Rate(kHz)	196.608 MHz-SysClk	200 MHz-SysClk	300 MHz-SysClk	400Mhz-SysClk
22.05	8916(±5)	9070(±5)	13605(±5)	18140(±5)
24	8192(±5)	8333(±5)	12500(±5)	16666(±5)
32	6144(±5)	6250(±5)	9375(±5)	12500(±5)
44.1	4458(±5)	4535(±5)	6802(±5)	9070(±5)
48	4096(±5)	4166(±5)	6250(±5)	8332(±5)
96	2048(±5)	2083(±5)	3125(±5)	4166(±5)
176.4	1114(±5)	1133(±5)	1700(±5)	2266(±5)
192	1024(±5)	1041(±5)	1562(±5)	2082(±5)

17.3.6 Programming Guidelines

The software operation of the OWA is divided into five steps: system setup, OWA initialization, channel setup, DMA setup and enable/disable module. The following sections describe these five steps.

Figure 17-21 OWA Operation Flow



17.3.6.1 System Setup and OWA Initialization

The first step in the OWA initialization is properly programming the GPIO because the OWA port is a multiplex pin. For functions of the multiplex pins, refer to the section GPIO.

For the system setup, perform the following steps to set clock source.

Step 1 Disable the PLL_AUDIO through PLL_AUDIOx Control Register[PLL_ENABLE].

Step 2 Set up the frequency of the PLL_AUDIO in PLL_AUDIOx Control Register. Then enable PLL_AUDIO.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 3 Enable the OWA gating through OWA_TX_CLK_REG and OWA_RX_CLK_REG when you check out that the LOCK bit of PLL_AUDIOx Control Register becomes 1.

Step 4 Reset and enable the OWA bus gating by OWA_BGR_REG.

After the system setup, the register of OWA can be set up.

Step 1 Reset the OWA by writing 1 to OWA_GENCTL[0] and clear the TX/RX FIFO by writing 1 to OWA_FCTL[17:16].

Step 2 Enable the globe enable bit by writing 1 to OWA_GENCTL[1].

Step 3 Clear the interrupt and TX/RX counter by setting OWA_ISTA and OWA_TX_CNT/OWA_RX_CNT.

17.3.6.2 Parameter Setup and DMA Setup

You can set up the audio type, clock divider ratio, the sample format, and the trigger level, and so on. The setup of the register can be found in the specification.

The OWA supports two methods to transfer the data. The most common way is DMA; the configuration of DMA can be found in section DMAC. In this module, you just enable the DRQ in OWA_INT[7].

17.3.6.3 Enable and Disable OWA

Step 1 Enable TX/RX by writing OWA_TX_CFIG[31]/OWA_RX_CFIG[0].

Step 2 Enable OWA by writing 1 to OWA_GENCTL[1].

Step 3 Write 0 to OWA_GENCTL[1] to disable OWA.

17.3.7 Register List

Module Name	Base Address
OWA	0x02537000

Register Name	Offset	Description
OWA_GEN_CTL	0x0000	OWA General Control Register
OWA_TX_CFIG	0x0004	OWA TX Configuration Register
OWA_RX_CFIG	0x0008	OWA RX Configuration Register
OWA_ISTA	0x000C	OWA Interrupt Status Register
OWA_RXFIFO	0x0010	OWA RXFIFO Register
OWA_FCTL	0x0014	OWA FIFO Control Register
OWA_FSTA	0x0018	OWA FIFO Status Register
OWA_INT	0x001C	OWA Interrupt Control Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
OWA_TX_FIFO	0x0020	OWA TX FIFO Register
OWA_TX_CNT	0x0024	OWA TX Counter Register
OWA_RX_CNT	0x0028	OWA RX Counter Register
OWA_TX_CHSTA0	0x002C	OWA TX Channel Status Register0
OWA_TX_CHSTA1	0x0030	OWA TX Channel Status Register1
OWA_RX_CHSTA0	0x0034	OWA RX Channel Status Register0
OWA_RX_CHSTA1	0x0038	OWA RX Channel Status Register1
OWA_INSERT_REDET_CTL	0x003C	OWA Insert Redetect Control Register
OWA_EXP_CTL	0x0040	OWA Expand Control Register
OWA_EXP_ISTA	0x0044	OWA Expand Interrupt Status Register
OWA_EXP_INFO_0	0x0048	OWA Expand Information Register0
OWA_EXP_INFO_1	0x004C	OWA Expand Information Register1
OWA_EXP_DBG_0	0x0050	OWA Expand Debug Register0
OWA_EXP_DBG_1	0x0054	OWA Expand Debug Register1
OWA_EXP_CDR_DBG	0x005C	OWA Expand CDR Debug Register

17.3.8 Register Description

17.3.8.1 0x0000 OWA General Control Register (Default Value: 0x0000_0080)

Offset: 0x0000			Register Name: OWA_GENCTL
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/WAC	0x0	RST_RX Reset RX 0: Normal 1: Reset Self-clear to 0 .
11:10	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: OWA_GENCTL
Bit	Read/Write	Default/Hex	Description
9:5	R/W	0x4	MCLKDIV MCLK Clock Divide Ratio MCLK Divide Ratio from PLL_AUDIO 0x0: Divide by 128 0x1: Divide by 2 0x2: Divide by 4 0x3: Divide by 6 0x4: Divide by 8 0x5: Divide by 10 0x6: Divide by 12 0x7: Divide by 14 0x8: Divide by 16 0x9: Divide by 18 0xA: Divide by 20 0xB: Divide by 22 0xC: Divide by 24 (p)(p)(p)(p)(p)(p) 0x1F: Divide by 62
4	/	/	/
3	R/W	0x0	MCLKEN MCLK Enable 0: Disable 1: Enable
2	R/W	0x0	LOOP Loopback Test 0: Normal Mode 1: Loopback Test When the bit is set to 1 , the DOUT and DIN need be connected.
1	R/W	0x0	GEN Global Enable A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable
0	R/W	0x0	RST_TX Reset TX 0: Normal 1: Reset Self-clear to 0.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

17.3.8.2 0x0004 OWA TX Configure Register (Default Value: 0x0000_00F0)

Offset: 0x0004			Register Name: OWA_TX_CFIG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TX_SINGLE_MODE TX Single Channel Mode 0: Disable 1: Enable
30:18	/	/	/
17	R/W	0x0	ASS Audio Sample Select when TX FIFO Underrun 0: Sending 0 1: Sending the last audio Note: This bit is only valid in PCM mode.
16	R/W	0x0	TX_AUDIO TX Data Type 0: Linear PCM (Valid bit of both sub-frame set to 0) 1: Non-audio (Valid bit of both sub-frame set to 1)
15:9	/	/	/
8:4	R/W	0xF	TX_RATIO TX Clock Divide Ratio Clock divide ratio = TX_TATIO + 1 Fs = PLL_AUDIO/[(TX_TATIO + 1)*64*2]
3:2	R/W	0x0	TX_SF TX Sample Format 00: 16 bits 01: 20 bits 10: 24 bits 11: Reserved
1	R/W	0x0	TX_CHM CHSTMODE 0: Channel status A and B set to 0 1: Channel status A and B generated from TX_CHSTA
0	R/W	0x0	TXEN TX Enable 0: Disable 1: Enable

17.3.8.3 0x0008 OWA RX Configure Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: OWA_RX_CFIG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: OWA_RX_CFIG
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	RX_CDR_MANUAL RX CDR mode 0: Automatic (in this mode, RX_CDR_PREAMBLE does not need to be configured) 1: Manual (in this mode, RX_CDR_PREAMBLE needs to be configured)
4	R	0x0	RX_LOCK_FLAG RX Lock Flag 0: Unlock 1: Lock
3	R/W	0x0	RX_CHST_SRC RX Channel State Source Select 0: RX_CH_STA register holds status from Channel A 1: RX_CH_STA register holds status from Channel B
2	R/W	0x0	RX_CDR_PREAMBLE RX channel CDR Preamble Type 0: support CDR from preamble X (11100010) 1: support CDR from preamble X (00011101)
1	R/W	0x0	CHST_CP Channel Status Capture 0: Idle or Capture End 1: Capture Channel Status Start Note: a) The field must be set to 1 at each operation (such as recording). b) When set to 1, the channel status information is capturing, the bit will clear to 0 after captured.
0	R/W	0x0	RXEN 0: Disabled 1: Enabled

17.3.8.4 0x000C OWA Interrupt Status Register (Default Value: 0x0000_0010)

Offset: 0x000C			Register Name: OWA_ISTA
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x000C			Register Name: OWA_ISTA
Bit	Read/Write	Default/Hex	Description
18	R/W1C	0x0	RX_LOCK_INT RX Lock Interrupt 0: No Pending IRQ 1: RX Lock Pending Interrupt (RX_LOCK_FLAG turns from 0 to 1) Write 1 to clear this interrupt.
17	R/W1C	0x0	RX_UNLOCK_INT RX Unlock Pending Interrupt 0: No Pending IRQ 1: RX Unlock Pending Interrupt (RX_LOCK_FLAG turns from 0 to 1) Write 1 to clear this interrupt.
16	R/W1C	0x0	RX_PARERRI_INT RX Parity Error Pending Interrupt 0: No Pending IRQ 1: RX Parity Error Pending Interrupt Write 1 to clear this interrupt.
15:7	/	/	/
6	R/W1C	0x0	TXU_INT TX FIFO Underrun Pending Interrupt 0: No Pending IRQ 1: TXFIFO Underrun Pending Interrupt Writing 1 to clear this interrupt.
5	R/W1C	0x0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: TXFIFO Overrun Pending Interrupt Writing 1 to clear this interrupt.
4	R/W1C	0x1	TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Write 1 to clear this interrupt or automatically clear if the interrupt condition fails.
3:2	/	/	/
1	R/W1C	0x0	RXO_INT RXFIFO Overrun Pending Interrupt 0: RXFIFO Overrun Pending Write 1 to clear this interrupt.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x000C			Register Name: OWA_ISTA
Bit	Read/Write	Default/Hex	Description
0	R/W1C	0x0	RXA_INT RXFIFO Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ Write 1 to clear this interrupt or automatically clear if the interrupt condition fails.

17.3.8.5 0x0010 OWA RXFIFO Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: OWA_RXFIFO
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RX_DATA The host can get one sample by reading this register. The first is A channel data and the latter is B channel data.

17.3.8.6 0x0014 OWA FIFO Control Register (Default Value: 0x0004_0200)

Offset: 0x0014			Register Name: OWA_FCTL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HUB_EN Audio Hub Enable The bit will take effect only when the TXEN is set to 1. I2S0/I2S1/I2S2/I2S3/I2S4/OWA TXFIFO Hub Enable. 0: Disable 1: Enable
30	R/W1C	0x0	FTX Write 1 to flush TXFIFO, self-clear to 0 .
29	R/W1C	0x0	FRX Write 1 to flush RXFIFO, self-clear to 0 .
28:22	/	/	/
21	R/W	0x0	RX_SYNC_EN_START The bit will take effect only when the RX_SYNC_EN is set to 1. I2S0/I2S1/I2S2/I2S3/I2S4/OWA RX Synchronize Enable Start. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: OWA_FCTL
Bit	Read/Write	Default/Hex	Description
20	R/W	0x0	RX_SYNC_EN OWA RX Synchronize Enable 0: Disable 1: Enable
19:12	R/W	0x40	TXTL TX FIFO Empty Trigger Level Interrupt and DMA request trigger level for TX FIFO normal condition. Trigger Level = TXTL
11	/	/	/
10:4	R/W	0x20	RXTL RX FIFO Trigger Level Interrupt and DMA request trigger level for RX FIFO normal condition. Trigger Level = RXTL + 1
3	/	/	/
2	R/W	0x0	TXIM TXFIFO Input Mode (Mode 0, 1) 0: Valid data at the MSB of TXFIFO Register 1: Valid data at the LSB of TXFIFO Register Example for 20-bit transmitted audio sample: Mode 0: TXFIFO [23:0] = {APB_WDATA [31:12], 4 h0} Mode 1: TXFIFO[23:0] = {APB_WDATA[19:0], 4 h0}
1:0	R/W	0x0	RXOM RXFIFO Output Mode (Mode 0, 1, 2, 3) 00: Expanding 0 at LSB of RXFIFO Register 01: Expanding received sample sign bit at MSB of RXFIFO Register 10: Truncating received samples at high half-word of RXFIFO Register and low half-word of RXFIFO Register is filled by 0 . 11: Truncating received samples at low half-word of RXFIFO Register and high half-word of RXFIFO. Register is expanded by its sigh bit Mode 0: APB_RDATA [31:0] = {RXFIFO [23:0], 8 h0} Mode 1: APB_RDATA [31:0] = {8 RXFIFO [23], RXFIFO [23:0]} Mode 2: APB_RDATA [31:0] = {RXFIFO [23:8], 16 h0} Mode 3: APB_RDATA[31:0] = {16 RXFIFO[23], RXFIFO[23:8]}

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

17.3.8.7 0x0018 OWA FIFO Status Register (Default Value: 0x8080_0000)

Offset: 0x0018			Register Name: OWA_FSTA
Bit	Read/Write	Default/Hex	Description
31	R	0x1	TXE TXFIFO Empty (indicate the TXFIFO is not full) 0: No room for new sample in TXFIFO 1: More than one room for new sample in TXFIFO (>= 1 Word)
30:24	/	/	/
23:16	R	0x80	TXE_CNT TXFIFO Empty Space Word Counter
15	R	0x0	RXA RXFIFO Available 0: No available data in RXFIFO 1: More than one sample in RXFIFO (>= 1 Word)
14:7	/	/	/
6:0	R	0x0	RXA_CNT RXFIFO Available Sample Word Counter

17.3.8.8 0x001C OWA Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: OWA_INT
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x0	RX_LOCKI_EN RX LOCK Interrupt Enable 0: Disable 1: Enable
17	R/W	0x0	RX_UNLOCKI_EN RX UNLOCK Interrupt Enable 0: Disable 1: Enable
16	R/W	0x0	RX_PARERRI_EN RX PARITY ERORR Interrupt Enable 0: Disable 1: Enable
15:8	/	/	/
7	R/W	0x0	TX_DRQ TXFIFO Empty DRQ Enable 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x001C			Register Name: OWA_INT
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	TXUI_EN TXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TXOI_EN TXFIFO Overrun Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	TXEI_EN TXFIFO Empty Interrupt Enable 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	RX_DRQ RXFIFO Data Available DRQ Enable When set to 1 , RXFIFO DMA Request is asserted if data is available in RXFIFO. 0: Disable 1: Enable
1	R/W	0x0	RXOI_EN RXFIFO Overrun Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RXAI_EN RXFIFO Data Available Interrupt Enable 0: Disable 1: Enable

17.3.8.9 0x0020 OWA TX FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: OWA_TXFIFO
Bit	Read/Write	Default/Hex	Description
31:0	W	0x0	TX_DATA Transmitting A, B channel data should be written by this register one by one. The first is A channel data, and the latter is B channel data.

17.3.8.10 0x0024 OWA TX Counter Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: OWA_TX_CNT
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0024			Register Name: OWA_TX_CNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial value at any time. After being updated by the initial value, the counter register should count on the base of this initial value.

17.3.8.11 0x0028 OWA RX Counter Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: OWA_RX_CNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Codec, the RX sample counter register increases by one. The RX counter register can be set to any initial value at any time. After being updated by the initial value, the counter register should count on the base of this value.

17.3.8.12 0x002C OWA TX Channel Status Register0 (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: OWA_TX_CHSTA0
Bit	Read/Write	Default/Hex	Description
31: 30	/	/	/
29:28	R/W	0x0	CA Clock Accuracy 00: Level 2 01: Level 1 10: Level 3 11: Not matched

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x002C			Register Name: OWA_TX_CHSTA0
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0x0	FREQ Sampling Frequency 0000: 44.1 kHz 0001: Not indicated 0010: 48 kHz 0011: 32 kHz 0100: 22.05 kHz 0101: Reserved 0110: 24 kHz 0111: Reserved 1000: Reserved 1001: 768 kHz 1010: 96 kHz 1011: Reserved 1100: 176.4 kHz 1101: Reserved 1110: 192 kHz 1111: Reserved
23:20	R/W	0x0	CN Channel Number
19:16	R/W	0x0	SN Source Number
15:8	R/W	0x0	CC Category Code Indicates the kind of equipment that generates the digital audio interface signal.
7:6	R/W	0x0	MODE Mode 00: Default Mode 01 to 11: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x002C			Register Name: OWA_TX_CHSTA0
Bit	Read/Write	Default/Hex	Description
5:3	R/W	0x0	EMP Emphasis Additional format information For bit 1 = 0 , Linear PCM audio mode: 000: 2 audio channels without pre-emphasis 001: 2 audio channels with 50 μs/15 μs pre-emphasis 010: Reserved (for 2 audio channels with pre-emphasis) 011: Reserved (for 2 audio channels with pre-emphasis) 100 to 111: Reserved For bit 1 = 1 , other than Linear PCM applications: 000: Default state 001 to 111: Reserved
2	R/W	0x0	CP Copyright 0: Copyright is asserted 1: No copyright is asserted
1	R/W	0x0	TYPE Audio Data Type 0: Linear PCM samples 1: Non-linear PCM audio
0	R/W	0x0	PRO Application Type 0: Consumer application 1: Professional application This bit must be fixed to 0 .

17.3.8.13 0x0030 OWA TX Channel Status Register1 (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: OWA_TX_CHSTA1
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:8	R/W	0x0	CGMS_A 00: Copying is permitted without restriction 01: One generation of copies may be made 10: Condition not be used 11: No copying is permitted

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0030			Register Name: OWA_TX_CHSTA1
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0x0	ORIG_FREQ Original Sampling Frequency 0000: Not indicated 0001: 192 kHz 0010: 12 kHz 0011: 176.4 kHz 0100: Reserved 0101: 96 kHz 0110: 8 kHz 0111: 88.2 kHz 1000: 16 kHz 1001: 24 kHz 1010: 11.025 kHz 1011: 22.05 kHz 1100: 32 kHz 1101: 48 kHz 1110: Reserved 1111: 44.1 kHz
3:1	R/W	0x0	WL Sample Word Length For bit 0 = 0 : 000: Not indicated 001: 16 bits 010: 18 bits 100: 19 bits 101: 20 bits 110: 17 bits 111: Reserved For bit 0 = 1 : 000: Not indicated 001: 20 bits 010: 22 bits 100: 23 bits 101: 24 bits 110: 21 bits 111: Reserved
0	R/W	0x0	MWL Max Word Length 0: Maximum audio sample word length is 20 bits 1: Maximum audio sample word length is 24 bits

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

17.3.8.14 0x0034 OWA RX Channel Status Register0 (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: OWA_RX_CHSTA0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R	0x0	CA Clock Accuracy 00: Level 2 01: Level 1 10: Level 3 11: Not Matched
27:24	R	0x0	FREQ Sampling Frequency 0000: 44.1 kHz 0001: Not Indicated 0010: 48 kHz 0011: 32 kHz 0100: 22.05 kHz 0101: Reserved 0110: 24 kHz 0111: Reserved 1000: Reserved 1001: 768 kHz 1010: 96 kHz 1011: Reserved 1100: 176.4 kHz 1101: Reserved 1110: 192 kHz 1111: Reserved
23:20	R	0x0	CN Channel Number
19:16	R	0x0	SN Source Number
15:8	R	0x0	CC Category Code Indicates the Kind of Equipment that Generates the digital audio interface Signal.
7:6	R	0x0	MODE Mode 00: Default mode 01 to 11: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0034			Register Name: OWA_RX_CHSTA0
Bit	Read/Write	Default/Hex	Description
5:3	R	0x0	EMP Emphasis Additional Format Information For bit 1 = 0 , Linear PCM Audio mode: 000: 2 Audio channels without pre-emphasis 001: 2 Audio channels with 50 μs/15 μs pre-emphasis 010: Reserved (For 2 Audio channels with pre-emphasis) 011: Reserved (For 2 Audio channels with pre-emphasis) 100 to 111: Reserved For bit 1 = 1 , Other than Linear PCM applications: 000: Default state 001 to 111: Reserved
2	R	0x0	CP Copyright 0: Copyright is asserted 1: No Copyright is asserted
1	R	0x0	TYPE Audio Data Type 0: Linear PCM samples 1: Non-linear PCM audio
0	R	0x0	PRO Application Type 0: Consumer application 1: Professional application

17.3.8.15 0x0038 OWA RX Channel Status Register1 (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: OWA_RX_CHSTA1
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:8	R	0x0	CGMS_A 00: Copying is permitted without restriction 01: One generation of copies may be made 10: Condition is not used 11: No copying is permitted

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0038			Register Name: OWA_RX_CHSTA1
Bit	Read/Write	Default/Hex	Description
7:4	R	0x0	ORIG_FREQ Original Sampling Frequency 0000: Not indicated 0001: 192 kHz 0010: 12 kHz 0011: 176.4 kHz 0100: Reserved 0101: 96 kHz 0110: 8 kHz 0111: 88.2 kHz 1000: 16 kHz 1001: 24 kHz 1010: 11.025 kHz 1011: 22.05 kHz 1100: 32 kHz 1101: 48 kHz 1110: Reserved 1111: 44.1 kHz
3:1	R	0x0	WL Sample Word Length For bit 0 = 0 : 000: Not indicated 001: 16 bits 010: 18 bits 100: 19 bits 101: 20 bits 110: 17 bits 111: Reserved For bit 0 = 1 : 000: Not indicated 001: 20 bits 010: 22 bits 100: 23 bits 101: 24 bits 110: 21 bits 111: Reserved
0	R	0x0	MWL Max Word Length 0: Maximum Audio sample word length is 20 bits 1: Maximum Audio sample word length is 24 bits

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

17.3.8.16 0x003C OWA Insert Redetect Control Register (Default Value: 0x0000_0180)

Offset: 0x003C			Register Name: OWA_INSERT_REDET_CTL
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x1	INSERT_REDET_MONITOR_ENABLE Insert Re-detect Monitor Enable 0: Disable 1: Enable
7:0	R/W	0x80	INSERT_REDET_MONITOR_LENGTH Insert Re-detect Monitor Length The unit is one 32KHz cycle. It is used to detect what time the rx insert will restart when there is no toggle in rerial_in.

17.3.8.17 0x0040 OWA Expand Control Register (Default Value: 0x0000_000F)

Offset: 0x0040			Register Name: OWA_EXP_CTL
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R/W	0x0	BURST_DATAOUT_SELECT Burst data output select 0: Burst preamble and payload 1: Burst payload
29:16	R/W	0x0	REPEAT_PERIOD_OF_FR_NUM The number for the repetition period of the burst frame Configure this field according to the type of RX data. A mismatch between the configuration data and the received data will result in an error interrupt.
15	R/W	0x0	UNIT_SELECT Unit Select Configure this field according to the RX data type 0: In the units of 16-bit 1: In the units of 2-byte
14	R/W	0x0	OWA_RX_MODE_MAN OWA RX Protocol Select 0: IEC60958 1: IEC61937

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0040			Register Name: OWA_EXP_CTL
Bit	Read/Write	Default/Hex	Description
13	R/W	0x0	OWA_RX_MODE OWA RX Mode Select 0: Manual Ctrl. It is configured by OWA RX_MODE_MAN. 1: Auto Ctrl. It is configured by the channel status values resolved by hardware.
12	R/W	0x0	AUDIO_DATA_BITORDER_EN Audio Data Bitorder Enable 0: The audio data received by RX is stored directly into FIFO 1: The high and low bits of the audio data received by RX are reversed and then stored into FIFO
11	R/W	0x0	DATA_LENGTH_BITORDER_EN Data Length Bitorder Enable 0: The received PD data is used as the length of the valid audio data. 1: The high and low bits of the received PD data are reversed and then used as the length of valid audio data.
10	R/W	0x0	DATA_TYPE_BITORDER_EN Data Type Bitorder Enable 0: The received PC data is used as the data length of the valid audio. 1: The high and low bits of the received PC data are reversed and then used as the length of the valid audio data.
9	R/W	0x0	SYNCW_BITORDER_EN 0: Pa/Pb is the sync code of audio data. 1: The Pa/Pb whose high and low bits are reversed is the sync code of audio data.
8	R/W	0x0	INSERT_DETECTION_ENABLE Insert Detection Enable 0: Disable 1: Enable
7:0	R/W	0x0F	INSERT_DETECTION_NUM Insert Detection Number Configure how many jumping edges are detected to generate an insertion interrupt

17.3.8.18 0x0044 OWA Expand Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0044	Register Name: OWA_EXP_ISTA

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	PD_CHANGE_INT_EN PD_LENGTH_CHANGE Interrupt Enable 0: Disable 1: Enable
23	R/W	0x0	PC_PAUSE_STOP_INT_EN PC_PAUSE_BURSTS_STOP Interrupt Enable 0: Disable 1: Enable
22	R/W	0x0	PC_BITSTRM_CHANGE_INT_EN PC_BITSTREAM_CHANGE Interrupt Enable 0: Disable 1: Enable
21	R/W	0x0	PC_ERR_FLAG_INT_EN PC_ERROR_FLAG Interrupt Enable 0: Disable 1: Enable
20	R/W	0x0	PC_DTYPE_CHANGE_INT_EN PC_DATATYPE_CHANGE Interrupt Enable 0: Disable 1: Enable
19	R/W	0x0	RPDB_ERR_INT_EN RPDB_ERROR Interrupt Enable 0: Disable 1: Enable
18	R/W	0x0	PCPD_CAP_INT_EN PCPD_CAP Interrupt Enable 0: Disable 1: Enable
17	R/W	0x0	PAPB_CAP_INT_EN PAPB_CAP Interrupt Enable 0: Disable 1: Enable
16	R/W	0x0	INSERT_INT_EN INSERT Interrupt Enable 0: Disable 1: Enable
15:9	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

8	R/W1C	0x0	PD_CHANGE_INT PD CHANGE INT 0: No Pending IRQ 1: PD Data length information is changed. (except Pause/Null data burst type) Write 1 to clear this interrupt.
7	R/W1C	0x0	PC_PAUSE_STOP_INT Audio bitstream is interrupted. When stopped, the interface becomes idle. 0: No Pending IRQ 1: PC Pause burst Stop, frame sequence discontinued. Transmitters may optionally use the STOP value to indicate that the transmission of the current encoded Write 1 to clear this interrupt.
6	R/W1C	0x0	PC_BITSTRM_CHANGE_INT PC BITSTRM CHANGE INT 0: No Pending IRQ 1: PC Bitstream Number is change. Bitstream Number indicates which bitstream the data burst belongs. (except Pause/Null data bursts type) Write 1 to clear this interrupt.
5	R/W1C	0x0	PC_ERR_FLAG_INT PC ERR FLAG INT 0: No Pending IRQ 1: PC Error-flag is available to indicate if the contents of the data-burst contain data errors (except Pause/Null data bursts type). The using of this bit by receivers is optional. Write 1 to clear this interrupt.
4	R/W1C	0x0	PC_DTYPE_CHANGE_INT PC DTYPE CHANGE INT 0: No Pending IRQ 1: PC Datatype (except Pause/Null data type) information is changed. Write 1 to clear this interrupt.
3	R/W1C	0x0	RPDB_ERR_INT RPDB ERR INT 0: No Pending IRQ 1: Hardware counts the repetition period of the burst frame is different from the register configuration number. Write 1 to clear this interrupt.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

2	R/W1C	0x0	PCPD_CAP_INT PCPD CAP INT 0: No Pending IRQ 1: IEC61937 mode captures PC and PD Write 1 to clear this interrupt.
1	R/W1C	0x0	PAPB_CAP_INT PAPB CAP INT 0: No Pending IRQ 1: IEC61937 mode captures PA and PB Write 1 to clear this interrupt.
0	R/W1C	0x0	INSERT_INT INSERT INT 0: No Pending IRQ 1: OWA RX detects device insertion Write 1 to clear this interrupt.

17.3.8.19 0x0048 OWA Expand Information Register 0 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: OWA_EXP_INFO_0
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	PC_DATA PC Data information
15:0	R	0x0	PD_DATA PD Data information

17.3.8.20 0x004C OWA Expand Information Register 1 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: OWA_EXP_INFO_1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	REPET_PERIOD_OF_FR_VALUE Repetition period of the burst frame value Check whether the repetition period of the burst frame calculated by hardware is consistent with the configured.
15:0	R	0x0	SR_VALUE Sample Rate Value Read this value after RX_LOCK.

17.3.8.21 0x0050 OWA Expand Debug Register 0 (Default Value: 0x0000_0000)

Offset: 0x0050	Register Name: OWA_EXP_DBG_0

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18:16	R	0x0	IEC61937_DATA_CAP_FSM IEC61937 Data Captures State Machine 000: IDLE 001: SYNC_PA 010: SYNC_PB 011: DTYPE_PC 100: DLEN_PD 101: RX_ACTIVE
15:0	R	0x0	DATA_CAP_NUM Remains Data Counter Value See the value of the sampled valid data in real time.

17.3.8.22 0x0054 OWA Expand Debug Register 1 (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: OWA_EXP_DBG_1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	REPET_PERIOD_OF_FR_CNT Repetition period of the burst frame counter See the value of repetition period counter in real time.
15:0	R	0x0	SR_CNT Sample Rate Counter See the value of audio sample ratio in real time.

17.3.8.23 0x005C OWA Expand CDR Debug Register (Default Value: 0x0000_07FF)

Offset: 0x005C			Register Name: OWA_EXP_CDR_DBG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R	0x0	CDR_STATE State of CDR. 0: idle 1: cnt_start
27	/	/	/
26:16	R	0x000	PERIOD_MAX Max period of RX recovery clock. Take one OWA_rx sys_clock cycle as unit.
15:11	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x005C			Register Name: OWA_EXP_CDR_DBG
Bit	Read/Write	Default/Hex	Description
10:0	R	0x7FF	PERIOD_MIN Min period of RX recovery clock. Take one OWA_rx sys_clock cycle as unit.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18 Peripherals

18.1 GMAC

18.1.1 Overview

The Gigabit Medium Access Controller (GMAC) enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2015 standard.

The GMAC has the following features:

- Supports 10/100/1000Mbps data transfer rates
- Supports RMII/RGMII PHY interface
- AMBA4 AXI master interface with 64bit data transfer
- Supports both full-duplex and half-duplex operation
- Full-duplex flow control
- IEEE 1588-2008 for precision networked clock synchronization. Supports Ethernet packet timestamping as described in IEEE 1588-2002 and IEEE 1588-2008
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Source Address field and VLAN insertion or replacement, Double VLAN
- Supports transmitting TCP/IP Checksum Offload
- Supports a variety of flexible address filtering modes, including Hash filter function
- Optimization for packet-oriented DMA transfers with frame delimiters
- Supports linked-list descriptor list structure
- Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention: each descriptor can transfer up to 32 KB of data
- Comprehensive status reporting for normal operation and transfers with errors
- Supports 4KB TXFIFO for transmission packets and 8KB RXFIFO for reception packets
- Supports 16Descriptors Descriptor Pre-fetch cache for TXDMA and RX DMA
- Programmable interrupt options for different operational conditions
- Supports MDIO Interface for PHY device configuration and management
- Configurable big-endian and little-endian mode for Transmit and Receive paths
- Supports statistics on the received and transmitted packets
- Supports Split Header

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- Supports Power Management Module (PMT) with remote wake-up packet and magic packet processing options
- Supports Energy Efficient Ethernet (EEE)

18.1.2 Block Diagram

The following figure shows the block diagram of GMAC.

Figure 18-1 GMAC Block Diagram

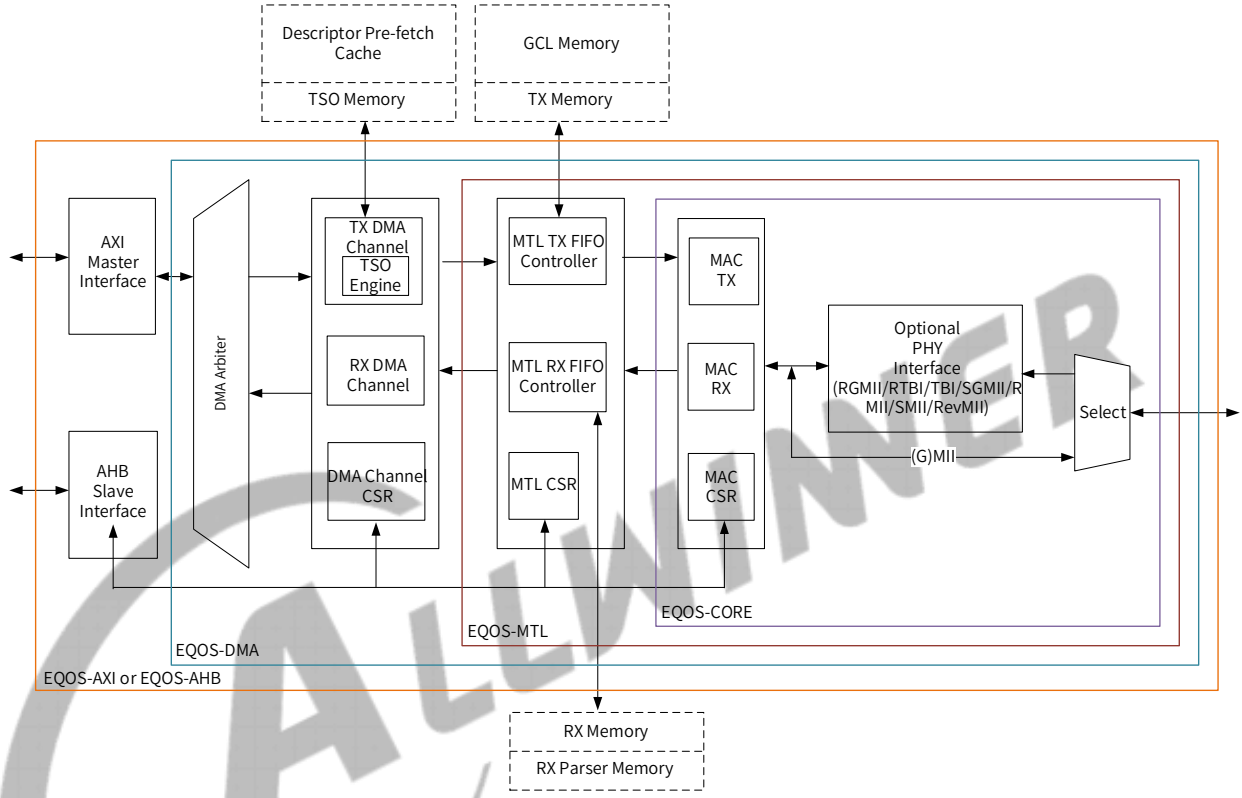


Table 18-1 GMAC Sub-blocks

Sub-blocks	Description
AHB Master Interface	The DMA controller interfaces with the application through the AMBA4 AXI interface. The AMBA4 AXI bus interface provides the characteristics to support highly-effective data traffic throughput.
AHB Slave Interface	The 32-bit AHB slave interface provides access to the DMA, MTL, and MAC CSR space.
PHY interface	The PHY interface can be configured to RGMII and RMII.
DMA	A DMA Channel has independent Transmit (TX) and Receive (RX) engines, and a CSR space. The TX engine transfers data from the system memory to the device port (MTL), whereas the RX engine transfers data from the device port to the system memory. The DMA engine uses descriptors to efficiently move data from source to destination with minimal application CPU intervention.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Sub-blocks	Description
MTL	The MAC Transaction Layer (MTL) provides the FIFO memory Interface to buffer and regulate the packets between the application system memory and the MAC. It also enables the data to be transferred between the application clock and MAC clock domains. One MTL queue. The MTL layer has two data paths: Transmit path and Receive Path.
MAC	Media Access Controller. The MAC supports many interfaces towards the PHY chip.

18.1.3 Clock Sources

The following table describes the clock sources of GMAC. For clock setting, configurations, and gating information, refer to the section Clock Controller Unit (CCU).

Module	Clock Sources	Description
GMAC_PTP	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.
	PERI0_200M	Its frequency is 200 MHz by default.
	DCXO	The external high-frequency crystal oscillator. Its frequency is 26 MHz.
GMAC0_PHY	PERI0_150M	Its frequency is 150 MHz by default.

18.1.4 External Signals

The following table describes the pin list of GMAC.

Table 18-2 GMAC External Signals

Signal Name	Description	Type
RGMII0-RXCK/RMII0-NULL	RGMII0 Receive Clock	I
RGMII0-TXCK/RMII0-TXCK	RGMII0/RMII0 50MHz Reference Clock For RGMII, IO type is output; For RMII, IO type is input.	I/O
RGMII0-CLKIN/RMII0-RXER	RGMII 125M Reference Clock Input/RMII0 Receive Error	I
RGMII0-RXCTL/RMII0-CRS-DV	RGMII0 Receive Control/RMII0 Carrier Sense Receive Data Valid	I
RGMII0-TXCTL/RMII0-TXEN	RGMII0 Transmit Control/RMII0 Transmit Enable	O
RGMII0-MDC	RGMII0 Management Data Clock	O
RGMII0-MDIO	RGMII0 Management Data Input/Output	I/O
RGMII0-EPHY-25/50M	GMAC PHY 25MHz or 50MHz Clock Output	O
RGMII0-RXD0/RMII0-RXD0	RGMII0/RMII0 Receive Data 0	I
RGMII0-RXD1/RMII0-RXD1	RGMII0/RMII0 Receive Data 1	I
RGMII0-RXD2/RMII0-NULL	RGMII0 Receive Data 2	I
RGMII0-RXD3/RMII0-NULL	RGMII0 Receive Data 3	I

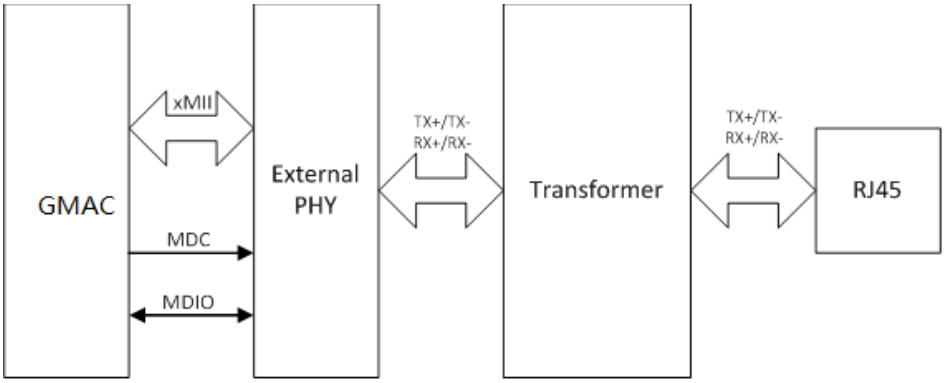
Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Signal Name	Description	Type
RGMII0-TXD0/RMII0-TXD0	RGMII0/RMII0 Transmit Data 0	O
RGMII0-TXD1/RMII0-TXD1	RGMII0/RMII0 Transmit Data 1	O
RGMII0-TXD2/RMII0-NULL	RGMII0 Transmit Data2	O
RGMII0-TXD3/RMII0-NULL	RGMII0 Transmit Data3	O
RGMII0-RXCK/RMII0-NULL	RGMII0 Receive Clock	I

18.1.5 Functional Description

The following table shows the GMAC Typical Application.

Figure 18-2 GMAC Typical Application



18.1.6 Register List

Module Name	Base Address
GMAC0	0x04508000

Register Name	Offset	Description
GMAC_CFG_REG	0x0000	GMAC Configuration Register
GMAC_PTP_TIMESTAMP_LOW_REG	0x0040	GMAC Captured Timestamp Low Bit Register
GMAC_PTP_TIMESTAMP_HIGH_REG	0x0048	GMAC Captured Timestamp High Bit Register
GMAC_STAT_INT_REG	0x004C	GMAC Low-power Interrupt Status Register
GMAC_CLK_GATE_CFG_REG	0x0080	GMAC Clock Gate Configuration Register

18.1.7 Register Description

18.1.7.1 0x0000 GMAC Configuration Register (Default Value: 0x0000_8000)

Offset: 0x0000	Register Name: GMAC_CFG_REG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:16	R/W	0x0	ETXDC_H Configure GMAC Transmit Clock Delay Chain high 2bits.
15	R/W	0x1	PHY_SELECT 0: External PHY 1: Internal PHY It is internal PHY by default. To select external PHY, configuration is needed.
14	R/W	0x0	Endianness_mode 0: little 1: big
13	R/W	0x0	RMII_EN RMII Enable. 0: Disable RMII Module 1: Enable RMII Module When this bit is enabled, RGMII interface will be disabled (This means bit13 is prior to bit2).
12:10	R/W	0x0	ETXDC_L Configure GMAC Transmit Clock Delay Chain low 3bits.
9:5	R/W	0x0	ERXDC Configure GMAC Receive Clock Delay Chain.
4	R/W	0x0	ERXIE Enable GMAC Receive Clock Invertor. 0: Disable 1: Enable
3	R/W	0x0	ETXIE Enable GMAC Transmit Clock Invertor 0: Disable 1: Enable
2	R/W	0x0	EPIT GMAC PHY Interface Type 0: RMII 1: RGMII
1:0	R/W	0x0	ETCS GMAC Transmit Clock Source 00: Transmit clock source for RMII 01: External transmit clock source for RGMII(clkin-125MHz) 10: Internal transmit clock source for RGMII(rxclk) 11: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.1.7.2 0x0040 GMAC Captured Timestamp Low Bit Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: GMAC_PTP_TIMESTAMP_LOW_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PTP_TIMESTAMP_L ptp_timestamp_low

18.1.7.3 0x0044 GMAC Captured Timestamp High Bit Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: GMAC_PTP_TIMESTAMP_HIGH_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PTP_TIMESTAMP_H ptp_timestamp_high

18.1.7.4 0x004C GMAC Low-power Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: GMAC_STAT_INT_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R	0x0	PWR_DOWN_ACK Power Down Acknowledge This signal is acknowledgment to start the power-down sequence.
3	R	0x0	SBD_TX_CLK_GATING LPI Tx Clock Gating Control. This signal is high after the MAC enters the Tx LPI mode. You can use this signal to control the Tx clock gating.
2	/	/	/
1	R	0x0	LPI_INT This signal is high when the MAC receiver exits the LPI state. You can use the lpi_intr_o signal to trigger the external clock-gating circuitry to restore the application clock to the MAC. If you do not want to gate-off the application clock during the Rx LPI state, you can leave the lpi_intr_o signal unconnected.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x004C			Register Name: GMAC_STAT_INT_REG
Bit	Read/Write	Default/Hex	Description
0	R	0x0	PMT_INT PMT Interrupt This signal indicates an interrupt event in the optional PMT module of the DWC_ether_qos core. You can use it to wake the system from the Sleep mode. This interrupt has no masking control.

18.1.7.5 0x0080 GMAC Clock Gate Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: GMAC_CLK_GATE_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	RX_CLK_GATING rx_clk_gating control 0: clk is on 1: clk is off
6	R/W	0x0	PTP_REFCLK_GATING ptp_refclk_gating control 0: clk is on 1: clk is off
5	R/W	0x0	CSR_CLK_GATING registers_clk_gating control 0: clk is on 1: clk is off
4	R/W	0x0	TX_CLK_GATING tx_clk_gating control 0: clk is on 1: clk is off
3	R/W	0x0	APP_CLK_GATING Application_clk_gating control 0: clk is on 1: clk is off
2:0	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.2 SerDes Subsystem

18.2.1 Overview

The SERDES is responsible for the data input/output through the high-speed interfaces. It integrates a PCIe3.0 DM controller, a USB3.1 GEN2 DRD controller, COMB0/1_PHY_SERDES, a AUX_HPD_PHY designed for DP, and a USB2.0 PHY.

The SERDES have the following features.

COMB0_PHY_ SERDES

- Supports PIPE interface mode
  - USB3.1 SS and SS+, up to 10 Gbps
- Supports Raw SerDes (or PMA direct connect) interface mode
  - DisplayPort Tx (RBR, HBR, HBR2)
  - embedded DisplayPort Tx (UI_Rate_1-UI_Rate_8), up to 5.4 Gbps
- Supports up to 4 lanes
- Supports single protocol and independent multi links
  - Up to 2 USB3.1 Links
  - Up to 2 DP/eDP TX Links
- Supports synchronous output of dual protocol and TYPE-C port connection
  - 1 USB3.1 Links + 1 DP/eDP Tx link
- PHY interface is compatible with PIPE revision 4.4.1
- Take the externally input differential clock as PHY reference clock
- Take internal oscillator as PHY reference clock and output differential clock for external devices
- Dual on-chip PLLs receive a wide range of reference clocks.

COMB1_PHY_SERDES

- Supports PIPE interface mode
  - PCIe Gen 1, 2 and 3, up to 8Gbps.
  - USB3.1 SS and SS+, up to 10Gbps.
- Supports up to 1 Lane
- PHY interface is compatible with PIPE revision 4.4.1
- Supports PCIe L1 PM Substates with CLKREQ
- Take the externally input differential clock as PHY reference clock

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- Take internal oscillator as PHY reference clock and output differential clock for external devices
- Dual on-chip PLLs receive a wide range of reference clocks

USB2.0 PHY

- Universal Serial Bus 2.0 physical layer connects a USB OTG controller to a USB system.
- The USB2.0 femtoPHY supports the USB2.0 480-Mbps protocol and data rate, and is backward compatible with the USB 1.1 1.5-Mbps and 12-Mbps protocol and data rates.
- USB2.0 Transceiver Macrocell Interface (UTMI + Level 3) (8-bit/60 MHz and 16-bit/30 MHz operation).
- On-chip PLL provides various clocks for USB operation, deriving from one input reference clock.
- Suspend, Resume, and Remote Wakeup mode support.

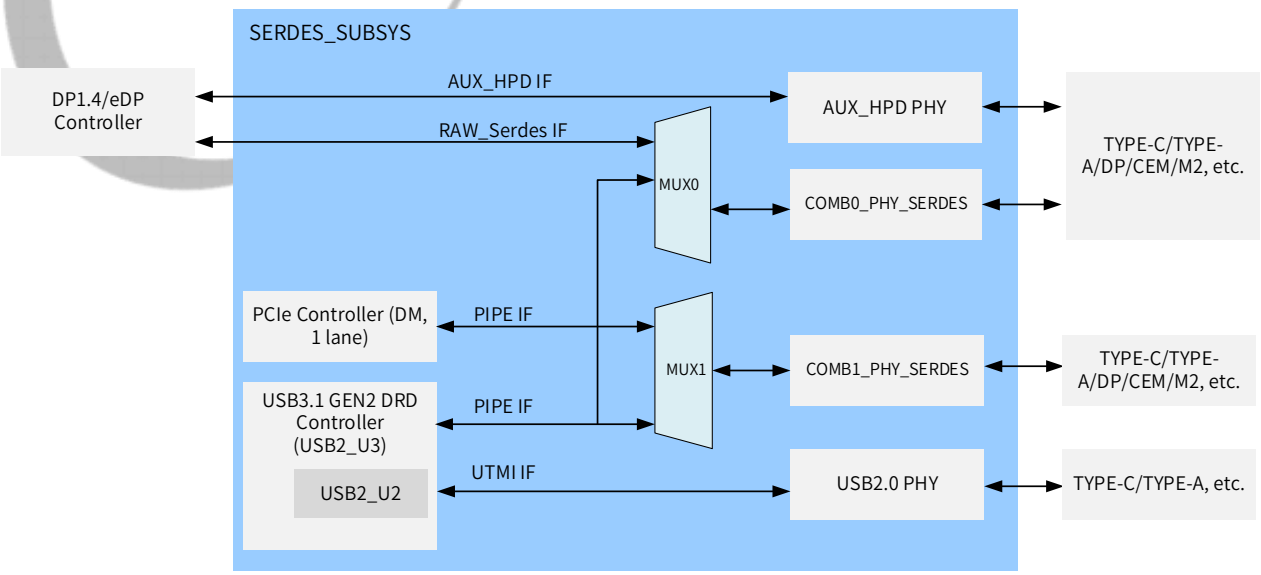
NOTE

For the features of PCIe3.0 DM controller and USB3.1 GEN2 DRD controller, please refer to the section PCIe3.0 DM and USB3.1 GEN2 DRD.

18.2.2 Block Diagram

The following figure shows the block diagram of SERDES.

Figure 18-3 SERDES Block Diagram



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.2.3 Clock Sources

The following table describes the clock sources of SERDES. For clock setting, configurations, and gating information, refer to the section CCU.

Module	Clock Sources	Description
SERDES	SYS_CLK24M	The clock is generated by the multiplexer between DCXO and PLL_REF. Its frequency is always 24 MHz.
	PERI0_600M	Its frequency is 600 MHz by default.

18.2.4 External Signals

Table 18-3 SERDES External Signals

Signal Name	Description	Type
USB2.0 PHY		
USB2-DM	USB2_U2 Data Signal DM	AI/O
USB2-DP	USB2_U2 Data Signal DP	AI/O
USB2-REXT	USB2_U2 External Reference Resistor	AI/O
VCC33-USB2-U2	3.3V Power Supply for USB2_U2 IO	P
VCC33-18-USB2-U2	3.3V/1.8V Power Supply for USB2_U2 IO	P
COMB0_PHY_SERDES		
COMB0-TX0P	COMB0 PHY Lane 0 differential Signal TX positive	AO
COMB0-TX0N	COMB0 PHY Lane 0 differential Signal TX negative	AO
COMB0-TX1P	COMB0 PHY Lane 1 differential Signal TX positive	AI/O
COMB0-TX1N	COMB0 PHY Lane 1 differential Signal TX negative	AI/O
COMB0-TX2P	COMB0 PHY Lane 2 differential Signal TX positive	AI/O
COMB0-TX2N	COMB0 PHY Lane 2 differential Signal TX negative	AI/O
COMB0-TX3P	COMB0 PHY Lane 3 differential Signal TX positive	AO
COMB0-TX3N	COMB0 PHY Lane 3 differential Signal TX negative	AO
COMB0-REF-CLKP	COMB0 PHY differential Signal reference clock positive	AI/O
COMB0-REF-CLKN	COMB0 PHY differential Signal reference clock negative	AI/O
COMB0-CMN-REXT	COMB0 PHY PMA external calibration resistor	AI/O
AVDD-C-COMB0	Clean analog power for high speed clock applications	P
AVDD-D-COMB0	Analog power for non high speed clock and digital applications	P
AVDD-H-COMB0	High voltage power for the bias and parts of the PLL	P
eDP1.4b/DP1.4 PHY		
EDP-AUXP	AUX Channel Positive Input/Output	AI/O
EDP-AUXN	AUX Channel Negative Input/Output	AI/O
AUX-HPD	AUX hot plug detect input signal	AI
AVDD-HPD-AUX	AUX HPD 3.3V high voltage powe supply	P
COMB1_PHY_SERDES		
COMB1-TX0P	COMB1 PHY Lane 0 differential Signal TX positive	AO
COMB1-TX0N	COMB1 PHY Lane 0 differential Signal TX negative	AO

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Signal Name	Description	Type
COMB1-RX0P	COMB1 PHY Lane 0 differential Signal RX positive	AI
COMB1-RX0N	COMB1 PHY Lane 0 differential Signal RX negative	AI
COMB1-REF-CLKP	COMB1 PHY differential Signal reference clock positive	AI/O
COMB1-REF-CLKN	COMB1 PHY differential Signal reference clock negative	AI/O
COMB1-REXT	COMB1 PHY PMA external calibration resistor	AI/O

18.2.5 Register List

Module Name	Base Address
SERDES_SUBSYS_APP	0x06C00000

Register Name	Offset	Description
SUBSYS_PCIE_BGR	0x0004	SUBSYS PCIE Bus Gating Reset Register
SUBSYS_USB3P1_BGR	0x0008	SUBSYS USB3.1 Bus Gating Reset Register
SUBSYS_PCIE_ITS_TAGT_ADDR	0x0220	SUBSYS PCIE ITS TAGT ADDR Register
SUBSYS_AXI2TO1_TH	0x0300	SUBSYS AXI2TO1 Threshold Register
COMB0_PHY_PINS_LINK_CTRL0	0x1000	COMB0 PHY PINS Link Control Register0
COMB0_PHY_PINS_LINK_CTRL1	0x1004	COMB0 PHY PINS Link Control Register1
COMB0_PHY_PINS_LINK_CTRL2	0x1008	COMB0 PHY PINS Link Control Register2
COMB0_PHY_PINS_LINK_CTRL3	0x100c	COMB0 PHY PINS Link Control Register3
COMB0_PHY_PINS_LINK_STUS0	0x1900	COMB0 PHY PINS Link Status Register0
COMB0_PHY_PINS_LINK_STUS1	0x1904	COMB1 PHY PINS Link Status Register0
COMB0_PHY_PINS_LINK_STUS2	0x1908	COMB2 PHY PINS Link Status Register0
AUX_HPD_PHY_PINS_CTRL0	0x1e00	AUX_HPD PHY PINS Control Register0
AUX_HPD_PHY_PINS_CTRL1	0x1e04	AUX_HPD PHY PINS Control Register1
AUX_HPD_PHY_PINS_CTRL2	0x1e08	AUX_HPD PHY PINS Control Register2
COMB1_PHY_PINS_LINK_CTRL0	0x2000	COMB1 PHY PINS Link Control Register0
COMB1_PHY_PINS_LINK_CTRL1	0x2004	COMB1 PHY PINS Link Control Register1

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
COMB1_PHY_PINS_LINK_CTRL2	0x2008	COMB1 PHY PINS Link Control Register2
COMB1_PHY_PINS_LINK_CTRL3	0x200c	COMB1 PHY PINS Link Control Register3
COMB1_PHY_PINS_LANE0_CTRL0	0x2100	COMB1 PHY PINS Lane0 Control Register0
COMB1_PHY_PINS_LINK_STUS0	0x2900	COMB1 PHY PINS Link Status Register0
COMB1_PHY_PINS_LINK_STUS1	0x2904	COMB1 PHY PINS Link Status Register1
COMB1_PHY_PINS_LINK_STUS2	0x2908	COMB1 PHY PINS Link Status Register2
COMB1_PHY_PINS_LANE0_STUS0	0x2a00	COMB1 PHY PINS Lane0 Status Register0
DP_RAWS_TXDW_CONV_CTRL	0x6004	DP RAWS TXData Width Conversion Control Register
USB3P1_PIPE_CLK_MAP_CTRL	0x6100	USB3.1 PIPE CLK MAP Control Register
USB3P1_PIPE_RXD_MAP_CTRL	0x6104	USB3.1 PIPE RXData MAP Control Register
COMB0_PHY_RAWS_TXD_MAP_CTRL	0x6c24	COMB0 PHY RAWS TXData MAP Control Register
COMB1_PHY_PIPE_TXD_MAP_CTRL	0x6c44	COMB1 PHY PIPE TXData MAP Control Register

18.2.6 Register Description

18.2.6.1 0x0004 SUBSYS PCIE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: SUBSYS_PCIE_BGR
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x0	PCIE_SLV_ACLK_EN PCIe slave axi clock enable
17	R/W	0x0	PCIE_MST_ACLK_EN PCIe master axi clock enable
16	R/W	0x0	PCIE_HCLK_EN PCIeahb clock enable
15:2	/	/	/
1	R/W	0x0	PCIE_PERSTN PCIE RC Optionally create the pesetn to EP/SW .
0	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.2.6.2 0x0008 SUBSYS USB3.1 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: SUBSYS_USB3P1_BGR
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21	R/W	0x0	USB3P1_USB2P0_UTMI_CLK_SEL 0: Select the UTMI CLK generated by USB2.0 PHY, which is applied in USB2.0 normal working scene within USB3.1. 1: Select the UTMI CLK generated by CCU, which is applied in USB3.1 only DRD independent working scene
20	R/W	0x0	USB3P1_ONLY_PIPE_CLK_SEL 0: Select the PIPE CLK generated by COMB0 PHY/COMB1 PHY, which is applied in USB3.1 only DRD normal working scene 1: Select the PIPE CLK generated by CCU, which is applied in USB2.0 independent working scene within USB3.1
19:18	/	/	/
17	R/W	0x0	USB3P1_ACLK_EN USB3P1 Axi clock enable
16	R/W	0x0	USB3P1_HCLK_EN USB3P1 Ahb clock enable
15:5	/	/	/
4	R/W	0x0	USB3P1_USB2P0_PHY_RSTN USB3P1 USB2P0 PHY Resetn
3:0	/	/	/

18.2.6.3 0x0220 SUBSYS PCIE ITS TAGT ADDR Register (Default Value: 0x0000_0345)

Offset: 0x0220			Register Name: SUBSYS_PCIE_ITS_TAGT_ADDR
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R/W	0x345	PCIE_ITS_TAGT_ADDR PCIe ITS Target address

18.2.6.4 0x0300 SUBSYS AXI2TO1 Threshold Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: SUBSYS_AXI2TO1_TH
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0300			Register Name: SUBSYS_AXI2TO1_TH
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0x0	USB2_AXI2TO1_AR_TH It is threshold of continuous read times when USB2(USB3.1 GEN1) is polled through AXI2TO1 Bridge. If its value is 0xf, it indicates that the continuous read times is 16.
19:16	R/W	0x0	PCIE0_AXI2TO1_AR_TH It is threshold of continuous read times when PCIe0 is polled through AXI2TO1 Bridge. If its value is 0xf, it indicates that the continuous read times is 16.
15:8	/	/	/
7:4	R/W	0x0	USB2_AXI2TO1_AW_TH It is threshold of continuous write times when USB2(USB3.1 GEN1) is polled through AXI2TO1 Bridge. If its value is 0xf, it indicates that the continuous write times is 16.
3:0	R/W	0x0	PCIE0_AXI2TO1_AW_TH It is threshold of continuous write times when PCIe0 is polled through AXI2TO1 Bridge. If its value is 0xf, it indicates that the continuous write times is 16.

18.2.6.5 0x1000 COMB0 PHY PINS Link Control Register0 (Default Value: 0x0000_0000)

Offset: 0x1000			Register Name: COMB0_PHY_PINS_LINK_CTRL0
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	COMB0_PHY_TYPEC_CONN_DIR Type-C Connector direction/orientation: 0: Normal orientation of the USB Type-C connector; 1: flipped orientation. Must be a static value when phy0_reset_n is de-asserted.
11:9	/	/	/
8	R/W	0x0	COMB0_PHY_DP_LINK_RESET_N_SOFT DisplayPort link reset : Asserting this signal low will reset the DP link and its associated lanes, with the exception of the APB registers.
7:6	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1000			Register Name: COMB0_PHY_PINS_LINK_CTRL0
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	COMB0_PHY_PIPE_LINK_RESET_N_USB3P1_MASK COMB0_PHY _PIPE_LINK_RESET_N_ USB3P1 is the pipe reset output by USB3P1 to PHY0. It is valid only when PHY0_PIPE_LINK_RESET_N_USB3P1_MASK is 0 and PHY0_PIPE_LINK_RESET_N_SOFT is 1. 0: NO MASK 1: MASK
4	R/W	0x0	COMB0_PHY_PIPE_LINK_RESET_N_SOFT PIPE link reset： Asserting this signal low will reset the USB link and its associated lanes, excluding the APB registers.
3:1	/	/	/
0	R/W	0x0	COMB0_PHY_RESET_N PHY reset: Asserting this signal low will reset all PHY logic for the entire PHY with the exception of the APB registers and TAP controller. Note: Upon de-assertion, all PHY inputs must be driven as described in the PIPE specification for a PIPE reset.

18.2.6.6 0x1004 COMB0 PHY PINS Link Control Register1 (Default Value: 0x0000_0000)

Offset: 0x1004			Register Name: COMB0_PHY_PINS_LINK_CTRL1
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	COMB0_PHY_PMA_CMN_PLL1_REFCLK_SEL PMA PLL reference clock select - selects which reference clock input to be used by the associated PLL. 0: cmn_refclk_<p/m>, 1: pma_cmn_refclk_int.
23:21	/	/	/
20	R/W	0x0	COMB0_PHY_PMA_CMN_PLL0_REFCLK_SEL PMA PLL reference clock select - selects which reference clock input to be used by the associated PLL. 0: cmn_refclk_<p/m>, 1: pma_cmn_refclk_int.
19:17	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1004			Register Name: COMB0_PHY_PINS_LINK_CTRL1
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	COMB0_PHY_PMA_CMN_REFCLK_TERM_EN PMA common differential reference clock termination enable - enables/disables termination for difference reference clock input (cmn_refclk_<p/m>). Must be set before the de-assertion of apb_preset_n/phy_reset_n. 0: termination disabled 1: termination enabled
13:12	R/W	0x0	COMB0_PHY_PMA_CMN_REFCLK_DIG_DIV PMA common reference clock digital divide ratio select - Must be set before the de-assertion of apb_preset_n/ phy_reset_n. 2'b00 - Divide by 1 (set for reference clock in the 19.2 to 27 MHz range) 01: Divide by 2 (Reserved) 10: Divide by 4 (set for 100 MHz reference clock) 11: Divide by 8 (Reserved)
11:10	/	/	/
9:8	R/W	0x0	COMB0_PHY_PMA_CMN_REFCLK_INT_MODE PMA common internal reference clock mode - Sets the mode of operation for internal reference clock input. Must be set before the de-assertion of apb_preset_n/phy_reset_n. 00: Reserved 01: 100 MHz and greater reference clock 10: Reserved 11: Less than 100 MHz reference clock
7:6	/	/	/
5:4	R/W	0x0	COMB0_PHY_PMA_CMN_REFCLK_MODE PMA common differential reference clock mode – Sets the mode of operation for differential reference clock input. Must be set before the de-assertion of apb_preset_n/phy_reset_n. 00: Differential reference clock. 01: Single ended DC coupled test clock reference clock. 10: Reserved. 11: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1004			Register Name: COMB0_PHY_PINS_LINK_CTRL1
Bit	Read/Write	Default/Hex	Description
3:1	/	/	/
0	R/W	0x0	COMB0_PHY_PMA_CMN_REFCLK_DIG_SEL PMA common reference clock select - Selects the reference clock source for the digital logic between cmn_refclk_< p/m> and pma_cmn_refclk_int. Must be set before the de-assertion of apb_preset_n/phy_reset_n. 0: cmn_refclk_<p/m> 1: pma_cmn_refclk_int

18.2.6.7 0x1008 COMB0 PHY PINS Link Control Register2 (Default Value: 0x0000_0000)

Offset: 0x1008			Register Name: COMB0_PHY_PINS_LINK_CTRL2
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21	R/W	0x0	COMB0_PHY_XCVR_BSCAN_MODE_EN_SEL 1: PHY0_XCVR_BSCAN_MODE_EN_SOFT 0: PHY0_XCVR_BSCAN_MODE_EN_SYS, which is controlled by the SoC through GPIO in test mode.
20	R/W	0x0	COMB0_PHY_XCVR_BSCAN_MODE_EN_SOFT PMA Transceiver boundary scan mode enable: This signal enables boundary scan mode. The bit is valid when PHY0_XCVR_BSCAN_MODE_EN_SEL=1.
19:17	/	/	/
16	R/W	0x0	COMB0_PHY_BSCAN_EXT_SELECT PMA external boundary scan select 1: external boundaryscan interface is selected 0: internal TAP controller selected
15:5	/	/	/
6:4	R/W	0x0	COMB0_PHY_DBG_RX_RD_LANE_SEL Receiver data debug lane select 0: PHY Lane1 1: PHY Lane2 Only Lane1 and Lane2 can be Rx lanes.
3:2	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1008			Register Name: COMB0_PHY_PINS_LINK_CTRL2
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	COMB0_PHY_IDDQ_EN_SEL 1: PHY0_IDDQ_EN_SOFT 0: PHY0_IDDQ_EN_SYS, which is controlled by the SoC through GPIO in test mode.
0	R/W	0x0	COMB0_PHY_IDDQ_EN_SOFT IDDQ mode enable: When asserted high, the PMA is placed into IDDQ mode with all analog logic powered down. This bit is valid when PHY0_IDDQ_EN_SEL=1.

18.2.6.8 0x100c COMB0 PHY PINS Link Control Register3 (Default Value: 0x0000_0000)

Offset: 0x100c			Register Name: COMB0_PHY_PINS_LINK_CTRL3
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x0	COMB0_PHY_PMA_TX_ELEC_IDLE_LN_3 PMA Tx electrical idle: 1 = Tx differential output placed into electrical idle for the associated lane. 0 = transmit data. (i_phy_lane_elec_idle)
14	R/W	0x0	COMB0_PHY_PMA_TX_ELEC_IDLE_LN_2 PMA Tx electrical idle: 1 = Tx differential output placed into electrical idle for the associated lane. 0 = transmit data. (i_phy_lane_elec_idle)
13	R/W	0x0	COMB0_PHY_PMA_TX_ELEC_IDLE_LN_1 PMA Tx electrical idle: 1 = Tx differential output placed into electrical idle for the associated lane. 0 = transmit data. (i_phy_lane_elec_idle)
12	R/W	0x0	COMB0_PHY_PMA_TX_ELEC_IDLE_LN_0 PMA Tx electrical idle: 1 = Tx differential output placed into electrical idle for the associated lane. 0 = transmit data. (i_phy_lane_elec_idle)
11	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x100c			Register Name: COMB0_PHY_PINS_LINK_CTRL3
Bit	Read/Write	Default/Hex	Description
9:4	R/W	0x0	COMB0_PHY_PMA_XCVR_POWER_STATE_REQ_LN Link power state request: Used to change the DP link's power state. When the link has completed the transition to the requested power state, the requested state will be reflected on pma_xcvr_power_state_ack. 0x0: Idle 0x1: A0 - Tx/Rx active 0x2: A1 - Powerdown 1 (equivalent to USB P1) 0x4: A2 - Powerdown 2 (equivalent to USB P2) 0x8: A3 - Powerdown 3 (equivalent to USB P3) 0x10: A4 - Powerdown 4 (lowest power state) 0x20: Reserved This is a one hot encoded signal. A change in the requested state shall not occur until after the current request has been acknowledged and pma_xcvr_power_state_req has been returned to 0. Upon reset release, either A0 or A2 must be requested. (i_xcvr_pwr_state_req)
3:1	/	/	/
0	R/W	0x0	COMB0_PHY_PMA_XCVR_PLLCLK_EN_LN Link PLL clock enable: Used to cleanly turn off the data rate clock in the PMA for all lanes in the associated link. (i_xcvr_pllclk_en)

18.2.6.9 0x1900 COMB0 PHY PINS Link Status Register0 (Default Value: 0x0000_0000)

Offset: 0x1900			Register Name: COMB0_PHY_PINS_LINK_STUS0
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1900			Register Name: COMB0_PHY_PINS_LINK_STUS0
Bit	Read/Write	Default/Hex	Description
13:8	R	0x0	COMB0_PHY_LINK_POWER_STATE_ACK Link power state acknowledgement: This signal provides indication that a power state change request has completed. 0x0: Idle 0x1: A0 0x2: A1 0x4: A2 0x8: A3 0x10: Reserved This is a one hot encoded signal. Once a power state is acknowledged, the value will remain unchanged until a new power state is requested and the link has completed the transition to the new power state.
7:5	/	/	/
4	R	0x0	COMB0_PHY_LINK_CLOCK_EN_ACK Link PLL clock enable acknowledgement: Indicates whether the data rate clock in the PMA for the associated link is running or not.
3:1	/	/	/
0	R	0x0	COMB0_PHY_PMA_CMN_READY PMA common ready: 1 = PMA common is ready for operation. Used as part of Raw SerDes startup sequence and power state changes.

18.2.6.10 0x1904 COMB0 PHY PINS Link Status Register1 (Default Value: 0x0000_0000)

Offset: 0x1904			Register Name: COMB0_PHY_PINS_LINK_STUS1
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R	0x0	COMB0_PHY_DBG_RX_BIST_SYNC Rx BIST sync - asserted high upon BIST logic has synchronize with the incoming Rx data (loopback or from serial pins) and is checking for errors. (See PMA specification for further description of this signal.)
27:25	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1904			Register Name: COMB0_PHY_PINS_LINK_STUS1
Bit	Read/Write	Default/Hex	Description
24	R	0x0	COMB0_PHY_DBG_RX_BIST_ERR_TOGGLE RX BIST error toggle - toggled upon BIST logic detecting an error in the Rx data. (See PMA specification for further description of this signal.)
23:21	/	/	/
20	R	0x0	COMB0_PHY_DBG_RX_BIST_STATUS Rx BIST status - asserted high upon BIST logic detecting an error in the Rx data. (See PMA specification for further description of this signal.)
19:0	R	0x0	COMB0_PHY_DBG_RX_RD COMB0 PHY Receiver parallel data out

18.2.6.11 0x1908 COMB0 PHY PINS Link Status Register2 (Default Value: 0x0000_0000)

Offset: 0x1908			Register Name: COMB0_PHY_PINS_LINK_STUS2
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	COMB0_PHY_DTB_DATA COMB0 PHY Digital test bus data out.

18.2.6.12 0x1e00 AUX_HPD PHY PINS Control Register0 (Default Value: 0x0033_0000)

Offset: 0x1e00			Register Name: AUX_HPD_PHY_ PINS_CTRL0
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0x0	RX_HYST_LVL Hysteresis control for AUX receiver front end. 000: no hysteresis 001: 5mV 010: 10mV 011: 15mV (default) 100: 20mV 101: 25mV 110: 30mV 111: 35mV (i_auxhpd_rx_hyst_lvl)
23:21	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1e00			Register Name: AUX_HPD_PHY_ PINS_CTRL0
Bit	Read/Write	Default/Hex	Description
21:20	R/W	0x3	RX_DEGLITCH_FILTER High-frequency AUX receiver output pulse suppression control. This signal provides hysteresis in the time domain. 00: Deglitch disabled 01: Deglitch enabled 10: Increased glitch duration rejection 11: Highest glitch duration rejection (default) (i_auxhpd_rx_deglitch_filter)
19:17	/	/	/
17:16	R/W	0x3	TX SLEW AUX TX slew rate adjust. 00: rise/fall time = 620 psec 01: rise/fall time = 418 psec 10: rise/fall time = 260 psec 11: rise/fall time = 81 psec (default) (i_auxhpd_tx_slew)
13:12	R/W	0x0	BG_START_ADJ Bandgap startup circuit sense voltage adjust 00: 543.0mV 01: 558.5mV (default) 10: 574.0mV 11: Reserved (i_auxhpd_bg_start_adj)
11:10	/	/	/
9	R/W	0x0	CFG_AUX_TX_DIRECTION 0: Enable AUX RX_EN and disable AUX TX_EN 1: Enable AUX TX_EN and disable AUX RX_EN (i_aux_tx_direction)
8	R/W	0x0	CFG_AUX_EN 0: Disable AUX TX_EN and AUX RX_EN 1: Enable AUX TX_EN and AUX RX_EN based on CFG_AUX_TX_DIRECTION (i_config_aux_en)
7:6	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1e00			Register Name: AUX_HPD_PHY_ PINS_CTRL0
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	DECAP_EN_DEL Delayed decap enable signal. In combination with decap_en, used to limit inrush current on avdd when charging decoupling cap. Also serves as the enable signal for the HPD circuitry. Both decap_en and decap_en_del must be asserted high to enable HPD circuitry. (i_aux_decap_en_delayed)
4	R/W	0x0	DECAP_EN Decap enable signal. Used in combination with decap_en_del to enable decoupling capacitance on avdd. (i_aux_decap_en)
3:1	/	/	/
0	R/W	0x0	BG_EN Bandgap enable - Enables the bias currents for AUX receiver and transmitter. (i_aux_bg_en)

18.2.6.13 0x1e04 AUX_HPD PHY PINS Control Register1 (Default Value: 0x0000_000D)

Offset: 0x1e04			Register Name: AUX_HPD_PHY_ PINS_CTRL1
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R/W	0x0	RX_OFFSET_DISABLE AUX receiver common mode offset disable. Only used in loopback mode to offset common mode of receiver input diff pair. 0: AUX receiver common mode increases to cancel drop from transmitter in loopback (default). 1: No effect on AUX receiver common mode in loopback mode. (i_rx_offset_disable)
27:25	/	/	/
24	R/W	0x0	HIGHZ_EN AUX high-z enable for on-chip termination. 1 = places termination in high-z state. For mission-mode operation, drive low. Set high for IDDQ testing. (i_term_highz_en)

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1e04			Register Name: AUX_HPD_PHY_ PINS_CTRL1
Bit	Read/Write	Default/Hex	Description
23:16	R/W	0x0	One-hot encoded ATB select enable 0x1: AUX receiver diff pair source voltage. 0x2: AUX transmitter diff pair source voltage. 0x4: 25uA poly current from bandgap All other codes reserved (i_auxhpd_atbsel_onehot)
15:13	/	/	/
12:8	R/W	0x0	TX_CUR_CTRL AUX TX current for output differential pair. Adjusting this signal varies the Tx output signal voltage swing (full swing/reduced swing as set by tx_reduced_swing pin). 0x0: 195/0 mVpp ... 0xE: 367/169 mVpp (DP default) ... 0x13: 428/230 mVpp (eDP default) ... 0x1F: 553/373 mVpp (i_auxhpd_tx_cur_ctrl)
7:6	/	/	/
4:0	R/W	0xd	TERM_SEG_EN Enables output resistor segments for on-chip termination impedance. The goal is to achieve 100 ohm differential termination. 0x0: 122 ohm ... 0xD: 94 ohm (default) ... 0x1F: 71 ohm (i_auxhpd_term_seg_en)

18.2.6.14 0x1e08 AUX_HPD PHY PINS Control Register2 (Default Value: 0x0000_0000)

Offset: 0x1e08			Register Name: AUX_HPD_PHY_PINS_CTRL2
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1e08			Register Name: AUX_HPD_PHY_PINS_CTRL2
Bit	Read/Write	Default/Hex	Description
29	R/W	0x0	AUX_DATA_OUT_POLAR_SEL 0: The polarity of AUX data output to DP controller through AUX PHY is normal. 1: The polarity of AUX data output to DP controller through AUX PHY is inverted.
28	R/W	0x0	AUX_DATA_IN_POLAR_SEL 0: The polarity of AUX data input from DP controller through AUX PHY is normal. 1: The polarity of AUX data input from DP controller through AUX PHY is inverted.
27:12	/	/	/
11:8	R/W	0x0	HPD_GP_ANA (i_hpd_gp_ana)
7:5	/	/	/
4	R/W	0x0	HPD_TX_OEN (i_hpd_tx_oen)
3:1	/	/	/
0	R/W	0x0	TX_REDUCED_SWING Control for lowering AUX transmitter swing level. Used for eDP. 0: Normal transmitter swing level (DP) 1: Reduced transmitter swing level (eDP) (i_tx_reduced_swing)

18.2.6.15 0x2000 COMB1 PHY PINS Link Control Register0 (Default Value: 0x0000_0000)

Offset: 0x2000			Register Name: COMB1_PHY_PINS_LINK_CTRL0
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x2000			Register Name: COMB1_PHY_PINS_LINK_CTRL0
Bit	Read/Write	Default/Hex	Description
6:4	R/W	0x0	COMB1_PHY_LINK_CFG_LN PHY link/lane configuration. Used to map lanes to links. 0: designates a lane as a link slave. 1: designates a lane as a link master. Lanes are grouped into links from lowest lane number to highest. Adjacent slave lanes are part of multilane link down to the lowest numbered adjacent master lane. Lane 0 is always a master and thus does not require its own phy_link_cfg input. For example, for a 4 lane PHY can be configured as follows: {phy_link_cfg_ln_3, phy_link_cfg_ln_2, phy_link_cfg_ln_1} 111: 4x1 configuration (i.e. 4 independent links) 000: 1x4 configuration (i.e. single 4 lane link with lane 0 as the master lane) 010: 2x2 configuration (i.e. 2 2-lane links with lane 0 and lane 2 as the master lanes) 011: 2x1+1x2 configuration (i.e. 2 single lane links plus 1 2-lane link with lanes 0, 1 and 2 as the master lanes) 101: 2x1+1x2 configuration (with lane 0, 1 and 3 as master lanes) 110: 2x1+1x2 configuration (with lane 0, 2 and 3 as master lanes) 100: 1x3+1x1 configuration (i.e. 1 3-lane link plus 1 single lane link with lane 0 and 3 as master lanes) 001: 1x3+1x1 configuration (with lane 0 and 1 master lanes) **Note**: phy_reset_n and apb_preset_n must be asserted to modify this signal. The master lane of each link is that link's lane 0. It shall not be disabled unless all other lane's in the link are disabled. When each phy_link_cfg_ln_* = 0, the PHY is in a single-link configuration.
3:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x2000			Register Name: COMB1_PHY_PINS_LINK_CTRL0
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	COMB1_PHY_RESET_N PHY reset: Asserting this signal low will reset all PHY logic for the entire PHY with the exception of the APB registers and TAP controller. Note: Upon de-assertion, all PHY inputs must be driven as described in the PIPE specification for a PIPE reset.

18.2.6.16 0x2004 COMB1 PHY PINS Link Control Register1 (Default Value: 0x0000_0000)

Offset: 0x2004			Register Name: COMB1_PHY_PINS_LINK_CTRL1
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R/W	0x0	COMB1_PHY_EN_REFCLK PHY reference clock enable: When cmn_refclk_<p/m> is configured as a reference clock output, 1: glitch-less enable of the reference clock output. 0: glitch-less turn off reference clock output. Used in L1.x entry/exit protocol. Note: When outputting a derived reference clock from the PLL, it is recommended to drive phy_en_refclk low until the PHY has completed start-up and de-asserted pipe_l*_reset_ n for PIPE operation or asserted cmn_ready for Raw SerDes operation. The clock will not be 'good' until the PHY has completed initial start-up.
27:25	/	/	/
24	R/W	0x0	COMB1_PHY_PMA_CMN_PLL1_REFCLK_SEL PMA PLL reference clock select - selects which reference clock input to be used by the associated PLL. 0: cmn_refclk_<p/m>, 1: pma_cmn_refclk_int.
23:21	/	/	/
20	R/W	0x0	COMB1_PHY_PMA_CMN_PLL0_REFCLK_SEL PMA PLL reference clock select - selects which reference clock input to be used by the associated PLL. 0: cmn_refclk_<p/m>, 1: pma_cmn_refclk_int.
19:17	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x2004			Register Name: COMB1_PHY_PINS_LINK_CTRL1
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	COMB1_PHY_PMA_CMN_REFCLK_TERM_EN PMA common differential reference clock termination enable - enables/disables termination for difference reference clock input (cmn_refclk_<p/m>). Must be set before the de-assertion of apb_preset_n/phy_reset_n. 0: termination disabled 1: termination enabled
13:12	R/W	0x0	COMB1_PHY_PMA_CMN_REFCLK_DIG_DIV PMA common reference clock digital divide ratio select must be set before the de-assertion of apb_preset_n/ phy_reset_n. 00: Divide by 1 (set for reference clock in the 19.2 to 27 MHz range) 01: Divide by 2 (Reserved) 10: Divide by 4 (set for 100 MHz reference clock) 11: Divide by 8 (Reserved)
11:10	/	/	/
9:8	R/W	0x0	COMB1_PHY_PMA_CMN_REFCLK_INT_MODE PMA common internal reference clock mode - Sets the mode of operation for internal reference clock input. Must be set before the de-assertion of apb_preset_n/phy_reset_n. 00: Reserved 01: 100 MHz and greater reference clock 10: Reserved 11: Less than 100 MHz reference clock
7:6	/	/	/
5:4	R/W	0x0	COMB1_PHY_PMA_CMN_REFCLK_MODE PMA common differential reference clock mode – Sets the mode of operation for differential reference clock input. Must be set before the de-assertion of apb_preset_n/phy_reset_n. 00: 100 MHz and greater differential reference clock. 01: 100 MHz and greater singled ended DC coupled test reference clock. 10: Less than 100 MHz differential reference clock. 11: Less than 100 MHz single ended DC coupled test reference clock.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x2004			Register Name: COMB1_PHY_PINS_LINK_CTRL1
Bit	Read/Write	Default/Hex	Description
3:1	/	/	/
0	R/W	0x0	COMB1_PHY_PMA_CMN_REFCLK_DIG_SEL PMA common reference clock select - Selects the reference clock source for the digital logic between cmn_refclk_< p/m> and pma_cmn_refclk_int. Must be set before the de-assertion of apb_preset_n/phy_reset_n. 0: cmn_refclk_<p/m> 1: pma_cmn_refclk_int

18.2.6.17 0x2008 COMB1 PHY PINS Link Control Register2 (Default Value: 0x0000_0000)

Offset: 0x2008			Register Name: COMB1_PHY_PINS_LINK_CTRL2
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	COMB1_PHY_PMA_CMN_CLOCK_STOP_REQ Clock Stop Request: Asserting high causes all clocks in the PMA macro to stop, such that the value of all of the digital F/Fs in the PMA can be scanned out.
7:5	/	/	/
4	R/W	0x0	COMB1_PHY_PMA_SUSPEND_OVERRIDE PHY PMA common suspend override enable: 1: Disables suspending the PMA common when all links are in low power state (L1 SS, PCIe P2, USB P3, powerdown disabled, etc.). 0: PMA common will be suspended when all links are in low power state. Driving this pin high has no effect if the PMA common is already suspended or is in the process of being suspended (i.e. it will not force the PMA common to resume). It only prevents the start of suspending the PMA common. However, if this pin is de-asserted when all links are in low power state, the PMA common will then be suspended.
3:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x2008			Register Name: COMB1_PHY_PINS_LINK_CTRL2
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	COMB1_PHY_PMA_CMN_EXT_REFCLK_DETECTED_CFG External reference clock active detection configuration: 1: Perform an external reference clock active detection operation upon de-assertion of apb_preset_n 0: Do not perform detection operation upon de-assertion of apb_preset_n

18.2.6.18 0x200c COMB1 PHY PINS Link Control Register3 (Default Value: 0x0000_0000)

Offset: 0x200c			Register Name: COMB1_PHY_PINS_LINK_CTRL3
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20	R/W	0x0	COMB1_PHY_XCVR_BSCAN_MODE_EN PMA Transceiver boundary scan mode enable: This signal enables boundary scan mode.
19:17	/	/	/
16	R/W	0x0	COMB1_PHY_BSCAN_EXT_SELECT PMA external boundary scan select (1 = external boundary scan interface is selected, 0 = internal TAP controller selected)
15:13	/	/	/
12:8	R/W	0x0	COMB1_PHY_DTB_MUX_SEL Digital test bus MUX select.
7:6	/	/	/
5:4	R/W	0x0	COMB1_PHY_DBG_RX_RD_LANE_SEL Receiver data debug lane select
3:2	/	/	/
1	R/W	0x0	COMB1_PHY_IDDQ_EN_SEL 1: COMB1_PHY_IDDQ_EN, which is controlled by the serdes top system. 0: COMB1_PHY_IDDQ_EN_SYS, which is controlled by the SoC through GPIO in test mode.
0	R/W	0x0	COMB1_PHY_IDDQ_EN IDDQ mode enable: When asserted high, the PMA is placed into IDDQ mode with all analog logic powered down.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.2.6.19 0x2100 COMB1 PHY PINS Lane0 Control Register0 (Default Value: 0x0000_0000)

Offset: 0x2100			Register Name: COMB1_PHY_PINS_LANE0_CTRL0
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	COMB1_PHY_L00_ENT_L1_X PHY enter L1 substate (sideband) : Asserted high to direct associated PHY link to enter a L1 substate. Once asserted or de-asserted, this signal shall not change state again until after the corresponding transaction on phy_ack_l1_x. Can only be asserted high when the link is in the P1 power state. For multi-lane links, only the master lane is valid. Disabled/ignored for slave lanes (per-link/shared signal). Only valid when phy_pcie_l1_ss_sel is low. When phy_l*_pcie_l1_ss_sel is high, tie low.
15:13	/	/	/
12	R/W	0x0	COMB1_PHY_L00_PCIE_L1_SS_SEL PIPE PCIe L1 substate enable: When high, PCIe L1 SS is entered using protocol defined in PIPE 4.4 specification and described in the PHY operations chapter. PIPE-based L1 SS entry/exit uses the pipe_l*_powerdown and pipe_l*_phy_status pins instead of the phy_l*_ent_l1_x/phy_l*_ack_l1_x pins. When low, the L1 substate side-band signaling protocol is used. The sideband protocol is described in the PHY operation chapter and uses the phy_l*_ent_l1_x/phy_l*_ack_l1_x pins. For both modes, the phy_l*_rx_elec_idle_det_en and phy_l*_tx_cmn_mode_en pins are used. However, the polarity of these pins is opposite depending on the mode. Note: These are 'strap' pins that are expected to be tied high or low depending on which L1 substate mode is supported by the PCIe controller(s) associated with the link. For multi-lane links, only the master lane is valid. Disabled/ ignored for slave lanes (per -link/shared signal).
11:10	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x2100			Register Name: COMB1_PHY_PINS_LANE0_CTRL0
Bit	Read/Write	Default/Hex	Description
9:8	R/W	0x0	COMB1_PHY_PMA_FULLRT_DIV_LN_0 PMA PLL full rate clock divider select - divide ratio for pma_pllclk_fullrt_ln_*. 00: Divide by 1 01: Divide by 2 10: Divide by 4 11: Divide by 8
7:6	/	/	/
5:4	R/W	0x0	COMB1_PHY_L00_MODE PHY mode: PHY mode of operation for the associated link. 00: PCIe across PIPE I/F 01: USB across PIPE I/F 10: SATA across PIPE I/F 11: Raw SerDes I/F mode These pins are only present when the PHY is configured to support both PIPE and RawSerDes I/Fs or PIPE only. For Raw SerDes only configuration, these pins are removed.
3:2	/	/	/
1	R/W	0x0	COMB1_PHY_L00_ RESET_N_HW_DIS PHY link Reset selects a hardware controller such as PCIe0, PCIe1, and USB3.1 to output reset signals 0: Select hardware reset and set PHY1_L00_RESET_N_SW bit[0] as 1 because the software reset has the higher priority. 1: Not select hardware reset
0	R/W	0x0	COMB1_PHY_L00_RESET_N_SW PHY Link reset From SoftWare config. Asserting this signal low will reset the PHYcomponents (PCS and PMA) for the associated link, with the exception of the APB registers. For multi-lane links, only the master lane is valid. Disabled/ignored for slave lanes (per -link/shared signal). When in a single-link configuration, only phy_reset_n is required. phy_l00_reset_n can be tied high.

18.2.6.20 0x2900 COMB1 PHY PINS Link Status Register0 (Default Value: 0x0000_0000)

Offset: 0x2900	Register Name: COMB1_PHY_PINS_LINK_STUS0

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R	0x0	COMB1_PHY_PMA_CMN_CLOCK_STOP_ACK Clock Stop Acknowledgement - Asserted high once all clocks in the PMA macro have stopped in response to assertion of pma_cmn_clock_stop_req. Note: This signal is only valid when pma_cmn_clock_stop_req is asserted high. At times such as power on reset, this signal may be high. Additionally, if the PMA is suspended (i.e. all links in L1.x), the internal PMA reference clock is disabled. Thus, upon assertion of pma_cmn_clock_stop_req, pma_cmn_-clock_stop_ack will not be asserted high, until the PMA reenables its internal reference clock upon exit from suspend.
7:6	/	/	/
5	R	0x0	COMB1_PHY_PMA_CMN_EXT_REFCLK_DETECTED_VALID External reference clock active detection result valid: 1: pma_cmn_ext_refclk_detected value is valid (i.e.detection operation has completed) 0: Not valid.
4	R	0x0	COMB1_PHY_PMA_CMN_EXT_REFCLK_DETECTED External reference clock active detection result: 1: External reference clock detected 0: Not detected
3:1	/	/	/
0	R	0x0	COMB1_PHY_PMA_CMN_READY PMA common ready : 1 = PMA common is ready for operation. Used as part of Raw SerDes startup sequence and power state changes.

18.2.6.21 0x2904 COMB1 PHY PINS Link Status Register1 (Default Value: 0x0000_0000)

Offset: 0x2904			Register Name: COMB1_PHY_PINS_LINK_STUS1
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x2904			Register Name: COMB1_PHY_PINS_LINK_STUS1
Bit	Read/Write	Default/Hex	Description
28	R	0x0	COMB1_PHY_DBG_RX_BIST_SYNC Rx BIST sync - asserted high upon BIST logic has synchronize with the incoming Rx data (loopback or from serial pins) and is checking for errors. (See PMA specification for further description of this signal.)
27:25	/	/	/
24	R	0x0	COMB1_PHY_DBG_RX_BIST_ERR_TOGGLE RX BIST error toggle - toggled upon BIST logic detecting an error in the Rx data. (See PMA specification for further description of this signal.)
23:21	/	/	/
20	R	0x0	COMB1_PHY_DBG_RX_BIST_STATUS Rx BIST status - asserted high upon BIST logic detecting an error in the Rx data. (See PMA specification for further description of this signal.)
19:0	R	0x0	COMB1_PHY_DBG_RX_RD COMB1 PHY Receiver parallel data out

18.2.6.22 0x2908 COMB1 PHY PINS Link Status Register2 (Default Value: 0x00A5_1000)

Offset: 0x2908			Register Name: COMB1_PHY_PINS_LINK_STUS2
Bit	Read/Write	Default/Hex	Description
31:0	R	0xA5_1000	COMB1_PHY_DTB_DATA COMB1 PHY Digital test bus data out.

18.2.6.23 0x2A00 COMB1 PHY PINS Lane0 Status Register0 (Default Value: 0x0000_0000)

Offset: 0x2A00			Register Name: COMB1_PHY_PINS_LANE0_STUS0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x2A00			Register Name: COMB1_PHY_PINS_LANE0_STUS0
Bit	Read/Write	Default/Hex	Description
0	R	0x0	COMB1_PHY_L00_ACK_L1_X COMB1 PHY LANE0 acknowledge L1 substate (sideband) : Acknowledgment from PHY that the requested L1_x entry or exit operation has been complete. Asserted high to indicate entry into L1 substate is complete. De-asserted low to indicate exit from L1 substate (back to P1 power state) is complete. For multi-lane links, only the master lane is valid. Disabled/ignored for slave lanes (per-link/shared signal). Only valid when phy_pcie_l1_ss_sel is low. When phy_l*_pcie_l1_ss_sel is high, leave unconnected

18.2.6.24 0x6004 DP RAWS TXData Width Conversion Control Register (Default Value: 0x0000_0000)

Offset: 0x6004			Register Name: DP_RAWS_TXDW_CONV_CTRL
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11	R/W	0x0	TX_PHY_CFG_LN3_RSTN 0: Disable 1: Enable
10	R/W	0x0	TX_PHY_CFG_LN2_RSTN 0: Disable 1: Enable
9	R/W	0x0	TX_PHY_CFG_LN1_RSTN 0: Disable 1: Enable
8	R/W	0x0	TX_PHY_CFG_LN0_RSTN 0: Disable 1: Enable
7	R/W	0x0	TX_PHY_CFG_LN3_EN 0: Disable 1: Enable
6	R/W	0x0	TX_PHY_CFG_LN2_EN 0: Disable 1: Enable
5	R/W	0x0	TX_PHY_CFG_LN1_EN 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x6004			Register Name: DP_RAWS_TXDW_CONV_CTRL
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	TX_PHY_CFG_LN0_EN 0: Disable 1: Enable
3:1	/	/	/
0	R/W	0x0	TX_PHY_CFG_DATA_EN 0: Disable 1: Enable

18.2.6.25 0x6100 USB3.1 PIPE CLK MAP Control Register (Default Value: 0x0000_000F)

Offset: 0x6100			Register Name: USB3P1_PIPE_CLK_MAP_CTRL
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0xF	USB3P1_PIPE_CLK_MAP 0: COMB0 PHY Lane0 or Lane3 PIPE CLK 1: COMB1 PHY Lane0 PIPE CLK 10-1111: Reserved

18.2.6.26 0x6104 USB3.1 PIPE RXData MAP Control Register (Default Value: 0x0000_000F)

Offset: 0x6104			Register Name: USB3P1_PIPE_RXD_MAP_CTRL
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0xF	USB3P1_PIPE_RXD_MAP 0: COMB0 PHY Lane1 or Lane2 PIPE RX_DATA 1: COMB1 PHY Lane0 PIPE RX_DATA 10-1111: Reserved

18.2.6.27 0x6C24 COMB0 PHY RAWS TXData MAP Control Register (Default Value: 0x0000_FFFF)

Offset: 0x6C24			Register Name: COMB0_PHY_RAWS_TXD_MAP_CTRL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:12	R/W	0xF	COMB0_PHY_LN3_RAWS_TXD_MAP 00: DP Lane0 Raw Serdes TX_DATA 01: DP Lane1 Raw Serdes TX_DATA 10: DP Lane2 Raw Serdes TX_DATA 11: DP Lane3 Raw Serdes TX_DATA 111-1111: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x6C24			Register Name: COMB0_PHY_RAWS_TXD_MAP_CTRL
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0xF	COMB0_PHY_LN2_RAWS_TXD_MAP 00: DP Lane0 Raw Serdes TX_DATA 01: DP Lane1 Raw Serdes TX_DATA 10: DP Lane2 Raw Serdes TX_DATA 11: DP Lane3 Raw Serdes TX_DATA 111-1111: Reserved
7:4	R/W	0xF	COMB0_PHY_LN1_RAWS_TXD_MAP 00: DP Lane0 Raw Serdes TX_DATA 01: DP Lane1 Raw Serdes TX_DATA 10: DP Lane2 Raw Serdes TX_DATA 11: DP Lane3 Raw Serdes TX_DATA 111-1111: Reserved
3:0	R/W	0xF	COMB0_PHY_LN0_RAWS_TXD_MAP 00: DP Lane0 Raw Serdes TX_DATA 01: DP Lane1 Raw Serdes TX_DATA 10: DP Lane2 Raw Serdes TX_DATA 11: DP Lane3 Raw Serdes TX_DATA others: Reserved

18.2.6.28 0x6C44 COMB1 PHY PIPE TXData MAP Control Register (Default Value: 0x0000_000F)

Offset: 0x6C44			Register Name: COMB1_PHY_PIPE_TXD_MAP_CTRL
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:4	R/W	0xF	000-1111: Reserved
3:0	R/W	0xF	COMB1_PHY_LN0_PIPE_TXD_MAP 000: USB3.1 PIPE TX_DATA 001: PCIE0 Lane0 PIPE TX_DATA 010-1111: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.3 PCIe3.0 DM

18.3.1 Overview

The PCI Express (PCIe) Controller is a general purpose I/O interconnect, which provides low pin count, high reliability, and high-speed data transfer at rates of up to 8.0 Gbps per lane per direction. There is 1 PCI Express controller in SoC, referred as PCIe.

The PCIe controller includes the following features:

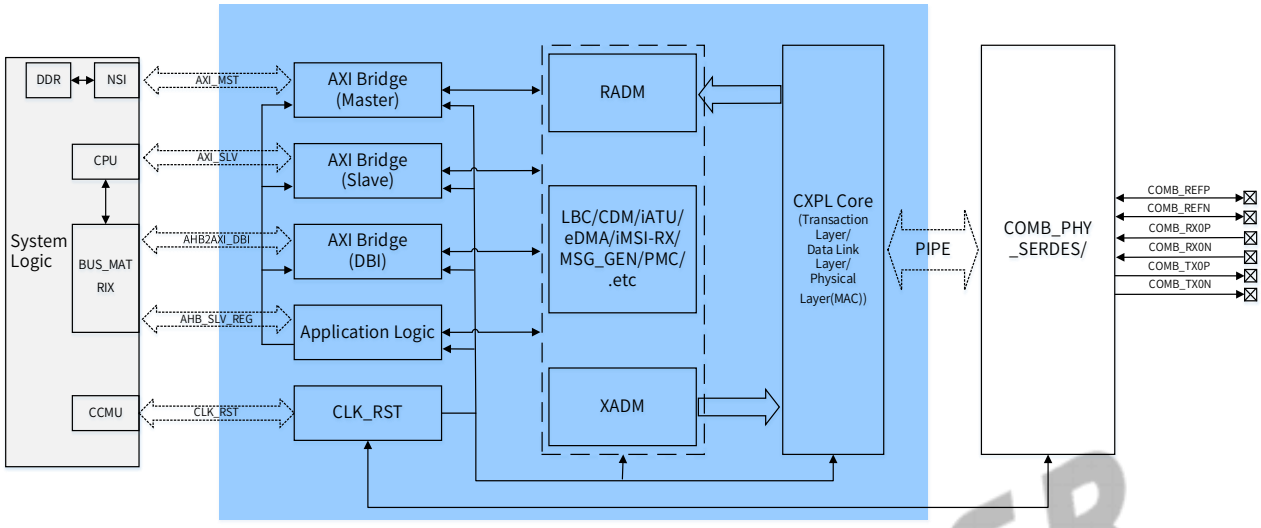
- All non-optional features of the PCI Express Base Specification, Revision 3.0, Version 1.0
- Supports Gen1 (2.5Gbps), Gen2 (5Gbps), Gen3 (8Gbps) speed
- Device Type: Supports DM
- Link Width: 1 lane
- 2 Virtual Channels (VCs)
- Multiple Functions: Supports 4 Functions for PCIe in EP Mode
- Configurable Max_Payload_Size, up to 512 bytes
- Embedded DMA with Hardware Flow Control. Supports 4 Write/Read Channels
- Internal Address Translation Unit. Supports 16 Inbound Address Translation regions and 16 Outbound Address Translation regions
- MSI with Per-Vector Masking (PVM), Extended message data for MSI
- The following optional features of the specification:
  - ID-Based Ordering (IDO) by your application
  - L1 Substates (L1SS)
  - Resizable BAR (RBAR) with Expanded RBAR and VF Resizable BAR support
  - Readiness Notifications (RN)
  - PCI Express Active State Power Management (ASPM)
  - PCI Express Advanced Error Reporting (AER)
  - Vital Product Data (VPD)
  - Access Control Services (ACS)
  - Dynamic Power Allocation (DPA)
  - Function Level Reset(FLR)

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.3.2 Block Diagram

The following figure shows the functional block diagram of the PCIe.

Figure 18-4 PCIe Block Diagram



The PCIe controller contains the following sub-blocks:

Table 18-4 PCIe Sub-blocks

Sub-block	Description
CXPL	Common Express Port Logic. This sub-block is the basic functionality for the PCI Express physical, link, and transaction layers. It implements a large part of the transaction layer logic, all of the data link layer logic, and the MAC portion of the physical layer, including the link training and status state machine (LTSSM). The CXPL connects to the external PHY through the PIPE.
XADM	Transmit Application-Dependent Module. It implements the application-specific functionality of the PCI Express transaction layer for packet transmission. Its functions include: ● TLP Arbitration ● TLP Formation ● Flow Control (FC) Credit checking The transmit path uses a cut-through architecture. It does not implement transmit buffering/queues (other than the retry buffer). The controller maintains an internal Target Completion Lookup Table to store certain TLP header information from the Rx request. Your application can use this information for transmitting completions.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Sub-block	Description
RADM	Receive Application-Dependent Module. It implements application-specific functionality of the PCI Express transaction layer for packet reception. Its functions include: ● Sorting/filtering of received TLPs. The filtering rules and routing are configurable. ● Buffering and queuing of the received TLPs. ● Routing of received TLP to the controller s receive interfaces. The RADM maintains a Receive Completion Lookup Table (LUT) for completion tracking and completion-timeout monitoring of Tx non-posted requests. It indicates a timeout when an expected Rx completion does not arrive within the timeout period.
CDM	Configuration-dependent Module. It implements: ● Standard PCI Express configuration space ● Controller-specific register space (Port Logic Registers)
PMC	Power Management Controller. It implements the power management features of the PCIe controller.
LBC& DBI	Local Bus Controller. It provides a mechanism for a link partner (in EP mode only) or a local CPU (through the Data Bus Interface) to access: ● Internal registers (in the CDM) ● External application registers connected externally to the ELBI
MSG_GEN	Message Generation Module. It transmits messages generated by the controller.
iMSI-RX	Integrated MSI Receiver. The AXI bridge provides an integrated MSI reception module to detect and terminate inbound MSI requests(received on the RX wire).
eDMA	Embedded DMA. The RC system CPU, or the EP application CPU, can offload the transferring of large blocks of data to the embedded DMA controller1, leaving the CPU free to perform other tasks. You can configure the DMA to have one to eight read channels and one to eight write channels.
iATU	Internal Address Translation Unit. The PCIe controller uses the iATU to implement a local address translation scheme that replaces the TLP address and TLP header fields in the current TLP request header.

18.3.3 Clock Sources

The following table describes the clock sources of PCIe. For clock setting, configurations, and gating information, refer to the section CCU.

Module	Clock Sources	Description
PCIE0_AUX	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.
	RTC_32K	Its frequency is 32.768 kHz by default.
PCIE0_AXI_SLV	PERI0_600M	Its frequency is 600 MHz by default.
	PERI0_480M	Its frequency is 480 MHz by default.
	PERI0_400M	Its frequency is 400 MHz by default.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.3.4 External Signals

The following table describes the external signals of the PCIe.

Table 18-5 PCIe External Signals

Signal Name	Description	Type
PCIE-CLKREQN	PCIe Clock Request from PCIe Peripheral	I/O
PCIE-WAKEN	PCIe Wake Up	I/O
PCIE-PERSTN	PCIe Warm Reset	I/O

18.3.5 Functional Description

18.3.5.1 PCIe Memory Mapping

The address space of PCIe controller can be partitioned into three spaces.

- Core Configuration Space (CCS): The configuration register space of the PCIe controller itself. It is also the standard configuration register space defined by the PCIe Specification.
- User Defined Space (UDS): The user-defined register space for the PCIe controller itself.
- Slave Command Space (SCS): Address space for configuration transaction and memory transaction. The read and write operations of this space will be transformed by the PCIe controller into configuration read and write transactions or memory read and write transactions in PCIe domain. The PCIe command space segmentation is 0x20000000-0x2FFFFFFF and 0x440000000-0x53FFFFFFF.

18.3.5.2 ATU Operation

ATU is an address translation unit in PCIe controller and is used for transaction transformation and address translation. There are two types of ATU: Outbound ATU and Inbound ATU.

Outbound ATU

Outbound ATU is used to transform the read/write operation in CPU domain of the original address space into the read/write transaction in PCIe domain of the target address space. If the Outbound ATU is not used, the PCIe controller will not perform address translation against the read/write operation in the CPU domain; instead, the read/write transaction initiated in the CPU domain will be transformed into the read/write operation at the same address in the PCIe domain. If the Outbound ATU is used, the read/write transaction initiated in the CPU domain will be transformed into that at the different address in the PCIe domain.

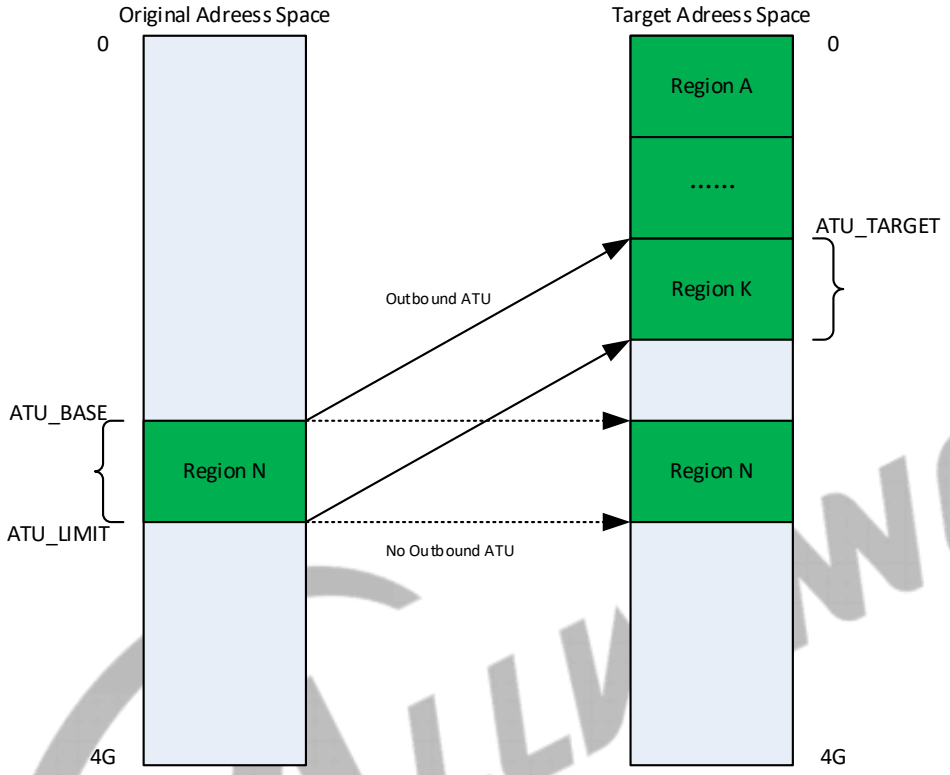
The following takes the region N as an example:

- When Outbound ATU is not used, read/write operation initiated at the address Region N of CPU domain will be directly transformed into the read/write transaction at the address Region N of PCIe domain.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- When Outbound ATU is used, set address transaction as “transform the Region N of CPU domain into the Region K of PCIe domain. The read/write operation initiated at the address Region N of CPU domain will be transformed into the read/write transaction at the address Region K of PCIe domain.

Figure 18-5 Outbound ATU



Inbound ATU

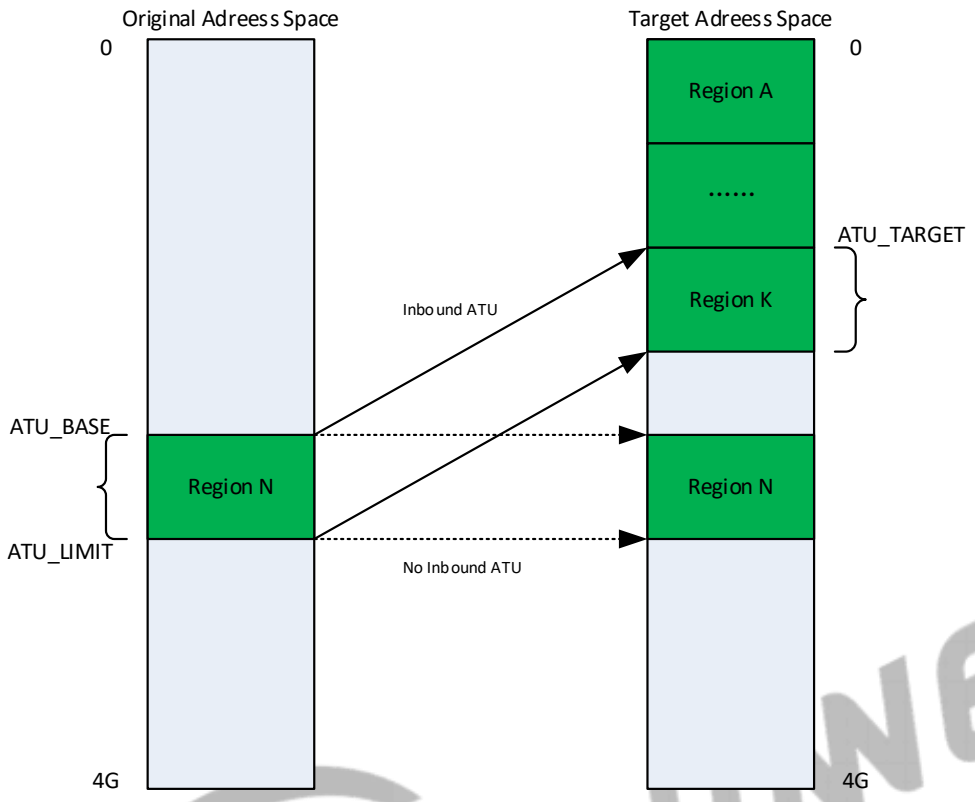
Inbound ATU is used to transform the read/write transaction in the PCIe domain of the original address space into the read/write operation in the CPU domain of the target address space. If the Inbound ATU is not used, the PCIe controller will not perform address translation; instead, the read/write transaction initiated in the PCIe domain will be transformed into the read/write operation at the same address in the CPU domain. If the Inbound ATU is used, the read/write transaction initiated in the PCIe domain will be transformed into that at the different address in the CPU domain.

The following takes the region N as an example:

- When Inbound ATU is not used, read/write transaction initiated at the address Region N of PCIe domain will be directly transformed into the read/write operation at the address Region N of CPU domain.
- When Inbound ATU is used, set address transaction as “transform the Region N of PCIe domain into the Region K of CPU domain. The read/write operation initiated at the address Region N of PCIe domain will be transformed into the read/write transaction at the address Region K of CPU domain.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 18-6 Inbound ATU

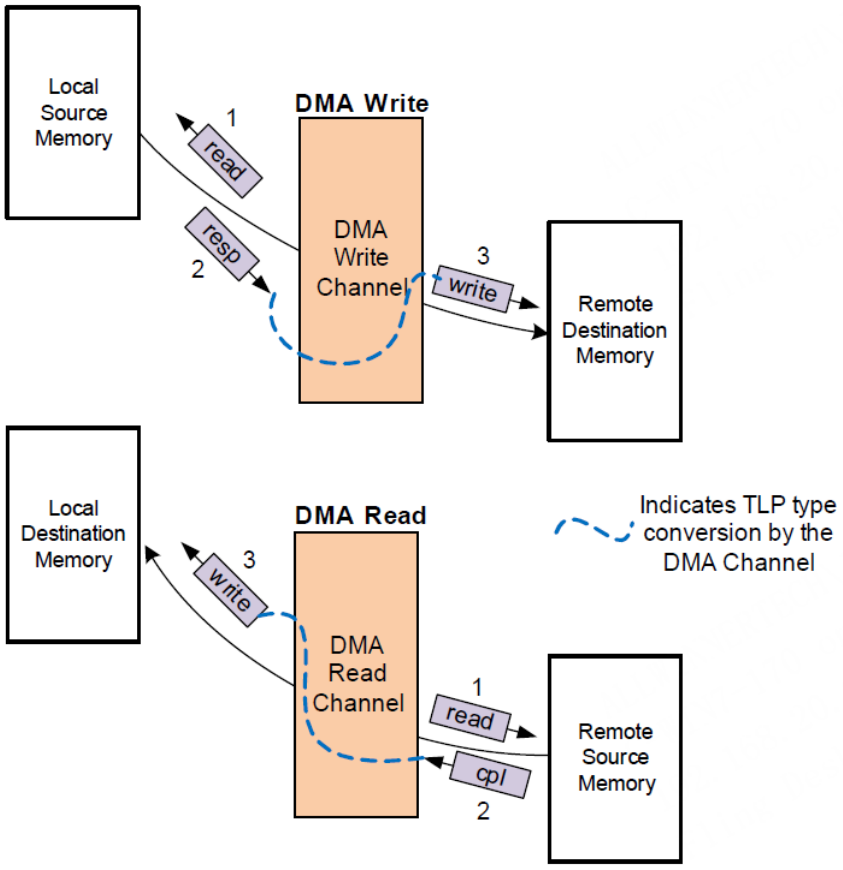


18.3.5.3 DMA Operation

There is a private DMA with read channels and write channels in the PCIe controller. The following figure describes the DMA write and read process.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 18-7 DMA Operation



- DMA Write Channel

  The DMA write channel is used for data transfer from local bus address space to the address space in the PCIe domain. First, DMA controller reads data from the local bus address space and writes them to the address space in the CPU domain. Then, the PCIe controller transforms the write operation initiated by DMA into a write transaction in the PCIe domain and writes data to the destination address space in the PCIe domain.

- DMA Read Channel

  The DMA read channel is used for data transfer from the address space in the PCIe domain to the local bus address space such as DRAM address space. If a read operation is initiated by DMA in the original address space of the CPU domain, the PCIe controller will transform the read operation into a read transaction in the PCIe domain and write data to the local bus address space.

18.3.5.4 MSI Operation

Message Signaled Interrupt (MSI) is a kind of mechanism that Endpoints send interrupt requests to the CPU connected with the Root Complex. The MSI uses memory write transaction. The memory write transaction message for transmitting interrupt information is MSI message.

Assume an Endpoint needs to send a MSI interrupt request to CPU. First, the Endpoint needs to initiate a memory write transaction in the MSI address of PCIe domain, which will be transformed

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

into a MSI interrupt signal to inform CPU by the PCIe controller after the transaction is detected by RC.

18.3.6 Programming Guidelines

18.3.6.1 PCIe System Initialization

Initialize the PCIe system before using the PCIe controller. The steps are as below.

Step 1 Write 2b'10 to the SERDES_RST/SERDES_NOPPU_RST (bit [17:16]) register to dis-assert Serdes_subsys reset.

Step 2 Write 2b'10 to PCIE0_BGR_REG (bit [17:16]) to dis-assert PCIe reset.

Step 3 Write 1 to XO_CTRL1_REG (bit[5]) to enable PCIe COMB PHY REF_CLK.

Step 4 Write 1 to the MBUS_MAT_CLK_GATING_REG (bit [28]) to enable MBUS_MCLK clock.

Step 5 Write 1 to the PCIE0_AUX_CLK_REG (bit [31]) to enable AUX clock.

Step 6 Write 1 to the PCIE0_AXI_SLV_CLK_REG (bit [31]) to enable SLV clock.

Step 7 Finish. CPU can access the PCIe registers.

18.3.6.2 PCIe Controller Initialization

Step 1 Write 0 to PCIe_LTSSM_ENABLE (bit [0])to disable LTSSM link training.

Step 2 Set the link, BAR space, and bus of PCIe controller

Step 3 Write 1 to PCIE_LTSSM_ENABLE (bit[0]) to enable LTSSM link training

Step 4 When like up finishes, the SII_INT_1 (bit[1:0]) will be asserted. Interrupts will be generated.

Step 5 Set Gen1 as Gen2

Step 6 End. Then, the PCIe controller can transfer data with devices.

18.3.7 Register List

Module Name	Base Address
PCIe	0x06400000

Register Name	Offset	Description
PCIE_ADDR_PAGE_CFG	0x0004	PCIe Address Page Configuration Register
MSTR_AWMISC_INFO_0	0x0100	PCIe AXI Master Write Misc Information Register0
MSTR_AWMISC_INFO_1	0x0104	PCIe AXI Master Write Misc Information Register1

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
MSTR_AWMISC_INFO_HDR_34DW_0	0x0108	PCIe AXI Master Write Misc Information Header Register0
MSTR_AWMISC_INFO_HDR_34DW_1	0x010c	PCIe AXI Master Write Misc Information Header Register1
MSTR_AWMISC_INFO_OTHER	0x0110	PCIe AXI Master Write Misc Information Other Register
MSTR_ARMISC_INFO_0	0x0120	PCIe AXI Master Read Misc Information Register0
MSTR_ARMISC_INFO_1	0x0124	PCIe AXI Master Read Misc Information Register1
MSTR_ARMISC_INFO_OTHER	0x0130	PCIe AXI Master Read Misc Information Other Register
MSTR_BMISC_INFO	0x0150	PCIe AXI Master Write Response Misc Information Register
MSTR_RMISC_INFO	0x0160	PCIe AXI Master Read Misc Information Register
PCIE_SLV_AWMISC_CTRL	0x0200	PCIe SLAVE Write Misc Control Register
SLV_AWMISC_INFO_ATU_BYP	0x0204	PCIe AXI SLAVE Write Misc Information ATU Register
SLV_AWMISC_INFO_HDR_34DW_0	0x0208	PCIe AXI SLAVE Write Misc Information Header Register0
SLV_AWMISC_INFO_HDR_34DW_1	0x020c	PCIe AXI SLAVE Write Misc Information Header Register1
SLV_AWMISC_INFO_OTHER_0	0x0210	PCIe AXI SLAVE Write Misc Information Other Register0
SLV_AWMISC_INFO_OTHER_1	0x0214	PCIe AXI SLAVE Write Misc Information Other Register1
SLV_ARMISC_CTRL	0x0220	PCIe AXI SLAVE Read Control Register
SLV_ARMISC_INFO_ATU_BYP	0x0224	PCIe AXI SLAVE Read Misc Information ATU Register
SLV_ARMISC_INFO_OTHER	0x0230	PCIe AXI SLAVE Read Misc Information Other Register
SLV_AWMISC_DATA_INFO	0x0240	PCIe AXI SLAVE Write Data Misc Information Register
SLV_BMISC_INFO	0x0250	PCIe AXI Slave Write Response Misc Information Register
SLV_RMISC_INFO	0x0260	PCIe AXI Slave Read Response Misc Information Register
RADM_TARGET1	0x0300	PCIe RADM Target1 Register
APP_CLK_REQ_N	0x0400	PCIe APP Clock Request Register
APP_INIT_RST	0x0500	PCIe APP Initial Reset Register
MSI_CTRL_0	0x0600	PCIe MSI Ctrl Register0
MSI_CTRL_1	0x0604	PCIe MSI Ctrl Register1
PF_N_CFG_MSI_EN	0x0610+N*0x20 (N=0~3)	PCIe Function Config MSI Enable Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
PF_N_CFG_MSI_MASK	0x0614+ N*0x20 (N=0~3)	PCIe Function Config MSI Mask Register
PF_N_CFG_MSI_ADDR_0	0x0618+ N*0x20 (N=0~3)	PCIe Function Config MSI Address Register0
PF_N_CFG_MSI_ADDR_1	0x061c+ N*0x20 (N=0~3)	PCIe Function Config MSI Address Register1
PF_N_CFG_MSI_DATA	0x0620+ N*0x20 (N=0~3)	PCIe Function Config MSI Data Register
PF_N_CFG_MSI_PEND	0x0624+ N*0x20 (N=0~3)	PCIe Function Config MSI Pending Register
VEN_MSI_REQ	0x06f0	PCIe VEN MSI Request Register
VEN_MSI_CTRL	0x06f4	PCIe VEN MSI Ctrl Register
VEN_MSG_REQ	0x0700	PCIe VEN MSG Request Register
VEN_MSG_CFG_0	0x0704	PCIe VEN MSG Config Register0
VEN_MSG_CFG_1	0x0708	PCIe VEN MSG Config Register1
VEN_MSG_DATA_0	0x070c	PCIe VEN MSG Data Register0
VEN_MSG_DATA_1	0x0710	PCIe VEN MSG Data Register1
PF_N_SII_CFG_0	0x0800+ N*0x10 (N=0~3)	PCIe Function SII Config Register0
PF_N_SII_CFG_1	0x0804+ N*0x10 (N=0~3)	PCIe Function SII Config Register1
PF_N_SII_CFG_LTR	0x0880+ N*0x04 (N=0~3)	PCIe Function SII Config LTR Register
PF_N_SII_CFG_BUS	0x08a0+ N*0x04 (N=0~3)	PCIe Function SII Config BUS Register
SII_CFG_VC_0	0x08d0	PCIe SII Config VC Register0
SII_CFG_VC_1	0x08d4	PCIe SII Config VC Register1
SII_CFG_TC	0x08d8	PCIe SII Config TC Register
SII_CFG_LTR_ACS	0x08dc	PCIe SII Config LTR ACS Register
SII_CFG_PBUS	0x08e0	PCIe SII Config PBUS Register
SII_ELEC	0x0a00	PCIe SII Electromechanical Register
SII_CFG_EML	0x0a04	PCIe SII CFG EML Register
FRS_INT_MSG_NUM	0x0b00	PCIe FRS INT Register
FRS_READY	0x0b04	PCIe FRS READY Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
PCIE_LTSSM_ENABLE	0x0c00	PCIe LTSSM Enable Register
SII_GEN_MES	0x0d00	PCIe SII General Messaging Register
SII_RADM_MES_0	0x0d04	PCIe SII RADM Messaging Register0
SII_RADM_MES_1	0x0d08	PCIe SII RADM Messaging Register1
SII_RADM_MES_2	0x0d0c	PCIe SII RADM Messaging Register2
SII_INT_MASK_0	0x0e00	PCIe SII Interrupt Mask Register0
SII_INT_MASK_1	0x0e04	PCIe SII Interrupt Mask Register1
SII_INT_0	0x0e08	PCIe SII Interrupt Register0
SII_INT_1	0x0e0c	PCIe SII Interrupt Register1
SII_INT_MASK_2	0x0e10	PCIe SII Interrupt Mask Register2
SII_INT_MASK_3	0x0e14	PCIe SII Interrupt Mask Register3
SII_INT_2	0x0e18	PCIe SII Interrupt Register2
SII_INT_3	0x0e1c	PCIe SII Interrupt Register3
SII_CFG_INT_PIN	0x0e80	PCIe SII CFG INT PIN Register
SII_CFG_INT_DIS	0x0e88	PCIe SII CFG INT Disable Register
SII_SYS_INT	0x0e90	PCIe SII SYS INT Register
SII_AER_INT_MSG_NUM	0x0ea0	PCIe SII CFG AER INT MSG_NUM Register
SII_PCIE_CAP_INT_MSG_NUM	0x0ea8	PCIe SII CFG CAP INT MSG NUM Register
SII_CFG_2ND_RESET	0x0f00	PCIe SII CFG 2ND RESET Register
SII_APP_LTR_MSG_REQ	0x0f10	PCIe SII APP LTR MSG REQ Register
SII_APP_LTR_MSG_LATENCY	0x0f14	PCIe SII APP LTR MSG LATENCY Register
SII_APP_LTR_MSG_FUNC_NUM	0x0f18	PCIe SII APP LTR MSG FUNC NUM Register
SII_APP_LTR_LATENCY	0x0f1c	PCIe SII APP LTR LATENCY Register
SII_APP_PM_UNLOCK	0x1000	PCIe SII APP PM UNLOCK Register
SII_APP_PM_0	0x1100	PCIe SII Power Manage Register0
SII_APP_PM_1	0x1104	PCIe SII Power Manage Register1
SII_APP_PM_2	0x1108	PCIe SII Power Manage Register2
SII_APP_PM_3	0x110c	PCIe SII Power Manage Register3
SII_RX_CPL	0x1200	PCIe SII Receive CPL Register
SII_TX	0x1300	PCIe SII Transmit Register
SII_GEN3_EQ	0x1350	PCIe SII Gen3-Only Equalization Register
FLR_CTRL	0x13f0	PCIe Function Level Reset Control Register
SII_TRGT_CPL	0x1400	PCIe SII Target Completion Register
SII_TRGT_LUP	0x1404	PCIe SII Target Lookup Register
SII_ERR_RPT	0x1500	PCIe SII Error Report Register
SII_CFG_HW_AUTO_SP_DIS	0x1600	PCIe SII CFG HW Register
SII_PF_N_CFG_BAR0_START0	0x1800+N*0x100 (N=0~3)	PCIe SII PF CFG BAR0 Start Register0

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
SII_PF_N_CFG_BAR0_START1	0x1804+N*0x100 (N=0~3)	PCIe SII PF CFG BAR0 Start Register1
SII_PF_N_CFG_BAR0_LIMIT0	0x1808+N*0x100 (N=0~3)	PCIe SII PF CFG BAR0 Limit Register0
SII_PF_N_CFG_BAR0_LIMIT1	0x180c+N*0x100 (N=0~3)	PCIe SII PF CFG BAR0 Limit Register1
SII_PF_N_CFG_BAR1_START	0x1810+N*0x100 (N=0~3)	PCIe SII PF CFG BAR1 Start Register
SII_PF_N_CFG_BAR1_LIMIT	0x1818+N*0x100 (N=0~3)	PCIe SII PF CFG BAR1 Limit Register
SII_PF_N_CFG_BAR2_START0	0x1820+N*0x100 (N=0~3)	PCIe SII PF CFG BAR2 Start Register0
SII_PF_N_CFG_BAR2_START1	0x1824+N*0x100 (N=0~3)	PCIe SII PF CFG BAR2 Start Register1
SII_PF_N_CFG_BAR2_LIMIT0	0x1828+N*0x100 (N=0~3)	PCIe SII PF CFG BAR2 Limit Register0
SII_PF_N_CFG_BAR2_LIMIT1	0x182c+N*0x100 (N=0~3)	PCIe SII PF CFG BAR2 Limit Register1
SII_PF_N_CFG_BAR3_START	0x1830+N*0x100 (N=0~3)	PCIe SII PF CFG BAR3 Start Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
SII_PF_N_CFG_BAR3_LIMIT	0x1838+N*0x100 (N=0~3)	PCIe SII PF CFG BAR3 Limit Register
SII_PF_N_CFG_BAR4_START0	0x1840+N*0x100 (N=0~3)	PCIe SII PF CFG BAR4 Start Register0
SII_PF_N_CFG_BAR4_START1	0x1844+N*0x100 (N=0~3)	PCIe SII PF CFG BAR4 Start Register1
SII_PF_N_CFG_BAR4_LIMIT0	0x1848+N*0x100 (N=0~3)	PCIe SII PF CFG BAR4 Limit Register0
SII_PF_N_CFG_BAR4_LIMIT1	0x184c+N*0x100 (N=0~3)	PCIe SII PF CFG BAR4 Limit Register1
SII_PF_N_CFG_BAR5_START	0x1850+N*0x100 (N=0~3)	PCIe SII PF CFG BAR5 Start Register
SII_PF_N_CFG_BAR5_LIMIT	0x1858+N*0x100 (N=0~3)	PCIe SII PF CFG BAR5 Limit Register
SII_PF_N_VF_RBAR_CTRL	0x1860+N*0x100 (N=0~3)	PCIe SII PF RBAR Ctrl Register
SII_PF_N_CFG_RBAR_SIZE_0	0x1870+N*0x100 (N=0~3)	PCIe SII PF RBAR Size Register0
SII_PF_N_CFG_RBAR_SIZE_1	0x1874+N*0x100 (N=0~3)	PCIe SII PF RBAR Size Register1

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
SII_PF_N_CFG_VF_RBAR_SIZE_0	0x1878+N*0x100 (N=0~3)	PCIe SII PF VF RBAR Size Register0
SII_PF_N_CFG_VF_RBAR_SIZE_1	0x187c+N*0x100 (N=0~3)	PCIe SII PF VF RBAR Size Register1
SII_PF_N_CFG_EXP_ROM_START	0x1880+N*0x100 (N=0~3)	PCIe SII PF CFG EXP ROM Start Register
SII_PF_N_CFG_EXP_ROM_LIMIT	0x1884+N*0x100 (N=0~3)	PCIe SII PF CFG EXP ROM Limit Register

18.3.8 Register Description

18.3.8.1 0x0004 PCIe Address Page Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: PCIE_ADDR_PAGE_CFG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	SLV_ADDR_PAGE_CFG Slave Address Page Configuration For a configuration transfer, the address bus should be driven as follows: ADDR[15:8] = Bus_Number ADDR[7:3] = Dev_Number ADDR[2:0] = Func_Number For a memory transfer, the address bus should be driven as follows: ADDR[15:0] = PCIe_ADDR[31:16]
15:1	/	/	/
0	R/W	0x0	BDF_CTRL BDF_Control 0: Not use SLV_ADDR_PAGE_CFG 1: use SLV_ADDR_PAGE_CFG

18.3.8.2 0x0100 PCIe AXI Master Write Misc Information Register0 (Default Value: 0x0000_0000)

Offset: 0x0100	Register Name: MSTR_AWMISC_INFO_0

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	MSTR_AWMISC_INFO_0 AXI Master Write Misc Information. AXI master write transaction associated miscellaneous information from the TLP received by the native PCIe controller. This is a signal that the application can optionally use. It is not part of the standard AXI interface. ɔ Bus number, device number, function number, and register numbers are overlaid to the address bus when type is configuration transactions. ɔ Message contents are also overlaid to the address bus for MSG TLPs. Bits [7:0] indicate the message code when the type is message. For more details, see 'AXI Master Interface Sideband Signals'. The bit fields are mapped as follows: ɔ [7:0]: Reserved except for MSG TLP. Bits [7:0] indicate the message code when the type is message. ɔ [8:6]: BAR number of TLP ɔ [9]: TLP is an I/O ɔ [10]: TLP is in ROM range ɔ [13:11]: TLP's Function number. Function numbering starts at '0'. This field is not used when CX_SRIOV_ENABLE =1 or CX_ARI_ENABLE =1. For more details, see mstr_awmisc_info_func_num. ɔ [14]: TLP's NS bit ɔ [15]: TLP's RO bit ɔ [18:16]: TLP's TC bits ɔ [23:19]: TLP's TYPE ɔ [31:24]: TLP's requester ID_0

18.3.8.3 0x0104 PCIe AXI Master Write Misc Information Register1 (Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: MSTR_AWMISC_INFO_1
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0104			Register Name: MSTR_AWMISC_INFO_1
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	MSTR_AWMISC_INFO_1 AXI Master Write Misc Information. AXI master write transaction associated miscellaneous information from the TLP received by the native PCIe controller. This is a signal that the application can optionally use. It is not part of the standard AXI interface. ɔ Bus number, device number, function number, and register numbers are overlaid to the address bus when type is configuration transactions. ɔ Message contents are also overlaid to the address bus for MSG TLPs. Bits [7:0] indicate the message code when the type is message. For more details, see 'AXI Master Interface Sideband Signals'. The bit fields are mapped as follows: ɔ [8:0]: TLP's requester ID_1 ɔ [15:9]: TLP's TAG

18.3.8.4 0x0108 PCIe AXI Master Write Misc Information Header Register0 (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: MSTR_AWMISC_INFO_HDR_34DW_0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	MSTR_AWMISC_INFO_HDR_34DW_0 mstr_awmisc_info_hdr_34dw_status[31:0]

18.3.8.5 0x010c PCIe AXI Master Write Misc Information Header Register1 (Default Value: 0x0000_0000)

Offset: 0x010c			Register Name: MSTR_AWMISC_INFO_HDR_34DW_1
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x010c			Register Name: MSTR_AWMISC_INFO_HDR_34DW_1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	MSTR_AWMISC_INFO_HDR_34DW_1 mstr_awmisc_info_hdr_34dw_status[63:32]

18.3.8.6 0x0110 PCIe AXI Master Write Misc Information Other Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: MSTR_AWMISC_INFO_OTHER
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R	0x0	MSTR_AWMISC_INFO_LAST_DCMP_TLP mstr_awmisc_info_last_dcmp_tlp_status
26	R	0x0	MSTR_AWMISC_INFO_EP mstr_awmisc_info_ep_status
25	R	0x0	MSTR_AWMISC_INFO_NW mstr_awmisc_info_nw_status
24	R	0x0	MSTR_AWMISC_INFO_IDO mstr_awmisc_info_ido_status
23:22	R	0x0	MSTR_AWMISC_INFO_ATS mstr_awmisc_info_ats_status[1:0]
21:16	R	0x0	MSTR_AWMISC_INFO_DMA mstr_awmisc_info_dma_status[5:0]
15:11	/	/	/
10:0	R	0x0	MSTR_AWMISC_INFO_TPH mstr_awmisc_info_tph_status[10:0]

18.3.8.7 0x0120 PCIe AXI Master Read Misc Information Register0 (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: MSTR_ARMISC_INFO_0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	MSTR_ARMISC_INFO_0 mstr_armisc_info_status[31:0]

18.3.8.8 0x0124 PCIe AXI Master Read Misc Information Register1 (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: MSTR_ARMISC_INFO_1
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	MSTR_ARMISC_INFO_1 mstr_armisc_info_status[47:32]

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.3.8.9 0x0130 PCIe AXI Master Read Misc Information Other Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: MSTR_ARMISC_INFO_OTHER
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R	0x0	MSTR_ARMISC_INFO_ZEROREAD mstr_armisc_info_zeroread_status
27	R	0x0	MSTR_ARMISC_INFO_LAST_DCMP_TLP mstr_armisc_info_last_dcmp_tlp_status
26	/	/	/
25	R	0x0	MSTR_ARMISC_INFO_NW mstr_armisc_info_nw_status
24	R	0x0	MSTR_ARMISC_INFO_IDO mstr_armisc_info_ido_status
23:22	/	/	/
21:16	R	0x0	MSTR_ARMISC_INFO_DMA mstr_armisc_info_dma_status[5:0]
15:11	/	/	/
10:0	R	0x0	MSTR_ARMISC_INFO_TPH mstr_armisc_info_tph_status[10:0]

18.3.8.10 0x0150 PCIe AXI Master Write Response Misc Information Register (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: MSTR_BMISC_INFO
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0150			Register Name: MSTR_BMISC_INFO
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x0	MSTR_BMISC_INFO_CPL_STAT AXI Master Write Response selection bus. This controls the response to be sent on the wire in the case of successful write requests. The controller always sends a CA (Completer Abort) response when it receives SLVERR/DECERR. ね 00: SC (Successful Completion) ね 01: CA (Completer Abort) ね 10: UR (Unsupported Request) ね 11: SC (Successful Completion) Your application must drive the same value on mstr_bmisc_info_cpl_stat throughout the complete response. For a multi-beat response, when you set mstr_bmisc_info_cpl_stat to UR: ね If the first beat of the response produces a slave error/decode error, the controller sends a CPL with status as CA. ね If any beat (other than the first beat) of the response has a slave/decode error, the controller sends a CPL with status as UR.

18.3.8.11 0x0160 PCIe AXI Master Read Misc Information Register (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: MSTR_RMISC_INFO
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0160			Register Name: MSTR_RMISC_INFO
Bit	Read/Write	Default/Hex	Description
17:16	R/W	0x0	MSTR_RMISC_INFO_CPL_STAT AXI Master Read Response selection bus. This bus controls the response sent on the PCIe wire in the case of successful read requests. The controller always sends a CA (Completer Abort) response when it receives SLVERR/DECERR. ▪00: SC (Successful Completion) ▪01: CA (Completer Abort) ▪10: UR (Unsupported Request) ▪11: SC (Successful Completion) Your application must drive the same value on mstr_rmisc_info_cpl_stat throughout the complete response. For a multi-beat response, when you set mstr_rmisc_info_cpl_stat to UR: ▪If the first beat of the response produces a slave error/decode error, the controller sends a CPL with status as CA. ▪If any beat (other than the first beat) of the response has a slave/decode error, the controller sends a CPL with status as UR.
15:13	/	/	/
12:0	R/W	0x0	MSTR_RMISC_INFO AXI Master Read Response Transaction Associated Misc Information. This is a signal that the application can optionally use. It is not part of standard AXI interface. For more details, see 'AXI Master Interface Sideband Signals'. All reserved bits must be connected to logic '0'. ▪ [1:0]: Reserved ▪ [2]: Reserved. ▪ [6:3]: Reserved ▪ [7]: TLP's EP bit ▪ [12:8]: Reserved.

18.3.8.12 0x0200 PCIe SLAVE Write Misc Control Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: PCIE_SLV_AWMISC_CTRL
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0200			Register Name: PCIE_SLV_AWMISC_CTRL
Bit	Read/Write	Default/Hex	Description
24:22	R/W	0x00	TLP_FUNC_NUM Function numbering starts at '0'.Not used when CX_SRIOV_ENABLE =1 or CX_ARI_ENABLE =1. For more details, see slv_awmisc_info_func_num. This field is only present when multifunction support (CX_NFUNC > 1) is enabled.
21	R/W	0x0	AXI_TRANS_DBI_ACCESS AXI transaction is a DBI access. This is for SHARED DBI mode only.
20:13	R/W	0x00	MSG TLP s MSG Code
12:10	R/W	0x0	TC TLP s TC bits
9	R/W	0x0	RO TLP s RO bit
8	R/W	0x0	NS TLP s NS bit
7	/	/	/
6	R/W	0x0	EP TLP s EP bit
5	R/W	0x0	SERIALIZE_NP_REQ Serialize NP Requests
4:0	R/W	0x0	TYPE TLP s TYPE

18.3.8.13 0x0204 PCIe AXI SLAVE Write Misc Information ATU Register (Default Value: 0x0000_0000)

Offset: 0x0204			Register Name: SLV_AWMISC_INFO_ATU_BYP
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	SLV_AWMISC_INFO_ATU_BYPASS AXI Slave Write Request Internal ATU Bypass. When set it indicates that this request should not be processed by the internal address translation unit

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.3.8.14 0x0208 PCIe AXI SLAVE Write Misc Information Header Register0 (Default Value: 0x0000_0000)

Offset: 0x0208			Register Name: SLV_AWMISC_INFO_HDR_34DW_0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	SLV_AWMISC_INFO_HDR_34DW_0 slv_awmisc_info_hdr_34dw[31:0] ,AXI Slave 3rd and 4th header DWs. The application drives this bus with the 3rd and 4th Header DWs it intends to send on a PCIe Msg/MsgD. Note: The data is in big endian format, that is, slv_awmisc_info_hdr_34dw[7:0] contains byte 15 of header DW.

18.3.8.15 0x020c PCIe AXI SLAVE Write Misc Information Header Register1 (Default Value: 0x0000_0000)

Offset: 0x020c			Register Name: SLV_AWMISC_INFO_HDR_34DW_1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	SLV_AWMISC_INFO_HDR_34DW_1 slv_awmisc_info_hdr_34dw [63:32] ,AXI Slave 3rd and 4th header DWs. The application drives this bus with the 3rd and 4th Header DWs it intends to send on a PCIe Msg/MsgD. Note: The data is in big endian format.

18.3.8.16 0x0210 PCIe AXI SLAVE Write Misc Information Other Register0 (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: SLV_AWMISC_INFO_OTHER_0
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25	R/W	0x0	SLV_AWMISC_INFO_NW AXI Slave Write Transaction's Request ATS No Write (NW) Bit. For more details, see 'PCI-SIG Address Translation Services (ATS)'. This is a signal that the application can optionally use. It is not part of the standard AXI interface. For more details, see 'AXI Slave Interface Sideband Signals'.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0210			Register Name: SLV_AWMISC_INFO_OTHER_0
Bit	Read/Write	Default/Hex	Description
24	R/W	0x0	SLV_AWMISC_INFO_IDO AXI Slave Write Transaction's IDO bit. Enables ID-base ordering on outbound requests. This is a signal that the application can optionally use. It is not part of the standard AXI interface. For more details, see 'AXI Slave Interface Sideband Signals'.
23:11	/	/	/
10:0	R/W	0x0	SLV_AWMISC_INFO_TPH AXI Slave Write Request TLP Processing Hints. The bits are mapped as follows: [0]: TH (TLP Processing Hint present) [2:1]: PH (TLP Processing Hint) [10:3]: ST (Steering Tag)

18.3.8.17 0x0214 PCIe AXI SLAVE Write Misc Information Other Register1 (Default Value: 0x0000_0000)

Offset: 0x0214			Register Name: SLV_AWMISC_INFO_OTHER_1
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	SLV_AWMISC_INFO_P_TAG AXI Slave Write Request Tag. Sets the TAG number for output posted requests. It is expected that your application normally sets this to '0' except when generating ATS invalidate requests.

18.3.8.18 0x0220 PCIe AXI SLAVE Read Control Register (Default Value: 0x0000_0000)

Offset: 0x0220			Register Name: SLV_ARMISC_CTRL
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:22	R/W	0x00	TLP_FUNC_NUM Function numbering starts at '0'. Not used when CX_SRIOV_ENABLE =1 or CX_ARI_ENABLE =1. For more details, see slv_armisc_info_func_num. This field is only present when multifunction support (CX_NFUNC > 1) is enabled.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0220			Register Name: SLV_ARMISC_CTRL
Bit	Read/Write	Default/Hex	Description
21	R/W	0x0	SLV_ARMISC_CTRL AXI transaction is a DBI access. This is for SHARED DBI mode only.
20:13	R/W	0x00	MSG TLP s MSG Code
12:10	R/W	0x0	TC TLP s TC bits
9	R/W	0x0	RO TLP s RO bit
8	R/W	0x0	NS TLP s NS bit
7	/	/	/
6	R/W	0x0	EP TLP s EP bit
5	/	/	/
4:0	R/W	0x0	TYPE TLP s TYPE

18.3.8.19 0x0224 PCIe AXI SLAVE Read Misc Information ATU Register (Default Value: 0x0000_0000)

Offset: 0x0224			Register Name: SLV_ARMISC_INFO_ATU_BYP
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	SLV_ARMISC_INFO_ATU_BYPASS AXI Slave Read Request Internal ATU Bypass. When set it indicates that this request should not be processed by the internal address translation unit

18.3.8.20 0x0230 PCIe AXI SLAVE Read Misc Information Other Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: SLV_ARMISC_INFO_OTHER
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0230			Register Name: SLV_ARMISC_INFO_OTHER
Bit	Read/Write	Default/Hex	Description
25	R/W	0x0	SLV_ARMISC_INFO_NW AXI Slave Read Transaction's Request AT No Write (NW) Bit. For more details, see 'PCI-SIG Address Translation Services (ATS)'. This is a signal that the application can optionally use. It is not part of the standard AXI interface. For more details, see 'AXI Slave Interface Sideband Signals'.
24	R/W	0x0	SLV_ARMISC_INFO_IDO AXI Slave Read Transaction's IDO bit. Enables ID-base ordering on outbound requests. This is a signal that the application can optionally use. It is not part of the standard AXI interface. For more details, see 'AXI Slave Interface Sideband Signals'.
23:11	/	/	/
10:0	R/W	0x0	SLV_ARMISC_INFO_TPH AXI Slave Read Request TLP Processing Hints. The bits are mapped as follows: [0]: TH (TLP Processing Hint present) [2:1]: PH (TLP Processing Hint) [10:3]: ST (Steering Tag)

18.3.8.21 0x0240 PCIe AXI SLAVE Write Data Misc Information Register (Default Value: 0x0000_0000)

Offset: 0x0240			Register Name: SLV_AWMISC_DATA_INFO
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	SLV_WMISC_INFO AXI Slave Write Data transaction related misc information. This is an optional signal that your application can use to poison write requests. When asserted, the controller sets the Poisoned TLP (EP) bit in the TLP header of the current and subsequent Write Data transactions. It is not a part of the standard AXI interface.

18.3.8.22 0x0250 PCIe AXI Slave Write Response Misc Information Register (Default Value: 0x0000_0000)

Offset: 0x0250			Register Name: SLV_BMISC_INFO
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0250			Register Name: SLV_BMISC_INFO
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	SLV_BMISC_INFO_STATUS slv_bmisc_info_status

18.3.8.23 0x0260 PCIe AXI Slave Read Response Misc Information Register (Default Value: 0x0000_0000)

Offset: 0x0260			Register Name: SLV_RMISC_INFO
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R	0x0	SLV_RMISC_INFO_IDO_STATUS slv_rmisc_info_ido_status
26:14	/	/	/
13:0	R	0x0	MSTR_RMISC_INFO mstr_rmisc_info

18.3.8.24 0x0300 PCIe RADM Target1 Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: RADM_TARGET1
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	R	0x0	RADM_TRGT1_VC radm_trgt1_vc

18.3.8.25 0x0400 PCIe APP Clock Request Register (Default Value: 0x0000_0000)

Offset: 0x0400			Register Name: APP_CLK_REQ_N
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	APP_CLK_REQ_N Indicates that the application logic is ready to have reference clock removed. In designs which support reference clock removal through either L1 PM Sub-states or L1 CPM, the application should set this signal to 1'b when it is ready to have reference clock removed. If the application does not want to remove reference clock it should set this signal to 1'b0.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.3.8.26 0x0500 PCIe APP Initial Reset Register (Default Value: 0x0000_0000)

Offset: 0x0500			Register Name: APP_INIT_RST
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	APP_INIT_RST app_init_rst_ahb Request from your application to send a hot reset to the upstream port. The hot reset request is sent when a single cycle pulse is applied to this pin. In an upstream port, you should set this input to '0'. Note: This signal is not used by the controller to set the SBR field in the BRIDGE_CTRL_INT_PIN_INT_LINE_REG register. During the transition from DL_Active to DL_inactive, assertion of app_init_rst signal indicates a Surprise Down Error, but setting of SBR field in the BRIDGE_CTRL_INT_PIN_INT_LINE_REG register through DBI does not trigger a Surprise Down Error.

18.3.8.27 0x0600 PCIe MSI Ctrl Register0 (Default Value: 0x0000_0000)

Offset: 0x0600			Register Name: MSI_CTRL_0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	MSI_CTRL_IO msi_ctrl_io

18.3.8.28 0x0604 PCIe MSI Ctrl Register1 (Default Value: 0x0000_0000)

Offset: 0x0604			Register Name: MSI_CTRL_1
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	MSI_CTRL_INT_VEC msi_ctrl_int_vec[7:0]

18.3.8.29 0x0610+N*0x20 (N=0~3) PCIe Function Config MSI Enable Register (Default Value: 0x0000_0010)

Offset: 0x0610+N*0x20 (N=0~3)	Register Name: PF_N_CFG_MSI_EN

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14:12	R	0x0	CFG_MULTI_MSI_EN cfg_multi_msi_en[2:0]
11:9	/	/	/
8	R	0x0	CFG_MSI_EXT_DATA_EN cfg_msi_ext_data_en[0]
7:5	/	/	/
4	R	0x1	CFG_MSI_64 cfg_msi_64[0]
3:1	/	/	/
0	R	0x0	CFG_MSI_EN cfg_msi_en[0]

18.3.8.30 0x0614+N*0x20 (N=0~3) PCIe Function Config MSI Mask Register (Default Value: 0x0000_0000)

Offset: 0x0614+N*0x20 (N=0~3)			Register Name: PF_N_CFG_MSI_MASK
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CFG_MSI_MASK cfg_msi_mask[31:0]

18.3.8.31 0x0618+N*0x20 (N=0~3) PCIe Function Config MSI Address Register0 (Default Value: 0x0000_0000)

Offset: 0x0618+N*0x20 (N=0~3)			Register Name: PF_N_CFG_MSI_ADDR_0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CFG_MSI_ADDR_0 cfg_msi_addr[31:0]

18.3.8.32 0x061c+N*0x20 (N=0~3) PCIe Function Config MSI Address Register1 (Default Value: 0x0000_0000)

Offset: 0x061c+N*0x20 (N=0~3)			Register Name: PF_N_CFG_MSI_ADDR_1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CFG_MSI_ADDR_1 cfg_msi_addr[63:32]

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.3.8.33 0x0620+N*0x20 (N=0~3) PCIe Function Config MSI Data Register (Default Value: 0x0000_0000)

Offset: 0x0620+N*0x20 (N=0~3)			Register Name: PF_N_CFG_MSI_DATA
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CFG_MSI_data cfg_msi_data[31:0]

18.3.8.34 0x0624+N*0x20 (N=0~3) PCIe Function Config MSI Pending Register (Default Value: 0x0000_0000)

Offset: 0x0624+N*0x20 (N=0~3)			Register Name: PF_N_CFG_MSI_PEND
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CFG_MSI_PEND cfg_msi_pending[31:0], Indication from application about which functions have a pending associated message. Used to determine the value of the Vector Interrupt Pending register in the MSI Capability structure.

18.3.8.35 0x06f0 PCIe VEN MSI Request Register (Default Value: 0x0000_0000)

Offset: 0x06f0			Register Name: VEN_MSI_REQ
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/WAC	0x0	VEN_MSI_REQ ven_msi_req_ahb, Request from your application to send an MSI when MSI is enabled. When MSI-X is enabled instead of MSI, assertion of ven_msi_req causes the controller to generate an MSI-X message. Once asserted, ven_msi_req must remain asserted until the controller asserts ven_msi_grant.

18.3.8.36 0x06f4 PCIe VEN MSI Ctrl Register (Default Value: 0x0000_0000)

Offset: 0x06f4			Register Name: VEN_MSI_CTRL
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x06f4			Register Name: VEN_MSI_CTRL
Bit	Read/Write	Default/Hex	Description
24:20	R/W	0x0	VEN_MSI_VECTOR Used to modulate the lower five bits of the MSI Data register when multiple message mode is enabled.
19	/	/	/
18:16	R/W	0x0	VEN_MSI_TC Traffic Class of the MSI request, valid when ven_msi_req is asserted.
15:3	/	/	/
2:0	R/W	0x0	VEN_MSI_FUNC_NUM The function number of the MSI request. Function numbering starts at '0'.

18.3.8.37 0x0700 PCIe VEN MSG Request Register (Default Value: 0x0000_0000)

Offset: 0x0700			Register Name: VEN_MSG_REQ
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/WAC	0x0	VEN_MSG_REQ ven_msG_req_ahb, Request from your application to send a vendor-defined Message. Once asserted, ven_msg_req must remain asserted until the controller asserts ven_msg_grant.

18.3.8.38 0x0704 PCIe VEN MSG Config Register0 (Default Value: 0x0000_0000)

Offset: 0x0704			Register Name: VEN_MSG_CFG_0
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	VEN_MSG_CODE The Message Code for the vendor-defined Message TLP.
23:16	/	/	/
15:13	R/W	0x0	VEN_MSG_ATTR The Attributes field for the vendor-defined Message TLP. ▪ Width is three bits when CX_IDO_ENABLE =1 ▪ Width is two bits when CX_IDO_ENABLE =0

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0704			Register Name: VEN_MSG_CFG_0
Bit	Read/Write	Default/Hex	Description
12:8	R/W	0x0	VEN_MSG_TYPE The Type field for the vendor-defined Message TLP.
7:6	R/W	0x0	VEN_MSG_FMT The Format field for the vendor-defined Message TLP. Should be set to 0x1.
5:3	R/W	0x0	VEN_MSG_TC The Traffic Class field for the vendor-defined Message TLP.
2	R/W	0x0	VEN_MSG_TD The TLP Digest (TD) bit for the vendor-defined Message TLP, valid when ven_msg_req is asserted.
1	R/W	0x0	VEN_MSG_EP The Poisoned TLP (EP) bit for the vendor-defined Message TLP.
0	/	/	/

18.3.8.39 0x0708 PCIe VEN MSG Config Register1 (Default Value: 0x0000_0000)

Offset: 0x0708			Register Name: VEN_MSG_CFG_1
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	VEN_MSG_TAG Tag for the vendor-defined Message TLP.
15:13	/	/	/
12:10	R/W	0x0	VEN_MSG_FUNC_NUM Function Number for the vendor-defined Message TLP. Function numbering starts at '0'.
9:0	R/W	0x0	VEN_MSG_LEN The Length field for the vendor-defined Message TLP (indicates length of data payload in dwords). Should be set to 0x0.

18.3.8.40 0x070c PCIe VEN MSG Data Register0 (Default Value: 0x0000_0000)

Offset: 0x070c			Register Name: VEN_MSG_DATA_0
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x070c			Register Name: VEN_MSG_DATA_0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VEN_MSG_DATA_0 fourth dwords of the Vendor Defined Message header where: ▪ Bytes 12-15 (fourth header dword) =ven_msg_data[31:0], where ven_msg_data[7:0] =byte 15

18.3.8.41 0x0710 PCIe VEN MSG Data Register1 (Default Value: 0x0000_0000)

Offset: 0x0710			Register Name: VEN_MSG_DATA_1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VEN_MSG_DATA_1 third dwords of the Vendor Defined Message header where: ▪Bytes 8-11 (third header dword) =ven_msg_data[63:32]

18.3.8.42 0x0800+N*0x10 (N=0~3) PCIe Function SII Config Register0 (Default Value: 0x0080_20F0)

Offset: 0x0800+N*0x10 (N=0~3)			Register Name: PF_N_SII_CFG_0
Bit	Read/Write	Default/Hex	Description
31	R	0x0	CFG_ATTEN_BUTTON_PRESSED_EN cfg_atten_button_pressed_en[0]
30	R	0x0	CFG_PWR_FAULT_DET_EN cfg_pwr_fault_det_en[0]
29	R	0x0	CFG_MRL_SENSOR_CHGED_EN cfg_mrl_sensor_chged_en[0]
28	R	0x0	CFG_PRE_DET_CHGED_EN cfg_pre_det_chged_en[0]
27	R	0x0	CFG_HP_INT_EN cfg_hp_int_en[0]
26	R	0x0	CFG_CMD_CPLED_INT_EN cfg_cmd_cpled_int_en[0]
25	R	0x0	CFG_DLL_STATE_CHGED_EN cfg_dll_state_chged_en[0]
24	R	0x0	CFG_HP_SLOT_CTRL_ACCESS cfg_hp_slot_ctrl_access[0]
23	R	0x1	CFG_RELAX_ORDER_EN cfg_relax_order_en[0]

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0800+N*0x10 (N=0~3)			Register Name: PF_N_SII_CFG_0
Bit	Read/Write	Default/Hex	Description
22	R	0x0	CFG_NO_SNOOP_EN cfg_no_snoop_en[0]
21	R	0x0	CFG_CRS_SW_VIS_EN cfg_crs_sw_vis_en[0]
20	R	0x0	CFG_RCB cfg_rcb[0]
19	/	/	/
18:16	R	0x0	CFG_MAX_PAYLOAD_SIZE cfg_max_payload_size[2:0]
15	/	/	/
14:12	R	0x2	CFG_MAX_RD_REQ_SIZE cfg_max_rd_req_size[2:0]
11:10	/	/	/
9	R	0x0	CFG_MEM_SPACE_EN cfg_mem_space_en[0]
8	R	0x0	CFG_BUS_MASTER_EN cfg_bus_master_en[0]
7:6	R	0x3	CFG_ATTEN_IND cfg_atten_ind[1:0]
5:4	R	0x3	CFG_PWR_IND cfg_pwr_ind[1:0]
3	R	0x0	CFG_PWR_CTRLER_CTRL cfg_pwr_ctrler_ctrl[0]
2	/	/	/
1:0	R	0x0	CFG_TPH_REQ_EN cfg_tph_req_en[1:0]

18.3.8.43 0x0804+N*0x10 (N=0~3) PCIe Function SII Config Register1 (Default Value: 0x0000_0000)

Offset: 0x0804+N*0x10 (N=0~3)			Register Name: PF_N_SII_CFG_1
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:12	R	0x0	CFG_ACS_EGRESS_CTRL_VEC cfg_acs_egress_ctrl_vec[3:0]
11:10	/	/	/
9	R	0x0	CFG_ACS_P2P_DIRECT_TRANSL_EN cfg_acs_p2p_direct_transl_en[0]
8	R	0x0	CFG_ACS_P2P_EGRESS_CTRL_EN cfg_acs_p2p_egress_ctrl_en[0]
7	R	0x0	CFG_ACS_P2P_COMPL_REDIRECT_EN cfg_acs_p2p_compl_redirect_en[0]

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0804+N*0x10 (N=0~3)			Register Name: PF_N_SII_CFG_1
Bit	Read/Write	Default/Hex	Description
6	R	0x0	CFG_ACS_P2P_REQ_REDIRECT_EN cfg_acs_p2p_req_redirect_en[0]
5:3	/	/	/
2	R	0x0	CFG_IDO_CPL_EN cfg_ido_cpl_en[0]
1	R	0x0	CFG_IDO_REQ_EN cfg_ido_req_en[0]
0	/	/	/

18.3.8.44 0x0880+N*0x04 (N=0~3) PCIe Function SII Config LTR Register (Default Value: 0x0000_0000)

Offset: 0x0880+N*0x04 (N=0~3)			Register Name: PF_N_SII_CFG_LTR
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CFG_LTR_MAX_LATENCY cfg_ltr_max_latency[31:0]

18.3.8.45 0x08a0+N*0x04 (N=0~3) PCIe Function SII Config BUS Register (Default Value: 0x0000_0000)

Offset: 0x08a0+N*0x04 (N=0~3)			Register Name: PF_N_SII_CFG_BUS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R	0x0	CFG_SUBBUS_NUM_0 cfg_subbus_num[7:0]
7:0	R	0x0	CFG_2NDBUS_NUM_0 cfg_2ndbus_num[7:0]

18.3.8.46 0x08d0 PCIe SII Config VC Register0 (Default Value: 0x0000_0001)

Offset: 0x08d0			Register Name: SII_CFG_VC_0
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:8	R	0x0	CFG_VC_STRUC_VC_ID_MAP cfg_vc_struc_vc_id_map
7:2	/	/	/
1:0	R	0x1	CFG_VC_ENABLE cfg_vc_enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.3.8.47 0x08d4 PCIe SII Config VC Register1 (Default Value: 0x0000_0000)

Offset: 0x08d4			Register Name: SII_CFG_VC_1
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R	0x0	CFG_VC_ID_VC_STRUC_MAP cfg_vc_id_vc_struc_map

18.3.8.48 0x08d8 PCIe SII Config TC Register (Default Value: 0x0000_00ff)

Offset: 0x08d8			Register Name: SII_CFG_TC
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	CFG_TC_STRUC_VC_ID_MAP cfg_tc_struc_vc_id_map
7:0	R	0xff	CFG_TC_ENABLE cfg_tc_enable

18.3.8.49 0x08dc PCIe SII Config LTR ACS Register (Default Value: 0x0000_0000)

Offset: 0x08dc			Register Name: SII_CFG_LTR_ACS
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10	R	0x0	CFG_ACS_UP_FORWARD_EN cfg_acs_up_forward_en
9	R	0x0	CFG_ACS_AT_BLOCKING_EN cfg_acs_at_blocking_en
8	R	0x0	CFG_ACS_VALIDATION_EN cfg_acs_validation_en
7:5	/	/	/
4	R	0x0	CFG_DISABLE_LTR_CLR_MSG cfg_disable_ltr_clr_msg
3:1	/	/	/
0	R	0x0	CFG_LTR_M_EN cfg_ltr_m_en

18.3.8.50 0x08e0 PCIe SII Config PBUS Register (Default Value: 0x0000_0000)

Offset: 0x08e0			Register Name: SII_CFG_PBUS
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R	0x0	CFG_PBUS_DEV_NUM cfg_pbus_dev_num

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x08e0			Register Name: SII_CFG_PBUS
Bit	Read/Write	Default/Hex	Description
15:8	/	/	/
7:0	R	0x0	CFG_PBUS_NUM cfg_pbus_num

18.3.8.51 0x0a00 PCIe SII Electromechanical Register (Default Value: 0x0000_0000)

Offset: 0x0a00			Register Name: SII_ELEC
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SYS_EML_INTERLOCK_ENGAGED_3 sys_eml_interlock_engaged[3] , System Electromechanical Interlock Engaged. Indicates whether the system electromechanical interlock is engaged and controls the state of the Electromechanical Interlock Status bit in the Slot Status register.
30	R/W	0x0	SYS_CMD_CPLED_INT_3 sys_cmd_cpled_int[3] , Command completed Interrupt. Indicates that the Hot-Plug controller completed a command. There is a separate sys_cmd_cpled_int input bit for each function in your controller configuration
29	R/W	0x0	SYS_PRE_DET_CHGED_3 sys_pre_det_chged[3] , Presence Detect Changed. Indicates that the state of card present detector has changed. There is a separate sys_pre_det_chged input bit for each function in your controller configuration.
28	R/W	0x0	SYS_MRL_SENSOR_CHGED_3 sys_mrl_sensor_chged[3] , MRL Sensor Changed. Indicates that the state of MRL sensor has changed. There is a separate sys_mrl_sensor_chged input bit for each function in your controller configuration.
27	R/W	0x0	SYS_PWR_FAULT_DET_3 sys_pwr_fault_det[3] , Power Fault Detected. Indicates the power controller detected a power fault at this slot. There is a separate sys_pwr_fault_det input bit for each function in your controller configuration.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0a00			Register Name: SII_ELEC
Bit	Read/Write	Default/Hex	Description
26	R/W	0x0	SYS_MRL_SENSOR_STATE_3 sys_mrl_sensor_state[3] , MRL Sensor State. Indicates the state of the manually-operated retention latch (MRL) sensor: 0: MRL is closed 1: MRL is open There is a separate sys_mrl_sensor_state input bit for each function in your controller configuration.
25	R/W	0x0	SYS_PRE_DET_STATE_3 sys_pre_det_state[3] , Presence Detect State. Indicates whether or not a card is present in the slot: 0: Slot is empty 1: Card is present in the slot There is a separate sys_pre_det_state input bit for each function in your controller configuration.
24	R/W	0x0	SYS_ATTEN_BUTTON_PRESSED_3 sys_atten_button_pressed[3] , Attention Button Pressed. Indicates that the system attention button was pressed, sets the Attention Button Pressed bit in the Slot Status Register. There is a separate sys_atten_button_pressed input bit for each function in your controller configuration.
23	R/W	0x0	SYS_EML_INTERLOCK_ENGAGED_2 sys_eml_interlock_engaged[2] , System Electromechanical Interlock Engaged. Indicates whether the system electromechanical interlock is engaged and controls the state of the Electromechanical Interlock Status bit in the Slot Status register.
22	R/W	0x0	SYS_CMD_CPLED_INT_2 sys_cmd_cpled_int[2] , Command completed Interrupt. Indicates that the Hot-Plug controller completed a command. There is a separate sys_cmd_cpled_int input bit for each function in your controller configuration.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0a00			Register Name: SII_ELEC
Bit	Read/Write	Default/Hex	Description
21	R/W	0x0	SYS_PRE_DET_CHGED_2 sys_pre_det_chged[2] , Presence Detect Changed. Indicates that the state of card present detector has changed. There is a separate sys_pre_det_chged input bit for each function in your controller configuration.
20	R/W	0x0	SYS_MRL_SENSOR_CHGED_2 sys_mrl_sensor_chged[2] , MRL Sensor Changed. Indicates that the state of MRL sensor has changed. There is a separate sys_mrl_sensor_chged input bit for each function in your controller configuration.
19	R/W	0x0	SYS_PWR_FAULT_DET_2 sys_pwr_fault_det[2] . Power Fault Detected. Indicates the power controller detected a power fault at this slot. There is a separate sys_pwr_fault_det input bit for each function in your controller configuration.
18	R/W	0x0	SYS_MRL_SENSOR_STATE_2 sys_mrl_sensor_state[2] , MRL Sensor State. Indicates the state of the manually-operated retention latch (MRL) sensor: 0: MRL is closed 1: MRL is open There is a separate sys_mrl_sensor_state input bit for each function in your controller configuration.
17	R/W	0x0	SYS_PRE_DET_STATE_2 sys_pre_det_state[2] , Presence Detect State. Indicates whether or not a card is present in the slot: 0: Slot is empty 1: Card is present in the slot There is a separate sys_pre_det_state input bit for each function in your controller configuration.
16	R/W	0x0	SYS_ATTEN_BUTTON_PRESSED_2 sys_atten_button_pressed[2] , Attention Button Pressed. Indicates that the system attention button was pressed, sets the Attention Button Pressed bit in the Slot Status Register. There is a separate sys_atten_button_pressed input bit for each function in your controller configuration.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0a00			Register Name: SII_ELEC
Bit	Read/Write	Default/Hex	Description
15	R/W	0x0	SYS_EML_INTERLOCK_ENGAGED_1 sys_eml_interlock_engaged[1] , System Electromechanical Interlock Engaged. Indicates whether the system electromechanical interlock is engaged and controls the state of the Electromechanical Interlock Status bit in the Slot Status register.
14	R/W	0x0	SYS_CMD_CPLED_INT_1 sys_cmd_cpled_int[1] , Command completed Interrupt. Indicates that the Hot-Plug controller completed a command. There is a separate sys_cmd_cpled_int input bit for each function in your controller configuration.
13	R/W	0x0	SYS_PRE_DET_CHGED_1 sys_pre_det_chged[1] , Presence Detect Changed. Indicates that the state of card present detector has changed. There is a separate sys_pre_det_chged input bit for each function in your controller configuration.
12	R/W	0x0	SYS_MRL_SENSOR_CHGED_1 sys_mrl_sensor_chged[1] , MRL Sensor Changed. Indicates that the state of MRL sensor has changed. There is a separate sys_mrl_sensor_chged input bit for each function in your controller configuration.
11	R/W	0x0	SYS_PWR_FAULT_DET_1 sys_pwr_fault_det[1] , Power Fault Detected. Indicates the power controller detected a power fault at this slot. There is a separate sys_pwr_fault_det input bit for each function in your controller configuration.
10	R/W	0x0	SYS_MRL_SENSOR_STATE_1 sys_mrl_sensor_state[1] , MRL Sensor State. Indicates the state of the manually-operated retention latch (MRL) sensor: 0: MRL is closed 1: MRL is open There is a separate sys_mrl_sensor_state input bit for each function in your controller configuration.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0a00			Register Name: SII_ELEC
Bit	Read/Write	Default/Hex	Description
9	R/W	0x0	SYS_PRE_DET_STATE_1 sys_pre_det_state[1] , Presence Detect State. Indicates whether or not a card is present in the slot: 0: Slot is empty 1: Card is present in the slot There is a separate sys_pre_det_state input bit for each function in your controller configuration.
8	R/W	0x0	SYS_ATTEN_BUTTON_PRESSED_1 sys_atten_button_pressed[1] , Attention Button Pressed. Indicates that the system attention button was pressed, sets the Attention Button Pressed bit in the Slot Status Register. There is a separate sys_atten_button_pressed input bit for each function in your controller configuration.
7	R/W	0x0	SYS_EML_INTERLOCK_ENGAGED_0 sys_eml_interlock_engaged[0] , System Electromechanical Interlock Engaged. Indicates whether the system electromechanical interlock is engaged and controls the state of the Electromechanical Interlock Status bit in the Slot Status register.
6	R/W	0x0	SYS_CMD_CPLED_INT_0 sys_cmd_cpled_int[0] , Command completed Interrupt. Indicates that the Hot-Plug controller completed a command. There is a separate sys_cmd_cpled_int input bit for each function in your controller configuration.
5	R/W	0x0	SYS_PRE_DET_CHGED_0 sys_pre_det_chged[0], Presence Detect Changed. Indicates that the state of card present detector has changed. There is a separate sys_pre_det_chged input bit for each function in your controller configuration.
4	R/W	0x0	SYS_MRL_SENSOR_CHGED_0 sys_mrl_sensor_chged[0] , MRL Sensor Changed. Indicates that the state of MRL sensor has changed. There is a separate sys_mrl_sensor_chged input bit for each function in your controller configuration.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0a00			Register Name: SII_ELEC
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	SYS_PWR_FAULT_DET_0 sys_pwr_fault_det[0] , Power Fault Detected. Indicates the power controller detected a power fault at this slot. There is a separate sys_pwr_fault_det input bit for each function in your controller configuration.
2	R/W	0x0	SYS_MRL_SENSOR_STATE_0 sys_mrl_sensor_state[0] , MRL Sensor State. Indicates the state of the manually-operated retention latch (MRL) sensor: 0: MRL is closed 1: MRL is open There is a separate sys_mrl_sensor_state input bit for each function in your controller configuration.
1	R/W	0x0	SYS_PRE_DET_STATE_0 sys_pre_det_state[0] , Presence Detect State. Indicates whether or not a card is present in the slot: 0: Slot is empty 1: Card is present in the slot There is a separate sys_pre_det_state input bit for each function in your controller configuration.
0	R/W	0x0	SYS_ATTEN_BUTTON_PRESSED_0 sys_atten_button_pressed[0] , Attention Button Pressed. Indicates that the system attention button was pressed, sets the Attention Button Pressed bit in the Slot Status Register. There is a separate sys_atten_button_pressed input bit for each function in your controller configuration.

18.3.8.52 0x0a04 PCIe SII CFG EML Register (Default Value: 0x0000_0000)

Offset: 0x0a04			Register Name: SII_CFG_EML
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R	0x0	CFG_EML_CONTROL_3 cfg_eml_control[3]
2	R	0x0	CFG_EML_CONTROL_2 cfg_eml_control[2]

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0a04			Register Name: SII_CFG_EML
Bit	Read/Write	Default/Hex	Description
1	R	0x0	CFG_EML_CONTROL_1 cfg_eml_control[1]
0	R	0x0	CFG_EML_CONTROL_0 cfg_eml_control[0]

18.3.8.53 0x0b00 PCIe FRS INT Register (Default Value: 0x0000_0000)

Offset: 0x0b00			Register Name: FRS_INT_MSG_NUM
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R	0x0	FRSQ_INT_MSG_NUM_3 frsq_int_msg_num[19:15]
23:21	/	/	/
20:16	R	0x0	FRSQ_INT_MSG_NUM_2 frsq_int_msg_num[14:10]
15:13	/	/	/
12:8	R	0x0	FRSQ_INT_MSG_NUM_1 frsq_int_msg_num[9:5]
7:5	/	/	/
4:0	R	0x0	FRSQ_INT_MSG_NUM_0 frsq_int_msg_num[4:0]

18.3.8.54 0x0b04 PCIe FRS READY Register (Default Value: 0x0000_0000)

Offset: 0x0b04			Register Name: FRS_READY
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	APP_PF3_FRS_READY app_pf_frs_ready[3] Defers FRS messaging when set to '0'.
6	R/W	0x0	APP_PF2_FRS_READY app_pf_frs_ready[2] Defers FRS messaging when set to '0'.
5	R/W	0x0	APP_PF1_FRS_READY app_pf_frs_ready[1] Defers FRS messaging when set to '0'.
4	R/W	0x0	APP_PF0_FRS_READY app_pf_frs_ready[0] Defers FRS messaging when set to '0'.
3:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0b04			Register Name: FRS_READY
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	APP_DRS_READY Defers DRS messaging when set to '0'.

18.3.8.55 0x0c00 PCIe LTSSM Enable Register (Default Value: 0x0000_0040)

Offset: 0x0c00			Register Name: PCIE_LTSSM_ENABLE
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	APP_DBI_RO_WR_DISABLE app_dbi_ro_wr_disable DBI Read-only Write Disable 0: MISC_CONTROL_1_OFF.DBI_RO_WR_EN register field is read-write. 1: MISC_CONTROL_1_OFF.DBI_RO_WR_EN register field is forced to 0 and is read-only.
30:9	/	/	/
8	R/W	0x0	APP_REQ_RETRY_EN Provides a capability to defer incoming configuration requests until initialization is complete. When app_req_retry_en is asserted, the controller completes incoming configuration requests with a configuration request retry status. Other incoming requests complete normally. When the Readiness Notification mechanism is supported, DRS messaging is blocked when app_req_retry_en=1. When app_req_retry_en=0 and app_drs_ready=1, the controller autonomously transmits a DRS message when the link transitions from DL_Down to DL_Up.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0c00			Register Name: PCIE_LTSSM_ENABLE
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0x4	DEVICE_TYPE Device/port type. Indicates the specific type of this PCI Express function. It is also used to set the 'Device/Port Type' field of the 'PCI Express Capabilities Register'. The controller uses this input to determine the operating mode of the controller at run time. Defined encodings are: ▪ 0000: PCI Express endpoint ▪ 0001: Legacy PCI Express endpoint ▪ 0100: Root port of PCI Express root complex All other encodings (including those for PCI/PCI-X bridges and RC Integrated endpoint) are not supported. If CX_CROSSLINK_ENABLE is defined and when smlh_crosslink_active is '1' then the value device_type is modified as follows before being used internally in the controller: ▪ if device_type =4'b0100 then device_type =4'b0000 ▪ if device_type =4'b000x then device_type =4'b0100
3:1	/	/	/
0	R/W	0x0	APP_LTSSM_ENABLE Link Training Enable 0: Disable link training 1: Enable link training Driven low by your application after cold, warm or hot reset to hold the LTSSM in the Detect state until your application is ready for the link training to begin. When your application has finished reprogramming the controller configuration registers using the DBI, it asserts app_ltssm_enable to allow the LTSSM to continue link establishment. Can also be used to delay hot resetting of the controller until you have read out any register status. Cold Reset: ▪ Optionally hold LTSSM and delay link training, so that you can reprogram some registers through DBI. ▪ Set app_ltssm_enable =0 before your application de-asserts Power-On Reset (power_up_rst_n). Best way is to set

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0c00			Register Name: PCIE_LTSSM_ENABLE
Bit	Read/Write	Default/Hex	Description
			app_ltssm_enable =0 at power-up or at assertion of core_rst_n. ▪ Wait for de-assertion of core_rst_n, sticky_rst_n, and non_sticky_rst_n. ▪ Write any register through DBI. ▪ Set app_ltssm_enable =1. ▪ Link training starts. Hot Reset (Link Down Reset) : ▪ Optionally delay reset of the controller, so that you can read some registers through DBI. ▪ Set app_ltssm_enable =0 immediately (combinatorically) upon falling edge of smlh_req_rst_not. ▪ Keep app_ltssm_enable =0 until bridge finishes "flushing mode". ▪ Read any register through DBI. ▪ Set app_ltssm_enable =1. ▪ Reset of controller begins (sticky_rst is not asserted). ▪ Optionally hold LTSSM and delay link training, so that you can reprogram some registers through DBI. ▪ Set app_ltssm_enable =0 immediately (combinatorically) upon falling edge of core_rst_n. ▪ Write any register through DBI. ▪ Set app_ltssm_enable =1. ▪ Link training starts. ▪ Note: For Hot Reset, you can do both or either of the above (delay reset and/or delay link training). If you do both, you must do in order presented. To do otherwise (that is, de-assert it outside of the Detect LTSSM state) causes the controller to be reset and the LTSSM moves immediately back to the Detect state. This transition is outside of the PCIe Specification and it might cause a PIPE protocol violation.

18.3.8.56 0x0d00 PCIe SII General Messaging Register (Default Value: 0x0000_0000)

Offset: 0x0d00	Register Name: SII_GEN_MES

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R	0x0	CFG_BR_CTRL_SERREN_3 cfg_br_ctrl_serren[3]
14	R	0x0	CFG_SEND_F_ERR_3 cfg_send_f_err[3]
13	R	0x0	CFG_SEND_NF_ERR_3 cfg_send_nf_err[3]
12	R	0x0	CFG_SEND_COR_ERR_3 cfg_send_cor_err[3]
11	R	0x0	CFG_BR_CTRL_SERREN_2 cfg_br_ctrl_serren[2]
10	R	0x0	CFG_SEND_F_ERR_2 cfg_send_f_err[2]
9	R	0x0	CFG_SEND_NF_ERR_2 cfg_send_nf_err[2]
8	R	0x0	CFG_SEND_COR_ERR_2 cfg_send_cor_err[2]
7	R	0x0	CFG_BR_CTRL_SERREN_1 cfg_br_ctrl_serren[1]
6	R	0x0	CFG_SEND_F_ERR_1 cfg_send_f_err[1]
5	R	0x0	CFG_SEND_NF_ERR_1 cfg_send_nf_err[1]
4	R	0x0	CFG_SEND_COR_ERR_1 cfg_send_cor_err[1]
3	R	0x0	CFG_BR_CTRL_SERREN_0 cfg_br_ctrl_serren[0]
2	R	0x0	CFG_SEND_F_ERR_0 cfg_send_f_err[0]
1	R	0x0	CFG_SEND_NF_ERR_0 cfg_send_nf_err[0]
0	R	0x0	CFG_SEND_COR_ERR_0 cfg_send_cor_err[0]

18.3.8.57 0x0d04 PCIe SII RADM Messaging Register0 (Default Value: 0x0000_0000)

Offset: 0x0d04			Register Name: SII_RADM_MES_0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RADM_MSG_PAYLOAD_STATUS radm_msg_payload_status[31:0]

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.3.8.58 0x0d08 PCIe SII RADM Messaging Register1 (Default Value: 0x0000_0000)

Offset: 0x0d08			Register Name: SII_RADM_MES_1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RADM_MSG_PAYLOAD_STATUS radm_msg_payload_status[63:32]

18.3.8.59 0x0d0c PCIe SII RADM Messaging Register2 (Default Value: 0x0000_0000)

Offset: 0x0d0c			Register Name: SII_RADM_MES_2
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	RADM_MSG_REQ_ID_STATUS radm_msg_req_id_status

18.3.8.60 0x0e00 PCIe SII Interrupt Mask Register0 (Default Value: 0x0000_0000)

Offset: 0x0e00			Register Name: SII_INT_MASK_0
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	RADM_PM_TURNOFF_MASK 0: Mask 1: Not Mask
30	R/W	0x0	RADM_MSG_UNLOCK_MASK 0: Mask 1: Not Mask
29	R/W	0x0	RADM_MSG_LTR_MASK 0: Mask 1: Not Mask
28	R/W	0x0	DEASSERT_INTD_GRT_MASK 0: Mask 1: Not Mask
27	R/W	0x0	DEASSERT_INTC_GRT_MASK 0: Mask 1: Not Mask
26	R/W	0x0	DEASSERT_INTB_GRT_MASK 0: Mask 1: Not Mask
25	R/W	0x0	DEASSERT_INTA_GRT_MASK 0: Mask 1: Not Mask

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e00			Register Name: SII_INT_MASK_0
Bit	Read/Write	Default/Hex	Description
24	R/W	0x0	ASSERT_INTD_GRT_MASK 0: Mask 1: Not Mask
23	R/W	0x0	ASSERT_INTC_GRT_MASK 0: Mask 1: Not Mask
22	R/W	0x0	ASSERT_INTB_GRT_MASK 0: Mask 1: Not Mask
21	R/W	0x0	ASSERT_INTA_GRT_MASK 0: Mask 1: Not Mask
20	R/W	0x0	CFG_LINK_EQ_REQ_INT_MASK 0: Mask 1: Not Mask
19	R/W	0x0	CFG_BW_MGT_MSI_MASK 0: Mask 1: Not Mask
18	R/W	0x0	CFG_BW_MGT_INT_MASK 0: Mask 1: Not Mask
17	R/W	0x0	CFG_LINK_AUTO_BW_MSI_MASK 0: Mask 1: Not Mask
16	R/W	0x0	CFG_LINK_AUTO_BW_INT_MASK 0: Mask 1: Not Mask
15	R/W	0x0	PF0_HP_MSI_MASK 0: Mask 1: Not Mask
14	R/W	0x0	PF0_HP_INT_MASK 0: Mask 1: Not Mask
13	R/W	0x0	PF0_HP_PME_MASK 0: Mask 1: Not Mask
12	R/W	0x0	RADM_INTD_DEASSERTED_MASK 0: Mask 1: Not Mask
11	R/W	0x0	RADM_INTC_DEASSERTED_MASK 0: Mask 1: Not Mask

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e00			Register Name: SII_INT_MASK_0
Bit	Read/Write	Default/Hex	Description
10	R/W	0x0	RADM_INTB_DEASSERTED_MASK 0: Mask 1: Not Mask
9	R/W	0x0	RADM_INTA_DEASSERTED_MASK 0: Mask 1: Not Mask
8	R/W	0x0	RADM_INTD_ASSERTED_MASK 0: Mask 1: Not Mask
7	R/W	0x0	RADM_INTC_ASSERTED_MASK 0: Mask 1: Not Mask
6	R/W	0x0	RADM_INTB_ASSERTED_MASK 0: Mask 1: Not Mask
5	R/W	0x0	RADM_INTA_ASSERTED_MASK 0: Mask 1: Not Mask
4	R/W	0x0	PF0_CFG_PME_MSI_MASK 0: Mask 1: Not Mask
3	R/W	0x0	PF0_CFG_PME_INT_MASK 0: Mask 1: Not Mask
2	R/W	0x0	PF0_CFG_AER_RC_ERR_MSI_MASK 0: Mask 1: Not Mask
1	R/W	0x0	PF0_CFG_AER_RC_ERR_INT_MASK 0: Mask 1: Not Mask
0	R/W	0x0	PF0_CFG_VPD_INT_MASK 0: Mask 1: Not Mask

18.3.8.61 0x0e04 PCIe SII Interrupt Mask Register1 (Default Value: 0x0000_0000)

Offset: 0x0e04			Register Name: SII_INT_MASK_1
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PCIe_WAKE_N_MASK 0: Mask 1: Not Mask

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e04			Register Name: SII_INT_MASK_1
Bit	Read/Write	Default/Hex	Description
30	R/W	0x0	WAKE_MASK 0: Mask 1: Not Mask
29	R/W	0x0	RADM_PM_TO_ACK_MASK 0: Mask 1: Not Mask
28	R/W	0x0	RADM_PM_PME_MASK 0: Mask 1: Not Mask
27	R/W	0x0	RADM_FATAL_ERR_MASK 0: Mask 1: Not Mask
26	R/W	0x0	RADM_NONFATAL_ERR_MASK 0: Mask 1: Not Mask
25	R/W	0x0	RADM_CORRECTABLE_ERR_MASK 0: Mask 1: Not Mask
24	R/W	0x0	CFG_SYS_ERR_RC_MASK 0: Mask 1: Not Mask
23	/	/	/
22	R/W	0x0	TRAINING_RST_N_MASK 0: Mask 1: Not Mask
21	R/W	0x0	PF0_FRS_GRANT_MASK 0: Mask 1: Not Mask
20	R/W	0x0	RADM_VENDOR_MSG_MASK 0: Mask 1: Not Mask
19	/	/	Reserved
18	R/W	0x0	PF0_FRSQ_MSI_MASK 0: Mask 1: Not Mask
17	R/W	0x0	PF0_CFG_UP_DRS_TO_FRS_MASK 0: Mask 1: Not Mask
16	R/W	0x0	PF0_CFG_DRS_MSI_MASK 0: Mask 1: Not Mask

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e04			Register Name: SII_INT_MASK_1
Bit	Read/Write	Default/Hex	Description
15	R/W	0x0	PF3_DPA_SUBSTATE_UPDATE_MASK 0: Mask 1: Not Mask
14	R/W	0x0	PF2_DPA_SUBSTATE_UPDATE_MASK 0: Mask 1: Not Mask
13	R/W	0x0	PF1_DPA_SUBSTATE_UPDATE_MASK 0: Mask 1: Not Mask
12	R/W	0x0	PF0_DPA_SUBSTATE_UPDATE_MASK 0: Mask 1: Not Mask
11	R/W	0x0	PCIe_PERI_AR_INT_MASK 0: Mask 1: Not Mask
10	R/W	0x0	PCIe_PERI_AW_INT_MASK 0: Mask 1: Not Mask
9	R/W	0x0	RADM_QOVERFLOW_1_MASK 0: Mask 1: Not Mask
8	R/W	0x0	RADM_QOVERFLOW_0_MASK 0: Mask 1: Not Mask
7:5	/	/	/
4	R/W	0x0	RTLH_RFC_UPD_0_MASK 0: Mask 1: Not Mask
3	R/W	0x0	LINK_REQ_RST_NOT_MASK 0: Mask 1: Not Mask
2	R/W	0x0	SMLH_REQ_RST_NOT_MASK 0: Mask 1: Not Mask
1	R/W	0x0	RDLH_LINK_UP_INT_MASK RDLH Link Up Interrupt Mask 0: Mask 1: Not Mask
0	R/W	0x0	SMLH_LINK_UP_INT_MASK SMLH Link Up Interrupt Mask 0: Mask 1: Not Mask

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.3.8.62 0x0e08 PCIe SII Interrupt Register0 (Default Value: 0x0000_0000)

Offset: 0x0e08			Register Name: SII_INT_0
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	RADM_PM_TURNOFF One-clock-cycle pulse that indicates that the controller received a PME Turnoff message. When RX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then no indication is given for the second message.
30	R/W1C	0x0	RADM_MSG_UNLOCK One-cycle pulse that indicates that the controller received an Unlock message. When RX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then no separate indication is given for the second message.
29	R/W1C	0x0	RADM_MSG_LTR One-clock-cycle pulse that indicates that the controller received an LTR message. The controller makes the message header available the radm_msg_payload output. It is also available the app_ltr_latency output. When RX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then no separate indication is given for the second message.
28	R/W1C	0x0	DEASSERT_INTD_GRT The signal deassert_intd_grt is a one-clock-cycle pulse that indicates that the controller sent an Deassert_INTD Message to the upstream device.
27	R/W1C	0x0	DEASSERT_INTC_GRT The signal deassert_intc_grt is a one-clock-cycle pulse that indicates that the controller sent an Deassert_INTC Message to the upstream device.
26	R/W1C	0x0	DEASSERT_INTB_GRT The signal deassert_intb_grt is a one-clock-cycle pulse that indicates that the controller sent an Deassert_INTB Message to the upstream device.
25	R/W1C	0x0	DEASSERT_INTA_GRT The signal deassert_inta_grt is a one-clock-cycle pulse that indicates that the controller sent an Deassert_INTA Message to the upstream device.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e08			Register Name: SII_INT_0
Bit	Read/Write	Default/Hex	Description
24	R/W1C	0x0	ASSERT_INTD_GRT The signal assert_intd_grt is a one-clock-cycle pulse that indicates that the controller sent an Assert_INTD Message to the upstream device.
23	R/W1C	0x0	ASSERT_INTC_GRT The signal assert_intd_grt is a one-clock-cycle pulse that indicates that the controller sent an Assert_INTD Message to the upstream device.
22	R/W1C	0x0	ASSERT_INTB_GRT The signal assert_intb_grt is a one-clock-cycle pulse that indicates that the controller sent an Assert_INTB Message to the upstream device.
21	R/W1C	0x0	ASSERT_INTA_GRT The signal assert_inta_grt is a one-clock-cycle pulse that indicates that the controller sent an Assert_INTA Message to the upstream device.
20	R/W1C	0x0	CFG_LINK_EQ_REQ_INT Interrupt indicating to your application that the Link Equalization Request bit in the Link Status 2 Register has been set and the Link Equalization Request Interrupt Enable (Link Control 3 Register bit 1) is set.
19	R/W1C	0x0	CFG_BW_MGT_MSI The controller sets this pin when following conditions are true: ▪ MSI or MSI-X is enabled. ▪ The Link Bandwidth Management Status register (Link Control Status register bit 14) is updated ▪ The Link Bandwidth Management Interrupt Enable (Link Control register bit 10) is set. reuse-pragma beginAttr Description This pin is set as a notification when the Link Bandwidth Management Status register (Link Status register bit 14) is updated and the Link Bandwidth Management Interrupt Enable (Link Control register bit 10) is set and in addition the msi or msix aare enabled. This bit is not applicable to, and is reserved, for endpoint devices and upstream ports of Switches. For upstream port: Reserved. <ct:CX_IS_EP>Reserved.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e08			Register Name: SII_INT_0
Bit	Read/Write	Default/Hex	Description
18	R/W1C	0x0	CFG_BW_MGT_INT The controller asserts cfg_bw_mgt_int when all of the following conditions are true: ▪ The INTx Assertion Disable bit in the Command register is 0, and ▪ The Bandwidth Management Interrupt Enable bit in the Link Control register is set to 1, and ▪ The Bandwidth Management Interrupt Status bit in the Link Status register is set to 1. The cfg_bw_mgt_msi output is a pulse signal (only asserted for one clock cycle); but cfg_bw_mgt_int is a level signal. For upstream port: Reserved.
17	R/W1C	0x0	CFG_LINK_AUTO_BW_MSI The controller sets this pin when following conditions are true: ▪ MSI or MSI-X is enabled. ▪ The Link Autonomous Bandwidth Status register (Link Status register bit 15) is updated. ▪ The Link Autonomous Bandwidth Interrupt Enable (Link Control register bit 11) is set. The controller does not check if the associated MSI vector (asserted cfg_pcie_cap_int_msg_num) is unmasked. It is up to the application to check whether the vector is masked or unmasked. For upstream port: Reserved. <ct:CX_IS_EP>Reserved.
16	R/W1C	0x0	CFG_LINK_AUTO_BW_INT The controller asserts cfg_link_auto_bw_int when all of the following conditions are true: ▪ The INTx assertion disable bit in the Command register is 0, and ▪ The Link Autonomous Bandwidth Interrupt Enable bit in the Link Control register is set to 1, and ▪ The Link Autonomous Bandwidth Interrupt Status bit in the Link Status register is set to 1. The cfg_link_auto_bw_msi output is a pulse signal (only asserted for one clock cycle); but cfg_link_auto_bw_int is a level signal. For upstream port: Reserved.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e08			Register Name: SII_INT_0
Bit	Read/Write	Default/Hex	Description
15	R/W1C	0x0	PF0_HP_MSI The controller asserts hp_msi (as a one-cycle pulse) when the logical AND of the following conditions transitions from false to true: ▪ MSI or MSI-X is enabled. ▪ Hot-Plug interrupts are enabled in the Slot Control register. ▪ Any bit in the Slot Status register transitions from 0 to 1 and the associated event notification is enabled in the Slot Control register. There is one bit of hp_int for each configured function. The controller pulses the hp_msi output only when any of the hot plug status bits change from 0 to 1 (as is hp_pme).
14	R/W1C	0x0	PF0_HP_INT The controller asserts hp_int when all of the following conditions are true: ▪ The INTx Assertion Disable bit in the Command register is 0. ▪ Hot-Plug interrupts are enabled in the Slot Control register. ▪ Any bit in the Slot Status register is equal to 1, and the associated event notification is enabled in the Slot Control register. There is one bit of hp_int for each configured function.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e08			Register Name: SII_INT_0
Bit	Read/Write	Default/Hex	Description
13	R/W1C	0x0	PF0_HP_PME The controller asserts hp_pme when all of the following conditions are true: ▪ The PME Enable bit in the Power Management Control and Status register is set to 1. ▪ Any bit in the Slot Status register transitions from 0 to 1 and the associated event notification is enabled in the Slot Control register. The controller does not check if the PM state is D1, D2, or D3hot. It is up to your application to check the value pm_dstate to make sure the device is in D1, D2, or D3hot. There is one bit of hp_pme for each configured function. The controller pulses the hp_pme output only when any hot plug status bit changes from 0 to 1 (as is hp_msi). hp_int stays asserted as long as the status bit is set. In addition, it asserts hp_pme only if PME is enabled, but it does not matter if hot-plug interrupts are enabled.
12	R/W1C	0x0	RADM_INTD_DEASSERTED One-clock-cycle pulse that indicates that the controller received a Deassert_INTD Message from the downstream device.
11	R/W1C	0x0	RADM_INTC_DEASSERTED One-clock-cycle pulse that indicates that the controller received a Deassert_INTC Message from the downstream device.
10	R/W1C	0x0	RADM_INTB_DEASSERTED One-clock-cycle pulse that indicates that the controller received a Deassert_INTB Message from the downstream device.
9	R/W1C	0x0	RADM_INTA_DEASSERTED One-clock-cycle pulse that indicates that the controller received a Deassert_INTA Message from the downstream device.
8	R/W1C	0x0	RADM_INTD_ASSERTED One-clock-cycle pulse that indicates that the controller received an Assert_INTD Message from the downstream device.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e08			Register Name: SII_INT_0
Bit	Read/Write	Default/Hex	Description
7	R/W1C	0x0	RADM_INTC_ASSERTED One-clock-cycle pulse that indicates that the controller received an Assert_INTC Message from the downstream device.
6	R/W1C	0x0	RADM_INTB_ASSERTED One-clock-cycle pulse that indicates that the controller received an Assert_INTB Message from the downstream device.
5	R/W1C	0x0	RADM_INTA_ASSERTED One-clock-cycle pulse that indicates that the controller received an Assert_INTA Message from the downstream device.
4	R/W1C	0x0	PF0_CFG_PME_MSI The controller asserts cfg_pme_msi (as a one-cycle pulse) when all of the following conditions are true: ▪ MSI or MSI-X is enabled. ▪ The PME Interrupt Enable bit in the Root Control register is set to 1. ▪ The PME Status bit in the Root Status register is set to 1. The controller does not check if the associated MSI vector (asserted cfg_pcie_cap_int_msg_num) is unmasked. It is up to the application to check whether the vector is masked or unmasked.
3	R/W1C	0x0	PF0_CFG_PME_INT The controller asserts cfg_pme_int when all of the following conditions are true: ▪ The INTx Assertion Disable bit in the Command register is 0. ▪ The PME Interrupt Enable bit in the Root Control register is set to 1. ▪ The PME Status bit in the Root Status register is set to 1. The cfg_pme_msi output is a pulse signal (only asserted for one clock cycle). But cfg_pme_int is a level signal; essentially an AND of the PME interrupt enable and receipt of the pm_pme message.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e08			Register Name: SII_INT_0
Bit	Read/Write	Default/Hex	Description
2	R/W1C	0x0	PF0_CFG_AER_RC_ERR_MSI The controller asserts cfg_aer_rc_err_msi for one clock cycle when all of the following conditions are true: ▪ MSI or MSI-X is enabled. ▪ A reported error condition causes a bit to be set in the Root Error Status register. ▪ The associated error message reporting enable bit is set in the Root Error Command register. The controller does not check if the associated MSI vector (asserted cfg_aer_int_msg_num) is unmasked. It is up to the application to check whether the vector is masked or unmasked.
1	R/W1C	0x0	PF0_CFG_AER_RC_ERR_INT Asserted when a reported error condition causes a bit to be set in the Root Error Status register and the associated error message reporting enable bit is set in the Root Error Command register. cfg_aer_rc_err_int is set when the RC internally generates an error or when an error message is received by the RC. Because the RC itself generates it, this needs to be propagated up to the system software which would then need to read the error registers to see which error occurred. Note: This signal is used when MSI/MSI-X is NOT enabled; otherwise see cfg_aer_rc_err_msi.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e08			Register Name: SII_INT_0
Bit	Read/Write	Default/Hex	Description
0	R/W1C	0x0	PF0_CFG_VPD_INT This pin is set as a one cycle pulse to notify your application to read the VPD registers. The sequence of events for a VPD read cycle is: ▪ The controller sends a request (single-cycle pulse of the cfg_vpd_int signal) to your application to read or write vital product data. ▪ Your application reads the VPD Control and Capabilities register. ▪ The VPD Flag (bit 31) is set to '0' indicating a read request. Your application fetches four bytes of data from the VPD Address location and transfers this to the VPD Data register. ▪ Your application sets the VPD Flag bit to '1' indicating the request is complete. The sequence of events for a VPD write cycle is: ▪ The controller sends a request (single-cycle pulse of the cfg_vpd_int signal) to your application to read or write vital product data. ▪ Your application reads the VPD Control and Capabilities register. ▪ The VPD Flag (bit 31) is set to '1' indicating a write request. Your application reads the VPD Data register and transfers this to the location specified by the VPD Address register. ▪ Your application sets the VPD Flag bit to '0' indicating the request is complete.

18.3.8.63 0x0e0c PCIe SII Interrupt Register1 (Default Value: 0x0000_0000)

Offset: 0x0e0c			Register Name: SII_INT_1
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	PCIe_WAKE_N remote wake (USP)

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e0c			Register Name: SII_INT_1
Bit	Read/Write	Default/Hex	Description
30	R/W1C	0x0	WAKE local wake. Wake up from power management unit. The controller generates wake to request the system to restore power and clock when a wakeup event has been detected such as apps_pm_xmt_pme, apps_pm_vf_xmt_pme, or outband_pwrup_cmd. The wake signal is an active high signal and its rising edge should be detected to drive the WAKE# the connector. Assertion of wake could be for a single clock cycle or multiple clock cycles. Not used in RC mode.
29	R/W1C	0x0	RADM_PM_TO_ACK One-clock-cycle pulse that indicates that the controller received a PME_TO_Ack message. Upstream port: Reserved.
28	R/W1C	0x0	RADM_PM_PME One-clock-cycle pulse that indicates that the controller received a PM_PME message.
27	R/W1C	0x0	RADM_FATAL_ERR One-clock-cycle pulse that indicates that the controller received an ERR_FATAL message.
26	R/W1C	0x0	RADM_NONFATAL_ERR One-clock-cycle pulse that indicates that the controller received an ERR_NONFATAL message.
25	R/W1C	0x0	RADM_CORRECTABLE_ERR One-clock-cycle pulse that indicates that the controller received an ERR_COR message. The controller makes the message header available the radm_msg_payload output.
24	R/W1C	0x0	PF0_CFG_SYS_ERR_RC System error detected. A one-clock-cycle pulse that indicates if any device in the hierarchy reports any of the following errors and the associated enable bit is set in the Root Control register: ERR_COR, ERR_FATAL, ERR_NONFATAL. Also asserted when an internal error is detected. There is one bit of cfg_sys_err_rc assigned to each configured function.
23	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e0c			Register Name: SII_INT_1
Bit	Read/Write	Default/Hex	Description
22	R/W1C	0x0	TRAINING_RST_N Hot reset from upstream component. When the controller LTSSM receives two consecutive TS1 ordered sets with the hot_reset bit asserted, it asserts training_rst_n for one clock cycle. This signal is only kept for legacy purposes. You should use the link_req_rst_not signal to reset the controller after a 'hot reset' request.
21	R/W1C	0x0	PF0_FRS_GRANT Indicator of when an FRS message for this function has been scheduled for transmission.
20	R/W1C	0x0	RADM_VENDOR_MSG One-cycle pulse that indicates the controller received a vendor-defined message. The controller makes the message header available the radm_msg_payload output. When FX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then both bits are asserted.
19	/	/	Reserved
18	R/W1C	0x0	PF0_FRSQ_MSI FRSQ Interrupt Pulse. The RC asserts this output when it receives an FRQ message or when the FRS queue overflows.
17	R/W1C	0x0	PF0_CFG_UP_DRS_TO_FRS DRS to FRS Pulse. The DSP controller asserts the cfg_up_drs_to_frsoutput and sends an FRS message with the reason code set to 'DRS Message Received' when: ▪ It receives a DRS message, and ▪ PCIe_CAP_DRS_SIGNALING_CONTROL in INK_CONTROL_LINK_STATUS_REG is 2'b10
16	R/W1C	0x0	PF0_CFG_DRS_MSI DRS Message Received Interrupt Pulse. The DSP controller asserts the cfg_drs_msi output when all of the following are true: ▪ It receives a DRS message ▪ PCIe_CAP_DRS_SIGNALING_CONTROL in INK_CONTROL_LINK_STATUS_REG is 2'b01 ▪ MSI or MSI-X is enabled

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e0c			Register Name: SII_INT_1
Bit	Read/Write	Default/Hex	Description
15	R/W1C	0x0	PF3_DPA_SUBSTATE_UPDATE PF3 DPA Substate-Updated Indication Signal. The controller asserts it for one core_clk cycle when the Substate Control field of the DPA Control Register has been updated with a new value for the associated function. The controller asserts it when the updated value of the Substate Control field does not match the Substate Status field of the Status Register when the Substate Control Enable bit field of the Status Register is set to "1". Note: Your application logic is required to do the following: ▪ Detect the one cycle pulse on the signal for the relevant function. ▪ Read the function's substate control register to determine the software's target substate (transition). ▪ Read the function's transition latency value, unit, and indicator. Calculate the maximum transition latency for the substate transition. ▪ Execute the substate transition and complete it within the maximum transition latency. ▪ Update the substate status after completing the transition through a DBI write. The controller updates the substate status during the substate transition if the transition is from a lower power substate to a higher; the status is the higher power substate during the substate transition.
14	R/W1C	0x0	PF2_DPA_SUBSTATE_UPDATE PF2 DPA Substate-Updated Indication Signal.
13	R/W1C	0x0	PF1_DPA_SUBSTATE_UPDATE PF1 DPA Substate-Updated Indication Signal.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e0c			Register Name: SII_INT_1
Bit	Read/Write	Default/Hex	Description
12	R/W1C	0x0	PF0_DPA_SUBSTATE_UPDATE PF0 DPA Substate-Updated Indication Signal.
11	R/W1C	0x0	PCIe_PERI_AR_INT PCIe read peripherals space(0-1G) int
10	R/W1C	0x0	PCIe_PERI_AW_INT PCIe write peripherals space(0-1G) int
9	R/W1C	0x0	RADM_QOVERFLOW_1 Pulse indicating that one or more of the P/NP/CPL receive queues have overflowed. There is a 1-bit indication for each configured virtual channel. You can connect this output to your internal error reporting mechanism.
8	R/W1C	0x0	RADM_QOVERFLOW_0 Pulse indicating that one or more of the P/NP/CPL receive queues have overflowed. There is a 1-bit indication for each configured virtual channel. You can connect this output to your internal error reporting mechanism.
7:5	/	/	/
4	R/W1C	0x0	RTLH_RFC_UPD Indicates that the controller received a flow control update DLLP. Used for applications that implement flow Control outside the controller.
3	R/W1C	0x0	LINK_REQ_RST_NOT Reset request because the link has gone down or the controller received a hot-reset request. A low level indicates that the controller is requesting external logic to reset the controller because the PHY link is down. When the AXI bridge module is enabled the link reset request is delayed until all pending AXI transfers have completed. When the AXI Bridge module is not enabled the link reset request is sent immediately.
2	R/W1C	0x0	SMLH_REQ_RST_NOT Early version of the link_req_rst_not signal.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e0c			Register Name: SII_INT_1
Bit	Read/Write	Default/Hex	Description
1	R/W1C	0x0	RDLH_LINK_UP Data link layer up/down indicator: This status from the flow control initialization state machine indicates that flow control has been initiated and the Data link layer is ready to transmit and receive packets. For multi-VC designs, this signal indicates status for VC0 only. 1: Link is up 0: Link is down
0	R/W1C	0x0	SMLH_LINK_UP PHY Link up/down indicator: 1: Link is up 0: Link is down

18.3.8.64 0x0e10 PCIe SII Interrupt Mask Register2 (Default Value: 0x0000_0000)

Offset: 0x0e10			Register Name: SII_INT_MASK_2
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PF1_VF_RBAR_CTRL_UPDATE_MASK 0: Mask 1: Not Mask
30	R/W	0x0	PF1_RBAR_CTRL_UPDATE_MASK 0: Mask 1: Not Mask
29	R/W	0x0	PF1_EXT_LBC_MASK 0: Mask 1: Not Mask
28	R/W	0x0	PF1_FRS_GRANT_MASK 0: Mask 1: Not Mask
27	R/W	0x0	PF1_CFG_SYS_ERR_RC_MASK 0: Mask 1: Not Mask
26	R/W	0x0	PF1_HP_MSI_MASK 0: Mask 1: Not Mask
25	R/W	0x0	PF1_HP_INT_MASK 0: Mask 1: Not Mask

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e10			Register Name: SII_INT_MASK_2
Bit	Read/Write	Default/Hex	Description
24	R/W	0x0	PF1_HP_PME_MASK 0: Mask 1: Not Mask
23	R/W	0x0	PF1_CFG_PME_MSI_MASK 0: Mask 1: Not Mask
22	R/W	0x0	PF1_CFG_PME_INT_MASK 0: Mask 1: Not Mask
21	R/W	0x0	PF1_CFG_AER_RC_ERR_MSI_MASK 0: Mask 1: Not Mask
20	R/W	0x0	PF1_CFG_AER_RC_ERR_INT_MASK 0: Mask 1: Not Mask
19	R/W	0x0	PF1_CFG_VPD_INT_MASK 0: Mask 1: Not Mask
18	R/W	0x0	PF1_FRSQ_MSI_MASK 0: Mask 1: Not Mask
17	R/W	0x0	PF1_CFG_UP_DRS_TO_FRS_MASK 0: Mask 1: Not Mask
16	R/W	0x0	PF1_CFG_DRS_MSI_MASK 0: Mask 1: Not Mask
15	R/W	0x0	PF0_VF_RBAR_CTRL_UPDATE_MASK 0: Mask 1: Not Mask
14	R/W	0x0	PF0_RBAR_CTRL_UPDATE_MASK 0: Mask 1: Not Mask
13	R/W	0x0	PF0_EXT_LBC_MASK 0: Mask 1: Not Mask
12:8	/	/	/
7	R/W	0x0	PF3_FLR_FINISH_MASK 0: Mask 1: Not Mask

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e10			Register Name: SII_INT_MASK_2
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	PF2_FLR_FINISH_MASK 0: Mask 1: Not Mask
5	R/W	0x0	PF1_FLR_FINISH_MASK 0: Mask 1: Not Mask
4	R/W	0x0	PF0_FLR_FINISH_MASK 0: Mask 1: Not Mask
3	R/W	0x0	PF3_FLR_START_MASK 0: Mask 1: Not Mask
2	R/W	0x0	PF2_FLR_START_MASK 0: Mask 1: Not Mask
1	R/W	0x0	PF1_FLR_START_MASK 0: Mask 1: Not Mask
0	R/W	0x0	PF0_FLR_START_MASK 0: Mask 1: Not Mask

18.3.8.65 0x0e14 PCIe SII Interrupt Mask Register3 (Default Value: 0x0000_0000)

Offset: 0x0e14			Register Name: SII_INT_MASK_3
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PF3_VF_RBAR_CTRL_UPDATE_MASK 0: Mask 1: Not Mask
30	R/W	0x0	PF3_RBAR_CTRL_UPDATE_MASK 0: Mask 1: Not Mask
29	R/W	0x0	PF3_EXT_LBC_3_MASK 0: Mask 1: Not Mask
28	R/W	0x0	PF3_FRS_GRANT_MASK 0: Mask 1: Not Mask
27	R/W	0x0	PF3_CFG_SYS_ERR_RC_MASK 0: Mask 1: Not Mask

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e14			Register Name: SII_INT_MASK_3
Bit	Read/Write	Default/Hex	Description
26	R/W	0x0	PF3_HP_MSI_MASK 0: Mask 1: Not Mask
25	R/W	0x0	PF3_HP_INT_MASK 0: Mask 1: Not Mask
24	R/W	0x0	PF3_HP_PME_MASK 0: Mask 1: Not Mask
23	R/W	0x0	PF3_CFG_PME_MSI_MASK 0: Mask 1: Not Mask
22	R/W	0x0	PF3_CFG_PME_INT_MASK 0: Mask 1: Not Mask
21	R/W	0x0	PF3_CFG_AER_RC_ERR_MSI_MASK 0: Mask 1: Not Mask
20	R/W	0x0	PF3_CFG_AER_RC_ERR_INT_MASK 0: Mask 1: Not Mask
19	R/W	0x0	PF3_CFG_VPD_INT_MASK 0: Mask 1: Not Mask
18	R/W	0x0	PF3_FRSQ_MSI_MASK 0: Mask 1: Not Mask
17	R/W	0x0	PF3_CFG_UP_DRS_TO_FRS_MASK 0: Mask 1: Not Mask
16	R/W	0x0	PF3_CFG_DRS_MSI_MASK 0: Mask 1: Not Mask
15	R/W	0x0	PF2_VF_RBAR_CTRL_UPDATE_MASK 0: Mask 1: Not Mask
14	R/W	0x0	PF2_RBAR_CTRL_UPDATE_MASK 0: Mask 1: Not Mask
13	R/W	0x0	PF2_EXT_LBC_MASK 0: Mask 1: Not Mask

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e14			Register Name: SII_INT_MASK_3
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	PF2_FRS_GRANT_MASK 0: Mask 1: Not Mask
11	R/W	0x0	PF2_CFG_SYS_ERR_RC_MASK 0: Mask 1: Not Mask
10	R/W	0x0	PF2_HP_MSI_MASK 0: Mask 1: Not Mask
9	R/W	0x0	PF2_HP_INT_MASK 0: Mask 1: Not Mask
8	R/W	0x0	PF2_HP_PME_MASK 0: Mask 1: Not Mask
7	R/W	0x0	PF2_CFG_PME_MSI_MASK 0: Mask 1: Not Mask
6	R/W	0x0	PF2_CFG_PME_INT_MASK 0: Mask 1: Not Mask
5	R/W	0x0	PF2_CFG_AER_RC_ERR_MSI_MASK 0: Mask 1: Not Mask
4	R/W	0x0	PF2_CFG_AER_RC_ERR_INT_MASK 0: Mask 1: Not Mask
3	R/W	0x0	PF2_CFG_VPD_INT_MASK 0: Mask 1: Not Mask
2	R/W	0x0	PF2_FRSQ_MSI_MASK 0: Mask 1: Not Mask
1	R/W	0x0	PF2_CFG_UP_DRS_TO_FRS_MASK 0: Mask 1: Not Mask
0	R/W	0x0	PF2_CFG_DRS_MSI_MASK 0: Mask 1: Not Mask

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.3.8.66 0x0e18 PCIe SII Interrupt Register2 (Default Value: 0x0000_0000)

Offset: 0x0e18			Register Name: SII_INT_2
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	PF1_VF_RBAR_CTRL_UPDATE Indicates that a resizable VF BAR control register has been updated: 1 bit per Physical function.
30	R/W1C	0x0	PF1_RBAR_CTRL_UPDATE Indicates that a resizable BAR control register has been updated: 1 bit per Physical function.
29	R/W1C	0x0	PF1_EXT_LBC The controller asserts lbc_ext_cs when a received TLP for a read or write request has an address in the range of your application device, as determined by the BAR configuration. The width of the lbc_ext_cs signal is equal to the number of functions in your controller configuration (CX_NFUNC). That is, there is one lbc_ext_cs bit for each configured function. The controller de-asserts lbc_ext_cs only after the external register block acknowledges completion of the access by asserting the corresponding bit of ext_lbc_ack.
28	R/W1C	0x0	PF1_FRS_GRANT Indicator of when an FRS message for this function has been scheduled for transmission.
27	R/W1C	0x0	PF1_CFG_SYS_ERR_RC System error detected. A one-clock-cycle pulse that indicates if any device in the hierarchy reports any of the following errors and the associated enable bit is set in the Root Control register: ERR_COR, ERR_FATAL, ERR_NONFATAL. Also asserted when an internal error is detected. There is one bit of cfg_sys_err_rc assigned to each configured function.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e18			Register Name: SII_INT_2
Bit	Read/Write	Default/Hex	Description
26	R/W1C	0x0	PF1_HP_MSI The controller asserts hp_msi (as a one-cycle pulse) when the logical AND of the following conditions transitions from false to true: ▪ MSI or MSI-X is enabled. ▪ Hot-Plug interrupts are enabled in the Slot Control register. ▪ Any bit in the Slot Status register transitions from 0 to 1 and the associated event notification is enabled in the Slot Control register. There is one bit of hp_int for each configured function. The controller pulses the hp_msi output only when any of the hot plug status bits change from 0 to 1 (as is hp_pme).
25	R/W1C	0x0	PF1_HP_INT The controller asserts hp_int when all of the following conditions are true: ▪ The INTx Assertion Disable bit in the Command register is 0. ▪ Hot-Plug interrupts are enabled in the Slot Control register. ▪ Any bit in the Slot Status register is equal to 1, and the associated event notification is enabled in the Slot Control register. There is one bit of hp_int for each configured function.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e18			Register Name: SII_INT_2
Bit	Read/Write	Default/Hex	Description
24	R/W1C	0x0	PF1_HP_PME The controller asserts hp_pme when all of the following conditions are true: ▪ The PME Enable bit in the Power Management Control and Status register is set to 1. ▪ Any bit in the Slot Status register transitions from 0 to 1 and the associated event notification is enabled in the Slot Control register. The controller does not check if the PM state is D1, D2, or D3hot. It is up to your application to check the value pm_dstate to make sure the device is in D1, D2, or D3hot. There is one bit of hp_pme for each configured function. The controller pulses the hp_pme output only when any hot plug status bit changes from 0 to 1 (as is hp_msi). hp_int stays asserted as long as the status bit is set. In addition, it asserts hp_pme only if PME is enabled, but it does not matter if hot-plug interrupts are enabled.
23	R/W1C	0x0	PF1_CFG_PME_MSI The controller asserts cfg_pme_msi (as a one-cycle pulse) when all of the following conditions are true: ▪ MSI or MSI-X is enabled. ▪ The PME Interrupt Enable bit in the Root Control register is set to 1. ▪ The PME Status bit in the Root Status register is set to 1. The controller does not check if the associated MSI vector (asserted cfg_pcie_cap_int_msg_num) is unmasked. It is up to the application to check whether the vector is masked or unmasked.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e18			Register Name: SII_INT_2
Bit	Read/Write	Default/Hex	Description
22	R/W1C	0x0	PF1_CFG_PME_INT The controller asserts cfg_pme_int when all of the following conditions are true: ▪ The INTx Assertion Disable bit in the Command register is 0. ▪ The PME Interrupt Enable bit in the Root Control register is set to 1. ▪ The PME Status bit in the Root Status register is set to 1. The cfg_pme_msi output is a pulse signal (only asserted for one clock cycle). But cfg_pme_int is a level signal; essentially an AND of the PME interrupt enable and receipt of the pm_pme message.
21	R/W1C	0x0	PF1_CFG_AER_RC_ERR_MSI The controller asserts cfg_aer_rc_err_msi for one clock cycle when all of the following conditions are true: ▪ MSI or MSI-X is enabled. ▪ A reported error condition causes a bit to be set in the Root Error Status register. ▪ The associated error message reporting enable bit is set in the Root Error Command register. The controller does not check if the associated MSI vector (asserted cfg_aer_int_msg_num) is unmasked. It is up to the application to check whether the vector is masked or unmasked.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e18			Register Name: SII_INT_2
Bit	Read/Write	Default/Hex	Description
20	R/W1C	0x0	PF1_CFG_AER_RC_ERR_INT Asserted when a reported error condition causes a bit to be set in the Root Error Status register and the associated error message reporting enable bit is set in the Root Error Command register. cfg_aer_rc_err_int is set when the RC internally generates an error or when an error message is received by the RC. Because the RC itself generates it, this needs to be propagated up to the system software which would then need to read the error registers to see which error occurred. Note: This signal is used when MSI/MSI-X is NOT enabled; otherwise see cfg_aer_rc_err_msi.
19	R/W1C	0x0	PF1_CFG_VPD_INT This pin is set as a one cycle pulse to notify your application to read the VPD registers. The sequence of events for a VPD read cycle is: ▪ The controller sends a request (single-cycle pulse of the cfg_vpd_int signal) to your application to read or write vital product data. ▪ Your application reads the VPD Control and Capabilities register. ▪ The VPD Flag (bit 31) is set to '0' indicating a read request. Your application fetches four bytes of data from the VPD Address location and transfers this to the VPD Data register. ▪ Your application sets the VPD Flag bit to '1' indicating the request is complete. The sequence of events for a VPD write cycle is: ▪ The controller sends a request (single-cycle pulse of the cfg_vpd_int signal) to your application to read or write vital product data. ▪ Your application reads the VPD Control and Capabilities register. ▪ The VPD Flag (bit 31) is set to '1' indicating a write request. Your application reads the VPD Data register and transfers this to the location specified by the VPD Address register. ▪ Your application sets the VPD Flag bit to '0' indicating the request is complete.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e18			Register Name: SII_INT_2
Bit	Read/Write	Default/Hex	Description
18	R/W1C	0x0	PF1_FRSQ_MSI FRSQ Interrupt Pulse. The RC asserts this output when it receives an FRQ message or when the FRS queue overflows.
17	R/W1C	0x0	PF1_CFG_UP_DRS_TO_FRS DRS to FRS Pulse. The DSP controller asserts the cfg_up_drs_to_frsoutput and sends an FRS message with the reason code set to 'DRS Message Received' when: ▪ It receives a DRS message, and ▪ PCIe_CAP_DRS_SIGNALING_CONTROL in LINK_CONTROL_LINK_STATUS_REG is 2'b10
16	R/W1C	0x0	PF1_CFG_DRS_MSI DRS Message Received Interrupt Pulse. The DSP controller asserts the cfg_drs_msi output when all of the following are true: ▪ It receives a DRS message ▪ PCIe_CAP_DRS_SIGNALING_CONTROL in LINK_CONTROL_LINK_STATUS_REG is 2'b01 ▪ MSI or MSI-X is enabled
15	R/W1C	0x0	PF0_VF_RBAR_CTRL_UPDATE Indicates that a resizable VF BAR control register has been updated: 1 bit per Physical function.
14	R/W1C	0x0	PF0_RBAR_CTRL_UPDATE Indicates that a resizable BAR control register has been updated: 1 bit per Physical function.
13	R/W1C	0x0	PF0_EXT_LBC The controller asserts lbc_ext_cs when a received TLP for a read or write request has an address in the range of your application device, as determined by the BAR configuration. The width of the lbc_ext_cs signal is equal to the number of functions in your controller configuration (CX_NFUNC). That is, there is one lbc_ext_cs bit for each configured function. The controller de-asserts lbc_ext_cs only after the external register block acknowledges completion of the access by asserting the corresponding bit of ext_lbc_ack.
12:8	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e18			Register Name: SII_INT_2
Bit	Read/Write	Default/Hex	Description
7	R/W1C	0x0	PF3_FLR_FINISH The FLR of function 3 finishes in EP mode.
6	R/W1C	0x0	PF2_FLR_FINISH The FLR of function 2 finishes in EP mode.
5	R/W1C	0x0	PF1_FLR_FINISH The FLR of function 1 finishes in EP mode.
4	R/W1C	0x0	PF0_FLR_FINISH The FLR of function 0 finishes in EP mode.
3	R/W1C	0x0	PF3_FLR_START Function 3 receives the FLR request from remote RC in EP mode.
2	R/W1C	0x0	PF2_FLR_START Function 2 receives the FLR request from remote RC in EP mode.
1	R/W1C	0x0	PF1_FLR_START Function 1 receives the FLR request from remote RC in EP mode.
0	R/W1C	0x0	PF0_FLR_START Function 0 receives the FLR request from remote RC in EP mode.

18.3.8.67 0x0e1c PCIe SII Interrupt Register3 (Default Value: 0x0000_0000)

Offset: 0x0e1c			Register Name: SII_INT_3
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	PF3_VF_RBAR_CTRL_UPDATE Indicates that a resizable VF BAR control register has been updated: 1 bit per Physical function.
30	R/W1C	0x0	PF3_RBAR_CTRL_UPDATE Indicates that a resizable BAR control register has been updated: 1 bit per Physical function.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e1c			Register Name: SII_INT_3
Bit	Read/Write	Default/Hex	Description
29	R/W1C	0x0	PF3_EXT_LBC The controller asserts lbc_ext_cs when a received TLP for a read or write request has an address in the range of your application device, as determined by the BAR configuration. The width of the lbc_ext_cs signal is equal to the number of functions in your controller configuration (CX_NFUNC). That is, there is one lbc_ext_cs bit for each configured function. The controller de-asserts lbc_ext_cs only after the external register block acknowledges completion of the access by asserting the corresponding bit of ext_lbc_ack.
28	R/W1C	0x0	PF3_FRS_GRANT Indicator of when an FRS message for this function has been scheduled for transmission.
27	R/W1C	0x0	PF3_CFG_SYS_ERR_RC System error detected. A one-clock-cycle pulse that indicates if any device in the hierarchy reports any of the following errors and the associated enable bit is set in the Root Control register: ERR_COR, ERR_FATAL, ERR_NONFATAL. Also asserted when an internal error is detected. There is one bit of cfg_sys_err_rc assigned to each configured function.
26	R/W1C	0x0	PF3_HP_MSI The controller asserts hp_msi (as a one-cycle pulse) when the logical AND of the following conditions transitions from false to true: ▪ MSI or MSI-X is enabled. ▪ Hot-Plug interrupts are enabled in the Slot Control register. ▪ Any bit in the Slot Status register transitions from 0 to 1 and the associated event notification is enabled in the Slot Control register. There is one bit of hp_int for each configured function. The controller pulses the hp_msi output only when any of the hot plug status bits change from 0 to 1 (as is hp_pme).

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e1c			Register Name: SII_INT_3
Bit	Read/Write	Default/Hex	Description
25	R/W1C	0x0	PF3_HP_INT The controller asserts hp_int when all of the following conditions are true: ▪ The INTx Assertion Disable bit in the Command register is 0. ▪ Hot-Plug interrupts are enabled in the Slot Control register. ▪ Any bit in the Slot Status register is equal to 1, and the associated event notification is enabled in the Slot Control register. There is one bit of hp_int for each configured function.
24	R/W1C	0x0	PF3_HP_PME The controller asserts hp_pme when all of the following conditions are true: ▪ The PME Enable bit in the Power Management Control and Status register is set to 1. ▪ Any bit in the Slot Status register transitions from 0 to 1 and the associated event notification is enabled in the Slot Control register. The controller does not check if the PM state is D1, D2, or D3hot. It is up to your application to check the value pm_dstate to make sure the device is in D1, D2, or D3hot. There is one bit of hp_pme for each configured function. The controller pulses the hp_pme output only when any hot plug status bit changes from 0 to 1 (as is hp_msi). hp_int stays asserted as long as the status bit is set. In addition, it asserts hp_pme only if PME is enabled, but it does not matter if hot-plug interrupts are enabled.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e1c			Register Name: SII_INT_3
Bit	Read/Write	Default/Hex	Description
23	R/W1C	0x0	PF3_CFG_PME_MSI The controller asserts cfg_pme_msi (as a one-cycle pulse) when all of the following conditions are true: ▪ MSI or MSI-X is enabled. ▪ The PME Interrupt Enable bit in the Root Control register is set to 1. ▪ The PME Status bit in the Root Status register is set to 1. The controller does not check if the associated MSI vector (asserted cfg_pcie_cap_int_msg_num) is unmasked. It is up to the application to check whether the vector is masked or unmasked.
22	R/W1C	0x0	PF3_CFG_PME_INT The controller asserts cfg_pme_int when all of the following conditions are true: ▪ The INTx Assertion Disable bit in the Command register is 0. ▪ The PME Interrupt Enable bit in the Root Control register is set to 1. ▪ The PME Status bit in the Root Status register is set to 1. The cfg_pme_msi output is a pulse signal (only asserted for one clock cycle). But cfg_pme_int is a level signal; essentially an AND of the PME interrupt enable and receipt of the pm_pme message.
21	R/W1C	0x0	PF3_CFG_AER_RC_ERR_MSI The controller asserts cfg_aer_rc_err_msi for one clock cycle when all of the following conditions are true: ▪ MSI or MSI-X is enabled. ▪ A reported error condition causes a bit to be set in the Root Error Status register. ▪ The associated error message reporting enable bit is set in the Root Error Command register. The controller does not check if the associated MSI vector (asserted cfg_aer_int_msg_num) is unmasked. It is up to the application to check whether the vector is masked or unmasked.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e1c			Register Name: SII_INT_3
Bit	Read/Write	Default/Hex	Description
20	R/W1C	0x0	PF3_CFG_AER_RC_ERR_INT Asserted when a reported error condition causes a bit to be set in the Root Error Status register and the associated error message reporting enable bit is set in the Root Error Command register. cfg_aer_rc_err_int is set when the RC internally generates an error or when an error message is received by the RC. Because the RC itself generates it, this needs to be propagated up to the system software which would then need to read the error registers to see which error occurred. Note: This signal is used when MSI/MSI-X is NOT enabled; otherwise see cfg_aer_rc_err_msi.
19	R/W1C	0x0	PF3_CFG_VPD_INT This pin is set as a one cycle pulse to notify your application to read the VPD registers. The sequence of events for a VPD read cycle is: ▪ The controller sends a request (single-cycle pulse of the cfg_vpd_int signal) to your application to read or write vital product data. ▪ Your application reads the VPD Control and Capabilities register. ▪ The VPD Flag (bit 31) is set to '0' indicating a read request. Your application fetches four bytes of data from the VPD Address location and transfers this to the VPD Data register. ▪ Your application sets the VPD Flag bit to '1' indicating the request is complete. The sequence of events for a VPD write cycle is: ▪ The controller sends a request (single-cycle pulse of the cfg_vpd_int signal) to your application to read or write vital product data. ▪ Your application reads the VPD Control and Capabilities register. ▪ The VPD Flag (bit 31) is set to '1' indicating a write request. Your application reads the VPD Data register and transfers this to the location specified by the VPD Address register. ▪ Your application sets the VPD Flag bit to '0' indicating the request is complete.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e1c			Register Name: SII_INT_3
Bit	Read/Write	Default/Hex	Description
18	R/W1C	0x0	PF3_FRSQ_MSI FRSQ Interrupt Pulse. The RC asserts this output when it receives an FRQ message or when the FRS queue overflows.
17	R/W1C	0x0	PF3_CFG_UP_DRS_TO_FRS DRS to FRS Pulse. The DSP controller asserts the cfg_up_drs_to_frs output and sends an FRS message with the reason code set to 'DRS Message Received' when: ▪ It receives a DRS message, and ▪ PCIe_CAP_DRS_SIGNALING_CONTROL in LINK_CONTROL_LINK_STATUS_REG is 2'b10
16	R/W1C	0x0	PF3_CFG_DRS_MSI DRS Message Received Interrupt Pulse. The DSP controller asserts the cfg_drs_msi output when all of the following are true: ▪ It receives a DRS message ▪ PCIe_CAP_DRS_SIGNALING_CONTROL in LINK_CONTROL_LINK_STATUS_REG is 2'b01 ▪ MSI or MSI-X is enabled
15	R/W1C	0x0	PF2_VF_RBAR_CTRL_UPDATE Indicates that a resizable VF BAR control register has been updated: 1 bit per Physical function.
14	R/W1C	0x0	PF2_RBAR_CTRL_UPDATE Indicates that a resizable BAR control register has been updated: 1 bit per Physical function.
13	R/W1C	0x0	PF2_EXT_LBC The controller asserts lbc_ext_cs when a received TLP for a read or write request has an address in the range of your application device, as determined by the BAR configuration. The width of the lbc_ext_cs signal is equal to the number of functions in your controller configuration (CX_NFUNC). That is, there is one lbc_ext_cs bit for each configured function. The controller de-asserts lbc_ext_cs only after the external register block acknowledges completion of the access by asserting the corresponding bit of ext_lbc_ack.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e1c			Register Name: SII_INT_3
Bit	Read/Write	Default/Hex	Description
12	R/W1C	0x0	PF2_FRS_GRANT Indicator of when an FRS message for this function has been scheduled for transmission.
11	R/W1C	0x0	PF2_CFG_SYS_ERR_RC System error detected. A one-clock-cycle pulse that indicates if any device in the hierarchy reports any of the following errors and the associated enable bit is set in the Root Control register: ERR_COR, ERR_FATAL, ERR_NONFATAL. Also asserted when an internal error is detected. There is one bit of cfg_sys_err_rc assigned to each configured function.
10	R/W1C	0x0	PF2_HP_MSI The controller asserts hp_msi (as a one-cycle pulse) when the logical AND of the following conditions transitions from false to true: ▪ MSI or MSI-X is enabled. ▪ Hot-Plug interrupts are enabled in the Slot Control register. ▪ Any bit in the Slot Status register transitions from 0 to 1 and the associated event notification is enabled in the Slot Control register. There is one bit of hp_int for each configured function. The controller pulses the hp_msi output only when any of the hot plug status bits change from 0 to 1 (as is hp_pme).
9	R/W1C	0x0	PF2_HP_INT The controller asserts hp_int when all of the following conditions are true: ▪ The INTx Assertion Disable bit in the Command register is 0. ▪ Hot-Plug interrupts are enabled in the Slot Control register. ▪ Any bit in the Slot Status register is equal to 1, and the associated event notification is enabled in the Slot Control register. There is one bit of hp_int for each configured function.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e1c			Register Name: SII_INT_3
Bit	Read/Write	Default/Hex	Description
8	R/W1C	0x0	PF2_HP_PME The controller asserts hp_pme when all of the following conditions are true: ▪ The PME Enable bit in the Power Management Control and Status register is set to 1. ▪ Any bit in the Slot Status register transitions from 0 to 1 and the associated event notification is enabled in the Slot Control register. The controller does not check if the PM state is D1, D2, or D3hot. It is up to your application to check the value pm_dstate to make sure the device is in D1, D2, or D3hot. There is one bit of hp_pme for each configured function. The controller pulses the hp_pme output only when any hot plug status bit changes from 0 to 1 (as is hp_msi). hp_int stays asserted as long as the status bit is set. In addition, it asserts hp_pme only if PME is enabled, but it does not matter if hot-plug interrupts are enabled.
7	R/W1C	0x0	PF2_CFG_PME_MSI The controller asserts cfg_pme_msi (as a one-cycle pulse) when all of the following conditions are true: ▪ MSI or MSI-X is enabled. ▪ The PME Interrupt Enable bit in the Root Control register is set to 1. ▪ The PME Status bit in the Root Status register is set to 1. The controller does not check if the associated MSI vector (asserted cfg_pcie_cap_int_msg_num) is unmasked. It is up to the application to check whether the vector is masked or unmasked.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e1c			Register Name: SII_INT_3
Bit	Read/Write	Default/Hex	Description
6	R/W1C	0x0	PF2_CFG_PME_INT The controller asserts cfg_pme_int when all of the following conditions are true: ▪ The INTx Assertion Disable bit in the Command register is 0. ▪ The PME Interrupt Enable bit in the Root Control register is set to 1. ▪ The PME Status bit in the Root Status register is set to 1. The cfg_pme_msi output is a pulse signal (only asserted for one clock cycle). But cfg_pme_int is a level signal; essentially an AND of the PME interrupt enable and receipt of the pm_pme message.
5	R/W1C	0x0	PF2_CFG_AER_RC_ERR_MSI The controller asserts cfg_aer_rc_err_msi for one clock cycle when all of the following conditions are true: ▪ MSI or MSI-X is enabled. ▪ A reported error condition causes a bit to be set in the Root Error Status register. ▪ The associated error message reporting enable bit is set in the Root Error Command register. The controller does not check if the associated MSI vector (asserted cfg_aer_int_msg_num) is unmasked. It is up to the application to check whether the vector is masked or unmasked.
4	R/W1C	0x0	PF2_CFG_AER_RC_ERR_INT Asserted when a reported error condition causes a bit to be set in the Root Error Status register and the associated error message reporting enable bit is set in the Root Error Command register. cfg_aer_rc_err_int is set when the RC internally generates an error or when an error message is received by the RC. Because the RC itself generates it, this needs to be propagated up to the system software which would then need to read the error registers to see which error occurred. Note: This signal is used when MSI/MSI-X is NOT enabled; otherwise see cfg_aer_rc_err_msi.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e1c			Register Name: SII_INT_3
Bit	Read/Write	Default/Hex	Description
3	R/W1C	0x0	PF2_CFG_VPD_INT This pin is set as a one cycle pulse to notify your application to read the VPD registers. The sequence of events for a VPD read cycle is: ▪ The controller sends a request (single-cycle pulse of the cfg_vpd_int signal) to your application to read or write vital product data. ▪ Your application reads the VPD Control and Capabilities register. ▪ The VPD Flag (bit 31) is set to '0' indicating a read request. Your application fetches four bytes of data from the VPD Address location and transfers this to the VPD Data register. ▪ Your application sets the VPD Flag bit to '1' indicating the request is complete. The sequence of events for a VPD write cycle is: ▪ The controller sends a request (single-cycle pulse of the cfg_vpd_int signal) to your application to read or write vital product data. ▪ Your application reads the VPD Control and Capabilities register. ▪ The VPD Flag (bit 31) is set to '1' indicating a write request. Your application reads the VPD Data register and transfers this to the location specified by the VPD Address register. ▪ Your application sets the VPD Flag bit to '0' indicating the request is complete.
2	R/W1C	0x0	PF2_FRSQ_MSI FRSQ Interrupt Pulse. The RC asserts this output when it receives an FRQ message or when the FRS queue overflows.
1	R/W1C	0x0	PF2_CFG_UP_DRS_TO_FRS DRS to FRS Pulse. The DSP controller asserts the cfg_up_drs_to_frs output and sends an FRS message with the reason code set to 'DRS Message Received' when: ▪ It receives a DRS message, and ▪ PCIe_CAP_DRS_SIGNALING_CONTROL in LINK_CONTROL_LINK_STATUS_REG is 2'b10

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0e1c			Register Name: SII_INT_3
Bit	Read/Write	Default/Hex	Description
0	R/W1C	0x0	PF2_CFG_DRS_MSI DRS Message Received Interrupt Pulse. The DSP controller asserts the cfg_drs_msi output when all of the following are true: ▪ It receives a DRS message ▪ PCIe_CAP_DRS_SIGNALING_CONTROL in LINK_CONTROL_LINK_STATUS_REG is 2'b01 ▪ MSI or MSI-X is enabled

18.3.8.68 0x0e80 PCIe SII CFG INT PIN Register (Default Value: 0x0101_0101)

Offset: 0x0e80			Register Name: SII_CFG_INT_PIN
Bit	Read/Write	Default/Hex	Description
31:24	R	0x1	CFG_INT_PIN_3 cfg_int_pin[31:24] , The cfg_int_pin indicates the configured value for the Interrupt Pin Register field in the BRIDGE_CTRL_INT_PIN_INT_LINE register.
23:16	R	0x1	CFG_INT_PIN_2 cfg_int_pin[23:16]
15:8	R	0x1	CFG_INT_PIN_1 cfg_int_pin[15:8]
7:0	R	0x1	CFG_INT_PIN_0 cfg_int_pin[7:0]

18.3.8.69 0x0e88 PCIe SII CFG INT Disable Register (Default Value: 0x0000_0000)

Offset: 0x0e88			Register Name: SII_CFG_INT_DIS
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R	0x0	CFG_INT_DIS_3 cfg_int_disable[3]
2	R	0x0	CFG_INT_DIS_2 cfg_int_disable[2]
1	R	0x0	CFG_INT_DIS_1 cfg_int_disable[1]
0	R	0x0	CFG_INT_DIS_0 cfg_int_disable[0]

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.3.8.70 0x0e90 PCIe SII SYS INT Register (Default Value: 0x0000_0000)

Offset: 0x0e90			Register Name: SII_SYS_INT
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	SYS_INT_3 sys_int[3] , When sys_int goes from low to high, the controller generates an Assert_INTx Message. When sys_int goes from high to low, the controller generates a Deassert_INTx Message. There is a separate sys_int input bit for each function in your controller configuration. The Interrupt Pin register for the corresponding function determines which INTx Message the controller generates (INTA, INTB, INTC, or INTD). Legacy and native PCIe devices capable of generating an interrupt must support both Assert_INTx/Deassert_INTx and MSI or MSI-X. sys_int is intended to generate a message that emulates the legacy PCI Interrupts.
2	R/W	0x0	SYS_INT_2 sys_int[2]
1	R/W	0x0	SYS_INT_1 sys_int[1]
0	R/W	0x0	SYS_INT_0 sys_int[0]

18.3.8.71 0x0ea0 PCIe SII CFG AER INT MSG_NUM Register (Default Value: 0x0000_0000)

Offset: 0x0ea0			Register Name: SII_AER_INT_MSG_NUM
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R	0x0	CFG_AER_INT_MSG_NUM_3 cfg_aer_int_msg_num[19:15] , From bits [31:27] of the Root Error Status register, used when MSI or MSI-X is enabled. Assertion of cfg_aer_rc_err_msi along with a value cfg_aer_int_msg_num is equivalent to the controller receiving an MSI with the cfg_aer_int_msg_num value as the MSI vector.
23:21	/	/	/
20:16	R	0x0	CFG_AER_INT_MSG_NUM_2 cfg_aer_int_msg_num[14:10]

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0ea0			Register Name: SII_AER_INT_MSG_NUM
Bit	Read/Write	Default/Hex	Description
15:13	/	/	/
12:8	R	0x0	CFG_AER_INT_MSG_NUM_1 cfg_aer_int_msg_num[9:5]
7:5	/	/	/
4:0	R	0x0	CFG_AER_INT_MSG_NUM_0 cfg_aer_int_msg_num[4:0]

18.3.8.72 0x0ea8 PCIe SII CFG CAP INT MSG NUM Register (Default Value: 0x0000_0000)

Offset: 0x0ea8			Register Name: SII_PCIE_CAP_INT_MSG_NUM
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R	0x0	CFG_PCIe_CAP_INT_MSG_NUM_3 cfg_pcie_cap_int_msg_num[19:15] , From bits [13:9] of the PCI Express Capabilities register, used when MSI or MSI-X is enabled. Assertion of hp_msi or cfg_pme_msi along with a value cfg_pcie_cap_int_msg_num is equivalent to the controller receiving an MSI with the cfg_pcie_cap_int_msg_num value as the MSI vector.
23:21	/	/	/
20:16	R	0x0	CFG_PCIe_CAP_INT_MSG_NUM_2 cfg_pcie_cap_int_msg_num[14:10]
15:13	/	/	/
12:8	R	0x0	CFG_PCIe_CAP_INT_MSG_NUM_1 cfg_pcie_cap_int_msg_num[9:5]
7:5	/	/	/
4:0	R	0x0	CFG_PCIe_CAP_INT_MSG_NUM_0 cfg_pcie_cap_int_msg_num[4:0]

18.3.8.73 0x0f00 PCIe SII CFG 2ND RESET Register (Default Value: 0x0000_0000)

Offset: 0x0f00			Register Name: SII_CFG_2ND_RESET
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R	0x0	CFG_2ND_RESET cfg_2nd_reset

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.3.8.74 0x0f10 PCIe SII APP LTR MSG REQ Register (Default Value: 0x0000_0000)

Offset: 0x0f10			Register Name: SII_APP_LTR_MSG_REQ
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/WAC	0x0	APP_LTR_MSG_REQ app_ltr_msg_req_ahb Indicates that your application is requesting to send an LTR message. Once asserted, app_ ltr_msg_req must remain asserted until the controller asserts app_ltr_msg_grant.

18.3.8.75 0x0f14 PCIe SII APP LTR MSG LATENCY Register (Default Value: 0x0000_0000)

Offset: 0x0f14			Register Name: SII_APP_LTR_MSG_LATENCY
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	APP_LTR_MSG_LATENCY LTR message that your application is requesting to send. The message format is defined in the PCI Express Specification.

18.3.8.76 0x0f18 PCIe SII APP LTR MSG FUNC NUM Register (Default Value: 0x0000_0000)

Offset: 0x0f18			Register Name: SII_APP_LTR_MSG_FUNC_NUM
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	R/W	0x0	APP_LTR_MSG_FUNC_NUM Function number in your application that is requesting to send an LTR message. Function numbering starts at '0'.

18.3.8.77 0x0f1c PCIe SII APP LTR LATENCY Register (Default Value: 0x0000_0000)

Offset: 0x0f1c			Register Name: SII_APP_LTR_LATENCY
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0f1c			Register Name: SII_APP_LTR_LATENCY
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	APP_LTR_LATENCY The current LTR values reported and in-use by the downstream device. For a downstream device, when LTR is disabled, or when any function is directed to a non-D0 state, if a device had previously reported one or both latency fields with the Requirement bit set, the application must send a new LTR Message with both Requirement bits clear. For an upstream device, it reflects the captured LTR values from received LTR message, one clock cycle after the controller asserts the radm_msg_ltr output. When RX_TLP > 1 and when two messages of the same type are received in the same clock cycle, then this output reflects the second captured message. For more details, see 'Port Logic Registers: Latency Tolerance Reporting (LTR) Registers'.

18.3.8.78 0x1000 PCIe SII APP PM UNLOCK Register (Default Value: 0x0000_0000)

Offset: 0x1000			Register Name: SII_APP_PM_UNLOCK
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	APP_UNLOCK_MSG app_unlock_msg_ahb Request from your application to generate an Unlock message. You must assert this signal for one clock cycle. The controller does not return an acknowledgment or grant signal. You must not pulse the same signal again, until the previous message has been transmitted.
0	R/W	0x0	APP_PM_XMT_TURNOFF apps_pm_xmt_turnoff_ahb Request from your application to generate a PM_Turn_Off message. You must assert this signal for one clock cycle. The controller does not return an acknowledgment or grant signal. You must not pulse the same signal again, until the previous message has been transmitted.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.3.8.79 0x1100 PCIe SII Power Manage Register0 (Default Value: 0x0000_0000)

Offset: 0x1100			Register Name: SII_APP_PM_0
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	APPS_PM_XMT_PME_3 apps_pm_xmt_pme[3] , Wake Up. If PME is enabled and PME support is configured for current PMCSR D-state asserting this signal will cause the controller to wake from either L1 or L2 state. When the controller has transitioned back to the L0 state it will transmit a PME message and set the PME_Status. Upon receiving the PME message the root complex should clear the PME_Status and change the D-state back to D0.
22	R/W	0x0	OUTBAND_PWRUP_CMD_3 outband_pwrup_cmd[3] , Wake Up. If PME is enabled and PME support is configured for current PMCSR D-state asserting this signal will cause the controller to wake from either L1 or L2 state. When the controller has transitioned back to the L0 state it will transmit a PME message and set the PME_Status. There is a separate outband_pwrup_cmd input bit for each function in your controller configuration. This port is functionally identical to apps_pm_xmt_pme. Upon receiving the PME message the root complex should clear the PME_Status and change the D-state back to D0.
21	R/W	0x0	APPS_PM_XMT_PME_2 apps_pm_xmt_pme[2]
20	R/W	0x0	OUTBAND_PWRUP_CMD_2 outband_pwrup_cmd[2]
19	R/W	0x0	APPS_PM_XMT_PME_1 apps_pm_xmt_pme[1]
18	R/W	0x0	OUTBAND_PWRUP_CMD_1 outband_pwrup_cmd[1]
17	R/W	0x0	APPS_PM_XMT_PME_0 apps_pm_xmt_pme[0]
16	R/W	0x0	OUTBAND_PWRUP_CMD_0 outband_pwrup_cmd[0]
15:13	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1100			Register Name: SII_APP_PM_0
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	APP_L1SUB_DISABLE The application can set this input to 1'b1 to prevent entry to L1 Sub-states. This pin is used to gate the L1 sub-state enable bits from the L1 PM Substates Control 1 Register.
11	R/W	0x0	APP_L1_PWR_OFF_EN Application permits to gate power to parts of the controller in L1 state
10	R/W	0x0	ACK_EN_VMAIN Acknowledge from power switch responsible for autonomous power-gating in L1.2. This signal is synchronized using aux_clk and can be driven/supplied asynchronously to the controller in certain low-power modes.
9	R/W	0x0	TEST_BYPASS_LP Test mode override of isolation enable
8	R/W	0x0	APP_CLK_PM_EN Clock PM feature enabled by application. Used to inhibit the programming of the Clock PM in Link Control Register. For more details, see 'L1 with Clock PM (L1 with REFCLK removal/PLL Off)'.
7	R/W	0x0	CLKREQ_IN_N Status of the CLKREQ# bidirectional CMOS board-level signal. Used by the controller to determine when to enter and exit L1 Substates when using the CLKREQ#-based mechanism. For more details, see 'L1 Substates'. This signal is synchronized using aux_clk and can be driven/supplied asynchronously to the controller in certain low-power modes.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1100			Register Name: SII_APP_PM_0
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	APP_XFER_PENDING Indicates that your application has transfers pending and prevents the controller from entering L1. This is a level signal used to inform the controller about the state of external queues and pipeline stages that contain transactions to be transmitted by the controller. The controller uses this information to determine when to enter/exit L1. When this signal is asserted, it indicates that there are transactions outside the controller that the controller needs to transmit. When de-asserted, it indicates that there are no transactions outside the controller. The controller responds to an assertion on this signal as follows: ▪ Upstream Ports: Prevents generation of requests to enter L1. Triggers exit if already in L1. ▪ Downstream Ports: Triggers exit if already in L1. You can instruct the controller to exit L1 by asserting either or both of app_xfer_pending and app_req_exit_l1. The controller only samples app_req_exit_l1 when the controller is already in the L1 state.
5	R/W	0x0	APP_REQ_EXIT_L1 Application request to Exit L1. Request from your application to exit L1. It is only effective when L1 is enabled.
4	R/W	0x0	APP_READY_ENTR_L23 Application Ready to Enter L23. Indication from your application that it is ready to enter the L23 state. The app_ready_entr_l23 signal is provided for applications that must control L23 entry (in case certain tasks must be performed before going into L23). The controller delays sending PM_Enter_L23 (in response to PM_Turn_Off) until this signal becomes active. When this signal has been asserted by the application, it must be kept asserted until L2 entry has completed. Hardwire to 1 for applications that do not require this feature. Note: The controller ignores this input in RC mode.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1100			Register Name: SII_APP_PM_0
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	APP_REQ_ENTR_L1_AHB app_req_entr_l1_ahb Application request to Enter L1 ASPM state. The app_req_entr_l1 signal is for use by applications that need to control L1 entry instead of using the L1 entry timer as defined in the PCI Express Specification. It is only effective when L1 is enabled. The controller latches this request when in L0 or L0s; to be acted upon later. Note: The controller ignores this input in RC mode.
2	R/W	0x0	SYS_AUX_PWR_DET Auxiliary Power Detected. Used to report to the host software that auxiliary power (Vaux) is present.
1:0	/	/	/

18.3.8.80 0x1104 PCIe SII Power Manage Register1 (Default Value: 0x0000_0000)

Offset: 0x1104			Register Name: SII_APP_PM_1
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R	0x0	PM_LINKST_L2_EXIT pm_linkst_l2_exit
23	R	0x0	PM_LINKST_IN_L2 pm_linkst_in_l2
22	R	0x0	PM_LINKST_IN_L1 pm_linkst_in_l1
21	R	0x0	PM_LINKST_IN_L0S pm_linkst_in_l0s
20:15	/	/	/
14	R	0x0	PCIe_WAKE_N pcie_wake_n
13	R	0x0	LOCAL_REF_CLK_REQ_N local_ref_clk_req_n
12	R	0x0	WAKE wake
11:10	/	/	/
9:4	R	0x0	SMLH_LTSSM_STATE smlh_ltssm_state
3	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1104			Register Name: SII_APP_PM_1
Bit	Read/Write	Default/Hex	Description
2:0	R	0x0	PM_CURNT_STATE pm_curnt_state

18.3.8.81 0x1108 PCIe SII Power Manage Register2 (Default Value: 0x0000_0000)

Offset: 0x1108			Register Name: SII_APP_PM_2
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18:16	R	0x0	PM_L1SUB_STATE pm_l1sub_state
15:13	/	/	/
12:8	R	0x0	PM_SLAVE_STATE pm_slave_state
7:5	/	/	/
4:0	R	0x0	PM_MASTER_STATE pm_master_state

18.3.8.82 0x110c PCIe SII Power Manage Register3 (Default Value: 0x0404_0404)

Offset: 0x110c			Register Name: SII_APP_PM_3
Bit	Read/Write	Default/Hex	Description
31	R	0x0	DPA_SUBSTATE_UPDATE_3 dpa_substate_update [3]
30	R	0x0	AUX_PM_EN_3 aux_pm_en[3]
29	R	0x0	PM_STATUS_3 pm_status[3]
28	R	0x0	PM_PME_EN_3 pm_pme_en[3]
27	/	/	/
26:24	R	0x4	PM_DSTATE_3 pm_dstate[11:9]
23	R	0x0	DPA_SUBSTATE_UPDATE_2 dpa_substate_update [2]
22	R	0x0	AUX_PM_EN_2 aux_pm_en[2]
21	R	0x0	PM_STATUS_2 pm_status[2]
20	R	0x0	PM_PME_EN_2 pm_pme_en[2]

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x110c			Register Name: SII_APP_PM_3
Bit	Read/Write	Default/Hex	Description
19	/	/	/
18:16	R	0x4	PM_DSTATE_2 pm_dstate[8:6]
15	R	0x0	DPA_SUBSTATE_UPDATE_1 dpa_substate_update [1]
14	R	0x0	AUX_PM_EN_1 aux_pm_en[1]
13	R	0x0	PM_STATUS_1 pm_status[1]
12	R	0x0	PM_PME_EN_1 pm_pme_en[1]
11	/	/	/
10:8	R	0x4	PM_DSTATE_1 pm_dstate[5:3]
7	R	0x0	DPA_SUBSTATE_UPDATE_0 dpa_substate_update [0]
6	R	0x0	AUX_PM_EN_0 aux_pm_en[0]
5	R	0x0	PM_STATUS_0 pm_status[0]
4	R	0x0	PM_PME_EN_0 pm_pme_en[0]
3	/	/	/
2:0	R	0x4	PM_DSTATE_0 pm_dstate[2:0]

18.3.8.83 0x1200 PCIe SII Receive CPL Register (Default Value: 0x0000_0000)

Offset: 0x1200			Register Name: SII_RX_CPL
Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	RADM_TIMEOUT_CPL_TAG radm_timeout_cpl_tag
23:21	/	/	/
20:9	R	0x0	RADM_TIMEOUT_CPL_LEN radm_timeout_cpl_len
8:7	R	0x0	RADM_TIMEOUT_CPL_ATTR radm_timeout_cpl_attr
6:4	R	0x0	RADM_TIMEOUT_CPL_TC radm_timeout_cpl_tc
3:1	R	0x0	RADM_TIMEOUT_FUNC_NUM radm_timeout_func_num

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1200			Register Name: SII_RX_CPL
Bit	Read/Write	Default/Hex	Description
0	R	0x0	RADM_CPL_TIMEOUT radm_cpl_timeout

18.3.8.84 0x1300 PCIe SII Transmit Register (Default Value: 0x0000_0000)

Offset: 0x1300			Register Name: SII_TX
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R	0x0	PM_XTLH_BLOCK_TLP pm_xtlh_block_tlp

18.3.8.85 0x1350 PCIe SII Gen3-Only Equalization Register (Default Value: 0x0000_0000)

Offset: 0x1350			Register Name: SII_GEN3_EQ
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R	0x0	SMLH_LTSSM_STATE_RCVRY_EQ smlh_ltssm_state_rcvry_eq

18.3.8.86 0x13F0 PCIe Function Level Reset Control Register (Default Value: 0x0000_0000)

Offset: 0x13F0			Register Name: FLR_CTRL
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:8	R	0x0	FLR_PF_ACTIVE The FLR state in EP mode Bit8-11 indicates function 0-3 When remote RC enables FLR for a specific function on EP, the corresponding bit is set to 1. When the FLR finishes, the corresponding bit is set to 0.
3:0	R/WAC	0x0	FLR_PF_DONE FLR signals in EP mode Bit0~3 indicates function 0-3 After FLR interrupts are enabled, the function data structure is initialized, and no TLP of the function exists in the transmission queue, the corresponding bit is set to 1. When the FLR finishes, the corresponding bit is set to 0.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.3.8.87 0x1400 PCIe SII Target Completion Register (Default Value: 0x0000_0000)

Offset: 0x1400			Register Name: SII_TRGT_CPL
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:9	R	0x0	TRGT_TIMEOUT_CPL_LEN trgt_timeout_cpl_len
8:7	R	0x0	TRGT_TIMEOUT_CPL_ATTR trgt_timeout_cpl_attr
6:4	R	0x0	TRGT_TIMEOUT_CPL_TC trgt_timeout_cpl_tc
3:1	R	0x0	TRGT_TIMEOUT_FUNC_NUM trgt_timeout_func_num
0	R	0x0	TRGT_CPL_TIMEOUT trgt_cpl_timeout

18.3.8.88 0x1404 PCIe SII Target Lookup Register (Default Value: 0x8000_0000)

Offset: 0x1404			Register Name: SII_TRGT_LUP
Bit	Read/Write	Default/Hex	Description
31	R	0x1	TRGT_LOOKUP_EMPTY trgt_lookup_empty
30:24	/	/	/
23:16	R	0x0	TRGT_LOOKUP_ID trgt_lookup_id
15:8	/	/	/
7:0	R	0x0	TRGT_TIMEOUT_LOOKUP_ID trgt_timeout_lookup_id

18.3.8.89 0x1500 PCIe SII Error Report Register (Default Value: 0x0000_0000)

Offset: 0x1500			Register Name: SII_ERR_RPT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R	0x0	CFG_F_ERR_RPT_EN_3 cfg_f_err_rpt_en[3]
14	R	0x0	CFG_NF_ERR_RPT_EN_3 cfg_nf_err_rpt_en[3]
13	R	0x0	CFG_COR_ERR_RPT_EN_3 cfg_cor_err_rpt_en[3]
12	R	0x0	CFG_REG_SERREN_3 cfg_reg_serren[3]

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x1500			Register Name: SII_ERR_RPT
Bit	Read/Write	Default/Hex	Description
11	R	0x0	CFG_F_ERR_RPT_EN_2 cfg_f_err_rpt_en[2]
10	R	0x0	CFG_NF_ERR_RPT_EN_2 cfg_nf_err_rpt_en[2]
9	R	0x0	CFG_COR_ERR_RPT_EN_2 cfg_cor_err_rpt_en[2]
8	R	0x0	CFG_REG_SERREN_2 cfg_reg_serren[2]
7	R	0x0	CFG_F_ERR_RPT_EN_1 cfg_f_err_rpt_en[1]
6	R	0x0	CFG_NF_ERR_RPT_EN_1 cfg_nf_err_rpt_en[1]
5	R	0x0	CFG_COR_ERR_RPT_EN_1 cfg_cor_err_rpt_en[1]
4	R	0x0	CFG_REG_SERREN_1 cfg_reg_serren[1]
3	R	0x0	CFG_F_ERR_RPT_EN_0 cfg_f_err_rpt_en[0]
2	R	0x0	CFG_NF_ERR_RPT_EN_0 cfg_nf_err_rpt_en[0]
1	R	0x0	CFG_COR_ERR_RPT_EN_0 cfg_cor_err_rpt_en[0]
0	R	0x0	CFG_REG_SERREN_0 cfg_reg_serren[0]

18.3.8.90 0x1600 PCIe SII CFG HW Register (Default Value: 0x0000_0000)

Offset: 0x1600			Register Name: SII_CFG_HW_AUTO_SP_DIS
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R	0x0	CFG_HW_AUTO_SP_DIS cfg_hw_auto_sp_dis

18.3.8.91 0x1800+N*0x100 (N=0~3) PCIe SII PF CFG BAR0 Start Register0 (Default Value: 0x0000_0000)

Offset: 0x1800+N*0x100 (N=0~3)			Register Name: SII_PF_N_CFG_BAR0_START0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PF_N_CFG_BAR0_START_0 cfg_bar0_start[31:0]

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.3.8.92 0x1804+N*0x100 (N=0~3) PCIe SII PF CFG BAR0 Start Register1 (Default Value: 0x0000_0000)

Offset: 0x1804+N*0x100 (N=0~3)			Register Name: SII_PF_N_CFG_BAR0_START1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PF_N_CFG_BAR0_START_1 cfg_bar0_start[63:32]

18.3.8.93 0x1808+N*0x100 (N=0~3) PCIe SII PF CFG BAR0 Limit Register0 (Default Value: 0x0000_0000)

Offset: 0x1808+N*0x100 (N=0~3)			Register Name: SII_PF_N_CFG_BAR0_LIMIT0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PF_N_CFG_BAR0_ LIMIT_0 cfg_bar0_limit[31:0]

18.3.8.94 0x180c+N*0x100 (N=0~3) PCIe SII PF CFG BAR0 Limit Register1 (Default Value: 0x0000_0000)

Offset: 0x180c+N*0x100 (N=0~3)			Register Name: SII_PF_N_CFG_BAR0_LIMIT1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PF_N_CFG_BAR0_ LIMIT_1 cfg_bar0_limit[63:32]

18.3.8.95 0x1810+N*0x100 (N=0~3) PCIe SII PF CFG BAR1 Start Register (Default Value: 0x0000_0001)

Offset: 0x1810+N*0x100 (N=0~3)			Register Name: SII_PF_N_CFG_BAR1_START
Bit	Read/Write	Default/Hex	Description
31:0	R	0x1	PF_N_CFG_BAR1_START cfg_bar1_start[31:0]

18.3.8.96 0x1818+N*0x100 (N=0~3) PCIe SII PF CFG BAR1 Limit Register (Default Value: 0x0000_0000)

Offset: 0x1818+N*0x100 (N=0~3)			Register Name: SII_PF_N_CFG_BAR1_LIMIT
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PF_N_CFG_BAR1_ LIMIT cfg_bar1_limit[31:0]

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.3.8.97 0x1820+N*0x100 (N=0~3) PCIe SII PF CFG BAR2 Start Register0 (Default Value: 0x0000_0001)

Offset: 0x1820+N*0x100 (N=0~3)			Register Name: SII_PF_N_CFG_BAR2_START0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x1	PF_N_CFG_BAR2_START_0 cfg_bar2_start[31:0]

18.3.8.98 0x1824+N*0x100 (N=0~3) PCIe SII PF CFG BAR2 Start Register1 (Default Value: 0x0000_0000)

Offset: 0x1824+N*0x100 (N=0~3)			Register Name: SII_PF_N_CFG_BAR2_START1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PF_N_CFG_BAR2_START_1 cfg_bar2_start[63:32]

18.3.8.99 0x1828+N*0x100 (N=0~3) PCIe SII PF CFG BAR2 Limit Register0 (Default Value: 0x0000_0000)

Offset: 0x1828+N*0x100 (N=0~3)			Register Name: SII_PF_N_CFG_BAR2_LIMIT0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PF_N_CFG_BAR2_ LIMIT_0 cfg_bar2_limit[31:0]

18.3.8.100 0x182c+N*0x100 (N=0~3) PCIe SII PF CFG BAR2 Limit Register1 (Default Value: 0x0000_0000)

Offset: 0x182c+N*0x100 (N=0~3)			Register Name: SII_PF_N_CFG_BAR2_LIMIT1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PF_N_CFG_BAR2_ LIMIT_1 cfg_bar2_limit[63:32]

18.3.8.101 0x1830+N*0x100 (N=0~3) PCIe SII PF CFG BAR3 Start Register (Default Value: 0x0000_0001)

Offset: 0x1830+N*0x100 (N=0~3)			Register Name: SII_PF_N_CFG_BAR3_START
Bit	Read/Write	Default/Hex	Description
31:0	R	0x1	PF_N_CFG_BAR3_START cfg_bar3_start[31:0]

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.3.8.102 0x1838+N*0x100 (N=0~3) PCIe SII PF CFG BAR3 Limit Register (Default Value: 0x0000_0000)

Offset: 0x1838+N*0x100 (N=0~3)			Register Name: SII_PF_N_CFG_BAR3_LIMIT
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PF_N_CFG_BAR3_ LIMIT cfg_bar3_limit[31:0]

18.3.8.103 0x1840+N*0x100 (N=0~3) PCIe SII PF CFG BAR4 Start Register0 (Default Value: 0x0000_0001)

Offset: 0x1840+N*0x100 (N=0~3)			Register Name: SII_PF_N_CFG_BAR4_START0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x1	PF_N_CFG_BAR4_START_0 cfg_bar4_start[31:0]

18.3.8.104 0x1844+N*0x100 (N=0~3) PCIe SII PF CFG BAR4 Start Register1 (Default Value: 0x0000_0000)

Offset: 0x1844+N*0x100 (N=0~3)			Register Name: SII_PF_N_CFG_BAR4_START1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PF_N_CFG_BAR4_START_1 cfg_bar4_start[63:32]

18.3.8.105 0x1848+N*0x100 (N=0~3) PCIe SII PF CFG BAR4 Limit Register0 (Default Value: 0x0000_0000)

Offset: 0x1848+N*0x100 (N=0~3)			Register Name: SII_PF_N_CFG_BAR4_LIMIT0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PF_N_CFG_BAR4_ LIMIT_0 cfg_bar4_limit[31:0]

18.3.8.106 0x184c+N*0x100 (N=0~3) PCIe SII PF CFG BAR4 Limit Register1 (Default Value: 0x0000_0000)

Offset: 0x184c+N*0x100 (N=0~3)			Register Name: SII_PF_N_CFG_BAR4_LIMIT1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PF_N_CFG_BAR4_ LIMIT_1 cfg_bar4_limit[63:32]

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.3.8.107 0x1850+N*0x100 (N=0~3) PCIe SII PF CFG BAR5 Start Register (Default Value: 0x0000_0001)

Offset: 0x1850+N*0x100 (N=0~3)			Register Name: SII_PF_N_CFG_BAR5_START
Bit	Read/Write	Default/Hex	Description
31:0	R	0x1	PF_N_CFG_BAR5_START cfg_bar5_start[31:0]

18.3.8.108 0x1858+N*0x100 (N=0~3) PCIe SII PF CFG BAR5 Limit Register (Default Value: 0x0000_0000)

Offset: 0x1858+N*0x100 (N=0~3)			Register Name: SII_PF_N_CFG_BAR5_LIMIT
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PF_N_CFG_BAR5_ LIMIT cfg_bar5_limit[31:0]

18.3.8.109 0x1860+N*0x100 (N=0~3) PCIe SII PF RBAR Ctrl Register (Default Value: 0x0000_0000)

Offset: 0x1860+N*0x100 (N=0~3)			Register Name: SII_PF_N_VF_RBAR_CTRL
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R	0x0	PF_N_VF_RBAR_CTRL_UPDATE_0 vf_rbar_ctrl_update[0]
15:1	/	/	/
0	R	0x0	PF_N_RBAR_CTRL_UPDATE_0 rbar_ctrl_update[0]

18.3.8.110 0x1870+N*0x100 (N=0~3) PCIe SII PF RBAR Size Register0 (Default Value: 0x0000_0000)

Offset: 0x1870+N*0x100 (N=0~3)			Register Name: SII_PF_N_CFG_RBAR_SIZE_0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PF_N_CFG_RBAR_SIZE_0 cfg_rbar_size[31:0]

18.3.8.111 0x1874+N*0x100 (N=0~3) PCIe SII PF RBAR Size Register1 (Default Value: 0x0000_0000)

Offset: 0x1874+N*0x100 (N=0~3)			Register Name: SII_PF_N_CFG_RBAR_SIZE_1
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R	0x0	PF_N_CFG_RBAR_SIZE_1 cfg_rbar_size[35:32]

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.3.8.112 0x1878+N*0x100 (N=0~3) PCIe SII PF VF RBAR Size Register0 (Default Value: 0x0000_0000)

Offset: 0x1878+N*0x100 (N=0~3)			Register Name: SII_PF_N_CFG_VF_RBAR_SIZE_0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PF_N_CFG_VF_RBAR_SIZE_0 cfg_vf_rbar_size[31:0]

18.3.8.113 0x187c+N*0x100 (N=0~3) PCIe SII PF VF RBAR Size Register1 (Default Value: 0x0000_0000)

Offset: 0x187c+N*0x100 (N=0~3)			Register Name: SII_PF_N_CFG_VF_RBAR_SIZE_1
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R	0x0	PF_N_CFG_VF_RBAR_SIZE_1 cfg_rbar_size[35:32]

18.3.8.114 0x1880+N*0x100 (N=0~3) PCIe SII PF CFG EXP ROM Start Register (Default Value: 0x0000_0000)

Offset: 0x1880+N*0x100 (N=0~3)			Register Name: SII_PF_N_CFG_EXP_ROM_START
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PF_N_CFG_EXP_ROM_START cfg_exp_rom_start[31:0]

18.3.8.115 0x1884+N*0x100 (N=0~3) PCIe SII PF CFG EXP ROM Limit Register (Default Value: 0x0000_0000)

Offset: 0x1884+N*0x100 (N=0~3)			Register Name: SII_PF_N_CFG_EXP_ROM_LIMIT
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PF_N_CFG_EXP_ROM_ LIMIT cfg_EXP_ROM_limit[31:0]

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.4 USB3.1 GEN2 DRD

18.4.1 Overview

The USB3.1 GEN2 DRD is a Dual-Role Device (DRD) controller, which supports both device and host functions which can also be configured as a Host-only or Device-only controller, fully compliant with the USB 3.1 Specification. It can support super-speed plus (SSP, 10-Gbps), super-speed (SS, 5-Gbps), high-speed (HS, 480-Mbps), full-speed (FS, 12-Mbps), and low-speed (LS, 1.5-Mbps) transfers in Host mode. It can support super-speed plus (SSP, 10-Gbps), super-speed (SS, 5-Gbps), high-speed (HS, 480-Mbps), and full-speed (FS, 12-Mbps) in Device mode. Standard USB transceiver can be used through its UTMI+ interface and PIPE interface.

The USB3.1 GEN2 DRD controller includes the following features:

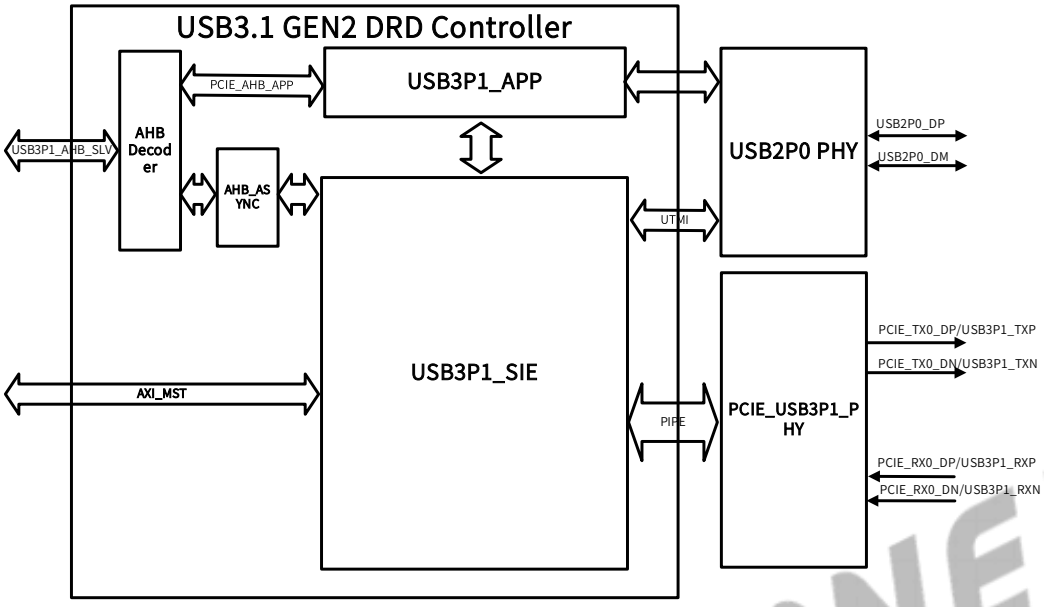
- Supports Super-Speed Plus (SSP, 10-Gbps), Super-Speed (SS, 5-Gbps), High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) in Device mode
- Supports Super-Speed Plus (SSP, 10-Gbps), Super-Speed (SS, 5-Gbps), High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) and Low-Speed (LS, 1.5-Mbps) in Host mode
- Supports Device or Host operation at a time
- AXI interface for DMA operation
- AHB Slave interface for read and write access to the core s Control and Status Registers (CSRs).
- USB3.1 PIPE PHY interface
- USB2.0 UTMI+ PHY interface. USB3.1 has independent USB2.0 PHY.
- Supports up to 16 Endpoints IN including control endpoint 0 , 16 Endpoints OUT including control endpoint 0 in device mode
- 15 pairs of endpoints share TX FIFO (21 KB) and RX FIFO (asynchronous transmission 8KB and periodic transmission 8KB). The size of Endpoint 0 RX/TX FIFO is 64B.
- Simultaneous IN and OUT transfer support in Super-Speed Plus and Super-Speed mode
- Dual-port interfaces for Tx data buffering, Rx data prefetching, and descriptor and register caching
- Three RAMs are configuration as Rx Data FIFO RAM, Tx Data FIFO RAM, Descriptor/Register Cache RAM
- Hardware handles all data transfer
- Implements both static and dynamic power reduction techniques at multiple levels
- Compatible with XHCI1.2 protocol.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.4.2 Block Diagram

The following figure shows the block diagram of USB3.1 GEN2 DRD Controller

Figure 18-8 USB3.1 GEN2 DRD Controller Block Diagram



18.4.3 Clock Sources

The following table describes the clock sources of USB3.1 GEN2 DRD (USB2_U3) and USB2.0 PHY (USB2_U2). For clock setting, configurations, and gating information, refer to the section CCU.

Module	Clock Sources	Description
USB2_U3_UTMI	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.
	PERI0_300M	Its frequency is 300 MHz by default.
	DCXO	The external high-frequency crystal oscillator. Its frequency is 26 MHz.
USB2_U2_PIPE	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.
	PERI0_480M	Its frequency is 480 MHz by default.
	DCXO	The external high-frequency crystal oscillator. Its frequency is 26 MHz.
USB2_U2_REF	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.
	DCXO	The external high-frequency crystal oscillator. Its frequency is 26 MHz.
USB2_SUSPEND	RTC_32K	It is 32.768 KHz by default.
	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.
USB2_MF	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

	PERI0_300M	Its frequency is 300 MHz by default.
	DCXO	The external high-frequency crystal oscillator. Its frequency is 26 MHz.

18.4.4 Register List

18.4.4.1 USB3.1 GEN2 DRD Controller Base Address

Module Name	Base Address
USB3P1_DRD	0x06A00000

18.4.4.2 USB3.1 GEN2 DRD Controller Register Class

Register Class	Offset	Description
xHCI Registers	0x00000000 - 0x00007FFF	For register definition and description, please see eXtensible Host Controller Interface for Universal Serial Bus (xHCI), Revision 1.1
Global Registers	0x0000C100 - 0x0000C6FF	For register definition and description, please see DesignWare® Cores Enhanced SuperSpeed USB3.1 Controller Program Guide, Version 1.90a.
Device Registers	0x0000C700 - 0x0000CBFF	
Application Registers	0x00100000 - 0x001007FF	For register definition and description, please see the section Application Register Description.

18.4.4.3 Application Register List

Register Name	Offset	Description
U2P0_ISCR	0x0000	USB2.0 Interface Status and Control Register
U2P0_PHYCTL	0x0010	USB2.0 PHY Control Register
U2P0_PHYTST	0x0014	USB2.0 PHY TEST Register
U2P0_PHYTUNE	0x0018	USB2.0 PHY Tune Register
U2P0_PHYSTS	0x0024	USB2.0 PHY Status Register

18.4.5 Register Description

The following are the application register description.

18.4.5.1 0x0000 USB2.0 Interface Status and Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: U2P0_ISCR
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: U2P0_ISCR
Bit	Read/Write	Default/Hex	Description
31:27	R	0	BC_ID_Value_Status These fields indicate the Mult ID value.
26:25	R	0	USB Line Status [26]-DM [27]-DP
24	R	0	USB VBUS Status These filed indicate the VBUS status.
23:18	R/W	0	Forcerid 1xxxxx: Force the ID value of bit[22:18] output to SIE 0xxxxx: Select phy output the ID value to SIE
17:16	/	/	/
15:14	R/W	0	Force ID 0x: use external ID Status 10: force ID to LOW 11: force ID to HIGH
13:12	R/W	0	Force VBUS Valid (For SIE) 0x: use external VBUS Valid Status from VBUS Input or Line State 10: force VBUS Valid to LOW 11: force VBUS Valid to HIGH
11:10	R/W	0	External VBUS Valid Source Select 0x: External VBUS Valid detected from VBUS Input 10: External VBUS Valid detected from DP/DM Input 11: External VBUS Valid detected from either VBUS or DP/DM input
9	R/W	0	USB Wakeup Enable 0: Disable 1: Enable
8	/	/	/
7	R/W1C	0	USB ID Mult Value Change Interrupt Status 0: No Change 1: Has Change
6	R/W1C	0	VBUS Input Change Detect Interrupt Status 0: No Change 1: Has Change
5	R/W1C	0	ID Input Change Detect Interrupt Status 0: No Change 1: Has Change
4	R/W1C	0	DP/DM Input Change Detect Interrupt Status 0: No Change 1: Has Change

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: U2P0_ISCR
Bit	Read/Write	Default/Hex	Description
3	R/W	0	USB ID Mult Value Detect Enable 0: Disable 1: Enable
2	R/W	0	VBUS Input Change Detect Interrupt Enable 0: Disable 1: Enable
1	R/W	0	ID Input Change Detect Interrupt Enable 0: Disable 1: Enable
0	R/W	0	DP/DM Input Change Detect Interrupt Enable 0: Disable 1: Enable

18.4.5.2 0x0010 USB2.0 PHY Control Register (Default Value: 0x0002_2418

Offset: 0x0010			Register Name: U2P0_PHYCTL
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20	R/W	0x0	ATERESET Reset Input from Automatic Test Equipment When the USB 2.0 femtoPHY is powered up (not in Suspend or Sleep mode), an automatic tester can use this test signal to disable PHYCLOCK<#> and FREECLK, then re-enable them with an aligned phase. 1: The PHYCLOCK<#> and FREECLK outputs are disabled. 0: The PHYCLOCK<#> and FREECLK outputs are available within a specific period after ATERESET is de-asserted.
19	R/W	0x1	TXBITSTUFFENH High-Byte Transmit Bit-Stuffing Enable This controller signal controls bit stuffing on DATAINH0[7:0] when OPMODE0[1:0] = 2'b11. 1: Bit stuffing is enabled. 0: Bit stuffing is disabled.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0010			Register Name: U2P0_PHYCTL
Bit	Read/Write	Default/Hex	Description
18	R/W	0x1	TXBITSTUFFEN Low-Byte Transmit Bit-Stuffing Enable This controller signal controls bit stuffing on DATAIN0[7:0] when OPMODE0[1:0] = 2'b11. 1: Bit stuffing is enabled. 0: Bit stuffing is disabled.
17	R/W	0x1	RETENABLEN
16	R/W	0x0	AUTORSMENB
15	/	/	/
14:12	R/W	0x2	FSEL PHY reference clock frequency 000: 19.2MHz; 001: 20MHz; 010: 24MHz
11	/	/	/
10	R/W	0x1	OTGDISABLE This signal powers down the VBUS Valid comparator, but not the Session Valid comparator, nor the ID detection circuitry. To save power, if the application does not use the OTG function, this input can be set high. 1: The OTG block is powered down. 0: The OTG block is powered up.
9	R/W	0x0	DRVVBUS This controller signal controls the VBUS Valid comparator. This signal drives 5 V on VBUS through an external charge pump. When OTGDISABLE0 is set to 1'b0 and DRVVBUS0 is asserted, the Bandgap circuitry and VBUS Valid comparator are powered, even in Suspend or Sleep mode. 1: The VBUS Valid comparator is enabled. 0: The VBUS Valid comparator is disabled.
8	R/W	0x0	VREGBYPASS This signal controls the VReg18 bypass mode. 1: The VReg18 is bypassed. 1.8V power supply needs to be provided on VDDH. 0: The VReg18 is not bypassed. A 3.3V supply needs to be provided on VDDH and the internal 1.8V supply is generated by the VReg18.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0010			Register Name: U2P0_PHYCTL
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	LOOPBACKENB This signal places the USB 2.0 femtoPHY in Loopback mode, which enables the receive and transmit logic concurrently. 1: During data transmission, the receive logic is enabled. 0: During data transmission, the receive logic is disabled.
6	R/W	0x0	IDPULLUP This controller signal controls ID line sampling. 1: ID pin sampling is enabled, and the IDDIG0 output is valid. 0: ID pin sampling is disabled, and the IDDIG0 output is not valid
5	R/W	0x0	VBUSVLDEXT 1: The VBUS signal is valid, and the pull-up resistor on D+ is enabled. 0: The VBUS signal is not valid, and the pull-up resistor on D+ is disabled.
4	R/W	0x1	VBUSVLDEXTSEL 1: The VBUSVLDEXT input is used to assert the DP pull-up resistor. 0: The internal Session Valid comparator is used to assert the DP pull-up resistor.
3	R/W	0x1	SIDDQ 1: Write 1 to disable phy. 0: Write 0 to enable phy.
2	R/W	0x0	COMMONONN 1: In Suspend mode, the REFCLK_LOGIC, Bias, and PLL blocks are powered down. In Sleep mode, the Bias and PLL blocks are powered down. 0: In Suspend or Sleep modes, the REFCLK_LOGIC, Bias, and PLL blocks remain powered. With this setting, the input reference clock must remain on and valid during suspend or sleep.
1:0	R/W	0x0	VATESTENB Analog Test Pin Select Enables analog test voltages to be placed on either the ANALOGTEST or ID0 pin. 11: Reserved. Invalid setting. 10: Analog test voltages can be viewed or applied on ANALOGTEST.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.4.5.3 0x0014 USB2.0 PHY TEST Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: U2P0_PHYTST
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14	R/W	0x0	TESTBURNIN Burn-in Test Enable This input enables the built-in, self-burn-in testing function of the PHY. At assertion of this signal, the PHY performs a power-on-reset sequence and then enters HS Loopback mode. In HS Loopback mode, the PHY continues to transmit alternating 1's and 0's at the maximum bit rate until TESTBURNIN is de-asserted. This input has precedence over the SUSPENDM0, PORTRESET0, ATERESET, and SLEEPM0 signals. Therefore, these signals are internally overridden when TESTBURNIN is asserted. Asserting TESTBURNIN causes the FSEL[2:0] and REFCLKSEL[1:0] signals to be overridden, so that the PHY requires a 50-MHz reference clock on CLKCORE. If this signal is not used, tie it low. To accomplish the same function with a different reference clock frequency, the PHY can be put into BIST Test Packet Repeat mode.
13	R/W	0x0	TESTDATAOUTSEL Test Data Out Select This test signal determines which signals appear on TESTDATAOUT[3:0]. 1: Mode-defined test register contents are output. 0: Mode-defined, internally generated signals are output. If this signal is not used, tie it low.
12	R/W	0x0	TESTCLK Clocking Signal for TESTDATAIN<#>[7:0] This is a clocking signal for TESTDATAIN<#>[7:0]. The test interface uses the positive edge of TESTCLK<#> to latch TESTDATAIN<#>[7:0]. TESTCLK<#> does not need to be a continuous clock. If this signal is not used, tie it low.
11:8	R/W	0x0	TESTADDR[3:0] Test Interface Register Address This bus specifies the register address for writing to or reading from the test interface register. If this bus is not used, tie it to 4'b0000.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: U2P0_PHYTST
Bit	Read/Write	Default/Hex	Description
7:0	R/W	0x0	TESTDATAIN[7:0] Test Data Write Bus This test bus holds test data to be written tothe USB 2.0 femtoPHY. Test data is presented on bits [3:0], and the corresponding write enable is presented on bits[7:4]. If this bus is not used, tie it low.

18.4.5.4 0x0018 USB2.0 PHY Tune Register (Default Value: 0x1433_33D4)

Offset: 0x0018			Register Name: U2P0_PHYTUNE
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	VDATREFTUNE[1:0] Data Detect Voltage Adjustment This bus adjusts the threshold voltage level (Vdat_ref) used to detect data during charger type detection. 11: -20% 10: -10% 01: 0, Design default 00: +10% This bus is a strapping option that must be set prior to a power-on reset and remain static during normal operation. Strapping options are not critical for STA, and any other timings or loading limits for the pin are specified in the .lib timing model included in the product deliverables.
27	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0018			Register Name: U2P0_PHYTUNE
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x4	COMPDISTUNE[2:0] Disconnect Threshold Adjustment This bus adjusts the voltage level for the threshold used to detect a disconnect event at the host. 111: +9.88% 110: +6.39 101: +3.07% 100: 0, Design default 011: -2.95% 010: -5.66% 001: -8.27% 000: -10.68% If this bus is not used, leave it at the default setting. When the PHY is in a HOST role where the HOSTDISCONNECT0 signal is used, any adjustment of the HS transmits voltage level tune bits (TXVREFTUNE0[3:0]) might also necessitate a change to the HS disconnect detection threshold tune bits (COMPDISTUNE0[2:0]). This change might be required because the HS disconnect detection threshold might need to be increased (or decreased) if the HS transmit voltage level is increased (or decreased). This bus is a strapping option that must be set prior to a power-on reset and remain static during normal operation. Strapping options are not critical for STA, and any other timings or loading limits for the pin are specified in the .lib timing model included in the product deliverables.
23	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0018			Register Name: U2P0_PHYTUNE
Bit	Read/Write	Default/Hex	Description
22:20	R/W	0x3	SQRXTUNE[2:0] Squelch Threshold Adjustment This bus adjusts the voltage level for the threshold used to detect valid high-speed data. 111: -20% 110: -15% 101: -10% 100: -5% 011: 0, Design default 010: +5% 001: +10% 000: +15% This bus is a strapping option that must be set prior to a power-on reset and remain static during normal operation. Strapping options are not critical for STA, and any other timings or loading limits for the pin are specified in the .lib timing model included in the product deliverables.
19	R/W	0x0	TXPREEMPPULSETUNE HS Transmitter Pre-Emphasis Duration Control This signal controls the duration for which the HS pre-emphasis current is sourced onto DP0 or DM0. The HS Transmitter pre-emphasis duration is defined in terms of unit amounts. One unit of pre-emphasis duration is approximately 580 ps and is defined as 1X pre-emphasis duration. This signal is valid only if either TXPREEMPAMPTUNE0[1] or TXPREEMPAMPTUNE0[0] is set to 1'b1. 1: 1x, short pre-emphasis current duration 0 (design default): 2x, long pre-emphasis current duration If TXPREEMPPULSETUNE0 is not used, set it to the design default. This signal is a strapping option that must be set prior to a power-on reset and remain static during normal operation. Strapping options are not critical for STA, and any other timings or loading limits for the pin are specified in the .lib timing model included in the product deliverables.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0018			Register Name: U2P0_PHYTUNE
Bit	Read/Write	Default/Hex	Description
18:16	R/W	0x3	OTGTUNE[2:0] VBUS Valid Threshold Adjustment This bus adjusts the voltage level for the VBUS Valid threshold. 111: +12.42% 110: +9.29% 101: +6.09% 100: +3.16% 011: 0, Design default 010: -3.16% 001: -6.32% 000: -9.48% If this bus is not used, leave it at the defaultsetting.
15:12	R/W	0x3	TXFSLSTUNE[3:0] FS/LS Source Impedance Adjustment This bus adjusts the low- and full-speed single-ended source impedance while driving high. The following adjustment valuesare based on nominal process, voltage, andtemperature. 1111: -11.18% 0111: -5.96% 0011: 0, Design default 0001: +5.78% 0000: +12.49% All other bit settings are reserved. This bus is a strapping option that must be set prior to a power-on reset and remain static during normal operation. Strapping options are not critical for STA, and any other timings or loading limits for the pinare specified in the .lib timing model included in the productdeliverables.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0018			Register Name: U2P0_PHYTUNE
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0x3	TXVREFTUNE[3:0] HS DC Voltage Level Adjustment This bus adjusts the high-speed DC level voltage. 1111: +24% 1110: +22% 1101: +20% 1100: +18% 1011: +16% 1010: +14% 1001: +12% 1000: +10% 0111: +8% 0110: +6% 0101: +4% 0100: +2% 0011: 0, Design default 0010: -2% 0001: -4% 0000: -6% When the PHY is in a HOST role where the HOSTDISCONNECT0 signal is used, any adjustment of the HS transmits voltage level tune bits (TXVREFTUNE0[3:0]) might also necessitate a change to the HS disconnect detection threshold tune bits (COMPDISTUNE0[2:0]). This change might be required because the HS disconnect detection threshold might need to be increased (or decreased) if the HS transmit voltage level is increased (or decreased). This bus is a strapping option that must be set prior to a power-on reset and remain static during normal operation. Strapping options are not critical for STA, and any other timings or loading limits for the pin are specified in the .lib timing model included in the product deliverables.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0018			Register Name: U2P0_PHYTUNE
Bit	Read/Write	Default/Hex	Description
7:6	R/W	0x3	TXHSXVTUNE[1:0] Transmitter High-Speed Crossover Adjustment This bus adjusts the voltage at which the DP0 and DM0 signals cross while transmitting in HS mode. 11: 0, Default setting 10: +15 mV 01: -15 mV 00: Reserved This bus is a strapping option that must be set prior to a power-on reset and remain static during normal operation. Strapping options are not critical for STA, and any other timings or loading limits for the pin are specified in the .lib timing model included in the product deliverables.
5:4	R/W	0x1	TXRISETUNE[1:0] HS Transmitter Rise/Fall Time Adjustment This bus adjusts the rise/fall times of the high-speed waveform. 11: -8.1% 10: -7.2% 01: 0, Design default 00: +5.4% If this bus is not used, leave it at the default setting. This bus is a strapping option that must be set prior to a power-on reset and remain static during normal operation. Strapping options are not critical for STA, and any other timings or loading limits for the pin are specified in the .lib timing model included in the product deliverables.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0018			Register Name: U2P0_PHYTUNE
Bit	Read/Write	Default/Hex	Description
3:2	R/W	0x1	TXRESTUNE[1:0] USB Source Impedance Adjustment In some applications, there can be significant series resistance on the D+ and D- paths between the transceiver and cable. This bus adjusts the driver source impedance to compensate for added series resistance on the USB. Note: Any setting other than the default can result in source impedance variation across process, voltage, and temperature conditions that does not meet USB 2.0 specification limits. 11: Source impedance is decreased by approximately 5.63 ohm 10: Source impedance is decreased by approximately 2.62 ohm 01: 0, Design default 00: Source impedance is increased by approximately 2.54 ohm If this bus is not used, leave it at the default setting.
1:0	R/W	0x0	TXPREEMPAMPTUNE[1:0] HS Transmitter Pre-Emphasis Duration Control This signal controls the duration for which the HS pre-emphasis current is sourced onto DP0 or DM0. The HS Transmitter pre-emphasis duration is defined in terms of unit amounts. One unit of pre-emphasis duration is approximately 580 ps and is defined as 1X pre-emphasis duration. This signal is valid only if either TXPREEMPAMPTUNE0[1] or TXPREEMPAMPTUNE0[0] is set to 1'b1. 1: 1x, short pre-emphasis current duration 0 (design default): 2x, long pre-emphasis current duration If TXPREEMPPULSETUNE0 is not used, set it to the design default. This signal is a strapping option that must be set prior to a power-on reset and remain static during normal operation. Strapping options are not critical for STA, and any other timings or loading limits for the pin are specified in the .lib timing model included in the product deliverables.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.4.5.5 0x0024 USB2.0 PHY Status Register (Default Value: 0x0000_0004)

Offset: 0x0024			Register Name: U2P0_PHYSTS
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R	0x4	TESTDATAOUT[3:0]

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.5 USB2.0 DRD

18.5.1 Overview

The USB2.0 dual-role device (USB2.0 DRD) supports both device and host functions which can also be configured as a Host-only or Device-only controller.

The USB2.0 DRD has the following features:

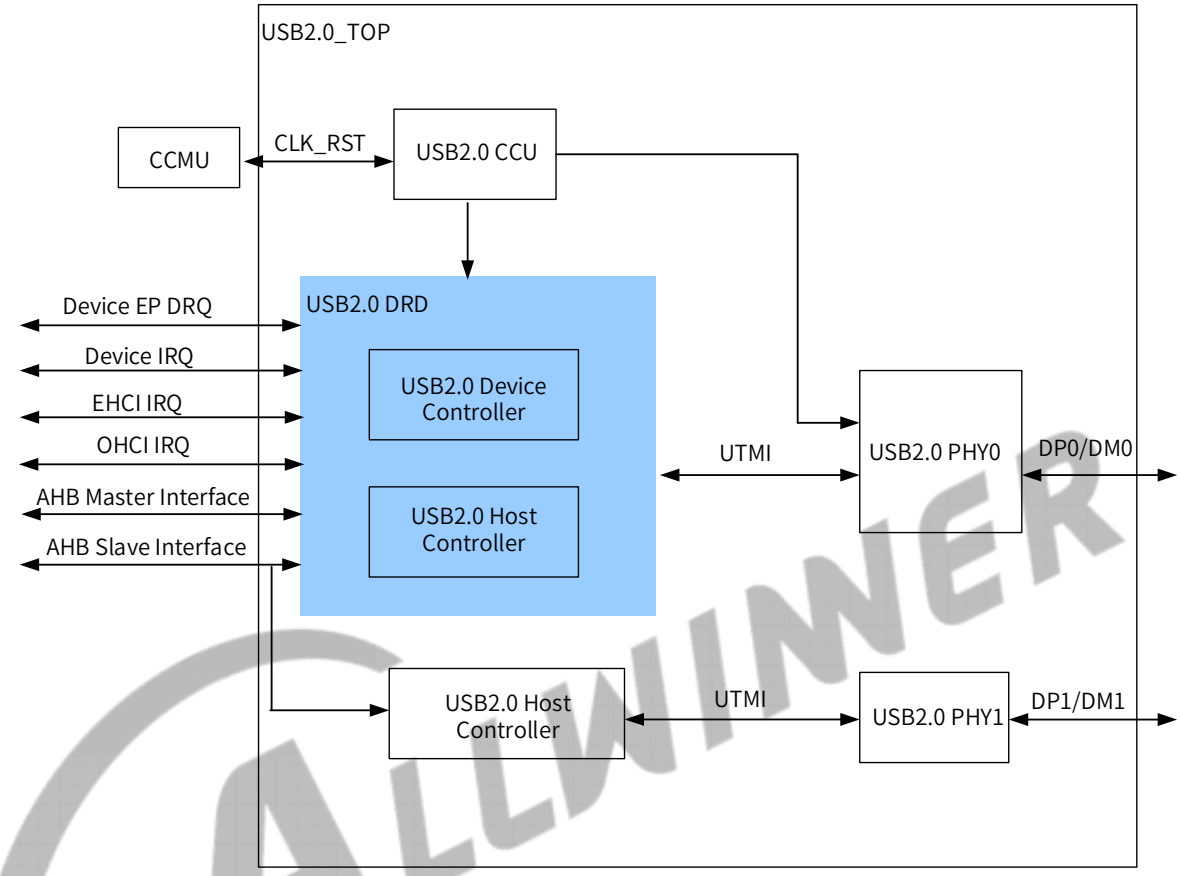
- Compatible with USB2.0 Specification
- Supports USB2.0 Host Function
  - Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0
  - Compatible with Open Host Controller Interface (OHCI) Specification, Version 1.0a
  - Supports High-Speed (HS, 480 Mbps)
  - Supports Full-Speed (FS, 12 Mbps)
  - Supports Low-Speed (LS, 1.5 Mbps)
  - Supports only 1 USB Root Port shared between EHCI and OHCI
- Supports USB2.0 Device Function
  - Supports High-Speed (HS, 480 Mbps)
  - Supports Full-Speed (FS, 12 Mbps)
  - Supports bi-directional Endpoint0 for Control transfer
  - Supports 9 Endpoints IN (including control endpoint 0), 9 Endpoints OUT (including control endpoint 0)
  - Supports up to (8KB+64Bytes) FIFO for EPs (Including EP0)
  - Supports interface to an external Normal DMA controller for every EPs (Endpoint1, Endpoint2, Endpoint3, Endpoint4, Endpoint5, Endpoint6, Endpoint7, Endpoint8)
- Supports an internal DMA Controller for data transfer with memory
- Supports High-bandwidth Isochronous & Interrupt transfers
- Supports Automated splitting/combining of packets for Bulk transfers
- Supports point-to-point and point-to-multipoint transfer in both Host and Peripheral mode
- Supports Automatic ping capabilities
- Supports Soft connect/disconnect function
- Supports all transaction scheduling in hardware
- Power Optimization and Power Management capabilities
- Device and Host controller share an 8K sram and a physical PHY

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.5.2 Block Diagram

The following figure shows the block diagram of USB2.0 DRD Controller.

Figure 18-9 USB2.0 DRD Controller Block Diagram



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.6 USB2.0 HOST

18.6.1 Overview

The USB2.0 Host Controller is fully compliant with USB 2.0 Specification, Enhanced Host Controller Interface (EHCI) Specification Revision 1.0 and Open Host Controller Interface (OHCI) Specification Release 1.0a. The controller supports high-speed, 480-Mbps transfers (40 times faster than USB 1.1 full-speed mode) using an EHCI Host Controller, as well as full and low speeds through one or more integrated OHCI Host Controllers.

The USB2.0 host controller includes the following features:

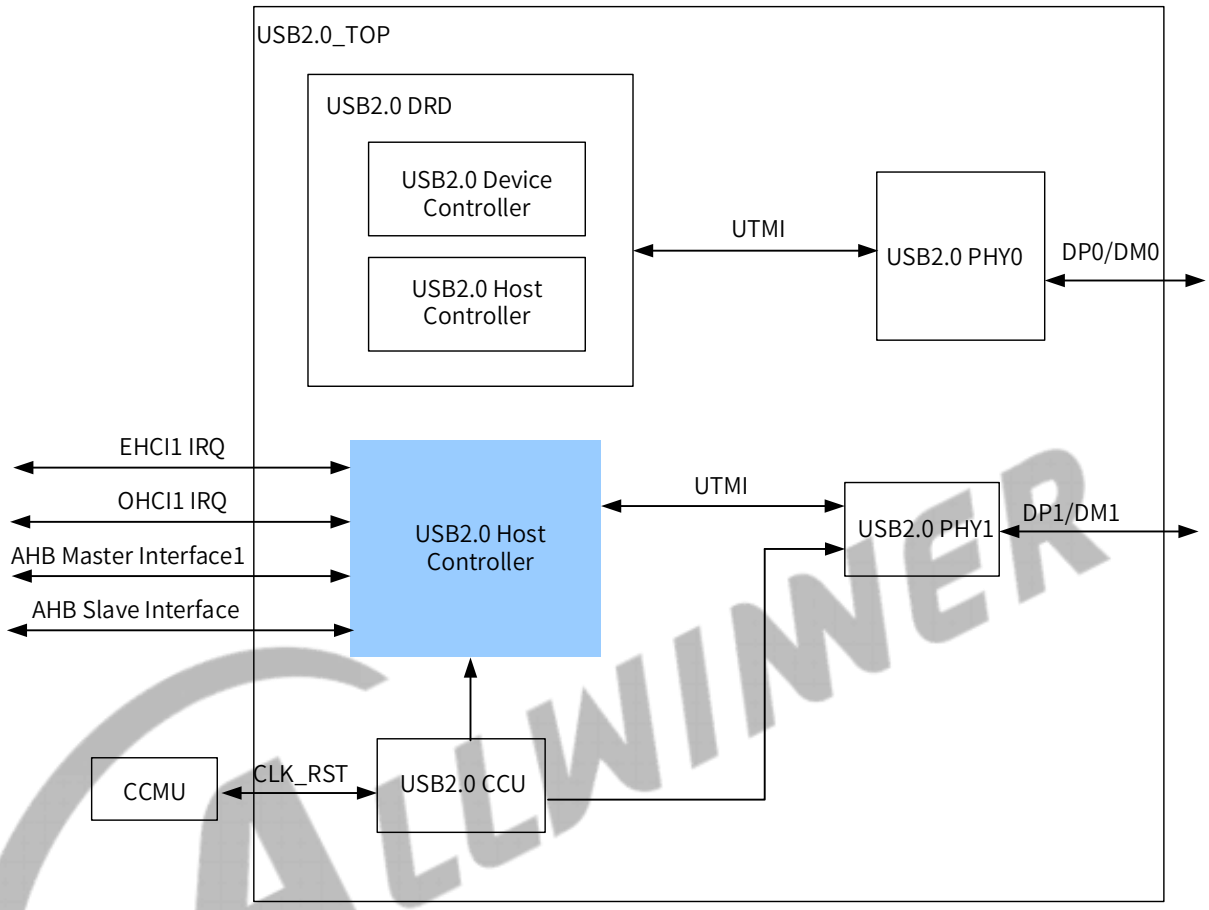
- Supports industry-standard AMBA High-Performance Bus (AHB) and it is fully compliant with the AMBA Specification, Revision 2.0.
- Supports 32-bit Little Endian AMBA AHB Slave Bus for Register Access.
- Supports 35-bit Little Endian AMBA AHB Master Bus for Memory Access.
- Includes an internal DMA controller for data transfer with memory.
- Complies with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.
- Supports High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) Device.
- Supports the UTMI+ Level 3 interface. The 8-bit bidirectional data buses are used.
- Supports only 1 USB Root Port shared between EHCI and OHCI.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.6.2 Block Diagram

The following figure shows the block diagram of USB2.0 Host Controller.

Figure 18-10 USB2.0 Host Controller Block Diagram



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.7 PWM

18.7.1 Overview

The Pulse Width Modulation (PWM) module can the configurable PWM waveform output and the input waveform capture.

The PWM has the following features:

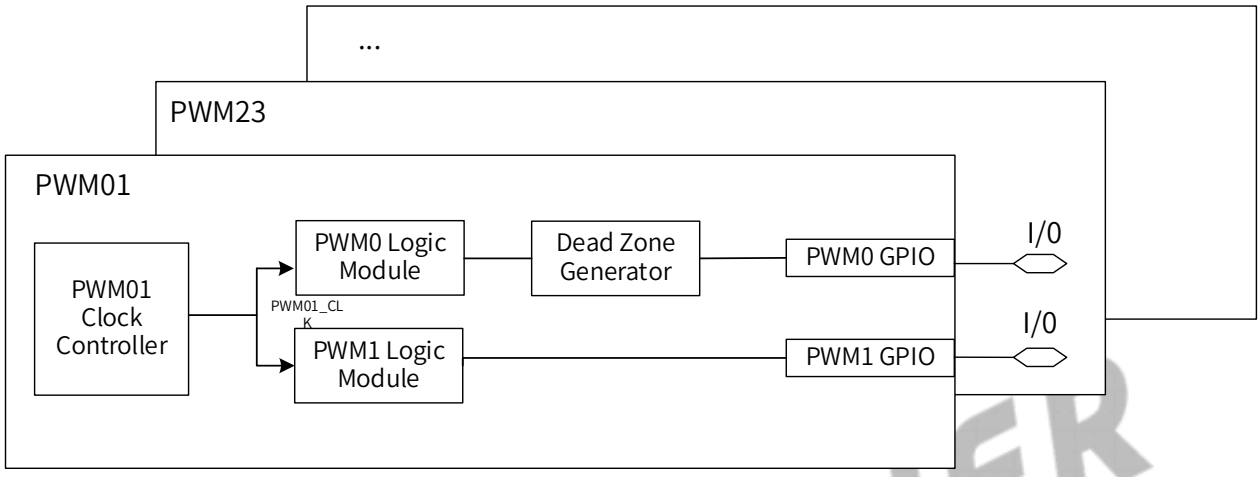
- Up to 30 PWM channels and 3 PWM controllers:
  - PWM0_[9:0] for PWM0 controller
  - PWM1_[9:0] for PWM1 controller
  - S_PWM0_[9:0] for S_PWM0 controller
- Maximum 10 independent PWM channels for each PWM controller
  - Supports PWM output in cycle mode
  - Supports PWM output in pulse mode, and the pulse number is configurable
  - Output frequency range:
    - 0 to 24 MHz if the clock source is SYS_CLK24M
    - 0 to 100 MHz if the clock source is APB0 clock
  - Various duty-cycle: 0% to 100%
  - Minimum resolution: 1/65536
- Maximum 5 complementary pairs output
  - PWM01 pair (PWM0 + PWM1), PWM23 pair (PWM2 + PWM3), PWM45 pair (PWM4 + PWM5), PWM67 pair (PWM6 + PWM7), PWM89 pair (PWM8 + PWM9)
  - Supports dead-zone generator, and the dead-time is configurable
- Maximum 4 groups of PWM channel output for controlling stepper motors
  - Supports any plural channels to form a group, and output the same duty-cycle pulse
  - In the group mode, the relative phase of the output waveform for each channel is configurable
- Maximum 10 channels of input capture
  - Supports detection at the rising and falling edges
  - Supports pulse-width measurement
- Supports 10 channels of input waveform counting

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.7.2 Block Diagram

The PWM includes multi PWM channels. Each channel can generate different PWM waveform by the independent counter and duty-cycle configuration register. Each PWM pair shares one group of clock and dead-zone generator to generate PWM waveform.

Figure 18-11 PWM Block Diagram



18.7.3 Clock Sources

The following table describes the clock sources of PWM. For clock setting, configurations, and gating information, refer to the section Clock Controller Unit (CCU).

Module	Clock Sources	Description
PWM0/1	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.
	APB	PWM clock source. Refer to CCU for details on APB.
S_PWM	DCXO	The external high-frequency crystal oscillator. Its frequency is 26 MHz.
	RTC_32K	Its frequency is 32.768 KHz by default.
	RC16M	The on-chip oscillator. Its frequency is 16MHz by default.
	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.

18.7.4 External Signals

The following table describes the external signals of the PWM.

Table 18-6 PWM External Signals

Signal	Description	Type
PWM0-[9:0]	Pulse Width Modulation Output Channel [9:0]	I/O
PWM1-[9:0]	Pulse Width Modulation Output Channel [9:0]	I/O

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Signal	Description	Type
S-PWM0-[9:0]	Pulse Width Modulation Output Channel [9:0]	I/O

18.7.5 Functional Description

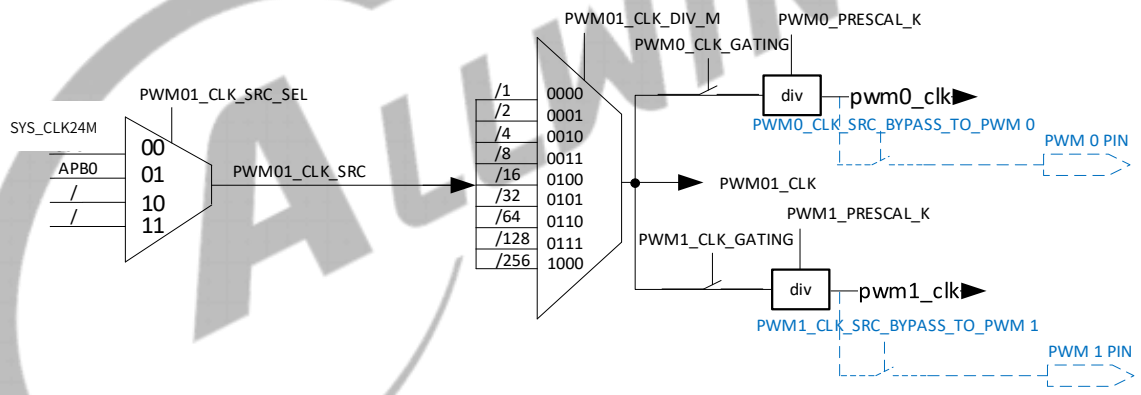
18.7.5.1 PWM Clock Controller

The clock controller of each PWM pair, for instance PWM01, includes clock source select (PWM01_CLK_SRC), 1-256 scaler (PWM01_CLK_DIV_M). Each PWM channel has the secondary frequency division (PWM_PRESCAL_K), clock source bypass (PWMx_CLK_BYPASS) and clock switch (PWMx_CLK_GATING).

The clock sources of PWM include SYS_CLK24M and APB0. The OSC comes from the external high-frequency oscillator or 24MHz internal PLL; the APB0 is usually the 100MHz APB0 bus clock.

The clock sources of S_PWM include DCXO, RTC_32K, RC16M, and SYS_CLK24M. For details, see the section PRCM. The clock bypass is to select the clock for PWM output. The following figure shows the PWM01 Clock Source Bypass.

Figure 18-12 PWM01 Clock Source Bypass

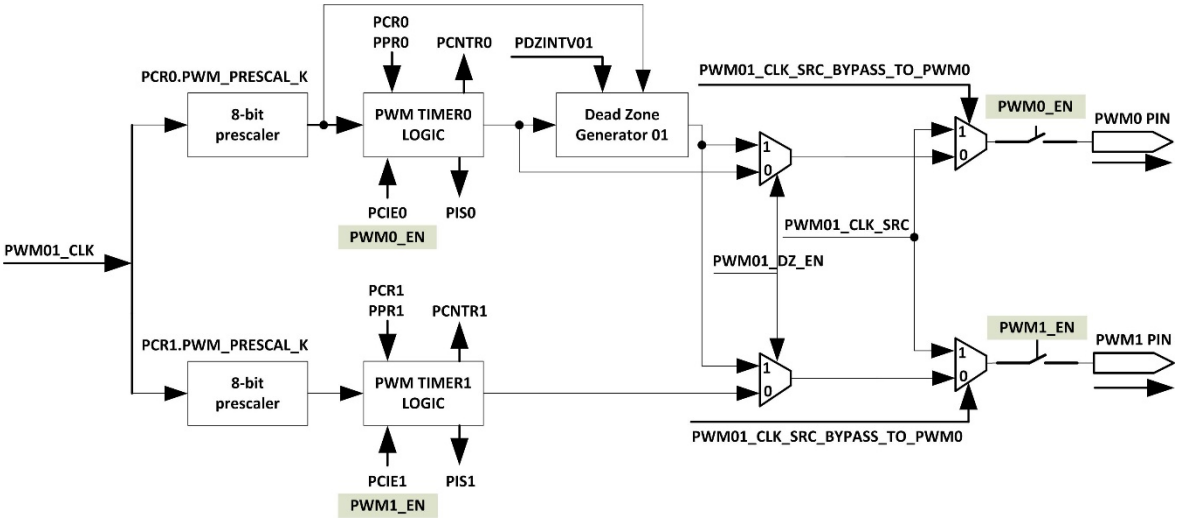


18.7.5.2 PWM Output

Take PWM01 as an example. Figure 18-13 indicates the PWM01 output logic diagram. The logic diagrams of other PWM pairs are the same as that of PWM01.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 18-13 PWM01 Output Logic Module Diagram



The timer logic module of PWM consists of one 16-bit up-counter (PCNTR) and three 16-bit parameters (PWM_ENTIRE_CYCLE, PWM_ACT_CYCLE, PWM_COUNTER_START). The PWM_ENTIRE_CYCLE is used to control the PWM cycle, the PWM_ACT_CYCLE is used to control the duty cycle, the PWM_COUNTER_START is used to control the output phase (multi-channel synchronization work requirements).

The PWM_ENTIRE_CYCLE and the PWM_ACT_CYCLE support the cache load. After PWM output is enabled, the register values of the PWM_ENTIRE_CYCLE and the PWM_ACT_CYCLE can be changed anytime, and the changed value caches into the cache register. When the PCNTR counter outputs a period of PWM waveform, the value of the cache register can be updated for the PCNTR control. The purpose of the cache load is to avoid the unstable PWM output waveform with glitches when updating the values of the PWM_ENTIRE_CYCLE and PWM_ACT_CYCLE. The PWM_CNTSTART doesn t support cache load, and only can be configured before enabling PWM output.

The PWM supports waveform output in cycle mode and pulse mode.

Cycle mode: The PWM outputs the set PWM waveform continually; that is, the output waveform is a continuous PWM square wave.

Pulse mode: After setting the PWM_PUL_NUM parameter, the PWM outputs (PWM_PULNUM+1) periods of PWM waveform; that is, the waveform with several pulses are output.

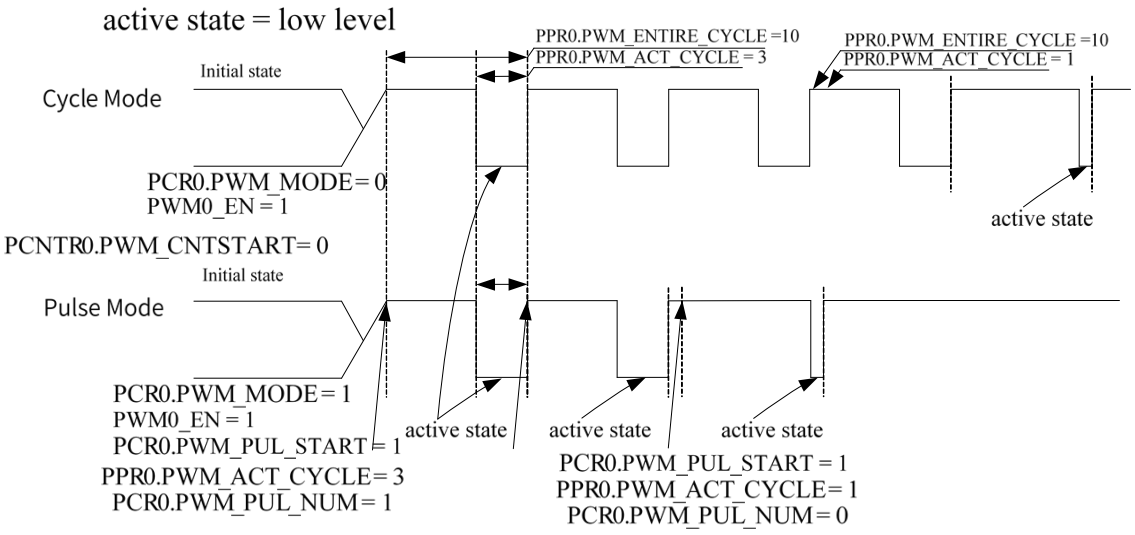
Note: As the data width of PWM_PUL_CNT is 16 bits, it output maximum 65536 PWM waveforms.

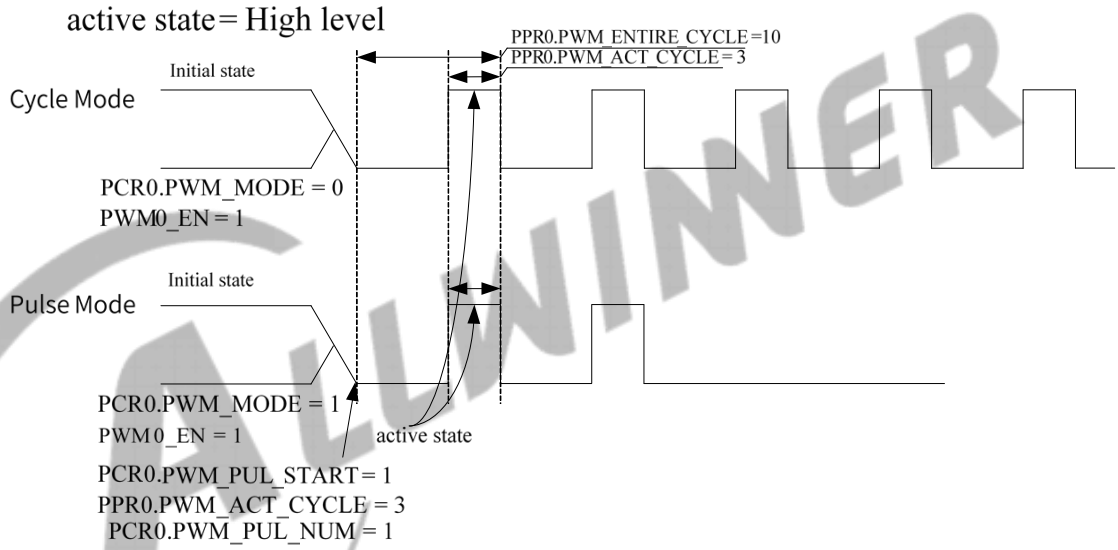
NOTE

As the data width of PWM_PUL_CNT is 16 bits, it output maximum 65536 PWM waveforms.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

The following figure shows active state in cycle mode and pulse mode.



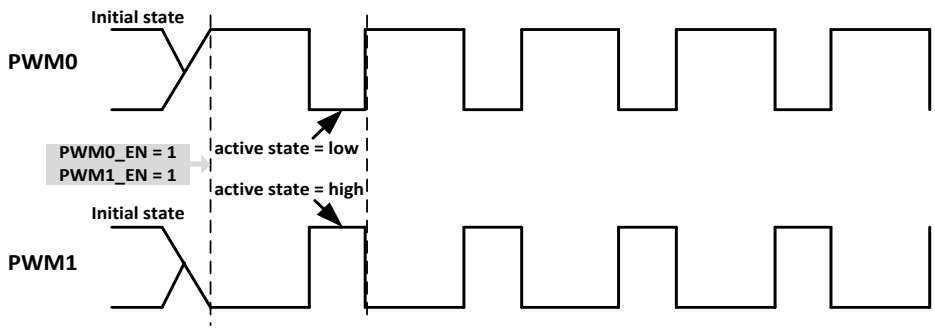


Every PWM pair supports two kinds of waveform output, including complementary pair Waveform output and PWM pair output with dead-time.

Complementary Pair Waveform Output

The following figure shows the complementary pair waveform output of PWM01.

Figure 18-14 PWM01 Complementary Pair Output



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

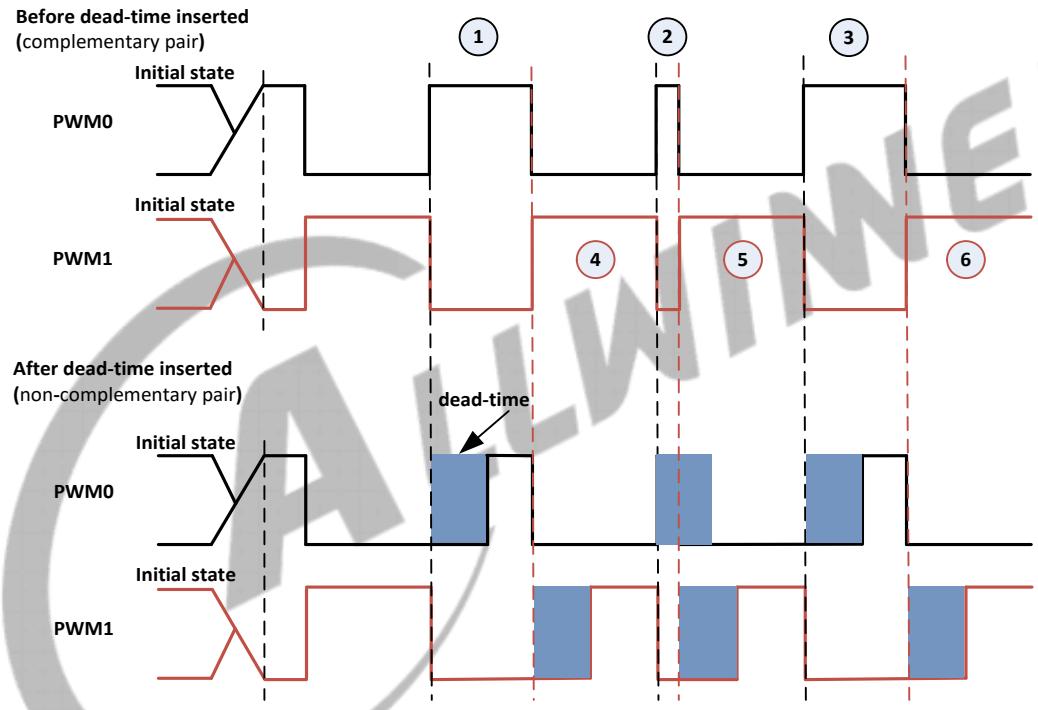
The complementary pair output needs to satisfy the following conditions:

- PWM0 and PWM1 share the same clock divider, frequency, duty-cycle, and phase
- PWM0 and PWM1 have an opposite active state
- Enable the clock gating of PWM0 and PWM1 at the same time
- Enable the waveform output of PWM0 and PWM1 at the same time

Waveform Output with Dead-time Insertion

Every PWM pair has a programmable dead-time generator. When the dead-time function of the PWM pair is enabled, the PWM01 waveform output is decided by PWM timer logic and DeadZone Generator. The following figure shows the waveform output with dead-time insertion.

Figure 18-15 Output Waveform with Dead-time Insertion



The principle of inserting dead-time is to insert dead-time at every rising edge. If the high level period in mark ⊣ is less than dead-time, then dead-time will override the high level period. Therefore, the setting of dead-time needs to consider the period and the duty-cycle of the output waveform. The dead-time formula is defined as follows:

Dead time = $(PWM01_CLK / PWM0_PRESCALE_K)^{-1} * PDZINTV01$

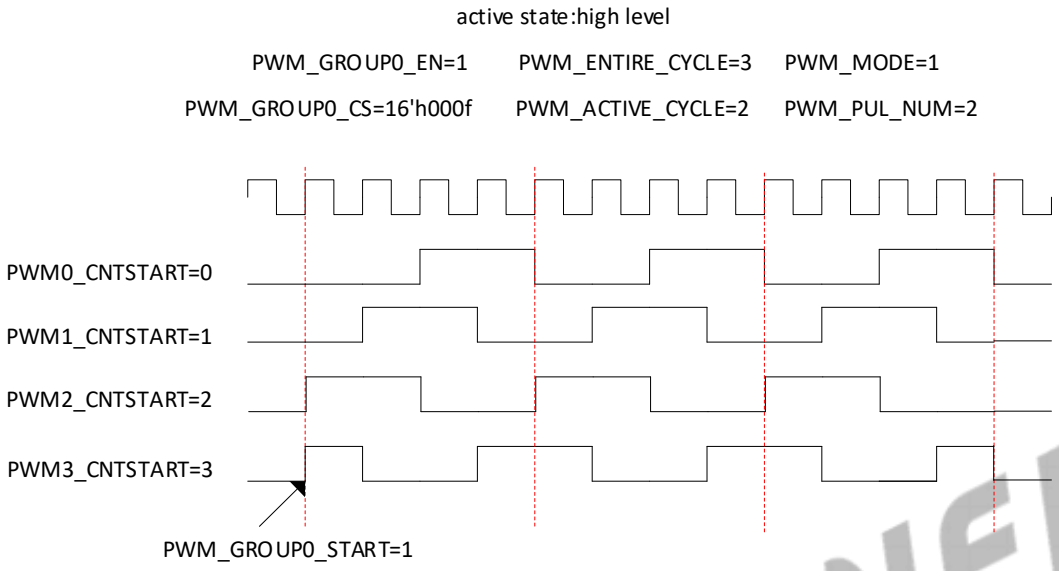
18.7.5.3 PWM Group Mode

The PWM group mode is used to satisfy the PWM group signals of stepper motors in different phases. Take PWM Group0 as an example. The PGR0.CS selects the PWM channel working in the same group; the same parameters of PWM_ENTIRE_CYCLE, PWM_ACT_CYCLE are set through the same clock configuration; the different PWM_COUNTER_START can output PWM group signals with the same duty-cycle and the different phase. PCNTR counting starts from 0 by default, and

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

the phase of output waveform can be controlled through PWM_CNTSTART configuration. If the stepper motor uses the PWM group mode, it is recommended to divide 0, 1, 2, 3 into a group, and 4, 5, 6, 7 another group.

Figure 18-16 Group 0-3 PWM Signal Output

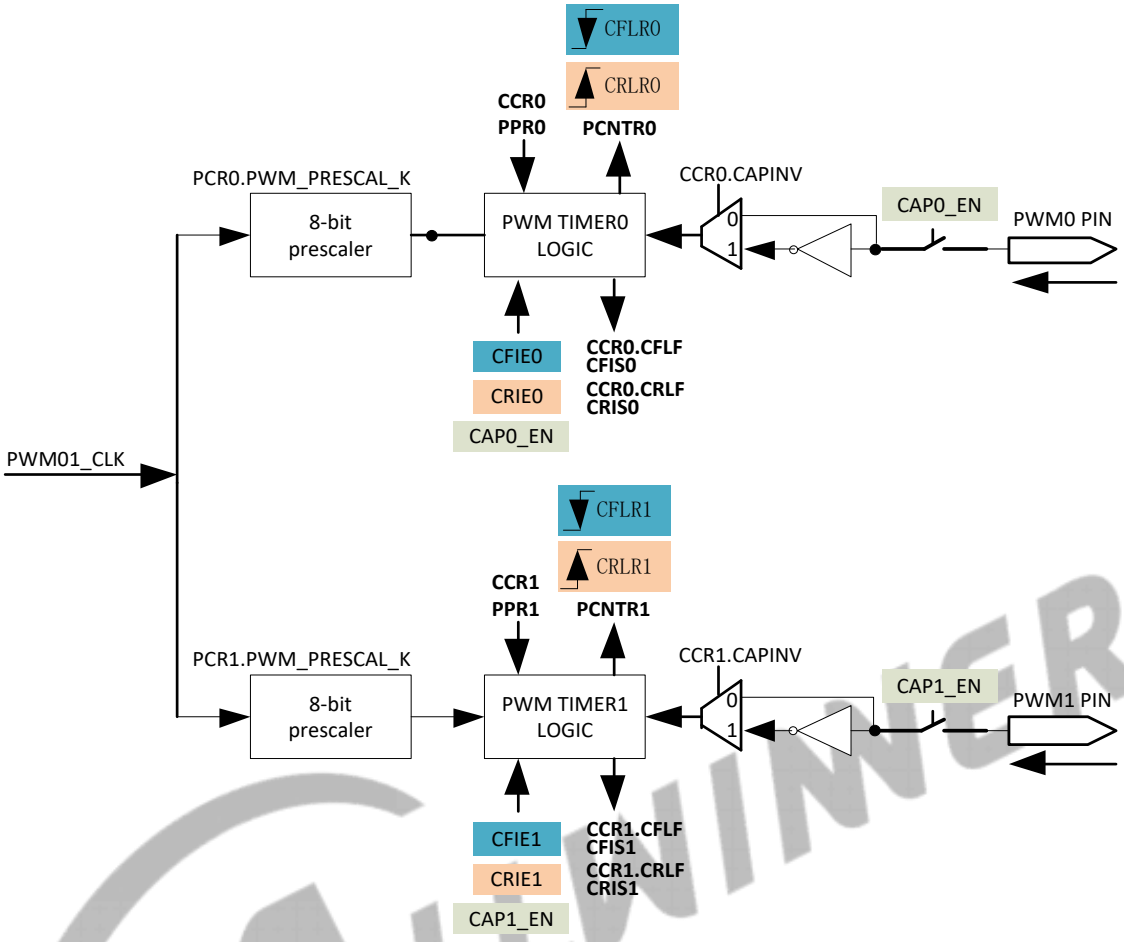


18.7.5.4 Waveform Capture

Each PWM pair is also used for capturing external clock. The following figure shows the PWM01 capture logic module diagram.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 18-17 PWM01 Capture Logic Module Diagram



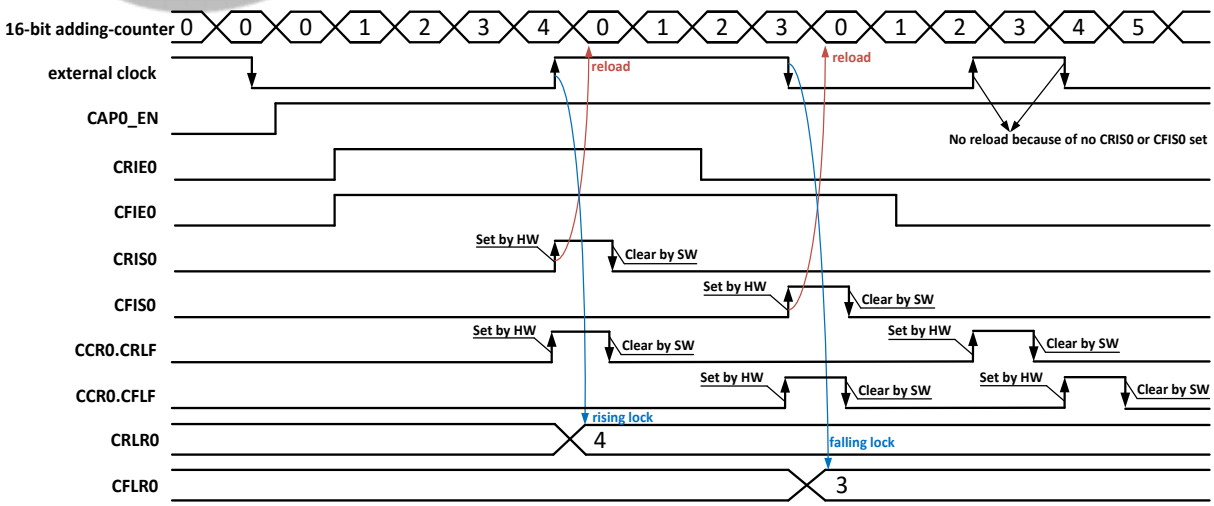
Take the PWM0 channel as an example. The PWM0 channel has one CFLR 0 and one CRLR 0 for capturing the values of up-counters on the falling edge and rising edge. You can calculate the period of the external clock by CFLR 0 and CRLR 0.

Thigh-level = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * CRLR0

Tlow-level = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * CFLR0

Tperiod = Thigh-level + Tlow-level

Figure 18-18 PWM0 Channel Capture Timing



When the capture input function of the PWM0 channel is enabled, the PCNTR of the PWM0 channel starts to work.

When the timer logic module of PWM0 captures a rising edge, the current value of PCNTR is locked to CRLR0, and CCR0[CRLF] is set to 1. If CRIE0 is 1, and CRIS0 is set to 1, the PWM0 channel will send interrupt requests, and the up-counter will be reloaded to 0 and continue to count. If CRIE0 is 0, CRIS0 will not be set to 1 when the timer logic module of PWM0 captures a rising edge; thus, the up-counter will not reloaded to 0.

When the timer logic module of PWM0 captures a falling edge, the current value of PCNTR is locked to CFLR0, and CCR0[CFLF] is set to 1. If CFIE0 is 1, and CFIS0 is set to 1, the PWM0 channel will send interrupt requests, and the up-counter will be reloaded to 0 and continue to count. If CFIE0 is 0, CFIS0 will not be set to 1 when the timer logic module of PWM0 captures a falling edge; thus, the up-counter will not reloaded to 0.

18.7.6 Programming Guidelines

18.7.6.1 Clock Configuration

Step 1 When using PWM, write 1 to PWMx_CLK_GATING in the PCGR; otherwise. Otherwise, write 0 to mask.

Step 2 Set PWMn_CLK_SRC in the PCCRn to select SYS_CLK24M or APB0 clock.

Step 3 Set PWM01_CLK_DIV_M in the PCCRn to select different frequency division coefficient (1/2/4/8/16/32/64/128/256).

Step 4 Set PWM_CLK_SRC_BYPASS_TO_PWM in the PCGR to 1, output the PWM clock after the secondary frequency division to the corresponding PWM output pin.

Step 5 Set PWM_PRESCAL_K in the PCR to select any frequency division coefficient from 1 to 256.

NOTE

The channels in the complementary output and group mode needs the same clock configuration, simultaneously opened clock gating, PWM parameter configuration, and enabled PWM output at the same time to ensure the synchronization among channels. Besides, as a PWM pair shares the same first-level clock division and gating, their two channels cannot be allocated to different groups in the group mode. If the allocation still exists, the same first-level clock division and the simultaneously opened gating is required. The total module needs to be reset when the group mode regroups.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.7.6.2 PWM Configuration

Step 1 To configure PWM mode, set PWM_MODE to select cycle mode or pulse mode; if pulse mode is to be selected, set PWM_PUL_NUM in the PCR.

Step 2 To configure PWM active level, set PWM_ACT_STA to select a low level or high level in the PCR.

Step 3 To configure PWM duty-cycle, set PWM_ENTIRE_CYCLE and PWM_ACT_CYCLE after clock gating is opened in PPR.

Step 4 To configure PWM starting phase, set PWM_COUNTER_START in the PCNTR before the PWM is enabled. You can verify whether the configuration is successful by reading back PWM_COUNTER_STATUS in the PCNTR.

Step 5 To enable PWM, select the corresponding PWM enable bit in the PER; pulse mode is to be selected, set PWM_PUL_NUM in the PCR.

18.7.6.3 Deadzone Configuration

Step 1 Set PDZINTVn to 1 to configure deadzone interval value in the PDZCRn.

Step 2 Set PWMn_DZ_CN to 1 to enable PWM01 deadzone in the PDZCRn.

18.7.6.4 Capture Input Configuration

Step 1 Set CAPn_EN to 1 to enable the capture functions of corresponding channels in the CER. In addition, set CFIEn or CRIEn to 1 in the CIER to generate the capture channel pending.

Step 2 To configure the capture method, confirm whether to capture in the rising edge or falling edge through CRLF and CFLF in the CCR. Confirm whether to invert the input signal through CAPINV in the CCR.

18.7.6.5 Number of Captured Input Signals

Enable Input Counting and Input Capture Simultaneously

To enable input counting and input capture simultaneously, follow the steps as below.

Step 1 To configure the capture method, confirm whether to capture in the rising edge or falling edge through CRLF and CFLF in the CCR. Confirm whether to invert the input signal through CAPINV in the CCR.

Step 2 Set the CCSR to 1 in the CCR.

Step 3 Confirm whether to count in the falling edge or rising edge through CCCRFR in the CCCR.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 4 Confirm whether to stop or restart counting when reaching the count value through CCCSRR in the CCCR.

Step 5 Set the number of CCCNR and enable the corresponding channels of CCCIER. When the input signal reach the set value of CCCNR, an interrupt will be generated.

Step 6 Set CFIEn or CRIEn to 1 in the CIER to generate the capture channel pending.

Step 7 Set CAPn_EN to 1 in the CER to enable corresponding capture functions.

Enable Input Counting Separately

To enable input counting separately, follow the steps as below.

Step 1 Confirm whether to invert the input signal through CAPINV in CCR.

Step 2 Set CCSR to 0 in CCR.

Step 3 Confirm whether to count in the falling edge or rising edge through CCCRFR in the CCCR.

Step 4 Confirm whether to stop or restart counting when reaching the count value through CCCSRR in the CCCR.

Step 5 Set the number of CCCNR and enable the corresponding channels of CCCIER. When the input signal reach the set value of CCCNR, an interrupt will be generated.

Step 6 Set CAP_CNTn_EN to 1 to enable the counting of corresponding channels of CCCER.

18.7.7 Register List

Module Name	Base Address	Comments
PWM0	0x02527000	
PMW1	0x02528000	PMW1 register is the same with PWM0.
S_PWM	0x07023000	S_PWM register is the same with PWM0.

Register Name	Offset	Description
PIER	0x0000	PWM IRQ Enable Register
PISR	0x0004	PWM IRQ Status Register
CIER	0x0010	Capture IRQ Enable Register
CISR	0x0014	Capture IRQ Status Register
CCCIER	0x0018	Capture Cycle Counter IRQ Enable Register
CCCISR	0x001C	Capture Cycle Counter IRQ Status Register
PCCR01	0x0020	PWM01 Clock Configuration Register
PCCR23	0x0024	PWM23 Clock Configuration Register
PCCR45	0x0028	PWM45 Clock Configuration Register
PCCR67	0x002c	PWM67 Clock Configuration Register
PCCR89	0x0030	PWM89 Clock Configuration Register
PCGR	0x0040	PWM Clock Gating Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
PDZCR01	0x0060	PWM01 Dead Zone Control Register
PDZCR23	0x0064	PWM23 Dead Zone Control Register
PDZCR45	0x0068	PWM45 Dead Zone Control Register
PDZCR67	0x006c	PWM67 Dead Zone Control Register
PDZCR89	0x0070	PWM89 Dead Zone Control Register
PER	0x0080	PWM Enable Register
PGR0	0x0090	PWM Group0 Register
PGR1	0x0094	PWM Group1 Register
PGR2	0x0098	PWM Group2 Register
PGR3	0x009c	PWM Group3 Register
CCCER	0x00a0	Capture Cycle Counter Enable Register
CER	0x00c0	Capture Enable Register
PCR	0x0100+0x0000+N*0x0040 (N= 0~9)	PWM Control Register
PPR	0x0100+0x0004+N*0x0040 (N= 0~9)	PWM Period Register
PCNTR	0x0100+0x0008+N*0x0040 (N= 0~9)	PWM Counter Register
PPCNTR	0x0100+0x000C+N*0x0040 (N= 0~9)	PWM Pulse Counter Register
CCR	0x0100+0x0010+N*0x0040 (N= 0~9	Capture Control Register
CRLR	0x0100+0x0014+N*0x0040 (N= 0~9)	Capture Rise Lock Register
CFLR	0x0100+0x0018+N*0x0040 (N= 0~9)	Capture Fall Lock Register
CCCSR	0x0100+0x001C+N*0x0040 (N= 0~9)	Capture Cycle Counter Status Register
CCCNR	0x0100+0x0020+N*0x0040 (N= 0~9)	Capture Cycle Counter Number Register
CCCR	0x0100+0x0024+N*0x0040 (N= 0~9)	Capture Cycle Counter Register

18.7.8 Register Description

18.7.8.1 0x0000 PWM IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: PIER
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: PIER
Bit	Read/Write	Default/Hex	Description
19	R/W	0x0	PGIE3 PWM group 3 Interrupt Enable 0: Disable 1: Enable
18	R/W	0x0	PGIE2 PWM group 2 Interrupt Enable 0: Disable 1: Enable
17	R/W	0x0	PGIE1 PWM group 1 Interrupt Enable 0: Disable 1: Enable
16	R/W	0x0	PGIE0 PWM group 0 Interrupt Enable 0: Disable 1: Enable
15:10	/	/	/
9	R/W	0x0	PCIE9 PWM channel 9 Interrupt Enable 0: PWM channel 9 Interrupt Disable 1: PWM channel 9 Interrupt Enable
8	R/W	0x0	PCIE8 PWM channel 8 Interrupt Enable 0: PWM channel 8 Interrupt Disable 1: PWM channel 8 Interrupt Enable
7	R/W	0x0	PCIE7 PWM channel 7 Interrupt Enable 0: PWM channel 7 Interrupt Disable 1: PWM channel 7 Interrupt Enable
6	R/W	0x0	PCIE6 PWM channel 6 Interrupt Enable 0: PWM channel 6 Interrupt Disable 1: PWM channel 6 Interrupt Enable
5	R/W	0x0	PCIE5 PWM channel 5 Interrupt Enable 0: PWM channel 5 Interrupt Disable 1: PWM channel 5 Interrupt Enable
4	R/W	0x0	PCIE4 PWM channel 4 Interrupt Enable 0: PWM channel 4 Interrupt Disable 1: PWM channel 4 Interrupt Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: PIER
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	PCIE3 PWM channel 3 Interrupt Enable 0: PWM channel 3 Interrupt Disable 1: PWM channel 3 Interrupt Enable
2	R/W	0x0	PCIE2 PWM channel 2 Interrupt Enable 0: PWM channel 2 Interrupt Disable 1: PWM channel 2 Interrupt Enable
1	R/W	0x0	PCIE1 PWM channel 1 Interrupt Enable 0: PWM channel 1 Interrupt Disable 1: PWM channel 1 Interrupt Enable
0	R/W	0x0	PCIE0 PWM channel 0 Interrupt Enable 0: PWM channel 0 Interrupt Disable 1: PWM channel 0 Interrupt Enable

18.7.8.2 0x0004 PWM IRQ Status Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: PISR
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19	R/W1C	0x0	PGIS3 PWM group 3 Interrupt Status
18	R/W1C	0x0	PGIS2 PWM group 2 Interrupt Status
17	R/W1C	0x0	PGIS1 PWM group 1 Interrupt Status
16	R/W1C	0x0	PGIS0 PWM group 0 Interrupt Status
15:10	/	/	/
9	R/W1C	0x0	PIS9 PWM channel 9 Interrupt Status. When PWM channel 9 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 9 interrupt is not pending. 1: PWM channel 9 interrupt is pending. Writes 0: No effect. 1: Clear PWM channel 9 interrupt status.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: PISR
Bit	Read/Write	Default/Hex	Description
8	R/W1C	0x0	PIS8 PWM channel 8 Interrupt Status. When PWM channel 8 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 8 interrupt is not pending. 1: PWM channel 8 interrupt is pending. Writes 0: No effect. 1: Clear PWM channel 8 interrupt status.
7	R/W1C	0x0	PIS7 PWM channel 7 Interrupt Status. When PWM channel 7 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 7 interrupt is not pending. 1: PWM channel 7 interrupt is pending. Writes 0: No effect. 1: Clear PWM channel 7 interrupt status.
6	R/W1C	0x0	PIS6 PWM channel 6 Interrupt Status. When PWM channel 6 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 6 interrupt is not pending. 1: PWM channel 6 interrupt is pending. Writes 0: No effect. 1: Clear PWM channel 6 interrupt status.
5	R/W1C	0x0	PIS5 PWM channel 5 Interrupt Status. When PWM channel 5 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 5 interrupt is not pending. 1: PWM channel 5 interrupt is pending. Writes 0: No effect. 1: Clear PWM channel 5 interrupt status.
4	R/W1C	0x0	PIS4 PWM channel 4 Interrupt Status. When PWM channel 4 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 4 interrupt is not pending. 1: PWM channel 4 interrupt is pending. Writes 0: No effect. 1: Clear PWM channel 4 interrupt status.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: PISR
Bit	Read/Write	Default/Hex	Description
3	R/W1C	0x0	PIS3 PWM channel 3 Interrupt Status. When PWM channel 3 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 3 interrupt is not pending. 1: PWM channel 3 interrupt is pending. Writes 0: No effect. 1: Clear PWM channel 3 interrupt status.
2	R/W1C	0x0	PIS2 PWM channel 2 Interrupt Status. When PWM channel 2 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 2 interrupt is not pending. 1: PWM channel 2 interrupt is pending. Writes 0: No effect. 1: Clear PWM channel 2 interrupt status.
1	R/W1C	0x0	PIS1 PWM channel 1 Interrupt Status. When PWM channel 1 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 1 interrupt is not pending. 1: PWM channel 1 interrupt is pending. Writes 0: No effect. 1: Clear PWM channel 1 interrupt status.
0	R/W1C	0x0	PIS0 PWM channel 0 Interrupt Status. When PWM channel 0 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 0 interrupt is not pending. 1: PWM channel 0 interrupt is pending. Writes 0: No effect. 1: Clear PWM channel 0 interrupt status.

18.7.8.3 0x0010 Capture IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CIER
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0010			Register Name: CIER
Bit	Read/Write	Default/Hex	Description
19	R/W	0x0	CFIE9 If this enable bit is set 1, when capture channel 9 captures falling edge, it generates a capture channel 9 pending. 0: Capture channel 9 fall lock Interrupt disable; 1: Capture channel 9 fall lock Interrupt enable.
18	R/W	0x0	CRIE9 If this enable bit is set 1, when capture channel 9 captures rising edge, it generates a capture channel 9 pending. 0: Capture channel 9 rise lock Interrupt disable; 1: Capture channel 9 rise lock Interrupt enable.
17	R/W	0x0	CFIE8 If this enable bit is set 1, when capture channel 8 captures falling edge, it generates a capture channel 8 pending. 0: Capture channel 8 fall lock Interrupt disable; 1: Capture channel 8 fall lock Interrupt enable.
16	R/W	0x0	CRIE8 If this enable bit is set 1, when capture channel 8 captures rising edge, it generates a capture channel 8 pending. 0: Capture channel 8 rise lock Interrupt disable; 1: Capture channel 8 rise lock Interrupt enable.
15	R/W	0x0	CFIE7 If this enable bit is set 1, when capture channel 7 captures falling edge, it generates a capture channel 7 pending. 0: Capture channel 7 fall lock Interrupt disable; 1: Capture channel 7 fall lock Interrupt enable.
14	R/W	0x0	CRIE7 If this enable bit is set 1, when capture channel 7 captures rising edge, it generates a capture channel 7 pending. 0: Capture channel 7 rise lock Interrupt disable; 1: Capture channel 7 rise lock Interrupt enable.
13	R/W	0x0	CFIE6 If this enable bit is set 1, when capture channel 6 captures falling edge, it generates a capture channel 6 pending. 0: Capture channel 6 fall lock Interrupt disable; 1: Capture channel 6 fall lock Interrupt enable.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0010			Register Name: CIER
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	CRIE6 If this enable bit is set 1, when capture channel 5 captures rising edge, it generates a capture channel 5 pending. 0: Capture channel 5 rise lock Interrupt disable; 1: Capture channel 5 rise lock Interrupt enable.
11	R/W	0x0	CFIE5 If this enable bit is set 1, when capture channel 5 captures falling edge, it generates a capture channel 5 pending. 0: Capture channel 5 fall lock Interrupt disable; 1: Capture channel 5 fall lock Interrupt enable.
10	R/W	0x0	CRIE5 If this enable bit is set 1, when capture channel 5 captures rising edge, it generates a capture channel 5 pending. 0: Capture channel 5 rise lock Interrupt disable; 1: Capture channel 5 rise lock Interrupt enable.
9	R/W	0x0	CFIE4 If this enable bit is set 1, when capture channel 4 captures falling edge, it generates a capture channel 4 pending. 0: Capture channel 4 fall lock Interrupt disable; 1: Capture channel 4 fall lock Interrupt enable.
8	R/W	0x0	CRIE4 If this enable bit is set 1, when capture channel 4 captures rising edge, it generates a capture channel 4 pending. 0: Capture channel 4 rise lock Interrupt disable; 1: Capture channel 4 rise lock Interrupt enable.
7	R/W	0x0	CFIE3 If this enable bit is set 1, when capture channel 3 captures falling edge, it generates a capture channel 3 pending. 0: Capture channel 3 fall lock Interrupt disable; 1: Capture channel 3 fall lock Interrupt enable.
6	R/W	0x0	CRIE3 If this enable bit is set 1, when capture channel 3 captures rising edge, it generates a capture channel 3 pending. 0: Capture channel 3 rise lock Interrupt disable; 1: Capture channel 3 rise lock Interrupt enable.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0010			Register Name: CIER
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	CFIE2 If this enable bit is set 1, when capture channel 2 captures falling edge, it generates a capture channel 2 pending. 0: Capture channel 2 fall lock Interrupt disable; 1: Capture channel 2 fall lock Interrupt enable.
4	R/W	0x0	CRIE2 If this enable bit is set 1, when capture channel 2 captures rising edge, it generates a capture channel 2 pending. 0: Capture channel 2 rise lock Interrupt disable; 1: Capture channel 2 rise lock Interrupt enable.
3	R/W	0x0	CFIE1 If this enable bit is set 1, when capture channel 1 captures falling edge, it generates a capture channel 1 pending. 0: Capture channel 1 fall lock Interrupt disable; 1: Capture channel 1 fall lock Interrupt enable.
2	R/W	0x0	CRIE1 If this enable bit is set 1, when capture channel 1 captures rising edge, it generates a capture channel 1 pending. 0: Capture channel 1 rise lock Interrupt disable; 1: Capture channel 1 rise lock Interrupt enable.
1	R/W	0x0	CFIE0 If this enable bit is set 1, when capture channel 0 captures falling edge, it generates a capture channel 0 pending. 0: Capture channel 0 fall lock Interrupt disable; 1: Capture channel 0 fall lock Interrupt enable.
0	R/W	0x0	CRIE0 If this enable bit is set 1, when capture channel 0 captures rising edge, it generates a capture channel 0 pending. 0: Capture channel 0 rise lock Interrupt disable; 1: Capture channel 0 rise lock Interrupt enable.

18.7.8.4 0x0014 Capture IRQ Status Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19	R/W1C	0x0	CFIS9 Capture channel 9 falling lock interrupt status. When capture channel 9 captures falling edge, if capture channel 9 fall lock interrupt (CFIE9) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 9 interrupt is not pending. 1: Capture channel 9 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 9 interrupt status.
18	R/W1C	0x0	CRIS9 Capture channel 9 rising lock interrupt status. When capture channel 9 captures rising edge, if capture channel 9 rise lock interrupt (CRIE9) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 9 interrupt is not pending. 1: Capture channel 9 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 9 interrupt status.
17	R/W1C	0x0	CFIS8 Capture channel 8 falling lock interrupt status. When capture channel 8 captures falling edge, if capture channel 8 fall lock interrupt (CFIE8) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 8 interrupt is not pending. 1: Capture channel 8 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 8 interrupt status.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
16	R/W1C	0x0	CRIS8 Capture channel 8 rising lock interrupt status. When capture channel 8 captures rising edge, if capture channel 8 rise lock interrupt (CRIE8) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 8 interrupt is not pending. 1: Capture channel 8 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 8 interrupt status.
15	R/W1C	0x0	CFIS7 Capture channel 7 falling lock interrupt status. When capture channel 7 captures falling edge, if capture channel 7 fall lock interrupt (CFIE7) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 7 interrupt is not pending. 1: Capture channel 7 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 7 interrupt status.
14	R/W1C	0x0	CRIS7 Capture channel 7 rising lock interrupt status. When capture channel 7 captures rising edge, if capture channel 7 rise lock interrupt (CRIE7) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 7 interrupt is not pending. 1: Capture channel 7 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 7 interrupt status.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
13	R/W1C	0x0	CFIS6 Capture channel 6 falling lock interrupt status. When capture channel 6 captures falling edge, if capture channel 6 fall lock interrupt (CFIE6) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 6 interrupt is not pending. 1: Capture channel 6 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 6 interrupt status.
12	R/W1C	0x0	CRIS6 Capture channel 6 rising lock interrupt status. When capture channel 6 captures rising edge, if capture channel 6 rise lock interrupt (CRIE6) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 6 interrupt is not pending. 1: Capture channel 6 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 6 interrupt status.
11	R/W1C	0x0	CFIS5 Capture channel 5 falling lock interrupt status. When capture channel 5 captures falling edge, if capture channel 5 fall lock interrupt (CFIE5) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 5 interrupt is not pending. 1: Capture channel 5 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 5 interrupt status.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
10	R/W1C	0x0	CRIS5 Capture channel 5 rising lock interrupt status. When capture channel 5 captures rising edge, if capture channel 5 rise lock interrupt (CRIE5) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 5 interrupt is not pending. 1: Capture channel 5 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 5 interrupt status.
9	R/W1C	0x0	CFIS4 Capture channel 4 falling lock interrupt status. When capture channel 4 captures falling edge, if capture channel 4 fall lock interrupt (CFIE4) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 4 interrupt is not pending. 1: Capture channel 4 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 4 interrupt status.
8	R/W1C	0x0	CRIS4 Capture channel 4 rising lock interrupt status. When capture channel 4 captures rising edge, if capture channel 4 rise lock interrupt (CRIE4) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 4 interrupt is not pending. 1: Capture channel 4 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 4 interrupt status.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
7	R/W1C	0x0	CFIS3 Capture channel 3 falling lock interrupt status. When capture channel 3 captures falling edge, if capture channel 3 fall lock interrupt (CFIE3) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 3 interrupt is not pending. 1: Capture channel 3 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 3 interrupt status.
6	R/W1C	0x0	CRIS3 Capture channel 3 rising lock interrupt status. When capture channel 3 captures rising edge, if capture channel 3 rise lock interrupt (CRIE3) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 3 interrupt is not pending. 1: Capture channel 3 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 3 interrupt status.
5	R/W1C	0x0	CFIS2 Capture channel 2 falling lock interrupt status. When capture channel 2 captures falling edge, if capture channel 2 fall lock interrupt (CFIE2) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 2 interrupt is not pending. 1: Capture channel 2 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 2 interrupt status.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
4	R/W1C	0x0	CRIS2 Capture channel 2 rising lock interrupt status. When capture channel 2 captures rising edge, if capture channel 2 rise lock interrupt (CRIE2) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 2 interrupt is not pending. 1: Capture channel 2 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 2 interrupt status.
3	R/W1C	0x0	CFIS1 Capture channel 1 falling lock interrupt status. When capture channel 1 captures falling edge, if capture channel 1 fall lock interrupt (CFIE1) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 1 interrupt is not pending. 1: Capture channel 1 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 1 interrupt status.
2	R/W1C	0x0	CRIS1 Capture channel 1 rising lock interrupt status. When capture channel 1 captures rising edge, if capture channel 1 rise lock interrupt (CRIE1) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 1 interrupt is not pending. 1: Capture channel 1 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 1 interrupt status.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
1	R/W1C	0x0	CFIS0 Capture channel 0 falling lock interrupt status. When capture channel 0 captures falling edge, if capture channel 0 fall lock interrupt (CFIE0) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 0 interrupt is not pending. 1: Capture channel 0 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 0 interrupt status.
0	R/W1C	0x0	CRIS0. Capture channel 0 rising lock interrupt status. When capture channel 0 captures rising edge, if capture channel 0 rise lock interrupt (CRIE0) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 0 interrupt is not pending. 1: Capture channel 0 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 0 interrupt status.

18.7.8.5 0x0018 Capture Cycle Counter IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: CCCIER
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9	R/W	0x00	CCIE9 Capture counter channel 9 Interrupt Enable. 0: Capture counter channel 9 Interrupt disable; 1: Capture counter channel 9 Interrupt enable.
8	R/W	0x00	CCIE8 Capture counter channel 8 Interrupt Enable. 0: Capture counter channel 8 Interrupt disable; 1: Capture counter channel 8 Interrupt enable.
7	R/W	0x00	CCIE7 Capture counter channel 7 Interrupt Enable. 0: Capture counter channel 7 Interrupt disable; 1: Capture counter channel 7 Interrupt enable.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0018			Register Name: CCCIER
Bit	Read/Write	Default/Hex	Description
6	R/W	0x00	CCIE6 Capture counter channel 6 Interrupt Enable. 0: Capture counter channel 6 Interrupt disable; 1: Capture counter channel 6 Interrupt enable.
5	R/W	0x00	CCIE5 Capture counter channel 5 Interrupt Enable. 0: Capture counter channel 5 Interrupt disable; 1: Capture counter channel 5 Interrupt enable.
4	R/W	0x00	CCIE4 Capture counter channel 4 Interrupt Enable. 0: Capture counter channel 4 Interrupt disable; 1: Capture counter channel 4 Interrupt enable.
3	R/W	0x00	CCIE3 Capture counter channel 3 Interrupt Enable. 0: Capture counter channel 3 Interrupt disable; 1: Capture counter channel 3 Interrupt enable.
2	R/W	0x00	CCIE2 Capture counter channel 2 Interrupt Enable. 0: Capture counter channel 2 Interrupt disable; 1: Capture counter channel 2 Interrupt enable.
1	R/W	0x00	CCIE1 Capture counter channel 1 Interrupt Enable. 0: Capture counter channel 1 Interrupt disable; 1: Capture counter channel 1 Interrupt enable.
0	R/W	0x00	CCIE0 Capture counter channel 0 Interrupt Enable. 0: Capture counter channel 0 Interrupt disable; 1: Capture counter channel 0 Interrupt enable.

18.7.8.6 0x001C Capture Cycle Counter IRQ Status Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: CCCISR
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x001C			Register Name: CCCISR
Bit	Read/Write	Default/Hex	Description
9	R/W1C	0x0	CCIS9 If capture counter 9 is enabled(CCIE9) and channel 9 capture counter up to channel 9 setting value (CCNR), this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture counter channel 9 interrupt is not pending. 1: Capture counter channel 9 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 9 interrupt status.
8	R/W1C	0x0	CCIS8 If capture counter 8 is enabled(CCIE8) and channel 9 capture counter up to channel 8 setting value (CCNR), this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture counter channel 8 interrupt is not pending. 1: Capture counter channel 8 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 8 interrupt status.
7	R/W1C	0x0	CCIS7 If capture counter 7 is enabled(CCIE7) and channel 7 capture counter up to channel 7 setting value (CCNR), this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture counter channel 7 interrupt is not pending. 1: Capture counter channel 7 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 7 interrupt status.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x001C			Register Name: CCCISR
Bit	Read/Write	Default/Hex	Description
6	R/W1C	0x0	CCIS6 If capture counter 6 is enabled(CCIE6) and channel 6 capture counter up to channel 6 setting value (CCNR), this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture counter channel 6 interrupt is not pending. 1: Capture counter channel 6 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 6 interrupt status.
5	R/W1C	0x0	CCIS5 If capture counter 5 is enabled(CCIE5) and channel 5 capture counter up to channel 5 setting value (CCNR), this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture counter channel 5 interrupt is not pending. 1: Capture counter channel 5 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 5 interrupt status.
4	R/W1C	0x0	CCIS4 If capture counter 4 is enabled(CCIE4) and channel 4 capture counter up to channel 4 setting value (CCNR), this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture counter channel 4 interrupt is not pending. 1: Capture counter channel 4 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 4 interrupt status.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x001C			Register Name: CCCISR
Bit	Read/Write	Default/Hex	Description
3	R/W1C	0x0	CCIS3 If capture counter 3 is enabled(CCIE3) and channel 3 capture counter up to channel 3 setting value (CCNR), this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture counter channel 3 interrupt is not pending. 1: Capture counter channel 3 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 3 interrupt status.
2	R/W1C	0x0	CCIS2 If capture counter 2 is enabled(CCIE2) and channel 2 capture counter up to channel 2 setting value (CCNR), this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture counter channel 2 interrupt is not pending. 1: Capture counter channel 2 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 2 interrupt status.
1	R/W1C	0x0	CCIS1 If capture counter 1 is enabled(CCIE1) and channel 1 capture counter up to channel 1 setting value (CCNR), this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture counter channel 1 interrupt is not pending. 1: Capture counter channel 1 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 1 interrupt status.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x001C			Register Name: CCCISR
Bit	Read/Write	Default/Hex	Description
0	R/W1C	0x0	CCIS0 If capture counter 0 is enabled(CCIE0) and channel 0 capture counter up to channel 0 setting value (CCNR), this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture counter channel 0 interrupt is not pending. 1: Capture counter channel 0 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 0 interrupt status.

18.7.8.7 0x0020 PWM01 Clock Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: PCCR01
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:7	R/W	0x0	PWM01_CLK_SRC. Select PWM01 clock source. 00: SYS_CLK24M 01: APB0 Others: /
6:4	/	/	/
3:0	R/W	0x0	PWM01_CLK_DIV_M. PWM01 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

18.7.8.8 0x0024 PWM23 Clock Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: PCCR23
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0024			Register Name: PCCR23
Bit	Read/Write	Default/Hex	Description
8:7	R/W	0x0	PWM23_CLK_SRC_SEL Select PWM23 clock source. 00: SYS_CLK24M 01: APB0 Others: /
6:4	/	/	/
3:0	R/W	0x0	PWM23_CLK_DIV_M PWM23 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

18.7.8.9 0x0028 PWM45 Clock Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: PCCR45
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:7	R/W	0x00	PWM45_CLK_SRC_SEL Select PWM45 clock source. 00: SYS_CLK24M 01: APB0 Others: /
6:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0028			Register Name: PCCR45
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	PWM45_CLK_DIV_M PWM45 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

18.7.8.10 0x002c PWM67 Clock Configuration Register (Default Value: 0x0000_0000)

Offset: 0x002c			Register Name: PCCR67
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:7	R/W	0x0	PWM67_CLK_SRC_SEL Select PWM67 clock source 00: SYS_CLK24M 01: APB0 Others: /
6:4	/	/	/
3:0	R/W	0x0	PWM67_CLK_DIV_M PWM67 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

18.7.8.11 0x0030 PWM89 Clock Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: PCCR89
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0030			Register Name: PCCR89
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:7	R/W	0x00	PWM89_CLK_SRC_SEL Select PWM89 clock source. 00: SYS_CLK24M 01: APB0 Others: /
6:4	/	/	/
3:0	R/W	0x0000	PWM89_CLK_DIV_M PWM89 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

18.7.8.12 0x0040 PWM Clock Gating Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: PCGR
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25	R/W	0x0	PWM9_CLK_BYPASS Bypass clock source (after pre-scale) to PWM9 output. 0: Not bypass 1: bypass
24	R/W	0x0	PWM8_CLK_BYPASS Bypass clock source (after pre-scale) to PWM8 output. 0: Not bypass 1: bypass
23	R/W	0x0	PWM7_CLK_BYPASS Bypass clock source (after pre-scale) to PWM7 output. 0: Not bypass 1: bypass

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0040			Register Name: PCGR
Bit	Read/Write	Default/Hex	Description
22	R/W	0x0	PWM6_CLK_BYPASS Bypass clock source (after pre-scale) to PWM6 output. 0: Not bypass 1: bypass
21	R/W	0x0	PWM5_CLK_BYPASS Bypass clock source (after pre-scale) to PWM5 output. 0: Not bypass 1: bypass
20	R/W	0x0	PWM4_CLK_BYPASS Bypass clock source (after pre-scale) to PWM4 output. 0: Not bypass 1: bypass
19	R/W	0x0	PWM3_CLK_BYPASS Bypass clock source (after pre-scale) to PWM3 output. 0: Not bypass 1: bypass
18	R/W	0x0	PWM2_CLK_BYPASS Bypass clock source (after pre-scale) to PWM2 output. 0: Not bypass 1: bypass
17	R/W	0x0	PWM1_CLK_BYPASS Bypass clock source (after pre-scale) to PWM1 output. 0: Not bypass 1: bypass
16	R/W	0x0	PWM0_CLK_BYPASS Bypass clock source (after pre-scale) to PWM0 output. 0: Not bypass 1: bypass
15:10	/	/	/
9	R/W	0x0	PWM9_CLK_GATING Gating clock for PWM9 0: Mask 1: Pass

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0040			Register Name: PCGR
Bit	Read/Write	Default/Hex	Description
8	R/W	0x0	PWM8_CLK_GATING Gating clock for PWM8 0: Mask 1: Pass
7	R/W	0x0	PWM7_CLK_GATING. Gating clock for PWM7. 0: Mask 1: Pass
6	R/W	0x0	PWM6_CLK_GATING. Gating clock for PWM6. 0: Mask 1: Pass
5	R/W	0x0	PWM5_CLK_GATING. Gating clock for PWM5. 0: Mask 1: Pass
4	R/W	0x0	PWM4_CLK_GATING. Gating clock for PWM4. 0: Mask 1: Pass
3	R/W	0x0	PWM3_CLK_GATING. Gating clock for PWM3. 0: Mask 1: Pass
2	R/W	0x0	PWM2_CLK_GATING. Gating clock for PWM2. 0: Mask 1: Pass
1	R/W	0x0	PWM1_CLK_GATING. Gating clock for PWM1. 0: Mask 1: Pass
0	R/W	0x0	PWM0_CLK_GATING. Gating clock for PWM0. 0: Mask 1: Pass

18.7.8.13 0x0060 PWM01 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: PDZCR01
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0060			Register Name: PDZCR01
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x0	PDZINTV01. PWM01 Dead Zone interval value.
7:1	/	/	/
0	R/W	0x0	PWM01_DZ_EN. PWM01 Dead Zone enable. 0: Dead Zone disable 1: Dead Zone enable.

18.7.8.14 0x0064 PWM23 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: PDZCR23
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x0	PWM23_DZ_INTV. PWM23 Dead Zone interval value.
7:1	/	/	/
0	R/W	0x0	PWM23_DZ_EN. PWM23 Dead Zone enable. 0: Dead Zone disable 1: Dead Zone enable.

18.7.8.15 0x0068 PWM45 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: PDZCR45
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x0	PWM45_DZ_INTV. PWM45 Dead Zone interval value.
7:1	/	/	/
0	R/W	0x0	PWM45_DZ_EN. PWM45 Dead Zone enable. 0: Dead Zone disable 1: Dead Zone enable.

18.7.8.16 0x006c PWM67 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset: 0x006c			Register Name: PDZCR67
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x006c			Register Name: PDZCR67
Bit	Read/Write	Default/Hex	Description
15:8	R/W	0x0	PWM67_DZ_INTV. PWM67 Dead Zone interval value.
7:1	/	/	/
0	R/W	0x0	PWM67_DZ_EN. PWM67 Dead Zone enable. 0: Dead Zone disable 1: Dead Zone enable.

18.7.8.17 0x0070 PWM89 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: PDZCR89
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x0	PWM89_DZ_INTV. PWM89 Dead Zone interval value.
7:1	/	/	/
0	R/W	0x0	PWM89_DZ_EN. PWM89 Dead Zone enable. 0: Dead Zone disable 1: Dead Zone enable.

18.7.8.18 0x0080 PWM Enable Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: PER
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9	R/W	0x0	PWM9_EN. PWM Channel 9 Enable 0: PWM disable 1: PWM enable.
8	R/W	0x0	PWM8_EN. PWM Channel 8 Enable 0: PWM disable 1: PWM enable.
7	R/W	0x0	PWM7_EN. PWM Channel 7 Enable 0: PWM disable 1: PWM enable.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0080			Register Name: PER
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	PWM6_EN. PWM Channel 6 Enable 0: PWM disable 1: PWM enable.
5	R/W	0x0	PWM5_EN. PWM Channel 5 Enable 0: PWM disable 1: PWM enable.
4	R/W	0x0	PWM4_EN. PWM Channel 4 Enable 0: PWM disable 1: PWM enable.
3	R/W	0x0	PWM3_EN. PWM Channel 3 Enable 0: PWM disable 1: PWM enable.
2	R/W	0x0	PWM2_EN. PWM Channel 2 Enable 0: PWM disable 1: PWM enable.
1	R/W	0x0	PWM1_EN. PWM Channel 1 Enable 0: PWM disable 1: PWM enable.
0	R/W	0x0	PWM0_EN. PWM Channel 0 Enable 0: PWM disable 1: PWM enable.

18.7.8.19 0x0090 PWM Group0 Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: PGR0
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/WAC	0x0	PWMG0_START PWM channels selected in PWMG0_CS start to output PWM waveform at the same time.
16	R/W	0x0	PWMG0_EN PWM Group0 Enable.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0090			Register Name: PGR0
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x0	PWMG0_CS If bit[i] is set, PWM i is selected as one channel of PWM Group0.

18.7.8.20 0x0094 PWM Group1 Register (Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: PGR1
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/WAC	0x0	PWMG1_START PWM channels selected in PWMG1_CS start to output PWM waveform at the same time.
16	R/W	0x0	PWMG1_EN PWM Group1 Enable.
15:0	R/W	0x0	PWMG1_CS If bit[i] is set, PWM i is selected as one channel of PWM Group1.

18.7.8.21 0x0098 PWM Group2 Register (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: PGR2
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/WAC	0x0	PWMG2_START PWM channels selected in PWMG2_CS start to output PWM waveform at the same time.
16	R/W	0x0	PWMG2_EN PWM Group2 Enable.
15:0	R/W	0x0	PWMG2_CS If bit[i] is set, PWM i is selected as one channel of PWM Group2.

18.7.8.22 0x009c PWM Group3 Register (Default Value: 0x0000_0000)

Offset: 0x009c			Register Name: PGR3
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/WAC	0x0	PWMG3_START PWM channels selected in PWMG3_CS start to output PWM waveform at the same time.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x009c			Register Name: PGR3
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	PWMG3_EN PWM Group2 Enable.
15:0	R/W	0x0	PWMG3_CS If bit[i] is set, PWM i is selected as one channel of PWM Group3.

18.7.8.23 0x00a0 Capture Cycle Counter Enable Register (Default Value: 0x0000_0000)

Offset: 0x00a0			Register Name: CCCER
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25	R	0x0	ATUO_CLEAR_FLAG_9 When choosing the CAP_CNT9_EN to enable capture counter, this bit is used to judge whether the channel9 capture counter is working or not. This bit=1 means the channel is processing, this bit=0 means the channel is disable. The user should not set CAP_CNT9_EN to 1 until ATUO_CLEAR_FLAG_9=0.
24	R	0x0	ATUO_CLEAR_FLAG_8 When choosing the CAP_CNT1_EN to enable capture counter, this bit is used to judge whether the channel8 capture counter is working or not. This bit=1 means the channel is processing, this bit=0 means the channel is disable. The user should not set CAP_CNT8_EN to 1 until ATUO_CLEAR_FLAG_8=0.
23	R	0x0	ATUO_CLEAR_FLAG_7 When choosing the CAP_CNT7_EN to enable capture counter, this bit is used to judge whether the channel7 capture counter is working or not. This bit=1 means the channel is processing. This bit=0 means the channel is disable. The user should not set CAP_CNT7_EN to 1 until ATUO_CLEAR_FLAG_7=0.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00a0			Register Name: CCCER
Bit	Read/Write	Default/Hex	Description
22	R	0x0	ATUO_CLEAR_FLAG_6 When choosing the CAP_CNT6_EN to enable capture counter, this bit is used to judge whether the channel6 capture counter is working or not. This bit=1 means the channel is processing, this bit=0 means the channel is disable. The user should not set CAP_CNT6_EN to 1 until ATUO_CLEAR_FLAG_6=0.
21	R	0x0	ATUO_CLEAR_FLAG_5 When choosing the CAP_CNT5_EN to enable capture counter, this bit is used to judge whether the channel5 capture counter is working or not. This bit=1 means the channel is processing, this bit=0 means the channel is disable. The user should not set CAP_CNT5_EN to 1 until ATUO_CLEAR_FLAG_5=0.
20	R	0x0	ATUO_CLEAR_FLAG_4 When choosing the CAP_CNT1_EN to enable capture counter, this bit is used to judge whether the channel4 capture counter is working or not. This bit=1 means the channel is processing, this bit=0 means the channel is disable. The user should not set CAP_CNT4_EN to 1 until ATUO_CLEAR_FLAG_4=0.
19	R	0x0	ATUO_CLEAR_FLAG_3 When choosing the CAP_CNT3_EN to enable capture counter, this bit is used to judge whether the channel3 capture counter is working or not. This bit=1 means the channel is processing, this bit=0 means the channel is disable. The user should not set CAP_CNT3_EN to 1 until ATUO_CLEAR_FLAG_3=0.
18	R	0x0	ATUO_CLEAR_FLAG_2 When choosing the CAP_CNT2_EN to enable capture counter, this bit is used to judge whether the channel2 capture counter is working or not. This bit=1 means the channel is processing, this bit=0 means the channel is disable. The user should not set CAP_CNT2_EN to 1 until ATUO_CLEAR_FLAG_2=0.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00a0			Register Name: CCCER
Bit	Read/Write	Default/Hex	Description
17	R	0x0	ATUO_CLEAR_FLAG_1 When choosing the CAP_CNT1_EN to enable capture counter, this bit is used to judge whether the channel1 capture counter is working or not. This bit=1 means the channel is processing, this bit=0 means the channel is disable. the user should not set CAP_CNT1_EN to 1 until ATUO_CLEAR_FLAG_1=0.
16	R	0x0	ATUO_CLEAR_FLAG_0 When choosing the CAP_CNT0_EN to enable capture counter, this bit is used to judge whether the channel0 capture counter is working or not. This bit=1 means the channel is processing, this bit=0 means the channel is disable. The user should not set CAP_CNT0_EN to 1 until ATUO_CLEAR_FLAG_0=0.
15:10	/	/	
9	R/W	0x0	CAP_CNT9_EN When relative PWM channel Capture Control Register bit5=0, setting CAP_CNT9_EN=1 will enabling capture counter. NOTE: CAP_CNT9_EN and CAP9_EN cannot be enabled together.
8	R/W	0x0	CAP_CNT8_EN When relative PWM channel Capture Control Register bit5=0, setting CAP_CNT8_EN=1 will enabling capture counter. NOTE: CAP_CNT8_EN and CAP8_EN cannot be enabled together.
7	R/W	0x0	CAP_CNT7_EN When relative PWM channel Capture Control Register bit5=0, setting CAP_CNT7_EN=1 will enabling capture counter. NOTE: CAP_CNT7_EN and CAP7_EN cannot be enabled together.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00a0			Register Name: CCCER
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	CAP_CNT6_EN When relative PWM channel Capture Control Register bit5=0, setting CAP_CNT6_EN=1 will enabling capture counter. NOTE: CAP_CNT6_EN and CAP6_EN cannot be enabled together.
5	R/W	0x0	CAP_CNT5_EN When relative PWM channel Capture Control Register bit5=0, setting CAP_CNT5_EN=1 will enabling capture counter. NOTE: CAP_CNT5_EN and CAP5_EN cannot be enabled together.
4	R/W	0x0	CAP_CNT4_EN When relative PWM channel Capture Control Register bit5=0, setting CAP_CNT4_EN=1 will enabling capture counter. NOTE: CAP_CNT4_EN and CAP4_EN cannot be enabled together.
3	R/W	0x0	CAP_CNT3_EN When relative PWM channel Capture Control Register bit5=0, setting CAP_CNT3_EN=1 will enabling capture counter. NOTE: CAP_CNT3_EN and CAP3_EN cannot be enabled together.
2	R/W	0x0	CAP_CNT2_EN When relative PWM channel Capture Control Register bit5=0, setting CAP_CNT2_EN=1 will enabling capture counter. NOTE: CAP_CNT2_EN and CAP2_EN cannot be enabled together.
1	R/W	0x0	CAP_CNT1_EN When relative PWM channel Capture Control Register bit5=0, setting CAP_CNT1_EN=1 will enabling capture counter. NOTE: CAP_CNT1_EN and CAP1_EN cannot be enabled together.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00a0			Register Name: CCCER
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	CAP_CNT0_EN When relative PWM channel Capture Control Register bit5=0, setting CAP_CNT0_EN=1 will enabling capture counter. NOTE: CAP_CNT0_EN and CAP0_EN cannot be enabled together.

18.7.8.24 0x00c0 Capture Enable Register (Default Value: 0x0000_0000)

Offset: 0x00c0			Register Name: CER
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9	R/W	0x0	CAP9_EN When enable capture function, the 16-bit up-counter starts working and channel 9 capture is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
8	R/W	0x0	CAP8_EN. When enable capture function, the 16-bit up-counter starts working and capture channel 8 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
7	R/W	0x0	CAP7_EN. When enable capture function, the 16-bit up-counter starts working and capture channel 7 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
6	R/W	0x0	CAP6_EN. When enable capture function, the 16-bit up-counter starts working and capture channel 6 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00c0			Register Name: CER
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	CAP5_EN. When enable capture function, the 16-bit up-counter starts working and capture channel5 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
4	R/W	0x0	CAP4_EN. When enable capture function, the 16-bit up-counter starts working and capture channel4 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
3	R/W	0x0	CAP3_EN. When enable capture function, the 16-bit up-counter starts working and capture channel3 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
2	R/W	0x0	CAP2_EN. When enable capture function, the 16-bit up-counter starts working and capture channel2 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
1	R/W	0x0	CAP1_EN. When enable capture function, the 16-bit up-counter starts working and capture channel1 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
0	R/W	0x0	CAP0_EN. When enable capture function, the 16-bit up-counter starts working and capture channel is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.7.8.25 0x0100+0x0000+N*0x0040 (N= 0~9) PWM Control Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0000+N*0x0040 (N= 0~9)			Register Name: PCR
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PWM_PUL_NUM In pulse mode, PWM output pulse for PWM_CYCLE_NUM+1 times and then stop.
15:12	/	/	/
11	R	0x0	PWM_PERIOD_RDY PWM period register ready 0: PWM period register is ready to write 1: PWM period register is busy.
10	R/WAC	0x0	PWM_PUL_START PWM pulse output start 0: No effect 1: Output pulse for PWM_CYCLE_NUM+1. After finishing configuration for outputting pulse, set this bit once and then PWM would output waveform. After the waveform is finished, the bit will be cleared automatically.
9	R/W	0x0	PWM_MODE PWM output mode select. 0: Cycle mode 1: Pulse mode.
8	R/W	0x0	PWM_ACT_STA. PWM active state. 0: Low Level 1: High Level.
7:0	R/W	0x0	PWM_PRESCAL_K. PWM pre-scale K, actual pre-scale is (K+1). K = 0, actual pre-scale: 1 K = 1, actual pre-scale: 2 K = 2, actual pre-scale: 3 K = 3, actual pre-scale: 4 ..... K = 255, actual pre-scale: 256.

18.7.8.26 0x0100+0x0004+N*0x0040 (N= 0~9) PWM Period Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0004+N*0x0040 (N= 0~9)			Register Name: PPR
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0100+0x0004+N*0x0040 (N= 0~9)			Register Name: PPR
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PWM_ENTIRE_CYCLE. Number of the entire cycles in the PWM clock. 0 = 1 cycle 1 = 2 cycles ..... N = N+1 cycles If the register need to be modified dynamically, the PCLK should be faster than the PWM CLK .
15:0	R/W	0x0	PWM_ACT_CYCLE. Number of the active cycles in the PWM clock. 0 = 0 cycle 1 = 1 cycles ..... N = N cycles

18.7.8.27 0x0100+0x0008+N*0x0040 (N= 0~9) PWM Counter Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0008+N*0x0040 (N= 0~9)			Register Name: PCNTR
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PWM_COUNTER_START PWM counter value is set for phase control.
15:0	R	0x0	PWM_COUNTER_STATUS On PWM output or capture input, reading this register could get the current value of the PWM 16bit up-counter.

18.7.8.28 0x0100+0x000C+N*0x0040 (N= 0~9) PWM Pulse Counter Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x000C+N*0x0040 (N= 0~9)			Register Name: PPCNTR
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	PWM_PUL_COUNTER_STATUS On PWM output , reading this register could get the current value of the PWM pulse counter.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.7.8.29 0x0100+0x0010+N*0x0040 (N= 0~9) Capture Control Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0010+N*0x0040 (N= 0~9)			Register Name: CCR
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	CCSR This bit is used to configure starting manner of capture counter. 0: staring capture counter when CAP_CNT*_EN=1 1: starting capture counter when CAP*_EN=1 NOTE: This bit needs to be configured before CAP_CNT*_EN=1 or CAP*_EN=1
4	R/W1C	0x0	CRLF. When capture channel captures rising edge, the 16-bit up-counter's current value is latched to CRLR and then this bit is set 1 by hardware. Write 1 to clear this bit.
3	R/W1C	0x0	CFLF. When capture channel captures falling edge, the 16-bit up-counter's current value is latched to CFLR and then this bit is set 1 by hardware. Write 1 to clear this bit.
2	R/W	0x0	CRTE. Rising edge capture trigger enable
1	R/W	0x0	CFTE. Falling edge capture trigger enable
0	R/W	0x0	CAPINV. Inversing the signal inputted form capture channel before capture channel's 16bit counter. 0: Not inverse 1: Inverse

18.7.8.30 0x0100+0x0014+N*0x0040 (N= 0~9) Capture Rise Lock Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0014+N*0x0040 (N= 0~9)			Register Name: CRLR
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0100+0x0014+N*0x0040 (N= 0~9)			Register Name: CRLR
Bit	Read/Write	Default/Hex	Description
15:0	R	0x0	CRLR. When capture channel captures rising edge, the 16-bit up-counter's current value is latched to this register.

18.7.8.31 0x0100+0x0018+N*0x0040 (N= 0~9) Capture Fall Lock Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0018+N*0x0040 (N= 0~9)			Register Name: CFLR
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	CFLR. When capture channel captures falling edge, the 16-bit up-counter's current value is latched to this register.

18.7.8.32 0x0100+0x001C+N*0x0040 (N= 0~9) Capture Cycle Counter Status Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x001C+N*0x0040 (N= 0~9)			Register Name: CCCSR
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CCCSR. When capture channel captures the cycles of input signal, the 32-bit up-counter's current value can be observed by this register.

18.7.8.33 0x0100+0x0020+N*0x0040 (N= 0~9) Capture Cycle Counter Number Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0020+N*0x0040 (N= 0~9)			Register Name: CCCNR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CCCNR This number is used to compare with capture counter number, and if capture counter up to the number, it will generate capture counter interrupt if capture counter interrupt is enable.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.7.8.34 0x0100+0x0024+N*0x0040 (N= 0~9) Capture Cycle Counter Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0024+N*0x0040 (N= 0~9)			Register Name: CCCR
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R	0x0	CCCNR_RDY Capture Cycle Counter Number Register ready. 0: Capture Cycle Counter Number Register is ready to write. 1: Capture Cycle Counter Number Register is busy.
1	R/W	0x0	CCCSRR This number is used to choose the behavior after counter value up to CCCNR. 0: stop counting and set CAP_CNT*_EN=0 if PWM channel Capture Control Register bit5=0 1: restart counting
0	R/W	0x0	CCCRFR This number is used to choose capture cycle counter using rising edge or falling edge to count. 0: Rising edge 1: Falling edge

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.8 SPI

18.8.1 Overview

The Serial Peripheral Interface (SPI) is a full-duplex, synchronous, four-wire serial communication interface between a CPU and SPI-compliant external devices. It can work in master mode and slave mode.

The SPI has the following features:

- Four SPI interfaces:
  - SPI0, SPI2, and SPI3 in CPUX Domain
  - S_SPI0 in CPUS Domain
- Supports multiple SPI mode
  - Master mode and Slave mode Standard SPI (4-wire)
  - Master mode Dual-Output/Dual-Input SPI/ Dual I/O SPI
  - Master mode Quad-Output/Quad-Input SPI
  - Master mode 3-wire SPI, with programmable serial data frame length: 1bit to 32bits
- Supports the Maximum clock frequency: 100MHz
- Supports TX/RX DMA Slave interface
- Transmits data FIFO with 8-bit wide and 64-entry
- Receives data FIFO with 8-bit wide and 64-entry
- Transmits data buffer with 8-bit wide and 4-entry
- Receives data buffer with 8-bit wide and 128-entry
- Supports Data Sample Mode
  - Mode0, Mode1, Mode2 and Mode3
- Supports Control signal config
  - Up to four chip selects to support multiple peripherals
  - Polarity and phase of the Chip Select (SPI_CS) and SPI Clock (SPI_CLK) are configurable

NOTE

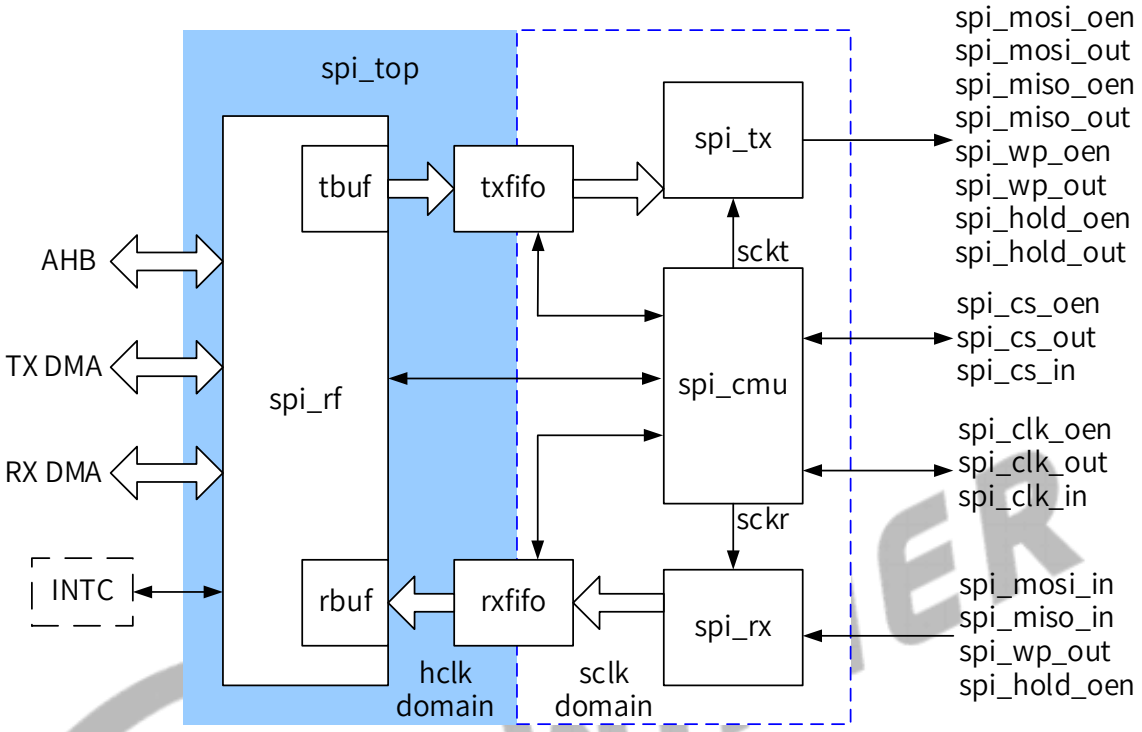
This chapter only describes SPI0, SPI2, SPI3, and S_SPI0. For the detailed information of SPI1 with SPI mode and DBI mode, please refer to section 18.9 SPI_DBI.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.8.2 Block Diagram

The following figure shows a block diagram of the SPI.

Figure 18-19 SPI Block Diagram



SPI contains the following sub-blocks:

Table 18-7 SPI Sub-blocks

Sub-block	Description
spi_rf	It is responsible for implementing the internal registers, interrupts, and DMA Requests.
spi_tbuf	The data length transmitted from AHB to TXFIFO is converted into 8 bits, then the data is written into the RXFIFO.
spi_rbuf	The block is used to convert the RXFIFO data into the reading data length of AHB.
txfifo, rxfifo	The data transmitted from the SPI to the external serial device is written into the TXFIFO; the data received from the external serial device into SPI is pushed into the RXFIFO.
spi_cmu	It is responsible for implementing SPI bus clock, chip select, internal sample, and the generation of transfer clock.
spi_tx	It is responsible for implementing SPI data transfer, the interface of the internal TXFIFO, and status register.
spi_rx	It is responsible for implementing SPI data receive, the interface of the internal RXFIFO, and status register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.8.3 Clock Sources

The following table describes the clock sources of SPI0/2/3/4 and S_SPI. For clock setting, configurations, and gating information, refer to the section CCU or PRCM.

Module	Clock Sources	Description
SPI0/2/3	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.
	PERI0_300M	Its frequency is 300 MHz by default.
	PERI0_200M	Its frequency is 200 MHz by default.
	PERI1_300M	Its frequency is 300 MHz by default.
	PERI1_200M	Its frequency is 200 MHz by default.
	PERI0_480M	Its frequency is 480 MHz by default.
	PERI1_480M	Its frequency is 480 MHz by default.
	DCXO	The external high-frequency crystal oscillator. Its frequency is 26 MHz.
S_SPI	DCXO	The external high-frequency crystal oscillator. Its frequency is 26 MHz.
	PERIPLL_DIV	Its frequency is 200 MHz by default.
	PERI0_300M	Its frequency is 300 MHz by default.
	PERI1_300M	Its frequency is 300 MHz by default.
	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.

18.8.4 External Signals

The following table describes the external signals of SPI. The MOSI and MISO are bidirectional I/O. when SPI is as a master device, the CLK and CS are the output pin; when SPI is as a slave device, the CLK and CS are the input pin. When using SPI, the corresponding PADs are selected as SPI function via section CCU.

Table 18-8 SPI External Signals

Signal Name[	Description	Type
SPI0-CS[1:0]	SPI0 Chip Select Signal, Low Active	I/O
SPI0-CLK	SPI0 Clock Signal	I/O
SPI0-MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0-MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI0-WP	SPI0 Write Protect, Low Active	I/O
SPI0-HOLD	SPI0 Hold Signal	I/O
SPI2-CS[3:0]	SPI2 Chip Select Signal, Low Active	I/O
SPI2-CLK	SPI2 Clock Signal	I/O
SPI2-MOSI	SPI2 Master Data Out, Slave Data In	I/O
SPI2-MISO	SPI2 Master Data In, Slave Data Out	I/O
SPI3-CS[1:0]	SPI3 Chip Select Signal, Low Active	I/O
SPI3-CLK	SPI3 Clock Signal	I/O

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Signal Name[	Description	Type
SPI3-MOSI	SPI3 Master Data Out, Slave Data In	I/O
SPI3-MISO	SPI3 Master Data In, Slave Data Out	I/O
S-SPI0-CS0	S-SPI0 Chip Select Signal, Low Active	I/O
S-SPI0-CLK	S-SPI0 Clock Signal	I/O
S-SPI0-MOSI	S-SPI0 Master Data Out, Slave Data In	I/O

18.8.5 Functional Description

18.8.5.1 SPI Master and Slave Mode

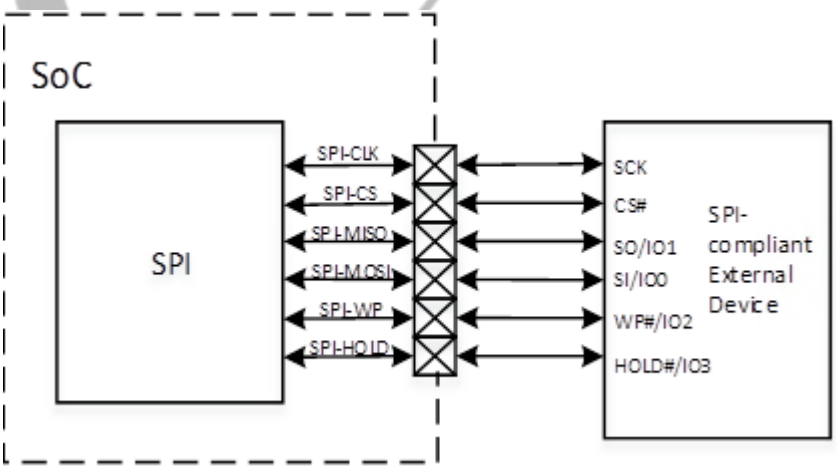
The SPI controller can be configured to a master or slave device. The master mode is selected by setting the MODE bit (SPI_GCR[1]); the slave mode is selected by clearing the MODE bit.

In master mode, the SPI_CLK is generated and transmitted to the external device, and the data from the TX FIFO is transmitted on the MOSI pin, the data from the slave is received on the MISO pin and sent to RX FIFO. The Chip Select (SPI_CS) is an active low signal, and it must be set low before the data are transmitted or received. The SPI_CS can be selected the auto control mode or the software manual control mode. When using auto control, the SS_OWNER (SPI_TCR[6]) must be cleared (default value is 0); when using manual control, the SS_OWNER must be set. And the level of SPI_CS is controlled by SS_LEVEL (SPI_TCR[7]).

In slave mode, after the software selects the MODE bit (SPI_GCR [1]) to '0', it waits for master to initiate a transaction. When the master asserts SPI_CS, and SPI_CLK is transmitted to the slave, the slave data is transmitted from TX FIFO on the MISO pin, and the data from the MOSI pin is received in RX FIFO.

If using the Master and Slave function of the SPIC, conform to the circuit connection between the Master and Slave as shown below.

Figure 18-20 Circuit Connection between the Master and Slave



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.8.5.2 SPI Transmit Format

The SPI supports 4 different formats for data transfer. The software can select one of the four modes in which the SPI works by setting the bit1 (Polarity) and bit0 (Phase) of SPI_TCR (Offset: 0x0008). The SPI controller master uses the SPI_CLK signal to transfer data in and out of the shift register. Data is clocked using any one of four programmable clock phase and polarity combinations.

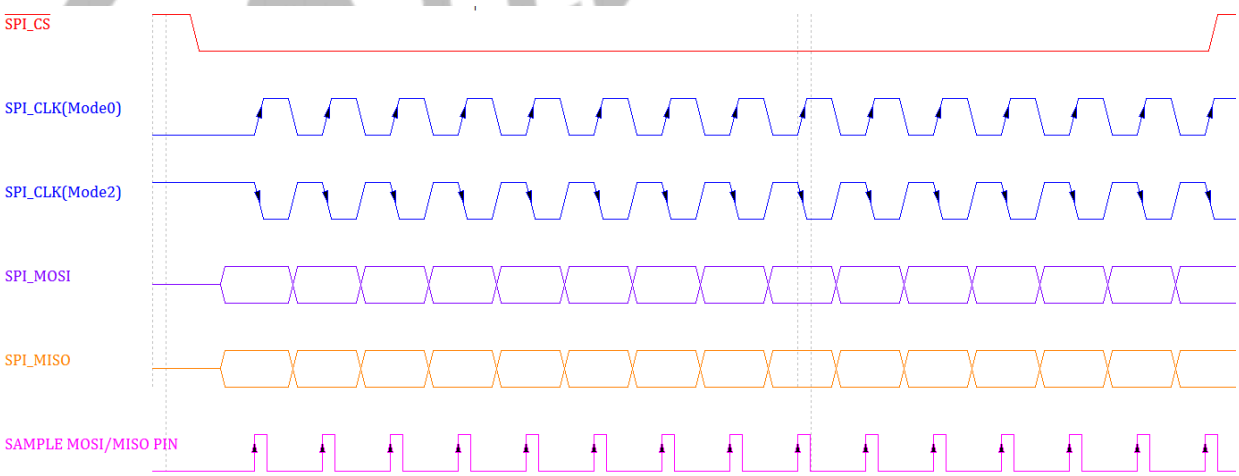
The CPOL (SPI_TCR [1]) defines the polarity of the clock signal (SPI_CLK). The SPI_CLK is a high level when CPOL is 1 and it is a low level when CPOL is 0 . The CPHA (SPI_TCR [0]) decides whether the leading edge of SPI_CLK is used to setup or sample data. The leading edge is used to setup data when CPHA is 1 , and sample data when CPHA is 0 . The following table lists the four modes.

Table 18-9 SPI Transmit Format

Mode	Polarity (CPOL)	Phase (CPHA)	Leading Edge	Trailing Edge
Mode0	0	0	Sample on the rising edge	Setup on the falling edge
Mode1	0	1	Setup on the rising edge	Sample on the falling edge
Mode2	1	0	Sample on the falling edge	Setup on the rising edge
Mode3	1	1	Setup on the falling edge	Sample on the rising edge

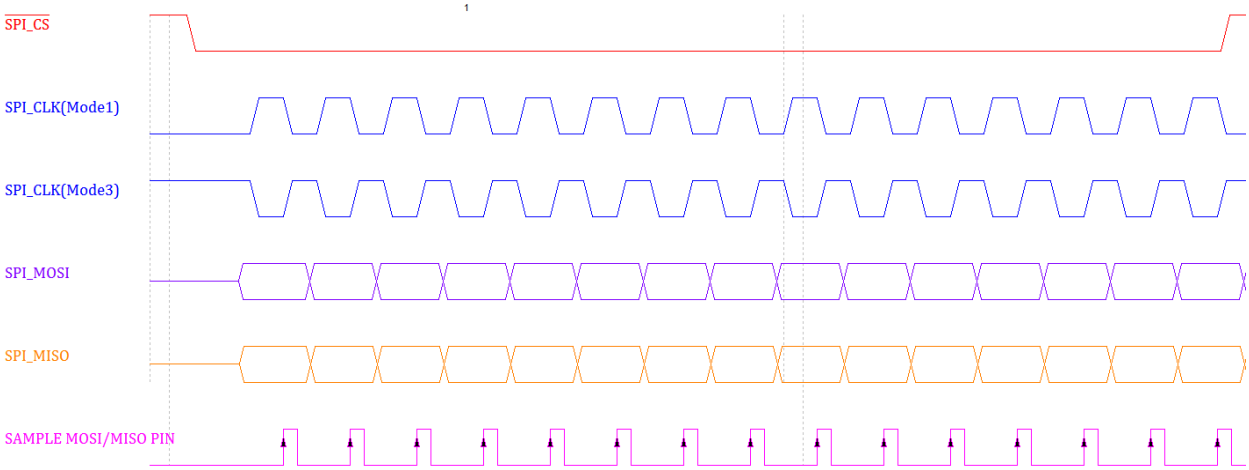
The following figures describe four waveforms for SPI_CLK.

Figure 18-21 SPI Phase 0 Timing Diagram



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

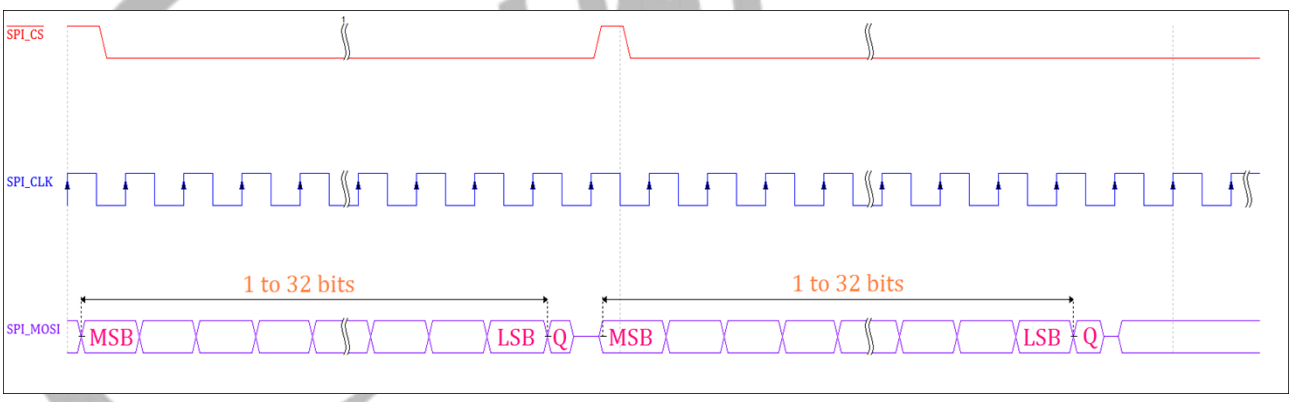
Figure 18-22 SPI Phase 1 Timing Diagram



18.8.5.3 SPI 3-Wire Mode

The SPI 3-wire mode is only valid when the SPI controller work in master mode, and is selected when the Work Mode Select bit (SPI_BATCR [1:0]) is equal to 0x2. And in the 3-wire mode, the input data and the output data use the same single data line. The following figure describes the 3-wire mode.

Figure 18-23 SPI 3-Wire Mode

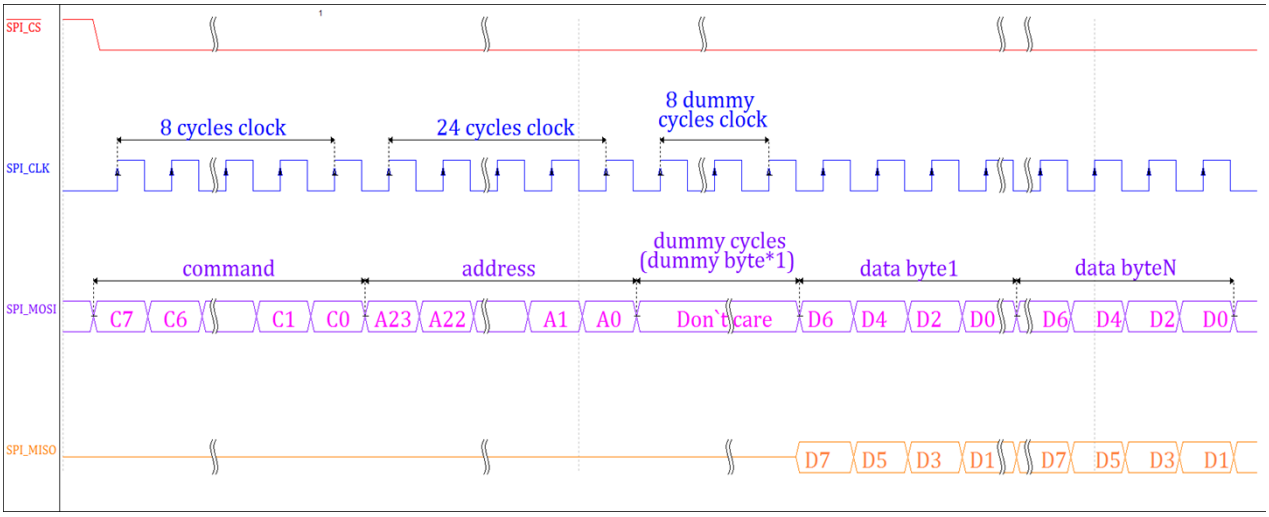


18.8.5.4 SPI Dual Mode

The dual read mode (SPI x2) is selected when the DRM is set in SPI_BCC (Offset: 0x0038) [28]. Using the dual mode allows data to be transferred to or from the device at double the rate of standard single mode, the data can be read at fast speed using two data bits (MOSI and MISO) at a time. The following figure describes the dual-input/dual-output SPI and the dual I/O SPI.

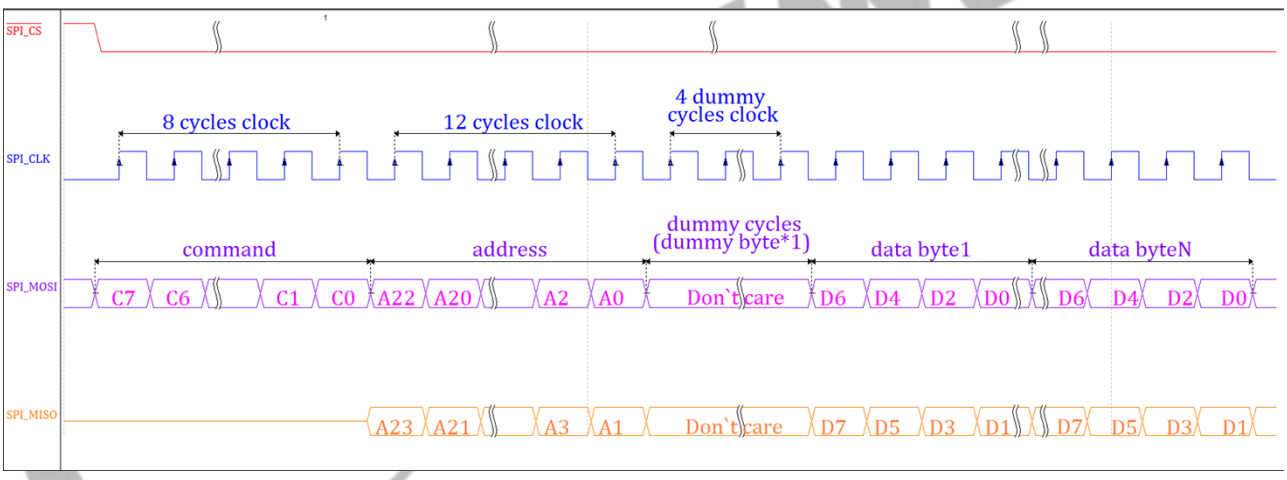
Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 18-24 SPI Dual-Input/Dual-Output Mode



In the dual-input/dual-output SPI mode, the command, address, and the dummy bytes output in a unit of a single bit in serial mode through the SPI_MOSI line, only the data bytes are output (write) and input (read) in a unit of dual bits through the SPI_MOSI and SPI_MISO.

Figure 18-25 SPI Dual I/O Mode



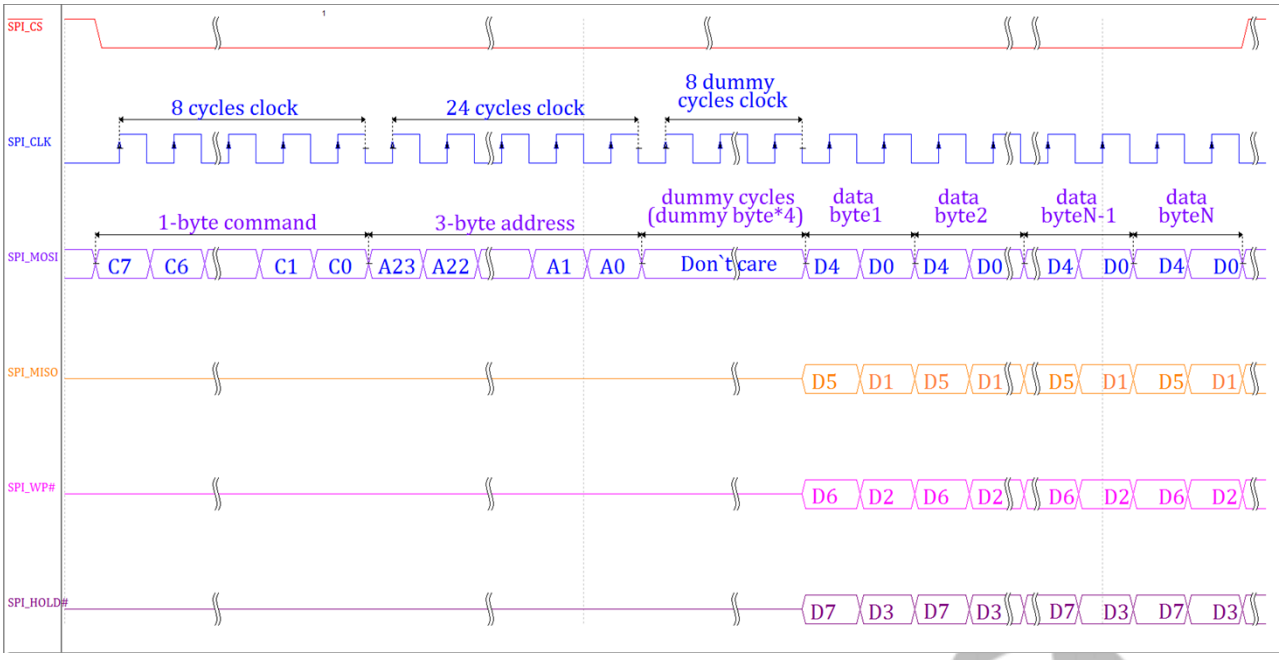
In the dual I/O SPI mode, only the command bytes output in a unit of a single bit in serial mode through the SPI_MOSI line. The address bytes and the dummy bytes output in a unit of dual bits through the SPI_MOSI and SPI_MISO. And the data bytes output (write) and input (read) in a unit of dual bits through the SPI_MOSI and SPI_MISO.

18.8.5.5 SPI Quad Mode

The quad read mode (SPI x4) is selected when the Quad_EN is set in SPI_BCC (Offset: 0x0038) [29]. Using the quad mode allows data to be transferred to or from the device at 4 times the rate of standard single mode, the data can be read at fast speed using four data bits (MOSI, MISO, IO2 (WP#) and IO3 (HOLD#)) at the same time. The following figure describes the quad-input/quad-output SPI.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 18-26 SPI Quad-Input/Quad-Output Mode



In the quad-input/quad-output SPI mode, the command, address, and the dummy bytes output in a unit of a single bit in serial mode through SPI_MOSI line. Only the data bytes output (write) and input (read) in a unit of quad bits through the SPI_MOSI, SPI_MISO, SPI_WP#, and SPI_HOLD#.

18.8.5.6 SPI Error Conditions

If any error conditions occur, the hardware will set the corresponding status bits in the SPI Interrupt Status Register (Offset: 0x0014) and stop the transfer. For the SPI controller, the following error scenarios can happen.

- TX_FIFO Underrun

The TX_FIFO underrun happens when the CPU/DMA reads data from the empty TX FIFO. In the case, the SPI controller will end the transaction and flag the error bit along with the TF_UDF bit in the SPI Interrupt Status Register (Offset: 0x0014). The SPI controller will generate an interrupt if interrupts are enabled. The software has to clear the error bit and the TF_UDF bit. To start a new transaction, the software has to reset the FIFO by writing to the SRST (soft reset) bit in the SPI Global Control Register (Offset: 0x0004).

- TX_FIFO Overflow

The TX_FIFO overflow happens when the CPU/DMA writes data into the full TX FIFO. In the case, the SPI controller will end the transaction and flag the error bit along with the TF_OVF bit in the SPI Interrupt Status Register (Offset: 0x0014). The SPI controller will generate an interrupt if interrupts are enabled. The software has to clear the error bit and the TF_OVF bit. To start a new transaction, the software has to reset the FIFO by writing to the SRST (soft reset) bit in the SPI Global Control Register (Offset: 0x0004).

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- RX_FIFO Underrun

The RX_FIFO underrun happens when the CPU/DMA reads data from RX FIFO when it is empty. In the case, the SPI controller will end the transaction and flag the error bit along with the RF_UDF bit in the SPI Interrupt Status Register (Offset: 0x0014). The SPI controller will generate an interrupt if interrupts are enabled. The software has to clear the error bit and the RF_UDF bit. To start a new transaction, the software has to reset the FIFO by writing to the SRST (soft reset) bit in the SPI Global Control Register (Offset: 0x0004).

- RX_FIFO Overflow

The RX_FIFO overflow happens when the CPU/DMA writes data into the RX FIFO when it is full. In the case, the SPI controller will end the transaction and flag the error bit along with the RF_OVF bit in the SPI Interrupt Status Register (Offset: 0x0014). The SPI controller will generate an interrupt if interrupts are enabled. The software has to clear the error bit and the RF_OVF bit. To start a new transaction, the software has to reset the FIFO by writing to the SRST (soft reset) bit in the SPI Global Control Register (Offset: 0x0004).

18.8.5.7 SPI Clock Frequency

The SPI clock source frequency can be configured according to CCU, which is assumed to be frequency A MHz. 2 stage division coefficient N & M should be set.

The SPI working frequency is $\frac{A}{(N+1)\times(M+1)}$ MHz.

18.8.6 Programming Guidelines

18.8.6.1 CPU or DMA Transfer

The SPI transfers serial data between the processor and peripheral devices. The CPU mode and DMA mode are the two main operational modes for SPI. For each SPI, the data is simultaneously transmitted (shifted out serially) and received (shifted in serially). The SPI has 2 channels, including the TX channel and RX channel. The TX channel has the path from TX FIFO to peripheral devices. The RX channel has the path from peripheral devices to RX FIFO.

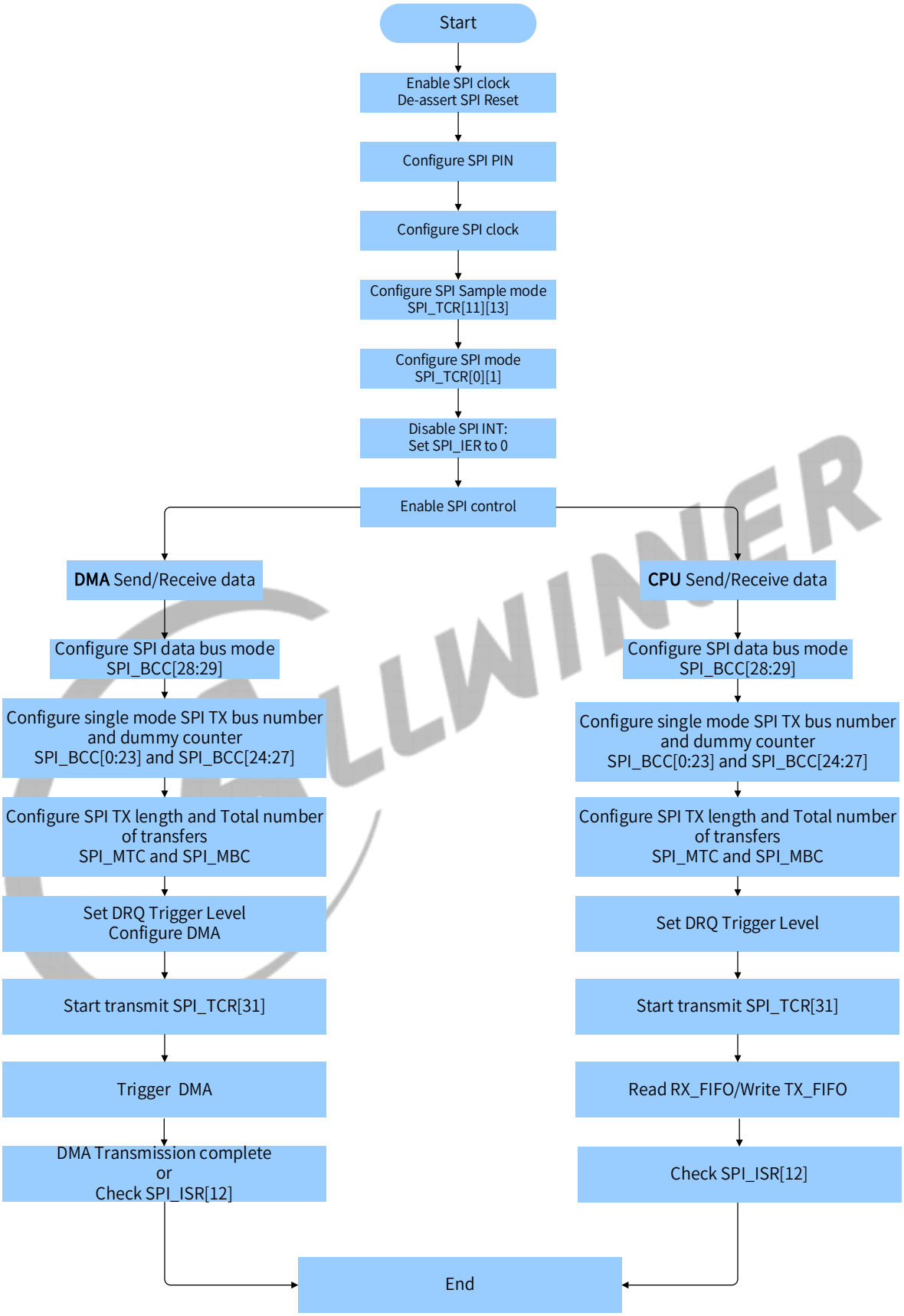
Write Data: The CPU or DMA must write data on the SPI_TXD (Offset: 0x0200), the data on the register are automatically moved to TX FIFO.

Read Data: To read data from RX FIFO, the CPU or DMA must access the SPI_RXD (Offset: 0x0300) and the data are automatically sent to the SPI_RXD (Offset: 0x0300).

In CPU or DMA mode, the SPI sends a completed interrupt (SPI_ISR[TC]) to the processor after each transmission is complete.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 18-27 Data Transfer in Query Mode



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.8.6.2 Master Transmit and Receive Burst

In the SPI Master mode, the transmit and receive bursts (byte in unit) are configured before the SPI transfers serial data between the processor and external device. The transmit burst write in MWTC (bit[23:0]) of SPI Master Transmit Counter Register. The transmit burst in single mode before automatically sending dummy burst write in STC (bit[23:0]) of SPI Master Burst Control Counter Register. For dummy data, SPI controller can automatically sent before receive by writing DBC (bit[27:24]) in SPI Master Burst Control Counter Register. If users don't use SPI controller to send dummy data automatically, then the dummy bursts are used as the transmit counters to write together in MWTC (bit[23:0]) of SPI Master Transmit Counter Register. In Master mode, the total burst numbers write in MBC (bit[23:0]) of SPI Master Burst Counter Register. When all transmit burst and receive burst are transferred, SPI controller will send a completed interrupt, at the same time, SPI controller will clear DBC, MWTC and MBC.

18.8.6.3 SPI Run Clock and Sample Mode

The SPI Controller runs at 24KHz~100MHz at its interface to external SPI devices. The internal SPI Clock should run at the same frequency as the outgoing clock in master mode. The SPI Clock is selected different clock sources, and SPI must configure different work mode. There are three work mode: normal sample mode, delay half cycle sample mode, delay one cycle sample mode. Delay half cycle sample mode is the default mode of SPI controller. When SPI runs at 48MHz or below 48MHz, SPI can work at normal sample mode or delay half cycle sample mode. When SPI runs over 48MHz, set SDC in SPI Transfer Control Register to 1 to make the internal read sample point with a delay of half cycle of SPI_CLK, which is used in high-speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave device. The different configuration of new/old SPI sample mode shows in the following tables.

Table 18-10 SPI Old Sample Mode

SPI Sample Mode	SDM(bit13)	SDC(bit11)	Run Clock
normal sample	1	0	<=24MHz
delay half cycle sample	0	0	<=40MHz
delay one cycle sample	0	1	>=80MHz

NOTE

The remaining frequencies are not recommended. When the SPI Flash output delay time is the same as the half-cycle time of the SPI working clock, it will cause the device output data edge to along with the controller clock sampling edge. Therefore, setting a delay of one cycle sampling may lead to instabilities.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Table 18-11 SPI New Sample Mode

SPI Sample Mode	SDM(bit13)	SDC(bit11)	SDC1(bit15)
normal sample	1	0	0
delay half cycle sample	0	0	0
delay one cycle sample	0	1	0
delay 1.5 cycle sample	1	1	0
delay 2 cycle sample	1	0	1
delay 2.5 cycle sample	0	0	1
delay 3 cycle sample	0	1	1

18.8.7 Register List

Module Name	Base Address	Comments
SPI0	0x02540000	SPI0 controller register
SPI2	0x02542000	SPI2 controller register is the same with SPI0
SPI3	0x02543000	SPI3 controller register is the same with SPI0
S_SPI	0x07092000	S_SPI controller register is the same with SPI0

Register Name	Offset	Description
SPI_GCR	0x0004	SPI Global Control Register
SPI_TCR	0x0008	SPI Transfer Control register
SPI_IER	0x0010	SPI Interrupt Control register
SPI_ISR	0x0014	SPI Interrupt Status register
SPI_FCR	0x0018	SPI FIFO Control register
SPI_FSR	0x001C	SPI FIFO Status register
SPI_WCR	0x0020	SPI Wait Clock Counter register
SPI_SAMP_DL	0x0028	SPI Sample Delay Control Register
SPI_MTC	0x0034	SPI Master Transmit Counter Register
SPI_BCC	0x0038	SPI Master Burst Control Counter register
SPI_BATCR	0x0040	SPI Bit-Aligned Transfer Configure Register
SPI_BA_CCR	0x0044	SPI Bit-Aligned CLOCK Configuration Register
SPI_TBR	0x0048	SPI TX Bit Register
SPI_RBR	0x004C	SPI RX Bit Register
SPI_NDMA_MODE_CTL	0x0088	SPI Normal DMA Mode Control Register
SPI_TXD	0x0200	SPI TX Data register
SPI_RXD	0x0300	SPI RX Data register
SPI_BSR	0x0400	SPI BUF Status register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.8.8 Register Description

18.8.8.1 0x0004 SPI Global Control Register (Default Value: 0x0000_0080)

Offset: 0x0004			Register Name: SPI_GCR
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	SRST Soft reset Write 1 to this bit will clear the SPI controller, and auto clear to 0 when reset operation completes Write 0 has no effect.
30:8	/	/	/
7	R/W	0x1	TP_EN Transmit Pause Enable In master mode, it is used to control transmit state machine to stop smart burst sending when RX FIFO is full. 1: stop transmit data when RXFIFO is full 0: Normal operation. Ignore RXFIFO status *Note: This bit cannot be written when XCH=1.*
6:3	/	/	/
2	R/W	0x0	MODE_SEL Sample Timing Mode Select 0: Old mode of Sample Timing 1: New mode of Sample Timing *Note: This bit cannot be written when XCH=1.*
1	R/W	0x0	MODE SPI Function Mode Select 0: Slave Mode 1: Master Mode *Note: This bit cannot be written when XCH=1.*
0	R/W	0x0	EN SPI Module Enable Control 0: Disable 1: Enable *Note: After transforming from bit_mode to byte_mode, it must Enable the SPI Module again.*

18.8.8.2 0x0008 SPI Transfer Control Register (Default Value: 0x0000_0087)

Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	XCH Exchange Burst In master mode it is used to start SPI burst 0: Idle 1: Initiates exchange. Write 1 to this bit will start the SPI burst, and will auto clear after finishing the bursts transfer specified by BC. Write 1 to SRST will also clear this bit. Write 0 to this bit has no effect. *Note: This bit cannot be written when XCH=1.*
30:16	/	/	/
15	R/W	0x0	SDC1 Master Sample Data Control register1 Set this bit to 1 to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. 0: Normal operation, do not delay internal read sample point 1: Delay internal read sample point *Note: This bit cannot be written when XCH=1.*
14	R/W	0x0	SDDM Sending Data Delay Mode 0: Normal sending 1: Delay sending Set the bit to"1" to make the data that should be sent with a delay of half cycle of SPI_CLK in dual I/O mode for SPI mode 0.
13	R/W	0x0	SDM Master Sample Data Mode 1: Normal Sample Mode 0: Delay Sample Mode In Normal Sample Mode, SPI master samples the data at the correct edge for each SPI mode; In Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the correct edge defined in respective SPI mode.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	FBS First Transmit Bit Select 0: MSB first 1: LSB first *Note: Can t be written when XCH=1.*
11	R/W	0x0	SDC Master Sample Data Control Set this bit to 1 to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. 0: Normal operation, do not delay internal read sample point 1: Delay internal read sample point *Note: This bit can t be written when XCH=1.*
10	R/W	0x0	RPSM Rapids mode select Select Rapids mode for high speed write. 0: Normal write mode 1: Rapid write mode Note: Can t be written when XCH=1.
9	R/W	0x0	DDB Dummy Burst Type 0: The bit value of dummy SPI burst is zero 1: The bit value of dummy SPI burst is one *Note: This bit can t be written when XCH=1.*
8	R/W	0x0	DHB Discard Hash Burst In master mode it controls whether discarding unused SPI bursts 0: Receiving all SPI bursts in BC period 1: Discard unused SPI bursts, only fetching the SPI bursts during dummy burst period. The bursts number is specified by TC. *Note: This bit can t be written when XCH=1.*

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description
7	R/W	0x1	SS_LEVEL When control SS signal manually (SPI_CTRL_REG.SS_CTRL==1), set this bit to 1 or 0 to control the level of SS signal. 0: set SS to low 1: set SS to high *Note: This bit can t be written when XCH=1.*
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software *Note: This bit can t be written when XCH=1.*
5:4	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_CS0 will be asserted 01: SPI_CS1 will be asserted 10: SPI_CS2 will be asserted 11: SPI_CS3 will be asserted *Note: This bit can t be written when XCH=1.*
3	R/W	0x0	SSCTL In master mode, this bit selects the output wave form for the SPI_CSx signal. Only valid when SS_OWNER = 0. 0: SPI_CSx remains asserted between SPI bursts 1: Negate SPI_CSx between SPI bursts *Note: This bit can t be written when XCH=1.*
2	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) *Note: This bit can t be written when XCH=1.*
1	R/W	0x1	CPOL SPI Clock Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) *Note: This bit can t be written when XCH=1.*

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description
0	R/W	0x1	CPHA SPI Clock/Data Phase Control 0: Phase 0 (Leading edge for sample data) 1: Phase 1 (Leading edge for setup data) *Note: This bit can t be written when XCH=1.*

18.8.8.3 0x0010 SPI Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SPI_IER
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R/W	0x0	SS_INT_EN SSI Interrupt Enable Chip Select Signal (SSx) from valid state to invalid state 0: Disable 1: Enable
12	R/W	0x0	TC_INT_EN Transfer Completed Interrupt Enable 0: Disable 1: Enable
11	R/W	0x0	TF_UDR_INT_EN TXFIFO under run Interrupt Enable 0: Disable 1: Enable
10	R/W	0x0	TF_OVF_INT_EN TX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
9	R/W	0x0	RF_UDR_INT_EN RXFIFO under run Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	RF_OVF_INT_EN RX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
7	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0010			Register Name: SPI_IER
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	TF_FUL_INT_EN TX FIFO Full Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TX_EMP_INT_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	TX_ERQ_INT_EN TX FIFO Empty Request Interrupt Enable 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	RF_FUL_INT_EN RX FIFO Full Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RX_EMP_INT_EN RX FIFO Empty Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RF_RDY_INT_EN RX FIFO Ready Request Interrupt Enable 0: Disable 1: Enable

18.8.8.4 0x0014 SPI Interrupt Status Register (Default Value: 0x0000_0032)

Offset: 0x0014			Register Name: SPI_ISR
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R/W1C	0x0	SSI SS Invalid Interrupt When SSI is 1, it indicates that SS has changed from valid state to invalid state. Writing 1 to this bit clears it.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: SPI_ISR
Bit	Read/Write	Default/Hex	Description
12	R/W1C	0x0	TC Transfer Completed In master mode, it indicates that all bursts specified by BC has been exchanged. In other condition, when set, this bit indicates that all the data in TXFIFO has been loaded in the Shift register, and the Shift register has shifted out all the bits. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed
11	R/W1C	0x0	TF_UDF TXFIFO underrun This bit is set when if the TXFIFO is underrun. Writing 1 to this bit clears it. 0: TXFIFO is not underrun 1: TXFIFO is underrun
10	R/W1C	0x0	TF_OVF TXFIFO Overflow This bit is set when if the TXFIFO is overflow. Writing 1 to this bit clears it. 0: TXFIFO is not overflow 1: TXFIFO is overflowed
9	R/W1C	0x0	RX_UDF RXFIFO Underrun When set, this bit indicates that RXFIFO has underrun. Writing 1 to this bit clears it.
8	R/W1C	0x0	RX_OVF RXFIFO Overflow When set, this bit indicates that RXFIFO has overflowed. Writing 1 to this bit clears it. 0: RXFIFO is available. 1: RXFIFO has overflowed.
7	/	/	/
6	R/W1C	0x0	TX_FULL TXFIFO Full This bit is set when if the TXFIFO is full. Writing 1 to this bit clears it. 0: TXFIFO is not Full 1: TXFIFO is Full

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: SPI_ISR
Bit	Read/Write	Default/Hex	Description
5	R/W1C	0x1	TX_EMP TXFIFO Empty This bit is set if the TXFIFO is empty. Writing 1 to this bit clears it. 0: TXFIFO contains one or more words. 1: TXFIFO is empty
4	R/W1C	0x1	TX_READY TXFIFO Ready 0: TX_WL > TX_TRIG_LEVEL 1: TX_WL <= TX_TRIG_LEVEL This bit is set any time if TX_WL <= TX_TRIG_LEVEL. Writing 1 to this bit clears it. Where TX_WL is the water level of RXFIFO
3	/	/	/
2	R/W1C	0x0	RX_FULL RXFIFO Full This bit is set when the RXFIFO is full. Writing 1 to this bit clears it. 0: Not Full 1: Full
1	R/W1C	0x1	RX_EMP RXFIFO Empty This bit is set when the RXFIFO is empty. Writing 1 to this bit clears it. 0: Not empty 1: Empty
0	R/W1C	0x0	RX_RDY RXFIFO Ready 0: RX_WL <= RX_TRIG_LEVEL 1: RX_WL > RX_TRIG_LEVEL This bit is set any time if RX_WL > RX_TRIG_LEVEL. Writing 1 to this bit clears it. Where RX_WL is the water level of RXFIFO.

18.8.8.5 0x0018 SPI FIFO Control Register (Default Value: 0x0040_0001)

Offset: 0x0018			Register Name: SPI_FCR
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0018			Register Name: SPI_FCR
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	TX_FIFO_RST TX FIFO Reset Write 1 to this bit will reset the control portion of the TX FIFO and auto clear to 0 when completing reset operation, write to 0 has no effect.
30	R/W	0x0	TF_TEST_ENB TX Test Mode Enable 0: Disable 1: Enable In normal mode, TX FIFO can only be read by SPI controller, write 1 to this bit will switch TX FIFO read and write function to AHB bus. This bit is used to test the TX FIFO, don t set in normal operation and don t set RF_TEST and TF_TEST at the same time.
29:25	/	/	/
24	R/W	0x0	TF_DRQ_EN TX FIFO DMA Request Enable 0: Disable 1: Enable
23:16	R/W	0x40	TX_TRIG_LEVEL TX FIFO Empty Request Trigger Level
15	R/WAC	0x0	RF_RST RXFIFO Reset Write 1 to this bit will reset the control portion of the receiver FIFO, and auto clear to 0 when completing reset operation, write 0 to this bit has no effect.
14	R/W	0x0	RF_TEST RX Test Mode Enable 0: Disable 1: Enable In normal mode, RX FIFO can only be written by SPI controller, write 1 to this bit will switch RX FIFO read and write function to AHB bus. This bit is used to test the RX FIFO, don t set in normal operation and don t set RF_TEST and TF_TEST at the same time.
13:9	/	/	/
8	R/W	0x0	RF_DRQ_EN RX FIFO DMA Request Enable 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0018			Register Name: SPI_FCR
Bit	Read/Write	Default/Hex	Description
7:0	R/W	0x1	RX_TRIG_LEVEL RX FIFO Ready Request Trigger Level CAUTION: Whether in CPU mode or in DMA mode, trigger level should be set properly that actual data amount reaches trigger level.

18.8.8.6 0x001C SPI FIFO Status Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SPI_FSR
Bit	Read/Write	Default/Hex	Description
31	R	0x0	TB_WR TX FIFO Write Buffer Write Enable
30:24	/	/	/
23:16	R	0x0	TF_CNT TX FIFO Counter These bits indicate the number of words in TX FIFO 0x0: 0 byte in TX FIFO 0x1: 1 byte in TX FIFO (p) 0x40: 64 bytes in TX FIFO other: Reserved
15	R	0x0	RB_WR RX FIFO Read Buffer Write Enable
14:8	/	/	/
7:0	R	0x0	RF_CNT RX FIFO Counter These bits indicate the number of words in RX FIFO + RX BUFFER 0x0: 0 byte in RX FIFO & RX BUFFER 0x1: 1 byte in RX FIFO & RX BUFFER (p) 0x64: 64 bytes in RX FIFO & RX BUFFER (p) 0xc0:192bytes in RX FIFO & RX BUFFER other: Reserved

18.8.8.7 0x0020 SPI Wait Clock Counter Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SPI_WCR
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0020			Register Name: SPI_WCR
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0x0	SWC Dual mode direction switch waits clock counter (for master mode only). 0: No wait states inserted n: n SPI_CLK wait states inserted Note: These bits control the number of wait states to be inserted before start dual data transfer in dual SPI mode. The SPI module counts SPI_CLK by SWC for delaying next word data transfer. *Note: This bit can t be written when XCH=1.*
15:0	R/W	0x0	WCC Wait Clock Counter (In Master mode) These bits control the number of wait states to be inserted in data transfers. The SPI module counts SPI_CLK by WCC for delaying next word data transfer. 0: No wait states inserted N: N SPI_CLK wait states inserted *Note: Can t be written when XCH=1.*

18.8.8.8 0x0028 SPI Sample Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0028			Register Name: SPI_SAMP_DL
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:8	R	0x20	Reserved
7	R/W	0x0	SAMP_DL_SW_EN Sample Delay Software Enable When set, enable sample delay specified at SAMP_DL_SW
6	/	/	/
5:0	R/W	0x0	SAMP_DL_SW Sample Delay Software The relative delay between clock line and command line, data lines. It can be determined according to the value of SAMP_DL, the cycle of card clock and device s input timing requirement.

18.8.8.9 0x0034 SPI Master Transmit Counter Register (Default Value: 0x0000_0000)

Offset: 0x0034	Register Name: SPI_MTC

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	MWTC Master Write Transmit Counter In master mode, this field specifies the burst number that should be sent to TXFIFO before automatically sending dummy burst. For saving bus bandwidth, the dummy burst (all zero bits or all one bits) is sent by SPI Controller automatically. 0: 0 burst 1: 1 burst (p) N: N bursts *Note: Can t be written when XCH=1.*

18.8.8.10 0x0038 SPI Master Burst Control Counter Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: SPI_BCC
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R/W	0x0	Quad_EN Quad_Mode_EN 0: Quad mode disable 1: Quad mode enable *Note:* *a) Can t be written when XCH=1.* *b) Quad mode includes Quad-Input and Quad-Output.*
28	R/W	0x0	DRM Master Dual Mode RX Enable 0: RX use single-bit mode 1: RX use dual mode *Note:* *a) Can t be written when XCH=1;* *b) It is only valid when Quad_Mode_EN=0.*

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0038			Register Name: SPI_BCC
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0x0	DBC Master Dummy Burst Counter In master mode, this field specifies the burst number that should be sent before receive in dual SPI mode. The data is don t care by the device. 0: 0 burst 1: 1 burst (p) N: N bursts *Note: Can t be written when XCH=1.*
23:0	R/W	0x0	STC Master Single Mode Transmit Counter In master mode, this field specifies the burst number that should be sent in single mode before automatically sending dummy burst. This is the first transmit counter in all bursts. 0: 0 burst 1: 1 burst (p) N: N bursts *Note: Can t be written when XCH=1.*

18.8.8.11 0x0040 SPI Bit-Aligned Transfer Configure Register (Default Value: 0x0000_00A0)

Offset: 0x0040			Register Name: SPI_BATCR
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	TCE Transfer Control Enable In master mode, it is used to start t1o transfer the serial bit s frame, it is only valid when Work Mode Select==0x10/0x11. 0: Idle 1: Initiates transfer. Write 1 to this bit will start to transfer serial bits frame (the value comes from the SPI TX Bit Register or SPI RX Bit Register), and will auto clear after the bursts transfer completely. Write 0 to this bit has no effect.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0040			Register Name: SPI_BATCR
Bit	Read/Write	Default/Hex	Description
30	R/W	0x0	MSMS Master Sample Standard 0: Standard Sample Mode 1: Delay Sample Mode In Standard Sample Mode, SPI master samples the data at the standard rising edge of SCLK for each SPI mode; In Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the standard rising edge of SCLK defined in respective SPI mode.
29:26	/	/	/
25	R/W1C	0x0	TBC Transfer Bits Completed When set, this bit indicates that the last bit of the serial data frame in SPI TX Bit Register (or SPI RX Bit Register) has been transferred completely. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed *Note: It is only valid when Work Mode Select is 0x10/0x11.*
24	R/W	0x0	TBC_INT_EN Transfer Bits Completed Interrupt Enable 0: Disable 1: Enable *Note: It is only valid when Work Mode Select is 0x10/0x11.*
23:22	/	/	/
21:16	R/W	0x00	RX_FEM_LEN Configure the length of serial data frame(burst) of RX 0x0: 0bit 0x1: 1bit (p) 0x20: 32bits Other values: reserved *Note: It is only valid when Work Mode Select==0x10/0x11, and can t be written when TCE=1.*
15:14	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0040			Register Name: SPI_BATCR
Bit	Read/Write	Default/Hex	Description
13:8	R/W	0x00	TX_FRM_LEN Configure the length of serial data frame(burst) of TX 000000: 0bit 000001: 1bit (p) 100000: 32bits Other values: reserved *Note: It is only valid when Work Mode Select==0x10/0x11, and can t be written when TCE=1.*
7	R/W	0x1	SS_LEVEL When control SS signal manually, set this bit to 1 or 0 to control the level of SS signal. 0: set SS to low 1: set SS to high *Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can t be written when TCE=1.*
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software *Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can t be written when TCE=1.*
5	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) *Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can t be written when TCE=1.*
4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0040			Register Name: SPI_BATCR
Bit	Read/Write	Default/Hex	Description
3:2	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_CS0 will be asserted 01: SPI_CS1 will be asserted 10: SPI_CS2 will be asserted 11: SPI_CS3 will be asserted *Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can t be written when TCE=1.*
1:0	R/W	0x0	*WMS* *Work Mode Select* 00: Data frame is byte aligned in Standard SPI, Dual-Output/Dual Input SPI, Dual IO SPI and Quad-Output/Quad-Input SPI. 01: Reserve 10: Data frame is bit aligned in 3-Wire SPI 11: Data frame is bit aligned in Standard SPI

18.8.8.12 0x0044 SPI Bit-Aligned CLOCK Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: SPI_BA_CCR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	CDR_N Clock Divide Rate (Master Mode Only) The SPI_CLK is determined according to the following equation: SPI_CLK = Source_CLK / (2*(CDR_N + 1)). *Note: It is only valid when Work Mode Select =0x10/0x11*

18.8.8.13 0x0048 SPI TX Bit Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: SPI_TBR
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0048			Register Name: SPI_TBR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VTB The Value of the Transmit Bits This register is used to store the value of the transmitted serial data frame. *Note:* *a) In the process of transmission, the LSB is transmitted first.* *b) This register is only valid when Work Mode Select==0x10/0x11.*

18.8.8.14 0x004C SPI RX Bit Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: SPI_RBR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VRB The Value of the Receive Bits This register is used to store the value of the received serial data frame. *Note:* *a) In the process of transmission, the LSB is transmitted first.* *b) This register is only valid when Work Mode Select==0x10/0x11.*

18.8.8.15 0x0088 SPI Normal DMA Mode Control Register (Default Value: 0x0000_00E5)

Offset: 0x0088			Register Name: SPI_NDMA_MODE_CTL
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:6	R/W	0x3	SPI_ACT_M SPI NDMA Active Mode 00: DMA_active is low 01: DMA_active is high 10: DMA_active is controlled by dma_request(DRQ) 11:DMA_active is controlled by controller
5	R/W	0x1	SPI_ACK_M SPI NDMA Acknowledge Mode 0: active fall do not care ACK 1: active fall must after detect ACK is high

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0088			Register Name: SPI_NDMA_MODE_CTL
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x05	SPI_DMA_WAIT The counts of hold cycles from DMA last signal high to dma_active high

18.8.8.16 0x0200 SPI TX Data Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: SPI_TXD
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TDATA Transmit Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are rooms in TXFIFO, one burst data is written to TXFIFO and the depth is increased by 1. In half-word accessing method, two SPI burst data are written and the TXFIFO depth is increase by 2. In word accessing method, four SPI burst data are written and the TXFIFO depth is increased by 4. *Note: This address is write-only if TF_TEST is 0, and if TF_TEST is set to 1, this address is readable and writable to test the TX FIFO through the AHB bus.*

18.8.8.17 0x0300 SPI RX Data Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: SPI_RXD
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RDATA Receive Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are data in RXFIFO, the top word is returned and the RXFIFO depth is decreased by 1. In half-word accessing method, two SPI bursts are returned and the RXFIFO depth is decrease by 2. In word accessing method, the four SPI bursts are returned and the RXFIFO depth is decreased by 4. *Note: This address is read-only if RF_TEST is 0, and if RF_TEST is set to 1, this address is readable and writable to test the RX FIFO through the AHB bus.*

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.8.8.18 0x0400 SPI BUF Status Register (Default Value: 0x0000_0000)

Offset: 0x0400			Register Name: SPI_BSR
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:24	R	0x0	TX_SHIFT_BUFFER_CNT TX SHIFT Buffer Counter These bits indicate the number of bytes in TX Shift Buffer, which is after TX FIFO, and maximum depth is 4 level with 8 bits.
23:19	/	/	/
18:16	R	0x0	TB_CNT TX FIFO Write Buffer Counter These bits indicate the number of words in TX FIFO Write Buffer
15:8	/	/	/
7:0	R	0x0	RB_CNT RX FIFO Read Buffer Counter These bits indicate the number of words in RX FIFO Read Buffer

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.9 SPI_DBI

18.9.1 Overview

The SoC provides a 3/4 line SPI display bus interface (SPI_DBI) for video data transmission. It supports DBI mode or SPI mode. The DBI mode can be configured with 3-wire/4-wire transmission and compatible with multiple video data formats at the same time. The integrated SPI mode is used for low-cost display schemes.

The SPI mode has the following features:

- Supports multiple SPI mode
  - Master mode and Slave mode Standard SPI (4wire)
  - Master mode Dual-Output/Dual-Input SPI/ Dual I/O SPI
  - Master mode Quad-Output/Quad-Input SPI
  - Master mode 3wire SPI, with programmable serial data frame length: 1bit to 32bits
- Supports the Maximum clock frequency: 100MHz
- Supports TX/RX DMA Slave interface
- Transmits data FIFO with 8-bit wide and 64-entry
- Receives data FIFO with 8-bit wide and 64-entry
- Transmits data buffer with 8-bit wide and 4-entry
- Receives data buffer with 8-bit wide and 128-entry
- Supports Data Sample Mode: Mode0, Mode1, Mode2 and Mode3
- Supports Control signal config
  - Two chip selects to support multiple peripherals
  - Polarity and phase of the Chip Select (SPI_CS) and SPI Clock (SPI_CLK) are configurable

The DBI mode has the following features:

- Supports DBI Type C 3 Line/4 Line Interface Mode
- Supports 2 Data Lane Interface Mode
- Supports RGB111/444/565/666/888 video format
- Supports maximum resolution of RGB666 240 x 320@30Hz with single data lane
- Supports maximum resolution of RGB888 240 x 320@60Hz or 320 x 480@30Hz with dual data lane
- Supports tearing effect
- Supports software flexible control video frame rate

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

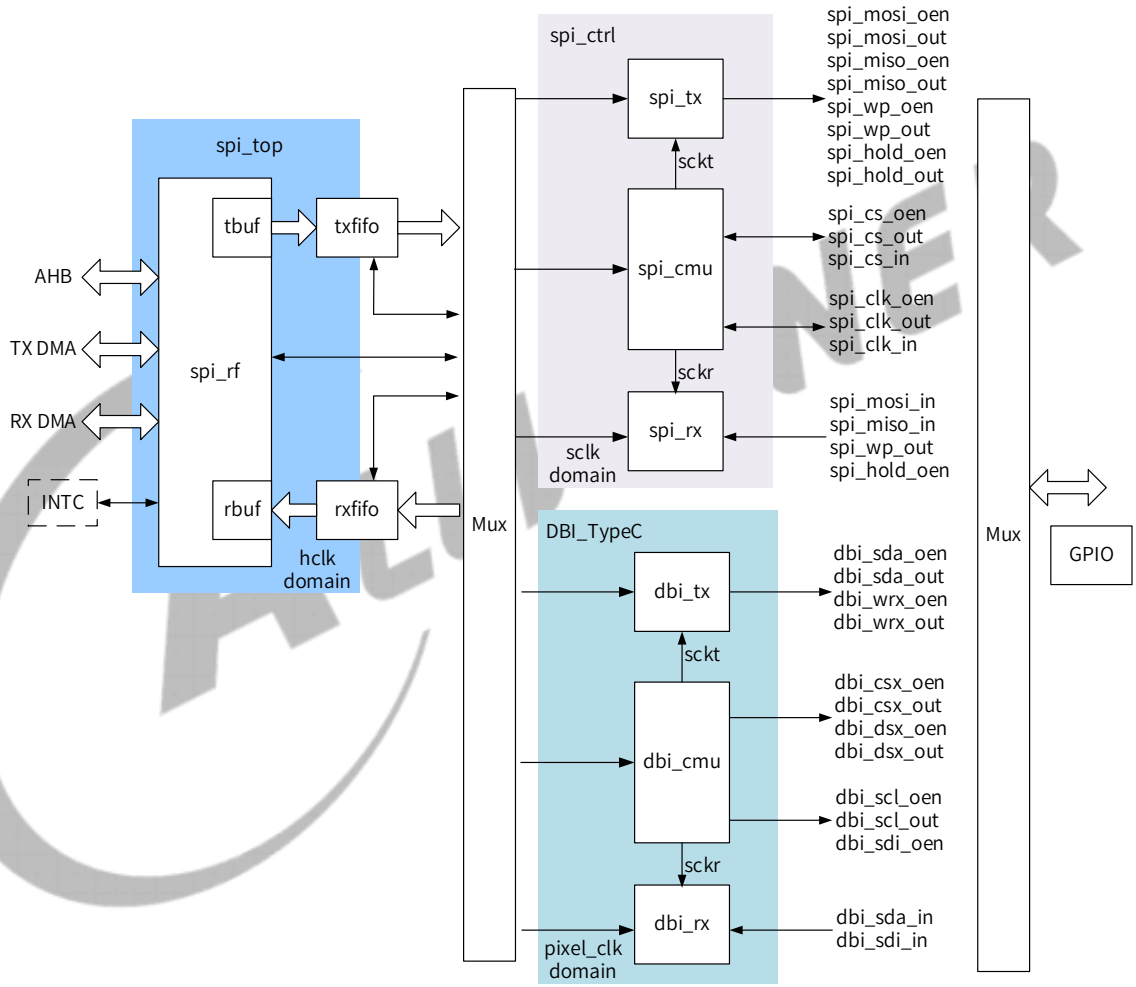
NOTE

This chapter only describes SPI1 (with SPI mode and DBI mode). For detailed information of SPI0, SPI2, SPI3, and S_SPI0, please refer to the section SPI.

18.9.2 Block Diagram

The following figure shows a block diagram of the SPI_DBI.

Figure 18-28 SPI_DBI Block Diagram



SPI_DBI contains the following sub-blocks:

Table 18-12 SPI_DBI Sub-blocks

Sub-block	Description
spi_rf	It is responsible for implementing the internal registers, interrupts, and DMA Requests.
spi_tbuf	The data length transmitted from AHB to TXFIFO is converted into 8 bits, then the data is written into the RXFIFO.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Sub-block	Description
spi_rbuf	The block is used to convert the RXFIFO data into the reading data length of AHB.
txfifo, rxfifo	The data transmitted from the SPI to the external serial device is written into the TXFIFO; the data received from the external serial device into SPI is pushed into the RXFIFO.
spi_cmu	It is responsible for implementing SPI bus clock, chip select, internal sample, and the generation of transfer clock.
spi_tx	It is responsible for implementing SPI data transfer, the interface of the internal TXFIFO, and status register.
spi_rx	It is responsible for implementing SPI data receive, the interface of the internal RXFIFO, and status register.
dbi_ctrl	It is responsible for implementing DBI bus clock, chip select, data command select, RGB format reshape.
dbi_tx	It is responsible for implementing DBI data transfer, the interface of the internal TXFIFO, and status register.
dbi_rx	It is responsible for implementing DBI data receive, the interface of the internal RXFIFO, and status register.

18.9.3 Clock Sources

he following table describes the clock sources of SPI_DBI. For clock setting, configurations, and gating information, refer to the section Clock Controller Unit (CCU).

Module	Clock Sources	Description
SPI1(SPI_DBI)	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.
	PERI0_300M	Its frequency is 300 MHz by default.
	PERI0_200M	Its frequency is 200 MHz by default.
	PERI1_300M	Its frequency is 300 MHz by default.
	PERI1_200M	Its frequency is 200 MHz by default.
	PERI0_480M	Its frequency is 480 MHz by default.
	PERI1_480M	Its frequency is 480 MHz by default.
	DCXO	The external high-frequency crystal oscillator. Its frequency is 26 MHz.

18.9.4 External Signals

The following table describes the external signals of SPI_DBI. When using SPI_DBI, the corresponding PADs are selected as SPI_DBI function via section GPIO.

Table 18-13 GPIO multiplexing of SPI1 and DBI

DBI	SPI1
DBI-CSX	SPI1-CS0
DBI-SCLK	SPI1-CLK

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

DBI	SPI1
DBI-SDO	SPI1-MOSI
DBI-SDI/ DBI-TE/ DBI-DCX	SPI1-MISO
DBI-DCX/DBI-WRX	SPI1-HOLD
DBI-TE	SPI1-WP

Table 18-14 SPI_DBI External Signals

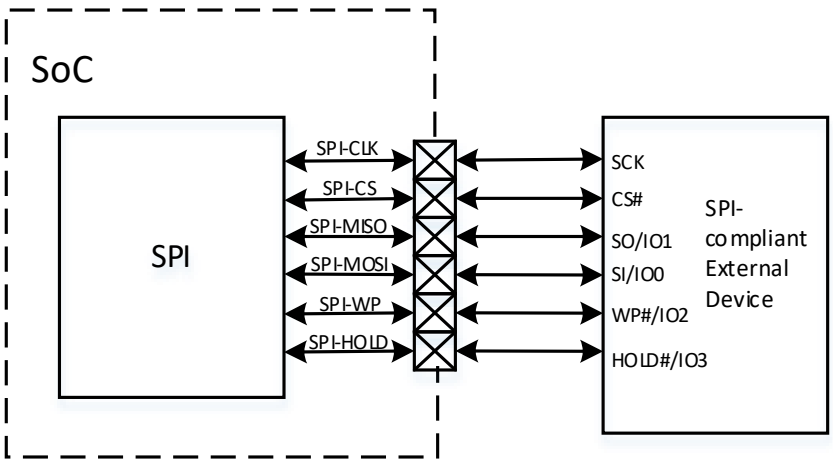
Signal Name	Description	Type
SPI Mode		
SPI1-CS[1:0]	SPI1 Chip Select Signal, Low Active	I/O
SPI1-CLK	SPI1 Clock Signal	I/O
SPI1-MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1-MISO	SPI1 Master Data In, Slave Data Out	I/O
SPI1-WP	SPI1 Write Protect, Low Active	I/O
SPI1-HOLD	SPI1 Hold Signal	I/O
DBI Mode		
DBI-CSX	Chip Select Signal, Low Active	I/O
DBI-SCLK	Serial Clock Signal	I/O
DBI-SDO	Data Output Signal	I/O
DBI-SDI	Data Input Signal	I/O
DBI-TE	Tearing Effect Input	I/O
DBI-DCX	DCX pin is the select output signal of data and command.	I/O
DBI-WRX	When DBI operates in dual data lane format, the RGB666 format 2 can use WRX to transfer data	I/O

18.9.5 Functional Description

18.9.5.1 Typical Application

The following figure shows the application block diagram when the SPI master device is connected to a slave device.

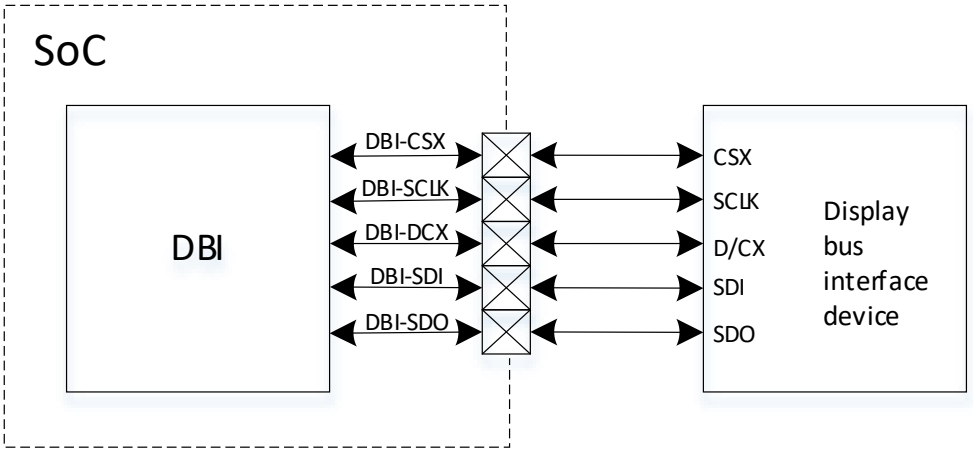
Figure 18-29 SPI Application Block Diagram



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

The following figure shows the application block diagram when the DBI master device is connected to a display bus interface device.

Figure 18-30 DBI Application Block Diagram



NOTE

For the function descriptions in SPI mode, refer to the section SPI.

18.9.5.2 DBI 3-Line Interface Write and Read Timing

DBI 3-Line Interface Write Timing

The 3-line DBI Interface I contains CSX, SDA, and SCL, where SDA shares this port for bidirectional port data input and output.

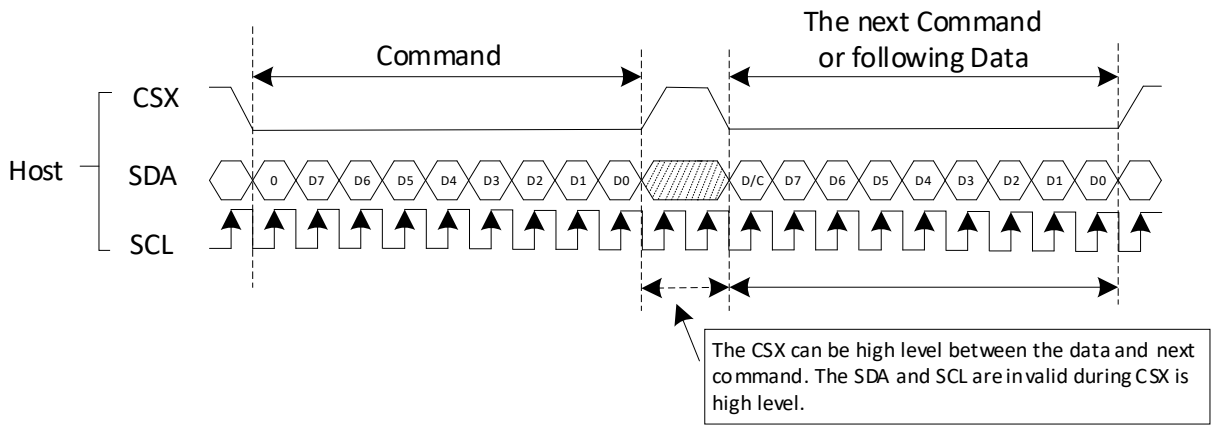
The 3-line DBI Interface II contains CSX, SDA, SCL, and SDI; Data input and output ports are independent of each other.

As there is no Data/Command data line in the 3-line display bus mode, whether Data or Command is currently being transmitted cannot be confirmed. Thus, an extra bit is added to the data-stream before MSB to indicate whether Data or Command is currently being transmitted. (0: Command, 1: Data)

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

The following figure shows the write operation format of 3-line DBI Interface I and Interface II.

Figure 18-31 DBI 3-Line Display Bus Serial Interface Write Operation Format

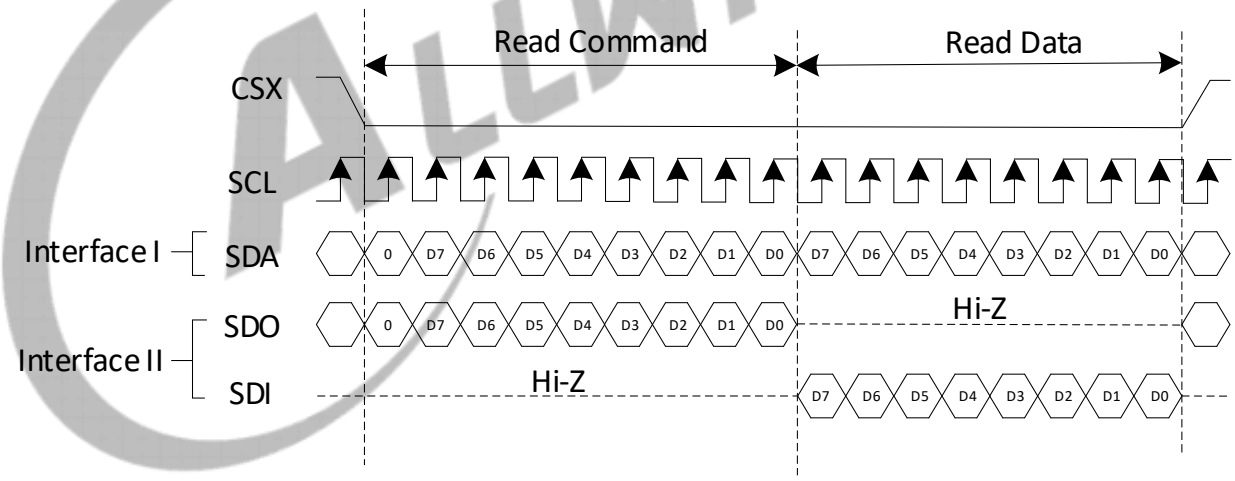


DBI 3-Line Interface Read Timing

The 3-line DBI Interface I uses the SDA port as bidirectional data input and output port. There are only three cases of data reading volume, 8bits/24bits/32bits, and the first data sampled is high.

The following figure shows the 8 bits read operation format of 3-line DBI Interface I and Interface II. After the read command is transmitted, the data is read immediately with no dummy period.

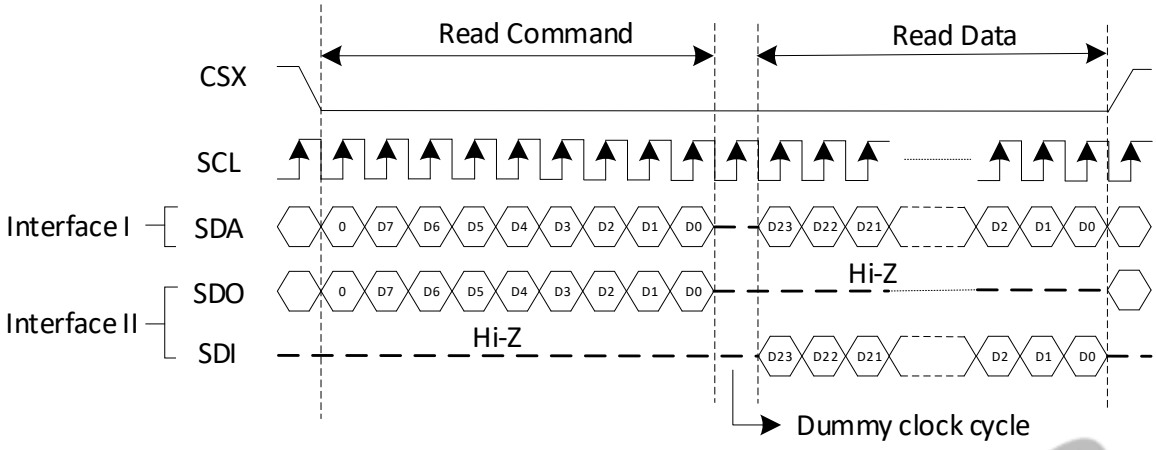
Figure 18-32 DBI 3-Line Display Bus Serial Interface 8-bit Read Operation Format



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

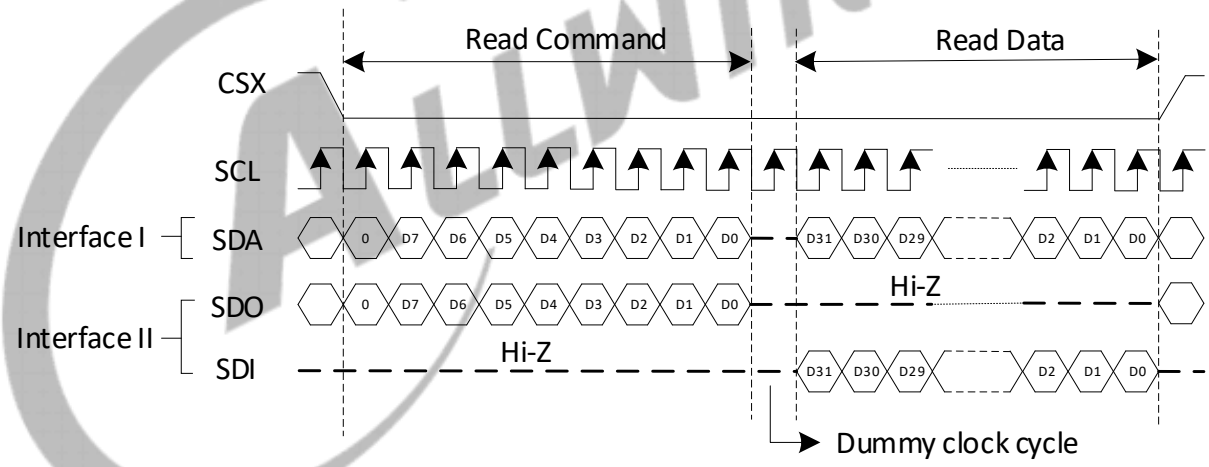
The following figure shows the 24 bits read operation format of 3-line DBI Interface I and Interface II. When the read command is transmitted, the data will be read after the dummy clock cycle.

Figure 18-33 DBI 3-Line Display Bus Serial Interface 24-bit Read Operation Format



The following figure shows the 32 bits read operation format of 3-line DBI Interface I and Interface II. When the read command is transmitted, the data will be read after the dummy clock cycle.

Figure 18-34 DBI 3-Line Display Bus Serial Interface 32-bit Read Operation Format



18.9.5.3 DBI 4-Line Interface Write and Read Timing

DBI 4-Line Interface Write Timing

The 4-line DBI Interface I contains CSX, D/CX, SDA, and SCL, where SDA shares this port for bidirectional port data input and output.

The 4-line DBI Interface II contains CSX, D/CX, SDA, SCL, and SDI; Data input and output ports are independent of each other.

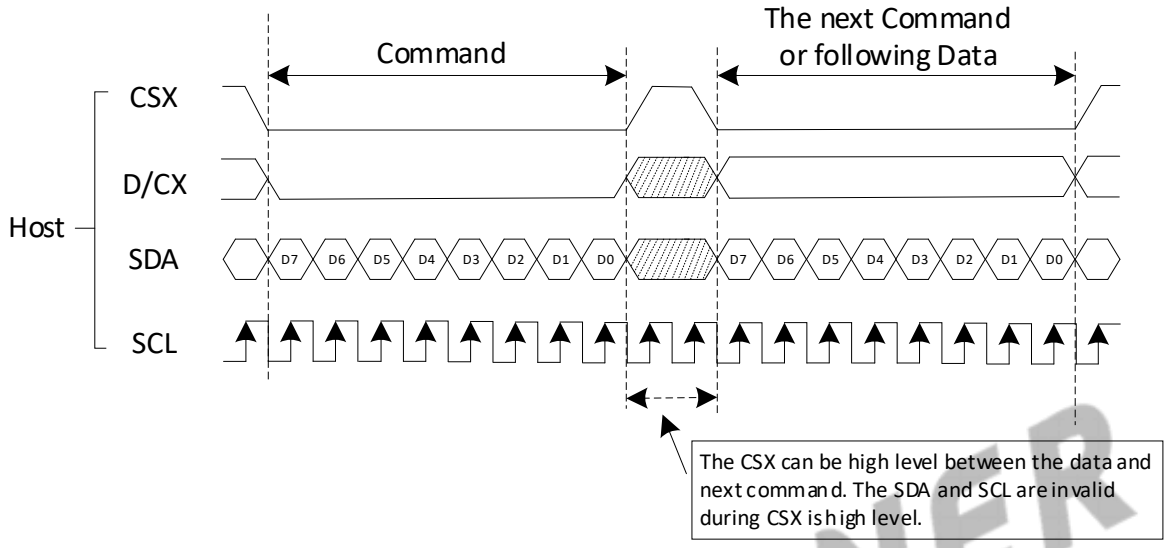
Since the 4-line display bus mode has a Data/Command data line indicating whether Data or Command is currently being transmitted (0: Command, 1: Data). So there is no need to add an extra bit to data-stream before MSB like the 3-line DBI.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

There is a Data/Command data line in the 4-line display bus mode to indicate whether Data or Command is currently being transmitted. (0: Command, 1: Data) Thus, no extra bit is needed.

The following figure shows the writing operation format of 4-line DBI Interface I and Interface II.

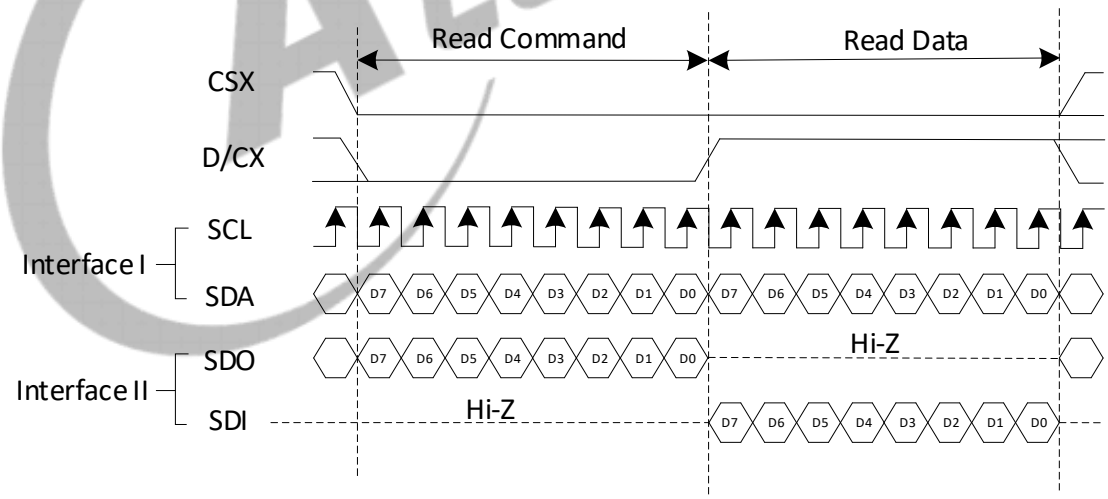
Figure 18-35 DBI 4-Line Display Bus Serial Interface Write Operation Format



DBI 4-Line Interface Read Timing

The following figure shows the 8 bits read operation format of 4-line DBI Interface I and Interface II.

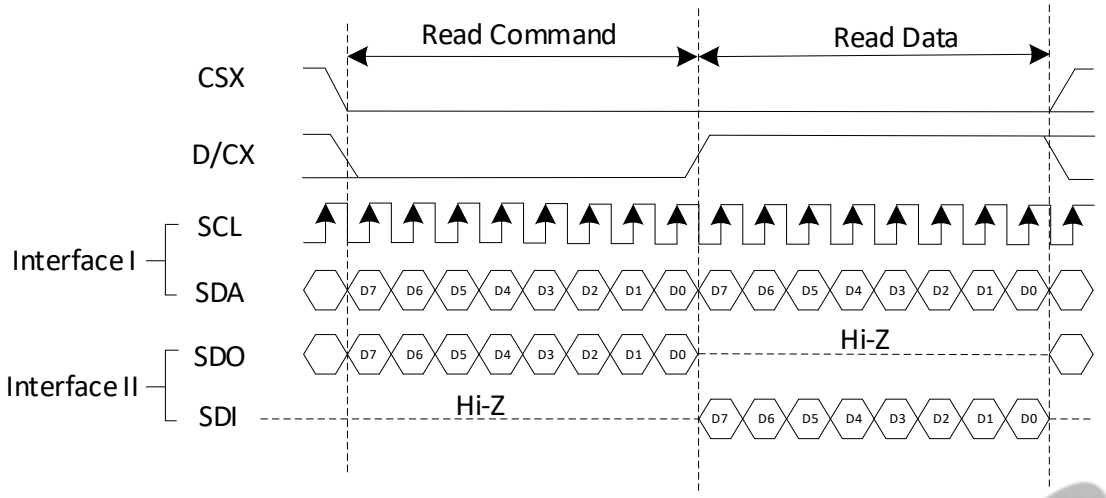
Figure 18-36 DBI 4-Line Display Bus Serial Interface 8-bit Read Operation Format



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

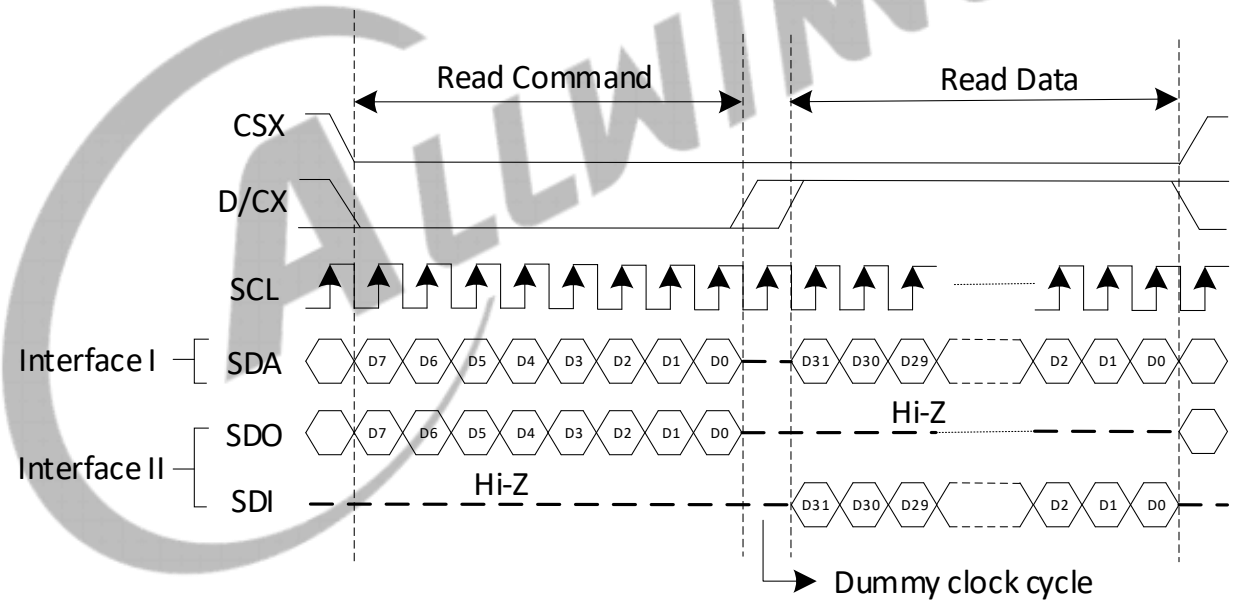
The following figure shows the 24 bits read operation format of 4-line DBI Interface I and Interface II.

Figure 18-37 DBI 4-Line Display Bus Serial Interface 24-bit Read Operation Format



The following figure shows the 32 bits read operation format of 4-line DBI Interface I and Interface II.

Figure 18-38 DBI 4-Line Display Bus Serial Interface 32-bit Read Operation Format



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.9.5.4 DBI 3-Line Interface Transmit Video Format

Figure 18-39 RGB111 3-Line Interface Transmit Video Format

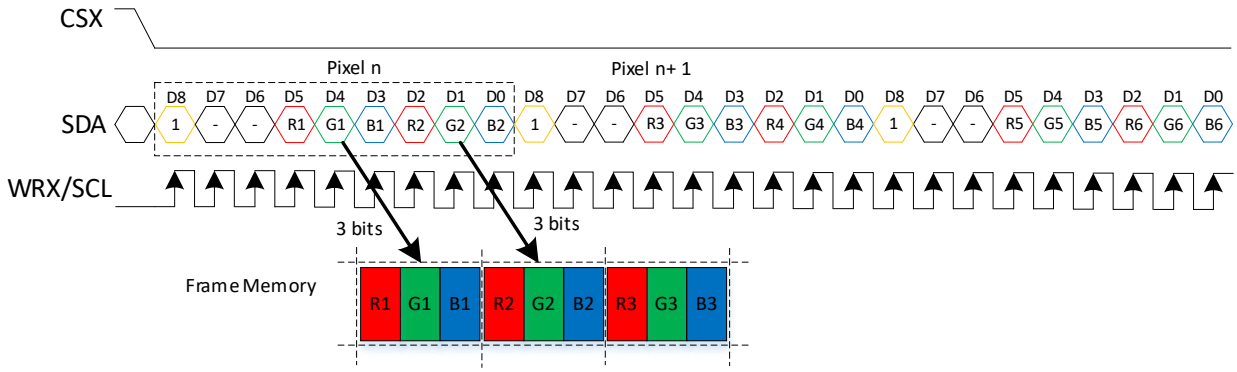
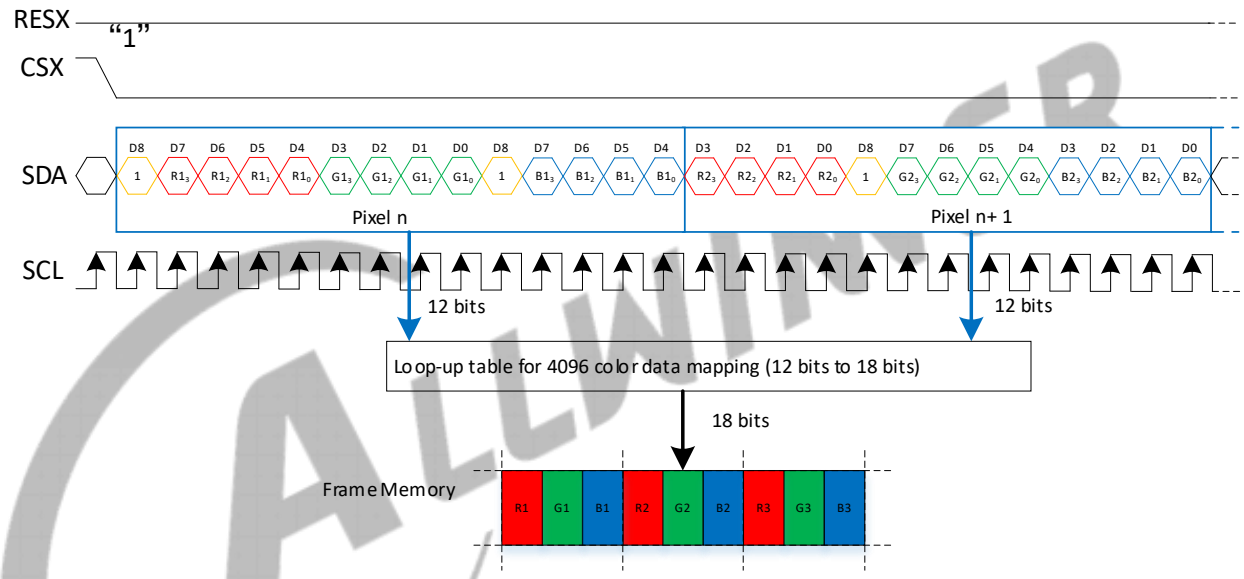


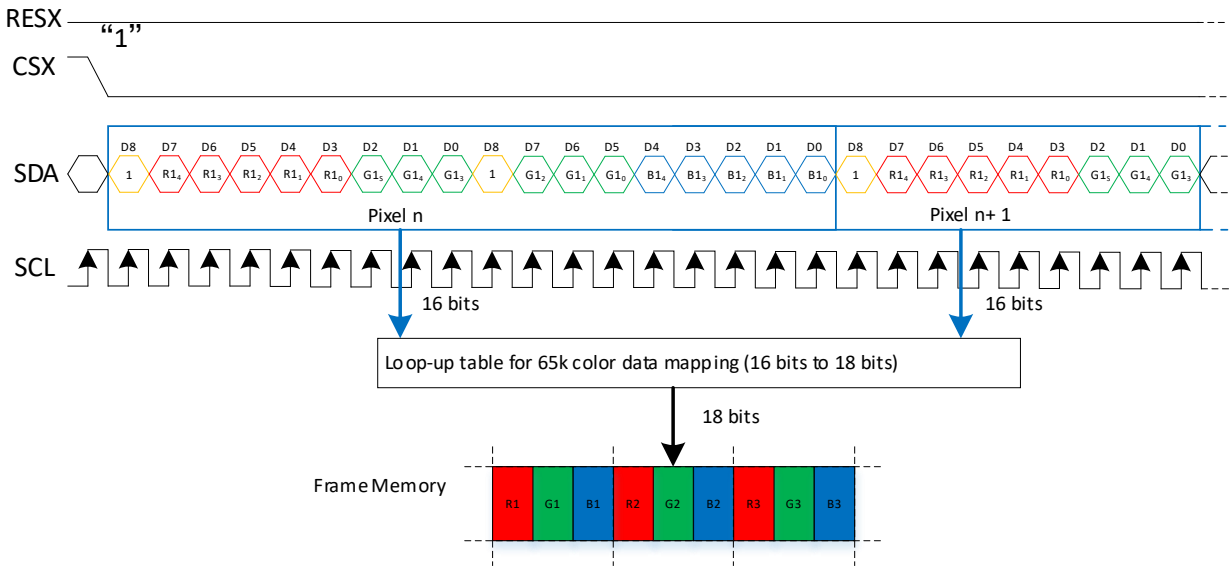
Figure 18-40 RGB444 3-Line Interface Transmit Video Format



Note 1. Pixel data with 12-bit color depth information
Note 2. The most significant bits are: Rx3, Gx3 and Bx3
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

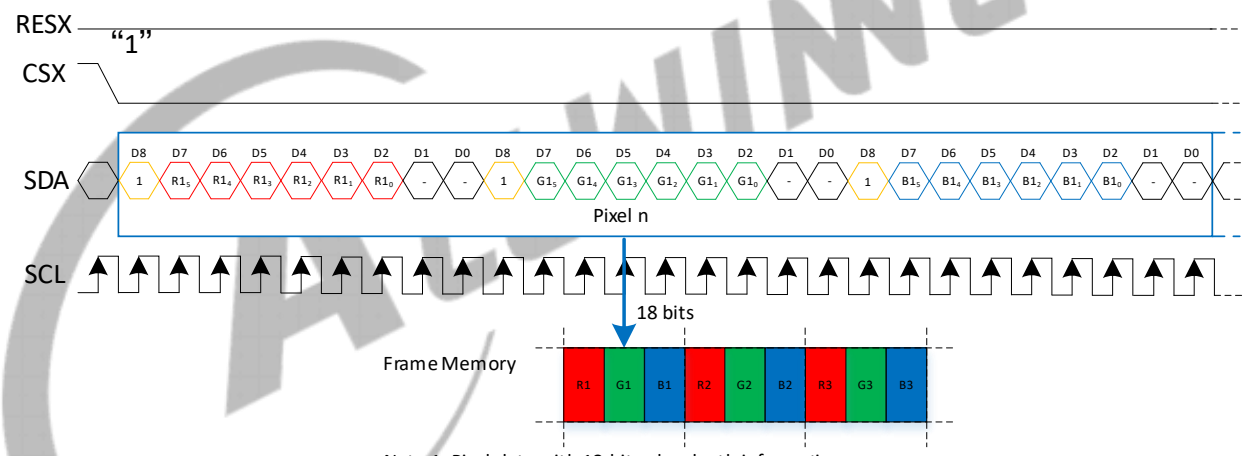
Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 18-41 RGB565 3-Line Interface Transmit Video Format



Note 1. Pixel data with 16-bit color depth information
Note 2. The most significant bits are: Rx4, Gx5 and Bx4
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Figure 18-42 RGB666 3-Line Interface Transmit Video Format



Note 1. Pixel data with 18-bit color depth information
Note 2. The most significant bits are: Rx5, Gx5 and Bx5
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.9.5.5 DBI 4-Line Interface Transmit Video Format

Figure 18-43 RGB111 4-Line Interface Transmit Video Format

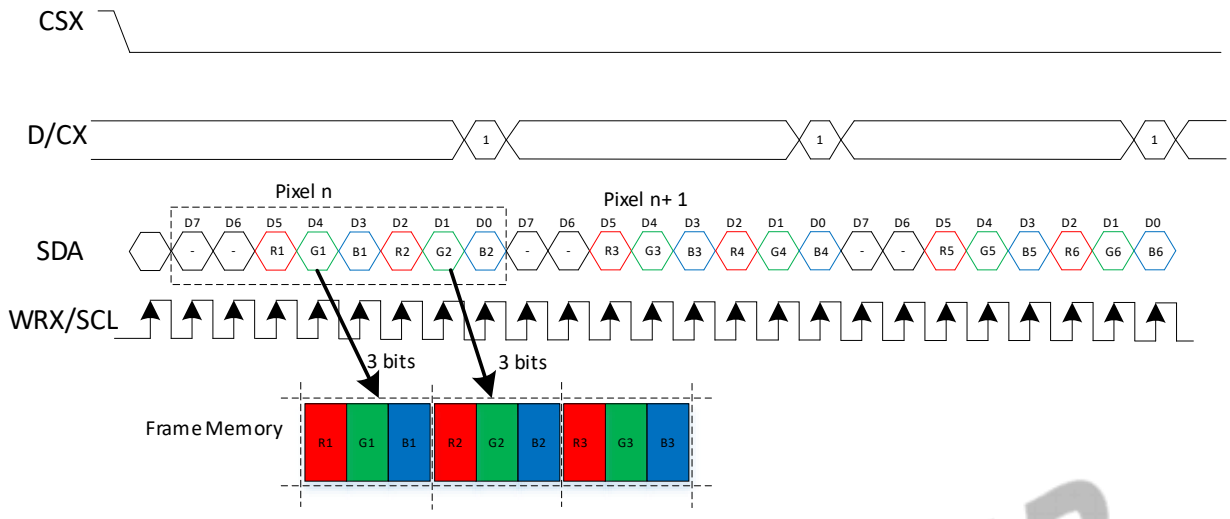
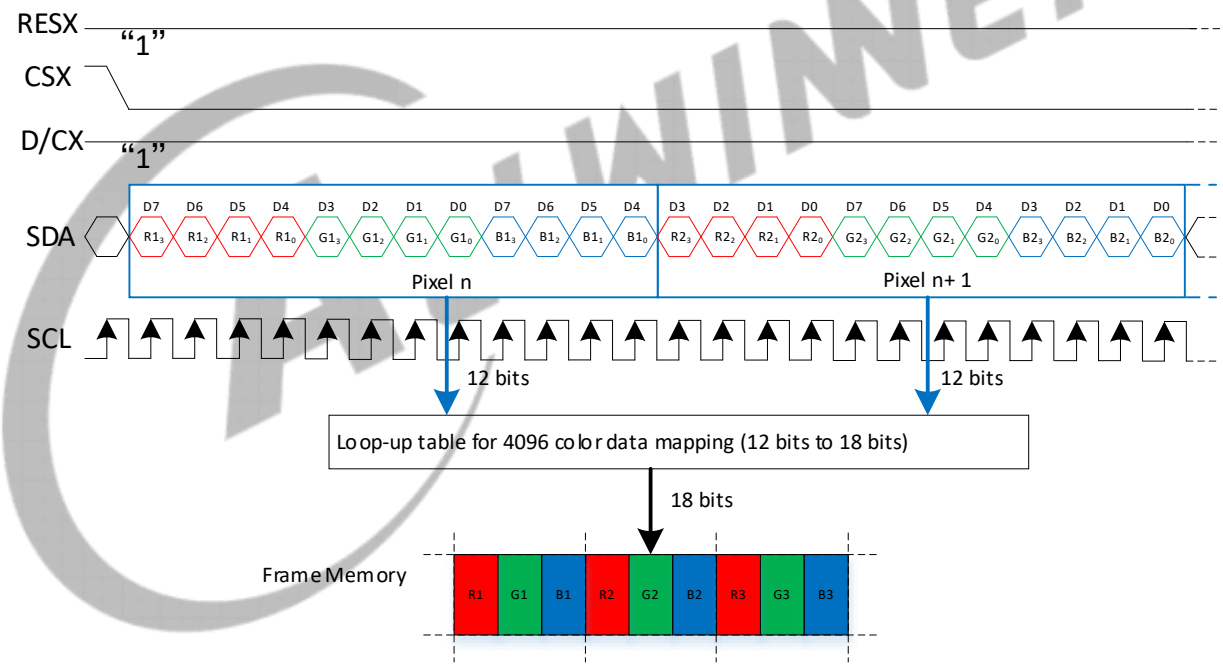


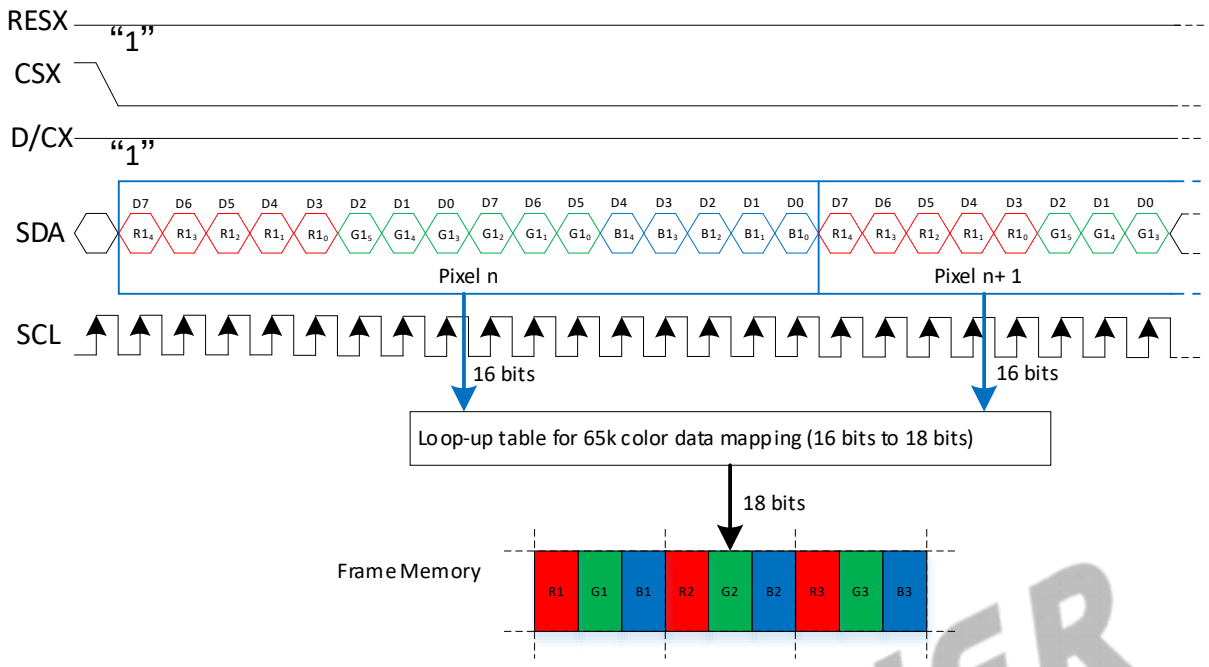
Figure 18-44 RGB444 4-Line Interface Transmit Video Format



Note 1. Pixel data with 12-bit color depth information
Note 2. The most significant bits are: Rx3, Gx3 and Bx3
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

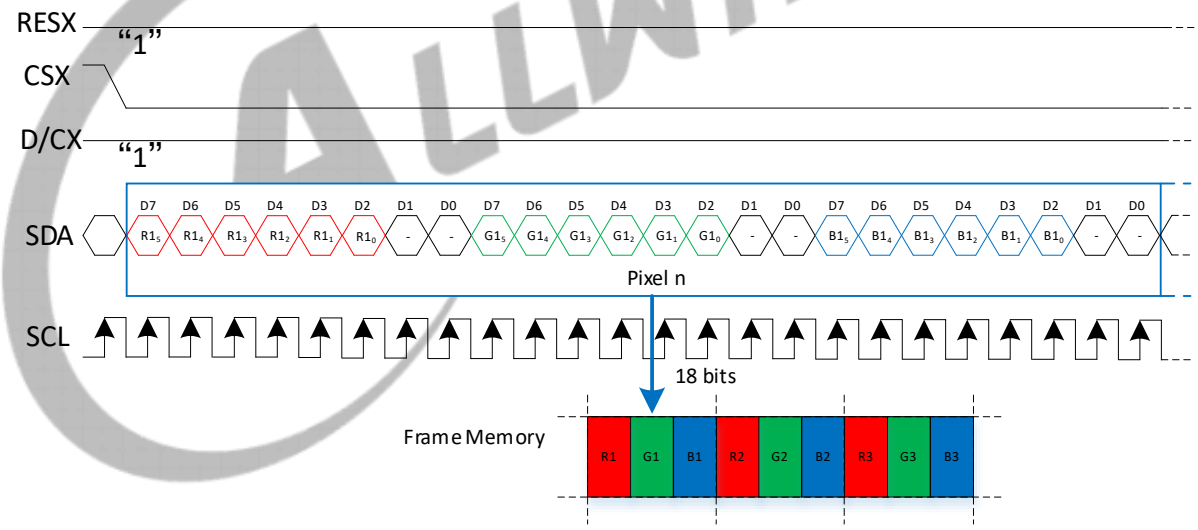
Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 18-45 RGB565 4-Line Interface Transmit Video Format



Note 1. Pixel data with 16-bit color depth information
Note 2. The most significant bits are: Rx4, Gx5 and Bx4
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Figure 18-46 RGB666 4-Line Interface Transmit Video Format

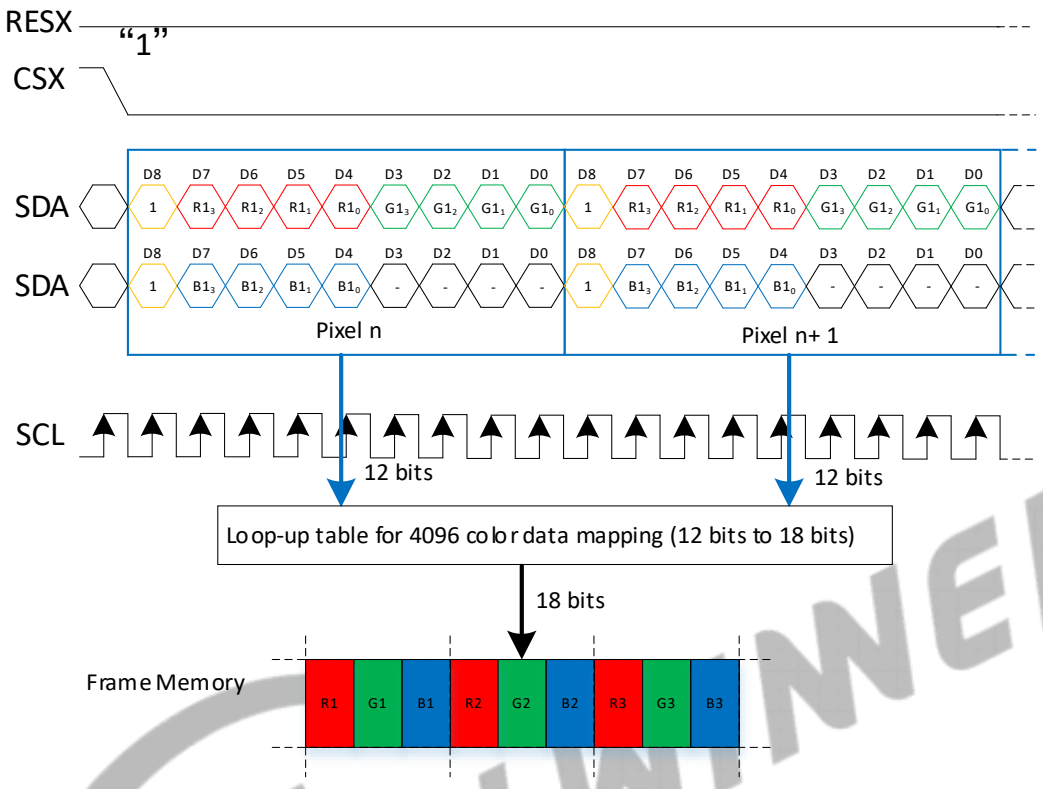


Note 1. Pixel data with 18-bit color depth information
Note 2. The most significant bits are: Rx5, Gx5 and Bx5
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.9.5.6 DBI 2 Data Lane Interface Transmit Video Format

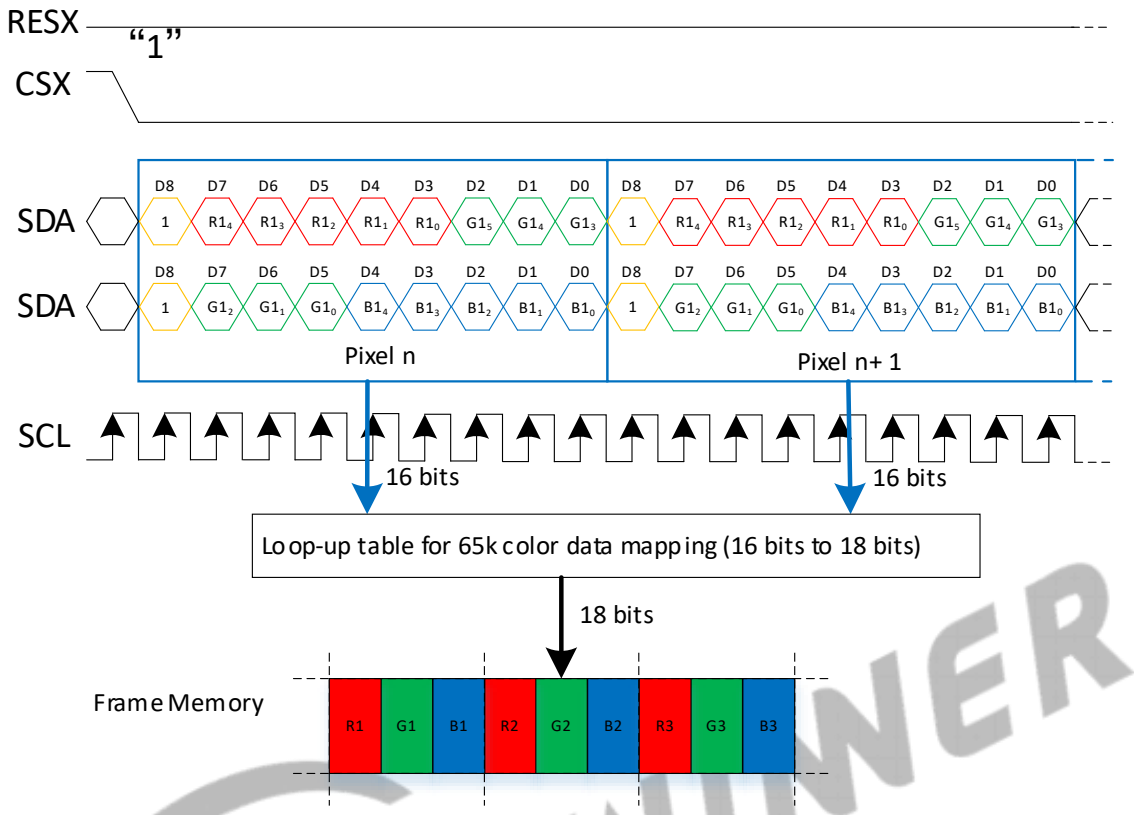
Figure 18-47 RGB444 2 Data Lane Interface Transmit Video Format



Note 1. Pixel data with 12-bit color information
Note 2. The most significant bits are: Rx3, Gx3 and Bx3
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

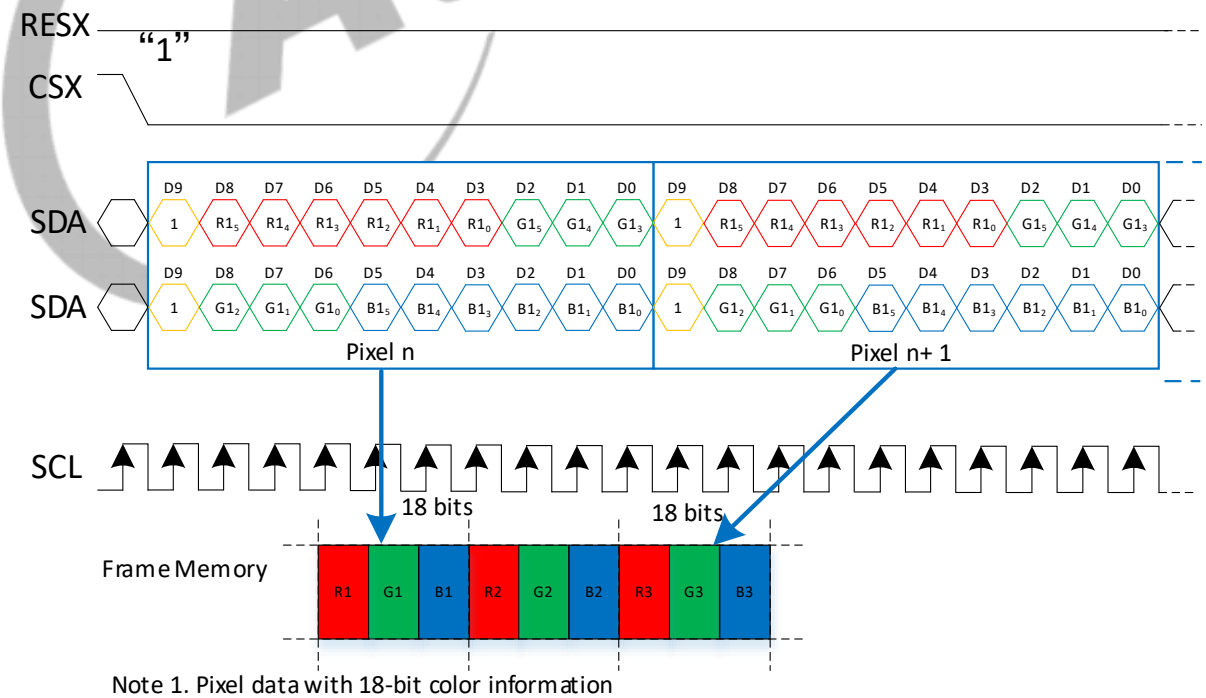
Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 18-48 RGB565 2 Data Lane Interface Transmit Video Format



Note 1. Pixel data with 16-bit color information
Note 2. The most significant bits are: Rx4, Gx5 and Bx4
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Figure 18-49 RGB666 2 Data Lane Interface Transmit Video Format 0



Note 1. Pixel data with 18-bit color information
Note 2. The most significant bits are: Rx5, Gx5 and Bx5
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 18-50 RGB666 2 Data Lane Interface Transmit Video Format 1 (ilitek)

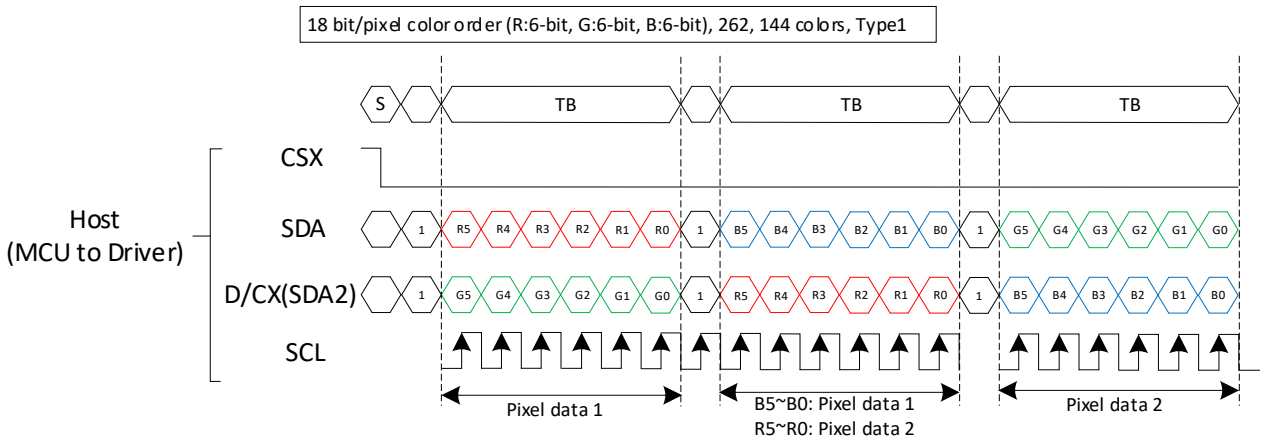


Figure 18-51 RGB666 2 Data Lane Interface Transmit Video Format 2 (New vision)

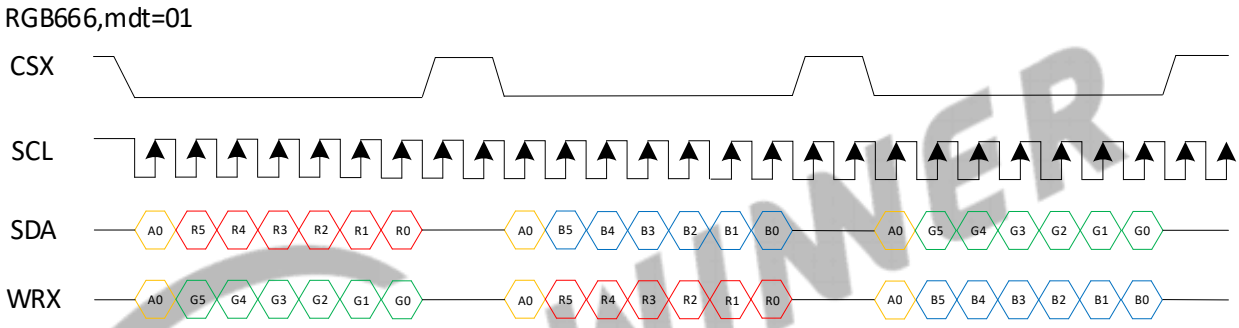
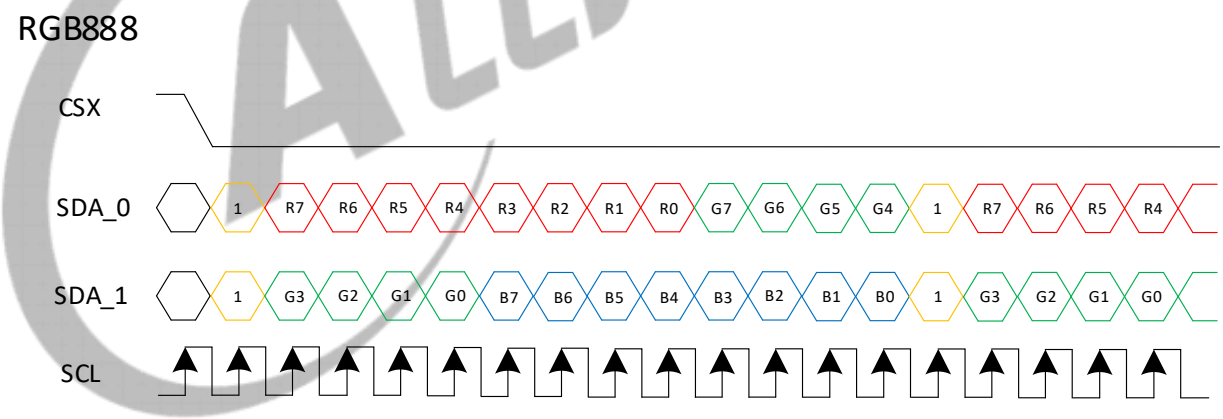


Figure 18-52 RGB888 2 Data Lane Interface Transmit Video Format



Note 1. Pixel data with 24-bit color information
Note 2. The most significant bits are: R7, G7 and B7
Note 3. The least significant bits are: R0, G0 and B0

18.9.5.7 SPI_DBI Clock Frequency

The equation of SPI_DBI clock frequency is

f_{SPI_CLK} = frame_rate * one_pixel_clock_cycle * one_frame_pixel_value

The meaning of each sub-item is as follows:

- frame_rate: The frame rate at the unit of Hz.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- one_pixel_clock_cycle: The clock period cycle of transferring a pixel. The period cycle differs from different transferring format.
  - 2-data lane-RGB444: 9 cycles
  - 2-data lane-RGB565: 9 cycles
  - 2-data lane-RGB666-Format0: 10 cycles
  - 2-data lane-RGB888: 13 cycles
- one_frame_pixel_value: The number of pixel in one frame.
  - 240*320
  - 320*480

For example, RGB data is transferred with 2 data line and RGB666 mode, and the resolution and frame rate of the display are 240*320 and 60Hz, then the SPI clock frequency is 60*10*240*320=46.08MHz.

The following tables show the SCLK frequency in different RGB modes.

Table 18-15 2 Data Lane SCLK Frequency

2 data lane					
RGB	Frame	30Hz		60Hz	
	Resolution	240*320	320*480	240*320	320*480
RGB111		/	/	/	/
RGB444		20.736	41.472	41.472	82.944
RGB565		20.736	41.472	41.472	82.944
RGB666		23.04	46.08	46.08	92.16
RGB888		29.952	59.904	59.904	/

Table 18-16 3 Line SCLK Frequency

3 line					
RGB	Frame	30Hz		60Hz	
	Resolution	240*320	320*480	240*320	320*480
RGB111		10.368	20.736	20.736	41.472
RGB444		31.104	62.208	62.208	/
RGB565		41.472	82.944	82.944	/
RGB666		62.208	/	/	/
RGB888		/	/	/	/

Table 18-17 4 Line SCLK Frequency

4 line					
	Frame	30Hz		60Hz	
RGB	Resolution	240*320	320*480	240*320	320*480
RGB111		9.216	18.432	18.432	36.864
RGB444		27.648	55.296	55.296	/
RGB565		36.864	73.728	73.728	/
RGB666		55.296	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

RGB888	/	/	/	/

18.9.6 Programming Guidelines

NOTE

The following are the programming guidelines in DBI mode. For those in SPI mode, see the section SPI.

18.9.6.1 Write Command Transfer

Step 1 Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.

Step 2 Set the DBI_EN_MODE_SEL (bit[30:29]) of DBI_CTL_1 (0x0104) to 0 to select the trigger mode of DBI.

Step 3 Configure the DBI_CTL_0 (0x0100).

a) Set DBI_CTL_0[Command Type] (bit31) to 0 to configure the writing command.

b) Set DBI_CTL_0[Write Command Dummy Cycles] (bit[30:20]) to configure the number of dummy cycles between commands.

c) Set DBI_CTL_0[Output Data Sequence] (bit19) to select the MSB or LSB.

d) Set DBI_CTL_0[Transmit Mode] (bit15) to 0 to select the command path.

e) Set DBI_CTL_0[Output Data Format] (bit[14:12]) to 0 to transmit the command.

f) Set DBI_CTL_0[DBI interface Select] (bit[10:8]) to select the DBI interface type.

g) The remaining values of the DBI_CTL_0 register remain the default value.

Step 4 Set DBI_CTL_1[DCX_DATA] (bit22) to 0 to send the command.

Step 5 DMA Path: Configure the SPI_FCR register (0x0018).

a) Set SPI_FCR[TF_DRQ_EN] (bit24) to 1 to enable TXFIFO DMA.

b) Set SPI_FCR[TX_TRIG_LEVEL] (bit[23:16]) to 255. It indicates the controller requests data from DMA if the remaining space of TX FIFO is greater than 255.

CPU Path: Write the command to be sent to the 0x200 address.

Step 6 Set SPI_GCR[DBI_EN] (bit4) to 1 to start transmitting the command.

Step 7 Wait until the TX FIFO underrun interrupt (SPI_ISR[TF_UDF]) is 1. It indicates that the command written to the TX FIFO is transmitted completely.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.9.6.2 Parameter Transfer

Step 1 Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.

Step 2 Set the DBI_EN_MODE_SEL (bit[30:29]) of DBI_CTL_1 (0x0104) to 0 to select the trigger mode of DBI.

Step 3 Configure the DBI_CTL_0 register (0x0100).

a) Set DBI_CTL_0[Command Type] (bit31) to 0 to configure the writing command.

b) Set DBI_CTL_0[Write Command Dummy Cycles] (bit[30:20]) to configure the number of dummy cycles between commands.

c) Set DBI_CTL_0[Output Data Sequence] (bit19) to select the MSB or LSB.

d) Set DBI_CTL_0[Transmit Mode] (bit15) to 0 to select the command path.

e) Set DBI_CTL_0[Output Data Format] (bit[14:12]) to 0 to transmit the command.

f) Set DBI_CTL_0[DBI interface Select] (bit[10:8]) to select the DBI interface type.

g) The remaining values of the DBI_CTL_0 register remain the default value.

Step 4 Set DBI_CTL_1[DCX_DATA] (bit22) to 1 to send the parameter.

Step 5 DMA Path: Configure the SPI_FCR register (0x0018).

a) Set SPI_FCR[TF_DRQ_EN] (bit24) to 1 to enable TXFIFO DMA.

b) Set SPI_FCR[TX_TRIG_LEVEL] (bit[23:16]) to 255. It indicates the controller requests data from DMA if the remaining space of TX FIFO is greater than 255.

CPU Path: Write the command to be sent to the 0x200 address.

Step 6 Set SPI_GCR[DBI_EN] (bit4) to 1 to start transmitting the command.

Step 7 Wait until the TX FIFO underrun interrupt (SPI_ISR[TF_UDF]) is 1. It indicates that the command written to the TX FIFO is transmitted completely.

18.9.6.3 Video Transfer

Before the video transmission configuration, confirm whether the data is from CPU path or DMA path.

a) If the data is from the CPU path, the controller writes the command to be sent to the 0x0200 address by the AHB bus.

b) If the data is from the DMA path, configure DBI_CTL_2[DBI_FIFO_DRQ_EN] (bit15) to 1 and DBI_CTL_2[TX_TRIG_LEVEL] (bit[14:8]) to 64. The controller will request data from DMA if the remaining space of TX FIFO is greater than 64. The empty & full interrupts and the status bit of DBI FIFO can be configured in the DBI_INT and DBI_DEBUG_0.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Software Trigger Mode

The software enables DBI_en_trigger when the edge interrupt of TE is detected.

After transmitting a frame of image, the controller automatically clears the line_cnt, pixel_cnt and stops data transmission.

The operation process is as follows.

Step 1 Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.

Step 2 Set the DBI EN MODE SEL (bit[30:29]) of DBI_CTL_1 (0x0104) to 01 to select the software trigger mode.

Step 3 Configure the DBI_CTL_0 register (0x0100).

a) Set DBI_CTL_0[Command Type] (bit31) to 0 to set the writing command.

b) Set DBI_CTL_0[Write Command Dummy Cycles] (bit[30:20]) to configure the number of dummy cycles between commands.

c) Set DBI_CTL_0[Output Data Sequence] (bit19) to select the MSB or LSB.

d) Set DBI_CTL_0[Transmit Mode] (bit15) to 1 to select the image path.

e) Set DBI_CTL_0[Output Data Format] (bit[14:12]) to select RGB111/444/565/666/888.

f) Set DBI_CTL_0[DBI interface Select] (bit[10:8]) to select the DBI interface type.

g) The remaining values of the DBI_CTL_0 register remain the default value.

Step 4 Set DBI_CTL_1[DCX_DATA] (bit22) to 0 to send the image data.

Step 5 Configure DBI_Video_Size (0x110) according to the sent image size.

Step 6 Configure DBI_CTL_2 (0x0108) to set the TE-related parameter.

Step 7 Detect the TE interrupt of the DBI_INT (0x0120) register.

Step 8 Configure DBI_CTL_1[DBI_soft_trigger] to 1.

Timer Trigger Mode

The software configures timer_en to enable timer counting, and when the counter reaches the specified value, the DBI_EN automatically will be enabled to start data transmission.

After transmitting a frame of image, the controller will automatically clear the line_cnt, pixel_cnt, and stop data transmission.

The timer starts counting again. When the counter reaches the specified value, the controller automatically enables DBI_EN again until the software turns off the timer_en.

The operation process is as follows.

Step 1 Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.

Step 2 Set the DBI EN MODE SEL (bit30:29) of DBI_CTL_1 (0x0104) to 10 to select the timer trigger mode.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 3 Configure the DBI_CTL_0 register (0x0100).

a) Set DBI_CTL_0[Command Type] (bit31) to 0 to set the writing command.

b) Set DBI_CTL_0[Write Command Dummy Cycles] (bit[30:20]) to configure the number of dummy cycles between commands.

c) Set DBI_CTL_0[Output Data Sequence] (bit19) to select the MSB or LSB.

d) Set DBI_CTL_0[Transmit Mode] (bit15) to 1 to select the image path.

e) Set DBI_CTL_0[Output Data Format] (bit[14:12]) to select RGB111/444/565/666/888.

f) Set DBI_CTL_0[DBI interface Select] (bit[10:8]) to select the DBI interface type.

g) The remaining values of the DBI_CTL_0 register remain the default value.

Step 4 Set DBI_CTL_1[DCX_DATA] (bit22) to 0 to send the image data.

Step 5 Configure DBI_Video_Size (0x110) to transmit the image size.

Step 6 Configure the related parameter of DBI_Timer (0x10C).

TE Trigger Mode

When the edge changes of the TE are detected (The rising and falling edges are optional), the DBI_EN can be automatically enabled to start data transmission.

After transmitting a frame of image, the controller will automatically clear the line_cnt, pixel_cnt, and stop transmitting data.

When the edge changes of the TE are detected (The rising and falling edges are optional), the DBI_EN can be automatically enabled to restart data transmission until the software shuts down TE_EN or the screen no longer sends TE signals.

The operation process is as follows.

Step 1 Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.

Step 2 Set the DBI EN MODE SEL (bit30:29) of DBI_CTL_1 (0x0104) to 11 to select the TE Configure the DBI_CTL_0 register (0x0100).

Step 3 Set DBI_CTL_0[Command Type] (bit31) to 0 to set the writing command.

a) Set DBI_CTL_0[Write Command Dummy Cycles] (bit[30:20]) to configure the number of dummy cycles between commands.

b) Set DBI_CTL_0[Output Data Sequence] (bit19) to select the MSB or LSB.

c) Set DBI_CTL_0[Transmit Mode] (bit15) to 1 to select the image path.

d) Set DBI_CTL_0[Output Data Format] (bit[14:12]) to select RGB111/444/565/666/888.

e) Set DBI_CTL_0[DBI interface Select] (bit[10:8]) to select the DBI interface type.

f) The remaining values of the DBI_CTL_0 register remain the default value.

Step 4 Configure DBI_CTL_1[DCX_DATA] (bit22) to 0 to send the image data.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 5 Configure DBI_Video_Size (0x0110) to transmit the image size.

Step 6 Configure DBI_CTL_2 (0x0108) to set the TE-related parameter.

18.9.6.4 Read Command & Read Data Transfer

Step 1 Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.

Step 2 Set the DBI EN MODE SEL (bit[30:29]) of DBI_CTL_1 (0x0104) to 0.

Step 3 Configure the DBI_CTL_0 register (0x0100).

a) Set DBI_CTL_0[Command Type] (bit31) to 0 to set the reading command.

b) Set DBI_CTL_0[Output Data Sequence] (bit19) to select the MSB or LSB.

c) Set DBI_CTL_0[Transmit Mode] (bit15) to 0 to select the command path.

d) Set DBI_CTL_0[Output Data Format] (bit[14:12]) to 0.

e) Set DBI_CTL_0[DBI interface Select] (bit[10:8]) to select the DBI interface type.

f) The remaining values of the DBI_CTL_0 register remain the default value.

Step 4 Configure the DBI_CTL_1 register (0x0104).

a) Configure DBI_CTL_1[DCX_DATA] (bit22) to 0 to send the command.

b) Configure DBI_CTL_1[Read_MSB_First] (bit20) to select whether the first bit of the read data is the highest or lowest bit of data.

c) Configure DBI_CTL_1[Read Data Number of Bytes] to set the byte number to be read.

d) Configure DBI_CTL_1[Read Command Dummy Cycles] to set the dummy cycle between the read command and the read data. When the dummy cycle is complete, the data starts to be sampled.

Step 5 DMA Path: Configure the SPI_FCR register (0x0018).

a) Set SPI_FCR[RF_DRQ_EN] (bit8) to 1 to enable RXFIFO DMA.

b) Set SPI_FCR[RX_TRIG_LEVEL] (bit[7:0]) to 32, which indicates the controller requests receiving data from DMA if the data of the RX FIFO is greater than 64.

CPU Path: Read data in RX FIFO from the 0x0300 address.

Step 6 Set SPI_GCR[DBI_EN] (bit4) to 1 to start transmitting command.

Step 7 Wait until DBI_INT[RD_DONE_INT] is 1. It indicates that the data is read completely.

18.9.7 Register List

Module Name	Base Address
SPI_DBI	0x02541000

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
SPI_GCR	0x0004	SPI Global Control Register
SPI_TCR	0x0008	SPI Transfer Control register
SPI_IER	0x0010	SPI Interrupt Control register
SPI_ISR	0x0014	SPI Interrupt Status register
SPI_FCR	0x0018	SPI FIFO Control register
SPI_FSR	0x001C	SPI FIFO Status register
SPI_WCR	0x0020	SPI Wait Clock Counter register
SPI_SAMP_DL	0x0028	SPI Sample Delay Control Register
SPI_MBC	0x0030	SPI Master Burst Counter register
SPI_MTC	0x0034	SPI Master Transmit Counter Register
SPI_BCC	0x0038	SPI Master Burst Control Counter register
SPI_BATCR	0x0040	SPI Bit-Aligned Transfer Configure Register
SPI_BA_CCR	0x0044	SPI Bit-Aligned CLOCK Configuration Register
SPI_TBR	0x0048	SPI TX Bit Register
SPI_RBR	0x004C	SPI RX Bit Register
SPI_NDMA_MODE_CTL	0x0088	SPI Normal DMA Mode Control Register
DBI_CTL_0	0x0100	DBI Control Register 0
DBI_CTL_1	0x0104	DBI Control Register 1
DBI_CTL_2	0x0108	DBI Control Register 2
DBI_TIMER	0x010C	DBI Timer Control Register
DBI_VIDEO_SIZE	0x0110	DBI Video Size Register
DBI_INT	0x0120	DBI Interrupt Register
DBI_DEBUG_0	0x0124	DBI DEBUG Register 0
DBI_DEBUG_1	0x0128	DBI DEBUG Register 1
SPI_TXD	0x0200	SPI TX Data register
SPI_RXD	0x0300	SPI RX Data register
SPI_BSR	0x0400	SPI BUF Status register

18.9.8 Register Description

18.9.8.1 0x0004 SPI Global Control Register (Default Value: 0x0000_0080)

Offset: 0x0004			Register Name: SPI_GCR
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	SRST Soft reset Write 1 to this bit will clear the SPI controller, and auto clear to 0 when reset operation completes Write 0 has no effect.
30:8	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: SPI_GCR
Bit	Read/Write	Default/Hex	Description
7	R/W	0x1	TP_EN Transmit Pause Enable In master mode, it is used to control transmit state machine to stop smart burst sending when RX FIFO is full. 1: Stop transmitting data when RXFIFO is full. 0: Normal operation, ignore RXFIFO status. *Note: This bit can t be written when XCH=1.*
6:5	/	/	/
4	R/W	0x0	DBI_EN DBI Module Enable Control 0: Disable 1: Enable
3	R/W	0x0	SPI_DBI_MODE_SEL SDBISPI_DBI Working Mode Select 0: SPI MODE 1: DBI MODE
2	R/W	0x0	MODE_SELEC Sample Timing Mode Select 0: Old mode of Sample Timing 1: New mode of Sample Timing *Note: This bit can t be written when XCH=1.*
1	R/W	0x0	MODE SPI Function Mode Select 0: Slave Mode 1: Master Mode *Note: This bit can t be written when XCH=1.*
0	R/W	0x0	EN SPI Module Enable Control 0: Disable 1: Enable *Note: After transforming from bit_mode to byte_mode, the SPI Module must be enabled again.*

18.9.8.2 0x0008 SPI Transfer Control Register (Default Value: 0x0000_0087)

Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	XCH Exchange Burst In master mode it is used to start SPI burst 0: Idle 1: Initiates exchange. Write 1 to this bit will start the SPI burst, and will auto clear after finishing the bursts transfer specified by BC. Write 1 to SRST will also clear this bit. Write 0 to this bit has no effect. *Note: This bit can t be written when XCH=1.*
30:16	/	/	/
15	R/W	0x0	SDC1 Master Sample Data Control register1 Set this bit to 1 to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. 0: Normal operation, do not delay internal read sample point 1: delay internal read sample point *Note: This bit can t be written when XCH=1.*
14	R/W	0x0	SDDM Sending Data Delay Mode 0: Normal sending 1: Delay sending Set the bit to 1 to make the data that should be sent with a delay of half cycle of SPI_CLK in dual io mode for SPI mode 0.
13	R/W	0x0	SDM Master Sample Data Mode 1: Normal Sample Mode 0: Delay Sample Mode In Normal Sample Mode, SPI master samples the data at the correct edge for each SPI mode; In Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the correct edge defined in respective SPI mode.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	FBS First Transmit Bit Select 0: MSB first 1: LSB first *Note: This bit can t be written when XCH=1.*
11	R/W	0x0	SDC Master Sample Data Control Set this bit to 1 to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. 0: Normal operation, do not delay internal read sample point 1: Delay internal read sample point *Note: This bit can t be written when XCH=1.*
10	R/W	0x0	RPSM Rapids mode select Select Rapids mode for high speed write. 0: Normal write mode 1: rapids write mode *Note: This bit can t be written when XCH=1.*
9	R/W	0x0	DDB Dummy Burst Type 0: The bit value of dummy SPI burst is zero 1: The bit value of dummy SPI burst is one *Note: This bit can t be written when XCH=1.*
8	R/W	0x0	DHB Discard Hash Burst In master mode it controls whether discarding unused SPI bursts 0: Receiving all SPI bursts in BC period 1: Discard unused SPI bursts, only fetching the SPI bursts during dummy burst period. The bursts number is specified by TC. *Note: This bit can t be written when XCH=1.*

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description
7	R/W	0x1	SS_LEVEL When control SS signal manually (SPI_CTRL_REG.SS_CTRL==1), set this bit to 1 or 0 to control the level of SS signal. 0: Set SS to low 1: Set SS to high *Note: This bit can t be written when XCH=1.*
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software *Note: This bit can t be written when XCH=1.*
5:4	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_CS0 will be asserted 01: SPI_CS1 will be asserted 10: SPI_CS2 will be asserted (not used) 11: SPI_CS3 will be asserted (not used) *Note: This bit can t be written when XCH=1.*
3	R/W	0x0	SSCTL In master mode, this bit selects the output wave form for the SPI_CSx signal. Only valid when SS_OWNER = 0. 0: SPI_CSx remains asserted between SPI bursts 1: Negate SPI_CSx between SPI bursts *Note: This bit can t be written when XCH=1.*
2	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) *Note: This bit can t be written when XCH=1.*
1	R/W	0x1	CPOL SPI Clock Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) *Note: This bit can t be written when XCH=1.*

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description
0	R/W	0x1	CPHA SPI Clock/Data Phase Control 0: Phase 0 (Leading edge for sample data) 1: Phase 1 (Leading edge for setup data) *Note: This bit can t be written when XCH=1.*

18.9.8.3 0x0010 SPI Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SPI_IER
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R/W	0x0	SS_INT_EN SSI Interrupt Enable Chip Select Signal (SSx) from valid state to invalid state 0: Disable 1: Enable
12	R/W	0x0	TC_INT_EN Transfer Completed Interrupt Enable 0: Disable 1: Enable
11	R/W	0x0	TF_UDR_INT_EN TXFIFO under run Interrupt Enable 0: Disable 1: Enable
10	R/W	0x0	TF_OVF_INT_EN TX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
9	R/W	0x0	RF_UDR_INT_EN RXFIFO under run Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	RF_OVF_INT_EN RX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
7	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0010			Register Name: SPI_IER
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	TF_FUL_INT_EN TX FIFO Full Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TX_EMP_INT_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	TX_ERQ_INT_EN TX FIFO Empty Request Interrupt Enable 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	RF_FUL_INT_EN RX FIFO Full Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RX_EMP_INT_EN RX FIFO Empty Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RF_RDY_INT_EN RX FIFO Ready Request Interrupt Enable 0: Disable 1: Enable

18.9.8.4 0x0014 SPI Interrupt Status Register (Default Value: 0x0000_0032)

Offset: 0x0014			Register Name: SPI_ISR
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R/W1C	0x0	SSI SS Invalid Interrupt When SSI is 1, it indicates that SS has changed from valid state to invalid state. Writing 1 to this bit clears it.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: SPI_ISR
Bit	Read/Write	Default/Hex	Description
12	R/W1C	0x0	TC Transfer Completed In master mode, it indicates that all bursts specified by BC has been exchanged. In other condition, when set, this bit indicates that all the data in TXFIFO has been loaded in the Shift register, and the Shift register has shifted out all the bits. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed
11	R/W1C	0x0	TF_UDF TXFIFO under run This bit is set when if the TXFIFO is underrun. Writing 1 to this bit clears it. 0: TXFIFO is not underrun 1: TXFIFO is underrun
10	R/W1C	0x0	TF_OVF TXFIFO Overflow This bit is set when if the TXFIFO is overflow. Writing 1 to this bit clears it. 0: TXFIFO is not overflow 1: TXFIFO is overflowed
9	R/W1C	0x0	RX_UDF RXFIFO Underrun When set, this bit indicates that RXFIFO has underrun. Writing 1 to this bit clears it.
8	R/W1C	0x0	RX_OVF RXFIFO Overflow When set, this bit indicates that RXFIFO has overflowed. Writing 1 to this bit clears it. 0: RXFIFO is available. 1: RXFIFO has overflowed.
7	/	/	/
6	R/W1C	0x0	TX_FULL TXFIFO Full This bit is set when if the TXFIFO is full. Writing 1 to this bit clears it. 0: TXFIFO is not full 1: TXFIFO is Full

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: SPI_ISR
Bit	Read/Write	Default/Hex	Description
5	R/W1C	0x1	TX_EMP TXFIFO Empty This bit is set if the TXFIFO is empty. Writing 1 to this bit clears it. 0: TXFIFO contains one or more words. 1: TXFIFO is empty
4	R/W1C	0x1	TX_READY TXFIFO Ready 0: TX_WL > TX_TRIG_LEVEL 1: TX_WL <= TX_TRIG_LEVEL This bit is set any time if TX_WL <= TX_TRIG_LEVEL. Writing 1 to this bit clears it. Where TX_WL is the water level of RXFIFO
3	/	/	/
2	R/W1C	0x0	RX_FULL RX Full This bit is set when the RX FIFO and RX buffer are full. Writing 1 to this bit clears it. 0: Not Full 1: Full
1	R/W1C	0x1	RX_EMP RX Empty This bit is set when the RX FIFO and RX buffer are empty. Writing 1 to this bit clears it. 0: Not empty 1: Empty
0	R/W1C	0x0	RX_RDY RX Ready 0: RX_WL <= RX_TRIG_LEVEL 1: RX_WL > RX_TRIG_LEVEL This bit is set any time if RX_WL > RX_TRIG_LEVEL. Writing 1 to this bit clears it. Where RX_WL is the water level of RX FIFO and RX buffer.

18.9.8.5 0x0018 SPI FIFO Control Register (Default Value: 0x0040_0001)

Offset: 0x0018			Register Name: SPI_FCR
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0018			Register Name: SPI_FCR
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	TX_FIFO_RST TX FIFO Reset Write 1 to this bit will reset the control portion of the TX FIFO and auto clear to 0 when completing reset operation, write to 0 has no effect.
30	R/W	0x0	TF_TEST_ENB TX Test Mode Enable 0: Disable 1: Enable In normal mode, TX FIFO can only be read by SPI controller, write 1 to this bit will switch TX FIFO read and write function to AHB bus. This bit is used to test the TX FIFO, don t set in normal operation and don t set RF_TEST and TF_TEST at the same time.
29:25	/	/	/
24	R/W	0x0	TF_DRQ_EN TX FIFO DMA Request Enable 0: Disable 1: Enable
23:16	R/W	0x40	TX_TRIG_LEVEL TX FIFO Empty Request Trigger Level
15	R/WAC	0x0	RF_RST RXFIFO Reset Write 1 to this bit will reset the control portion of the receiver FIFO, and auto clear to 0 when completing reset operation, write 0 to this bit has no effect.
14	R/W	0x0	RF_TEST RX Test Mode Enable 0: Disable 1: Enable In normal mode, RX FIFO can only be written by SPI controller, write 1 to this bit will switch RX FIFO read and write function to AHB bus. This bit is used to test the RX FIFO, don t set in normal operation and don t set RF_TEST and TF_TEST at the same time.
13:9	/	/	/
8	R/W	0x0	RF_DRQ_EN RX FIFO DMA Request Enable 0: Disable 1: Enable
7:0	R/W	0x1	RX_TRIG_LEVEL RX FIFO Ready Request Trigger Level

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.9.8.6 0x001C SPI FIFO Status Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SPI_FSR
Bit	Read/Write	Default/Hex	Description
31	R	0x0	TB_WR TX FIFO Write Buffer Write Enable
30:24	/	/	/
23:16	R	0x0	TF_CNT TX FIFO Counter These bits indicate the number of words in TX FIFO 0x0: 0 byte in TX FIFO 0x1: 1 byte in TX FIFO (p) 0x40: 64 bytes in TX FIFO others: Reserved
15	R	0x0	RB_WR RX FIFO Read Buffer Write Enable
14:8	/	/	/
7:0	R	0x0	RF_CNT RX FIFO Counter These bits indicate the number of words in RX FIFO + RX BUFFER 0x0: 0 byte in RX FIFO & RX BUFFER 0x1: 1 byte in RX FIFO & RX BUFFER (p) 0x40: 64 bytes in RX FIFO & RX BUFFER (p) 0xc0:192 bytes in RX FIFO & RX BUFFER other: Reserved

18.9.8.7 0x0020 SPI Wait Clock Counter Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SPI_WCR
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0020			Register Name: SPI_WCR
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0x0	SWC Dual mode direction switch waits clock counter (for master mode only). 0: No wait states inserted n: n SPI_CLK wait states inserted These bits control the number of wait states to be inserted before start dual data transfer in dual SPI mode. The SPI module counts SPI_CLK by SWC for delaying next word data transfer. *Note: It can t be written when XCH=1.*
15:0	R/W	0x0	WCC Wait Clock Counter (In Master mode) These bits control the number of wait states to be inserted in data transfers. The SPI module counts SPI_CLK by WCC for delaying next word data transfer. 0: No wait states inserted N: N SPI_CLK wait states inserted *Note: It can t be written when XCH=1.*

18.9.8.8 0x0028 SPI Sample Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0028			Register Name: SPI_SAMP_DL
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:8	R	0x20	Reserved
7	R/W	0x0	SAMP_DL_SW_EN Sample Delay Software Enable When set, enable sample delay specified at SAMP_DL_SW
6	/	/	/
5:0	R/W	0x0	SAMP_DL_SW Sample Delay Software The relative delay between clock line and command line, data lines. It can be determined according to the value of SAMP_DL, the cycle of card clock and device's input timing requirement.

18.9.8.9 0x0030 SPI Master Burst Counter Register (Default Value: 0x0000_0000)

Offset: 0x0030	Register Name: SPI_MBC

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	MBC Master Burst Counter In master mode, this field specifies the total burst number. 0: 0 burst 1: 1 burst (p) N: N bursts *Note:* a) *It can t be written when XCH=1.* b) *Total transfer data include the TXD, RXD and dummy burst.*

18.9.8.10 0x0034 SPI Master Transmit Counter Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: SPI_MTC
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	MWTC Master Write Transmit Counter In master mode, this field specifies the burst number that should be sent to TXFIFO before automatically sending dummy burst. For saving bus bandwidth, the dummy burst (all zero bits or all one bits) is sent by SPI Controller automatically. 0: 0 burst 1: 1 burst (p) N: N bursts *Note: It can t be written when XCH=1.*

18.9.8.11 0x0038 SPI Master Burst Control Counter Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: SPI_BCC
Bit	Read/Write	Default/Hex	Description
31: 30	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0038			Register Name: SPI_BCC
Bit	Read/Write	Default/Hex	Description
29	R/W	0x0	Quad_EN Quad_Mode_EN 0: Quad mode disable 1: Quad mode enable *Note:* a) *It can t be written when XCH=1;* b) *Quad mode includes Quad-Input and Quad-Output.*
28	R/W	0x0	DRM Master Dual Mode RX Enable 0: RX use single-bit mode 1: RX use dual mode *Note:* a) *It can t be written when XCH=1.* b) *It is only valid when Quad_Mode_EN=0.*
27:24	R/W	0x0	DBC Master Dummy Burst Counter In master mode, this field specifies the burst number that should be sent before receive in dual SPI mode. The data is don t care by the device. 0: 0 burst 1: 1 burst (p) N: N bursts *Note: It can t be written when XCH=1.*
23:0	R/W	0x0	STC Master Single Mode Transmit Counter In master mode, this field specifies the burst number that should be sent in single mode before automatically sending dummy burst. This is the first transmit counter in all bursts. 0: 0 burst 1: 1 burst (p) N: N bursts *Note: It can t be written when XCH=1.*

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.9.8.12 0x0040 SPI Bit-Aligned Transfer Configure Register (Default Value: 0x0000_00A0)

Offset: 0x0040			Register Name: SPI_BATCR
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	TCE Transfer Control Enable In master mode, it is used to start to transfer the serial bits frame, it is only valid when Work Mode Select==0x10/0x11. 0: Idle 1: Initiates transfer. Write 1 to this bit will start to transfer serial bits frame (the value comes from the SPI TX Bit Register or SPI RX Bit Register), and will auto clear after the bursts transfer completely. Write 0 to this bit has no effect.
30	R/W	0x0	MSMS Master Sample Standard 0: Standard Sample Mode 1: Delay Sample Mode In Standard Sample Mode, SPI master samples the data at the standard rising edge of SCLK for each SPI mode. In Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the standard rising edge of SCLK defined in respective SPI mode.
29:26	/	/	/
25	R/W1C	0x0	TBC Transfer Bits Completed When set, this bit indicates that the last bit of the serial data frame in SPI TX Bit Register (or SPI RX Bit Register) has been transferred completely. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed *Note: It is only valid when Work Mode Select=0x10/0x11.*
24	R/W	0x0	TBC_INT_EN Transfer Bits Completed Interrupt Enable 0: Disable 1: Enable *Note: It is only valid when Work Mode Select=0x10/0x11.*
23:22	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0040			Register Name: SPI_BATCR
Bit	Read/Write	Default/Hex	Description
21:16	R/W	0x00	RX_FEM_LEN Configure the length of serial data frame(burst) of RX 000000: 0bit 000001: 1bit (p) 100000: 32bits Other values: reserved *Note: It is only valid when Work Mode Select=0x10/0x11, and can t be written when TCE=1.*
15:14	/	/	/
13:8	R/W	0x00	TX_FEM_LEN Configure the length of serial data frame(burst) of TX 000000: 0bit 000001: 1bit (p) 100000: 32bits Other values: reserved *Note: It is only valid when Work Mode Select=0x10/0x11, and can t be written when TCE=1.*
7	R/W	0x1	SS_LEVEL When control SS signal manually, set this bit to 1 or 0 to control the level of SS signal. 0: set SS to low 1: set SS to high *Note: It is only valid when Work Mode Select=0x10/0x11, and only work in Mode0, can t be written when TCE=1.*
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software *Note: It is only valid when Work Mode Select=0x10/0x11, and only work in Mode0, can t be written when TCE=1.*

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0040			Register Name: SPI_BATCR
Bit	Read/Write	Default/Hex	Description
5	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) *Note: It is only valid when Work Mode Select=0x10/0x11, and only work in Mode0, can t be written when TCE=1.*
4	/	/	/
3:2	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_CS0 will be asserted 01: SPI_CS1 will be asserted 10: SPI_CS2 will be asserted 11: SPI_CS3 will be asserted *Note: It is only valid when Work Mode Select =0x10/0x11, and only work in Mode0, can t be written when TCE=1.*
1:0	R/W	0x0	WMS Work Mode Select 00: Data frame is byte aligned in Standard SPI, Dual-Output/Dual Input SPI, Dual IO SPI and Quad-Output/Quad-Input SPI. 01: Reserved 10: Data frame is bit aligned in 3-Wire SPI 11: Data frame is bit aligned in Standard SPI

18.9.8.13 0x0044 SPI Bit-Aligned CLOCK Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: SPI_BA_CCR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	CDR_N Clock Divide Rate (Master Mode Only) The SPI_CLK is determined according to the following equation: SPI_CLK = Source_CLK / (2*(CDR_N + 1)). *Note: It is only valid when Work Mode Select =0x10/0x11*

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.9.8.14 0x0048 SPI TX Bit Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: SPI_TBR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VTB The Value of the Transmit Bits This register is used to store the value of the transmitted serial data frame. In the process of transmission, the LSB is transmitted first. *Note: This register is only valid when Work Mode Select=0x10/0x11.*

18.9.8.15 0x004C SPI RX Bit Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: SPI_RBR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VRB The Value of the Receive Bits This register is used to store the value of the received serial data frame. In the process of transmission, the LSB is transmitted first. *Note: This register is only valid when Work Mode Select=0x10/0x11.*

18.9.8.16 0x0088 SPI Normal DMA Mode Control Register (Default Value: 0x0000_00E5)

Offset: 0x0088			Register Name: SPI_NDMA_MODE_CTL
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:6	R/W	0x3	SPI_ACT_M SPI NDMA Active Mode 00: DMA_ACTIVE is low 01: DMA_ACTIVE is high 10: DMA_ACTIVE is controlled by DMA_REQUEST(DRQ) 11: DMA_ACTIVE is controlled by controller
5	R/W	0x1	SPI_ACK_M SPI NDMA Acknowledge Mode 0: active fall do not care ack 1: active fall must after detect ack is high
4:0	R/W	0x05	SPI_DMA_WAIT The counts of hold cycles from DMA last signal high to DMA_ACTIVE high.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.9.8.17 0x0100 DBI Control Register 0 (Default Value: 0x0010_0000)

Offset: 0x0100			Register Name: DBI_CTL_0
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CMDT Command Type 0: Write Command 1: Read Command
30:20	R/W	0x1	WCDC Write Command Dummy Cycles Controls dummy cycles between two write commands Range 1-255 Default Condition: there is a dbi_clk cycle between each command or parameter.
19	R/W	0x0	DAT_SEQ Output Data Sequence 0: MSB First 1: LSB First
18:16	R/W	0x0	RGB_SEQ Output RGB Sequence 000: RGB 001: RBG 010: GRB 011: GBR 100: BRG 101: BGR 110-111: Reserved
15	R/W	0x0	TRAN_MOD Transmit Mode 0: Command / Parameter 1: Video
14:12	R/W	0x0	DAT_FMT Output Data Format 000: RGB111 001: RGB444 010: RGB565 011: RGB666 100: RGB888 (only for 2 Data Lane Interface) 101-111: Reserved
11	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0100			Register Name: DBI_CTL_0
Bit	Read/Write	Default/Hex	Description
10:8	R/W	0x0	DBI_INTF DBI Interface 000: 3 Line Interface I 001: 3 Line Interface II 010: 4 Line Interface I 011: 4 Line Interface II 100: 2 Data Lane Interface
7:4	R/W	0x0	RGB_FMT RGB_Source_Format When Video Source_Type is RGB32 0000: RGB 0001: RBG 0010: GRB 0011: GBR 0100: BRG 0110: BGR Others: Reserved When Video Source_Type is RGB16 0: RGB 0001-0100: Reserved 0101: BGR 0110: GRBG_0: {G[5:3] R[4:0] B[4:0] G[2:0]} 0111: GBRG_0: {G[5:3] B[4:0] R[4:0] G[2:0]} 1000: GRBG_1: {G[2:0] R[4:0] B[4:0] G[5:3]} 1001: GBRG_1: {G[2:0] B[4:0] R[4:0] G[5:3]} Others: Reserved
3	R/W	0x0	DUM_VAL Dummy Cycle Value Output Value During Dummy Cycle
2	R/W	0x0	RGB_BO RGB Bit Order 0: Remain the sequence of RGB data 1: Swap the higher bit and the lower bit for each component of DRAM RGB
1	R/W	0x0	ELEMENT_A_POS Element A Position Only for RGB32 Data Format 0: A component is in the bit [31:24] of data source 1: A component is in the bit [7:0] of data source

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0100			Register Name: DBI_CTL_0
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	VI_SRC_TYPE RGB Source Type 0: RGB32 1: RGB16

18.9.8.18 0x0104 DBI Control Register 1 (Default Value: 0x0000_0001)

Offset: 0x0104			Register Name: DBI_CTL_1
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	DBI_SOFT_TRG It is only available for software trigger mode. Write 1 to this bit will start DBI TX module and auto clear to 0 when completing start operation, write to 0 has no effect.
30:29	R/W	0x0	DBI_EN_MOD_SEL DBI Enable Mode Select 00: always on mode 01: Software trigger mode 10: timer trigger mode 11: te trigger mode
28	/	/	/
27:26	R/W	0x0	RGB666_FMT 2 Data Lane RGB666 Format 00: Normal Format 01: Special Format for ILITEK 10: Special Format for New Vision
25	R/W	0x0	DBI_RXCLK_INV DBI rx clock inverse 0: Sample data at the positive edge of the output clock 1: Sample data at the negative edge of the output clock
24	R/W	0x0	DBI_CLKO_MOD DBI output clock mode 0: DBI clock always on(DCX Setup/hold equals one clock cycle) 1: DBI clock auto gating(DCX Setup/hold equals to a half clock cycle)

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0104			Register Name: DBI_CTL_1
Bit	Read/Write	Default/Hex	Description
23	R/W	0x0	DBI_CLKO_INV DBI Clock Output Inverse When the bit24 (DBI output clock mode) is 0. 0: Release CSX signals and data at the falling edge. 1: Release CSX signals and data at the rising edge. When the bit24 (DBI output clock mode) is 1. 0: Release CSX signals at the rising edge, and release data at the falling edge. 1: Release CSX signals at the falling edge, and release data at the rising edge.
22	R/W	0x0	DCX_DATA DCX Data Value 0: DCX Value equal to 0 1: DCX Value equal to 1
21	R/W	0x0	RGB 16 Data Source Select RGB 16 Data Source Select 0: Pixel1 is stored in the higher bits of address, and Pixel0 is stored in the lower bits of address. 1: Pixel0 is stored in the higher bits of address, and Pixel1 is stored in the lower bits of address.
20	R/W	0x0	RDAT_LSB Bit Order of Read Data 0: A read data is in the highest bit. 1: A read data is in the lowest bit.
19:16	/	/	/
15:8	R/W	0x0	RCDC Read Command Dummy Cycles The dummy cycle between the read command and read data Reading 1-byte (8 bits) data has not dummy cycle.
7:0	R/W	0x1	RDBN Read Data Number of Bytes Sample Bytes data based on configuration.

18.9.8.19 0x0108 DBI Control Register 2 (Default Value: 0x0000_4000)

Offset: 0x0108			Register Name: DBI_CTL_2
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0108			Register Name: DBI_CTL_2
Bit	Read/Write	Default/Hex	Description
15	R/W	0x0	DBI_FIFO_DRQ_EN DBI FIFO DMA Request Enable 0: Disable 1: Enable
14:8	R/W	0x40	DBI_TRIG_LEVEL DBI FIFO Empty Request Trigger Level
7	/	/	/
6	R/W	0x0	DBI_SDI_OUT_SEL DBI SDI PIN Output Select The signal is used with the DBI SDI PIN Function Sel bit. 0: Output WRX (When DBI DCX PIN Function Sel = 0, the SDI pin outputs data) 1: Output DCX
5	R/W	0x0	DBI_DCX_SEL DBI DCX PIN Function Sel 0: DBI DCX Function 1:WRX(2 Data Lane Interface)
4:3	R/W	0x0	DBI_SDI_SEL DBI SDI PIN Function sel 00: DBI_SDI (Interface II) , WRX(2 Data Lane Interface) 01: DBI_TE 10: DBI_DCX 11: Reserved
2	R/W	0x0	TE_DBC_SEL TE debounce function select 0: debounce 1: no-debounce
1	R/W	0x0	TE_TRIG_SEL TE edge trigger select 0: TE rising edge 1: TE falling edge
0	R/W	0x0	TE_EN TE enable 0: TE Disable 1: TE Enable

18.9.8.20 0x010C DBI Timer Control Register (Default Value: 0x0000_0000)

Offset: 0x010C	Register Name: DBI_TIMER

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DBI_TM_EN DBI Timer enable 0: Enable 1: Disable
30:0	R/W	0x0	DBI_TM_VAL DBI Timer Value It is used to set the time at which the interrupt of the DBI Timer is triggered. When the Timer_EN is 1, the timer starts to count (the counting clock is SCLK). When the counter reaches the target value to trigger the Timer_INT of DBI, the data will start to be sent in serially. *Note: Counting will stop when the data is being sent serially. The interval between two data transfers set by DBI Timer Value is called frame blanking.*

18.9.8.21 0x0110 DBI Video Size Register (Default Value: 0x01E0_0140)

Offset: 0x0110			Register Name: DBI_VIDEO_SIZE
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:16	R/W	0x1e0	V_SIZE It is used to generate the Frame int.
15:11	/	/	/
10:0	R/W	0x140	H_SIZE It is used to generate the Line int.

18.9.8.22 0x0120 DBI Interrupt Register (Default Value: 0x0000_4000)

Offset: 0x0120			Register Name: DBI_INT
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14	R/W1C	0x1	DBI_FIFO_EMPTY_INT DBI FIFO Empty Interrupt Status 0: DBI_FIFO is not empty 1: DBI_FIFO is empty
13	R/W1C	0x0	DBI_FIFO_FULL_INT DBI FIFO Full Interrupt Status 0: DBI_FIFO is not full. 1: DBI_FIFO is full.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0120			Register Name: DBI_INT
Bit	Read/Write	Default/Hex	Description
12	R/W1C	0x0	TIMER_INT It indicates that timer has been count sclk cycles to the value of DBI_Timer Register[30:0] . Writing 1 to this bit clears it. 0: Timer hasn t been achieved objectively. 1: Timer has been achieved objectively.
11	R/W1C	0x0	RD_DONE_INT It indicates that the number of byte setting in DBI_Control Register 1 [19:8] has been read. Writing 1 to this bit clears it. 0: All of data hasn t been read. 1: All of data has been read.
10	R/W1C	0x0	TE_INT It indicates that TE signal has been changed. Writing 1 to this bit clears it. 0: TE signal isn t changed. 1: TE signal has been changed.
9	R/W1C	0x0	FRAM_DONE_INT It indicates that a frame video data has been send. Writing 1 to this bit clears it. 0: A frame of video has not been send. 1: A frame of video has been send.
8	R/W1C	0x0	LINE_DONE_INT It indicates that a line of video data has been send. Writing 1 to this bit clears it. 0: A line of video data has not been send 1: A line of video data has been send
7	/	/	/
6	R/W	0x0	DBI_FIFO_EMPTY_INT_EN DBI FIFO Empty Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	DBI_FIFO_FULL_INT_EN DBI FIFO Full Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	TIMER_INT_EN Timer Interrupt Enable 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0120			Register Name: DBI_INT
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	RD_DONE_INT_EN Read Done Interrupt Enable 0: Disable 1: Enable
2	R/W	0x0	TE_INT_EN TE Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	FRAM_DONE_INT_EN Frame Done Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	LINE_DONE_INT_EN Line Done Interrupt Enable 0: Disable 1: Enable

18.9.8.23 0x0124 DBI Debug Register 0 (Default Value: 0x007F_0000)

Offset: 0x0124			Register Name: DBI_DEBUG_0
Bit	Read/Write	Default/Hex	Description
31:23	/	/	/
22:16	R	0x7F	DBI_FIFO_AVAIL DBI FIFO ROOM VALID 0-127 Words
15:13	/	/	/
12	R	0x0	TE_VAL TE input value 0: TE not Trigger 1: TE Trigger
11:8	R	0x0	DBI_RXCS FSM for DBI Receive RX_BS0 - RX_BS6 , Gray - Code
7:4	R	0x0	SH_CS FSM for shifter 0000-0011: SH0-SH11

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0124			Register Name: DBI_DEBUG_0
Bit	Read/Write	Default/Hex	Description
3:2	R	0x0	DBI_TXCS FSM for DBI Transmit 00: IDLE 01: SHIF 10: DUMY 11: READ
1:0	R	0x0	MEM_CS FSM for DBI Memory 00: IDLE_FRM 01: FRM_POS 10: FRM_RDY

18.9.8.24 0x0128 DBI Debug Register 1 (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: DBI_DEBUG_1
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:16	R	0x0	LCNT Line counter The number of pixel lines that are currently sent
15:12	/	/	/
11:0	R	0x0	CCNT Component counter The number of RGB components that are currently sent The field is equal to pixel_cnt *3.

18.9.8.25 0x0200 SPI TX Data Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: SPI_TXD
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0200			Register Name: SPI_TXD
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TDATA Transmit Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are rooms in TXFIFO, one burst data is written to TXFIFO and the depth is increased by 1. In half-word accessing method, two SPI burst data are written and the TXFIFO depth is increased by 2. In word accessing method, four SPI burst data are written and the TXFIFO depth is increased by 4. *Note: This address is writing-only if TF_TEST is 0, and if TF_TEST is set to 1, this address is readable and writable to test the TX FIFO through the AHB bus.*

18.9.8.26 0x0300 SPI RX Data Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: SPI_RXD
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RDATA Receive Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are data in RXFIFO, the top word is returned and the RXFIFO depth is decreased by 1. In half-word accessing method, two SPI bursts are returned and the RXFIFO depth is decrease by 2. In word accessing method, the four SPI bursts are returned and the RXFIFO depth is decreased by 4. *Note: This address is read-only if RF_TEST is 0, and if RF_TEST is set to 1, this address is readable and writable to test the RX FIFO through the AHB bus.*

18.9.8.27 0x0400 SPI BUF Status Register (Default Value: 0x0000_0000)

Offset: 0x0400			Register Name: SPI_BSR
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0400			Register Name: SPI_BSR
Bit	Read/Write	Default/Hex	Description
26:24	R	0x0	TX_SHIFT_BUFFER_CNT TX SHIFT Buffer Counter These bits indicate the number of bytes in TX Shift Buffer, which is after TX FIFO, and maximum depth is 4 level with 8 bits.
23:19	/	/	/
18:16	R	0x0	TB_CNT TX FIFO Write Buffer Counter These bits indicate the number of bytes in TX FIFO Write Buffer
15:8	/	/	/
7:0	R	0x0	RB_CNT RX FIFO Read Buffer Counter These bits indicate the number of bytes in RX FIFO Read Buffer

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.10 UART

18.10.1 Overview

The universal asynchronous receiver transmitter (UART) provides an asynchronous serial communication with external devices, modem (data carrier equipment, DCE). It performs serial-to-parallel conversion on the data received from peripherals and transmits the converted data to the internal bus. It also performs parallel-to-serial conversion on the data that is transmitted to peripherals.

The UART has the following features:

- Up to 9 UART controllers
  - 7 UART controllers in CPUX domain: UART0, UART1, UART2, UART3, UART4, UART5, and UART6
  - 2 UART controllers in CPUS domain: S_UART0 and S_UART1
- Compatible with industry-standard 16450/16550 UARTs
- Transmit and Receive data FIFOs
  - UART0 (RX-64 Layer, TX-64 Layer)
  - UART1 (RX-256 Layer, TX-256 Layer)
  - UART2 (RX-256 Layer, TX-256 Layer)
  - UART3 (RX-256 Layer, TX-256 Layer)
  - UART4 (RX-256 Layer, TX-256 Layer)
  - UART5 (RX-256 Layer, TX-256 Layer)
  - UART6 (RX-256 Layer, TX-256 Layer)
  - S_UART0 (RX-64 Layer, TX-64 Layer)
  - S_UART1 (RX-64 Layer, TX-64 Layer)
- Supports baud rate generator from APB bus clock
  - Speed up to 10 Mbps with 160 MHz APB clock (excluding S_UART0, S_UART1)
  - Speed up to 5 Mbps with 80 MHz APB clock (excluding S_UART0, S_UART1)
  - Speed up to 3.75 Mbps with 60 MHz APB clock (excluding S_UART0, S_UART1)
  - Speed up to 1.5 Mbps with 24 MHz APB clock
- Supports 5-8 data bits and 1/1.5/2 stop bits
- Supports Even, Odd or No Parity
- Supports TX/RX DMA Slave interface
- Supports Software/ Hardware Flow Control

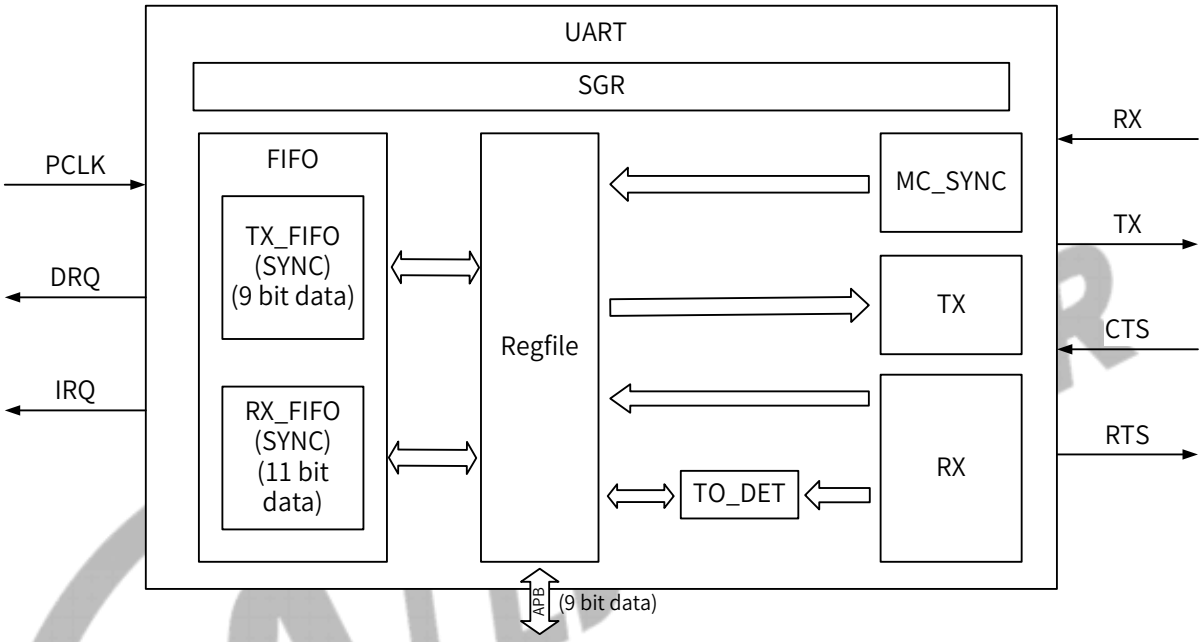
Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- Supports IrDA 1.0 SIR
- Supports RS-485/9-bit mode
- Supports Auto-Flow by using CTS & RTS (Only UART1/2/3/4/5/6)

18.10.2 Block Diagram

The following figure shows a block diagram of the UART.

Figure 18-53 UART Block Diagram



18.10.3 Clock Sources

The following table describes the clock sources for UART. After selecting a proper clock, users must open the gating of TWI and release the corresponding reset bit.

For more details on the clock setting, configuration, and gating information, see section CCU or PRCM.

Module	Clock Sources	Description
UART0-6	APB_UART	UART clock source. Refer to CCU for details on APB_UART.
S_UART0-1	APBS1	UART clock source. Refer to PRCM for details on APBS1.

18.10.4 External Signals

The following table describes the external signals of UART.

Table 18-18 UART External Signals

Signal Name	Description	Type
UART0-TX	UART0 Data Transmitter	O

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

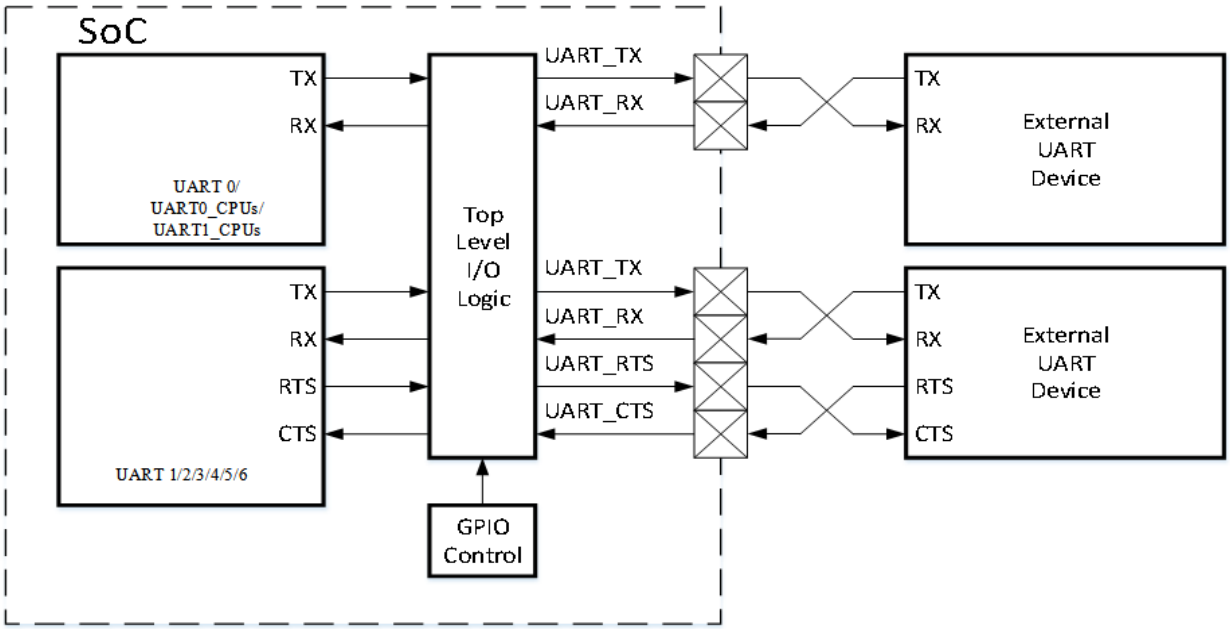
Signal Name	Description	Type
UART0-RX	UART0 Data Receiver	I
UART1-RTS	UART1 Data Request to Send	O
UART1-CTS	UART1 Data Clear to Send	I
UART1-TX	UART1 Data Transmitter	O
UART1-RX	UART1 Data Receiver	I
UART2-RTS	UART2 Data Request to Send	O
UART2-CTS	UART2 Data Clear to Send	I
UART2-TX	UART2 Data Transmitter	O
UART2-RX	UART2 Data Receiver	I
UART3-RTS	UART3 Data Request to Send	O
UART3-CTS	UART3 Data Clear to Send	I
UART3-TX	UART3 Data Transmitter	O
UART3-RX	UART3 Data Receiver	I
UART4-RTS	UART4 Data Request to Send	O
UART4-CTS	UART4 Data Clear to Send	I
UART4-TX	UART4 Data Transmitter	O
UART4-RX	UART4 Data Receiver	I
UART5-RTS	UART5 Data Request to Send	O
UART5-CTS	UART5 Data Clear to Send	I
UART5-TX	UART5 Data Transmitter	O
UART5-RX	UART5 Data Receiver	I
UART6-RTS	UART6 Data Request to Send	O
UART6-CTS	UART6 Data Clear to Send	I
UART6-TX	UART6 Data Transmitter	O
UART6-RX	UART6 Data Receiver	I
UART6-DCD	UART6 Line State of Data Carrier Detect	I
UART6-DSR	UART6 Line State of Data Set Ready	I
UART6-DTR	UART6 Data Terminal Ready	O
UART6-RI	UART6 Line State of Ring Indicator	I
S-UART0-TX	S-UART0 Data Transmitter	O
S-UART0-RX	S-UART0 Data Receiver	I
S-UART1-TX	S-UART1 Data Transmitter	O
S-UART1-RX	S-UART1 Data Receiver	I

18.10.5 Typical Application

The following figure shows UART controller IO signals. The GPIO controller can be configured to enable UART model connecting with external device.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 18-54 UART Controller IO Signals



18.10.5.1 RTS/CTS Auto Flow Control

The following figures show the RTS/CTS Auto Flow Control and its timing.

Figure 18-55RTS/CTS Auto Flow Control

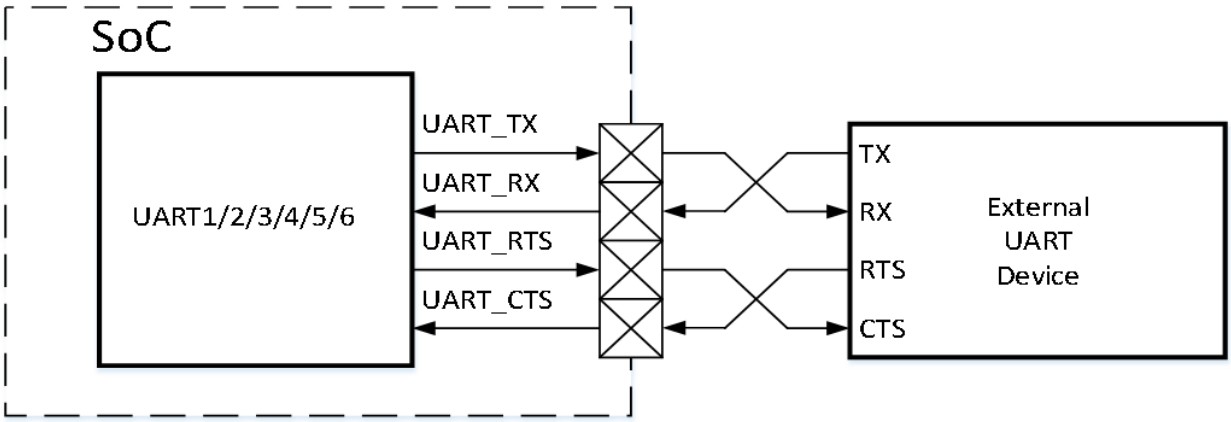
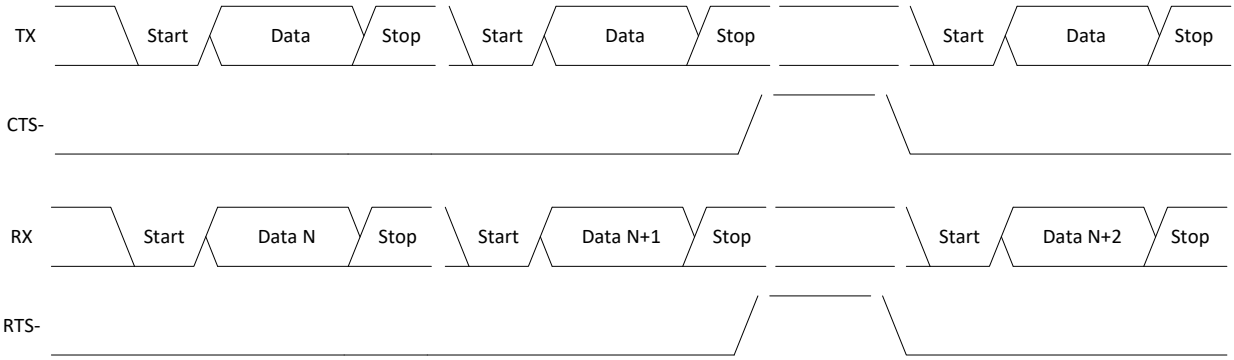


Figure 18-56 RTS/CTS Auto Flow Control Timing



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.10.5.2 Serial IrDA

The following figures show the IrDA transceiver and its timing.

Figure 18-57 IrDA Transceiver

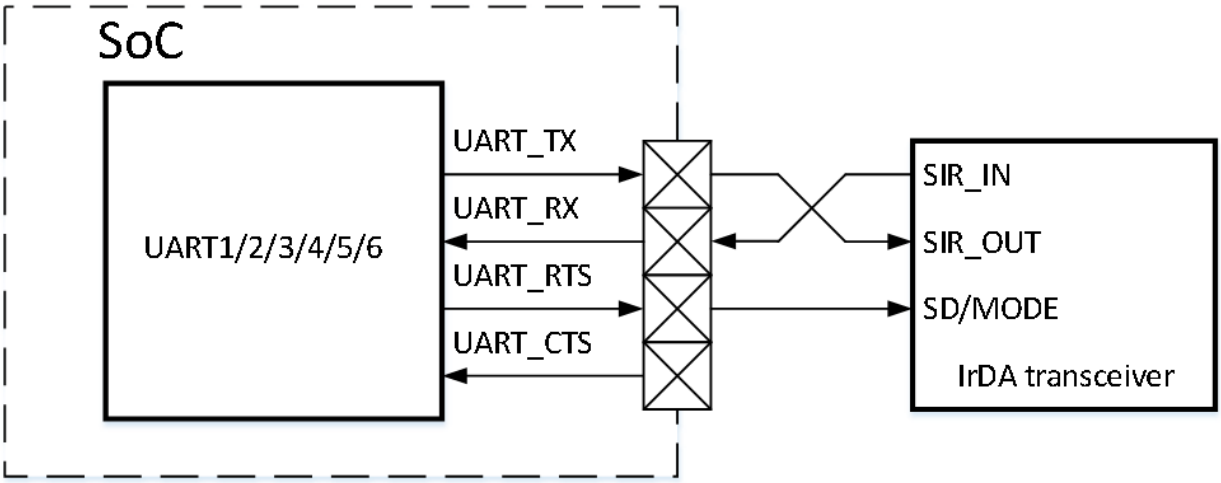
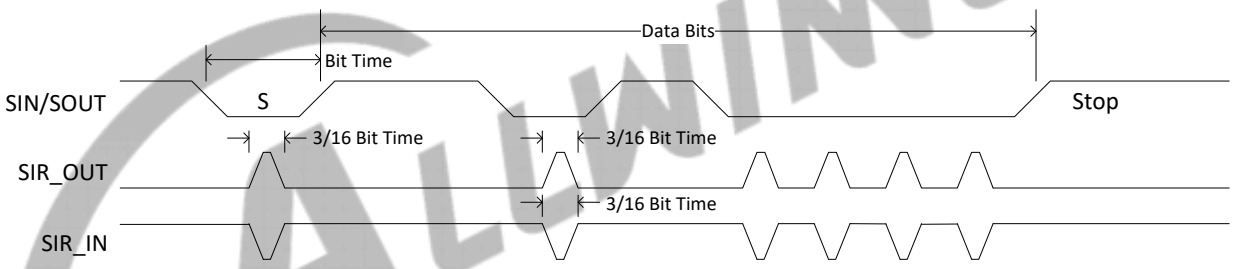


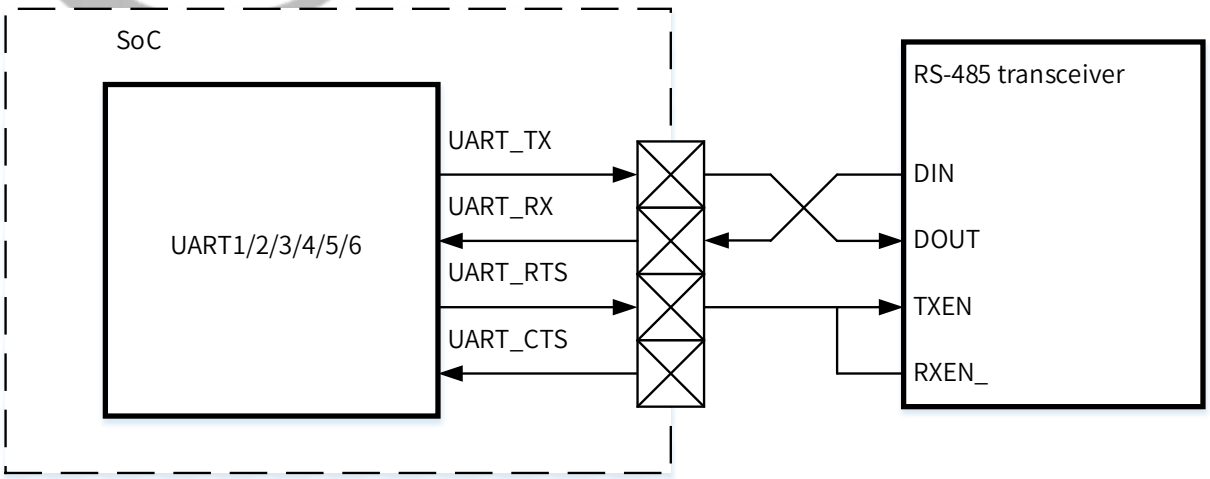
Figure 18-58 Serial IrDA Timing



18.10.5.3 RS-485

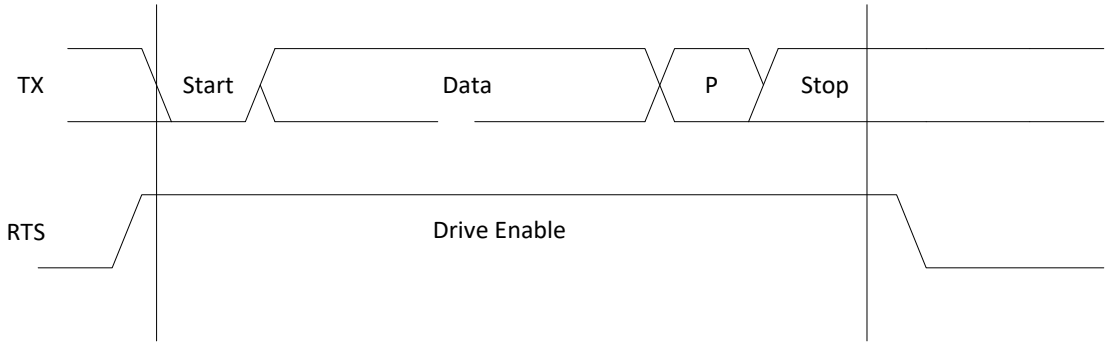
The following figures show the RS-485 transceiver and its timing.

Figure 18-59 RS-485 Transceiver



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 18-60 RS-485 Timing

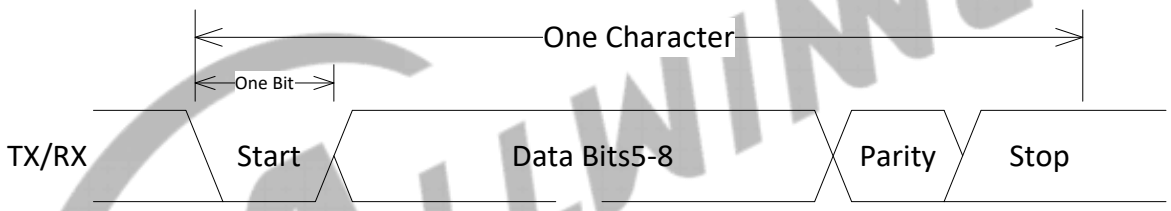


18.10.6 Functional Description

18.10.6.1 Serial Data Format

The following figure shows the UART serial data format. The start bit, data bit, parity bit, and stop bit can be configured.

Figure 18-61 UART Serial Data Format



Start bit: It is the start flag of a data frame. In accordance with the UART protocol, the low level of the TXD signal indicates the start of a data frame. When the UART transmits data, the level needs to hold high.

Data bit: The data bit width can be configured as 5-bit, 6-bit, 7-bit, and 8-bit based on the different applications. If the RS-485 mode is enabled, the data bit width is 8-bit.

Parity bit: It is a 1-bit error correction signal. Parity bit includes odd parity, even parity. The UART can enable and disable the parity bit by setting the UART_LCR register. If RS-485 mode is enabled, the parity bit must be enabled.

Stop bit: It is the stop bit of a data frame. It can be set to 1-bit, 1.5-bit, and 2-bit by the UART_LCR register. The high level of the TXD signal indicates the end of a data frame.

18.10.6.2 Baud and Error Rates

The baud rate is calculated as follows: Baud rate = SCLK/(16 * divisor).

The SCLK is usually APB2 or APS2 and can be set in the section CCMU.

The divisor is the frequency divider of UART, which has 16-bit. The low 8-bit is in the UART_DLL register, and the high 8-bit is in the UART_DLH register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

The following figures show the errors of baud rate in different clock sources.

Table 18-19 Errors of Baud Rate in UART Mode

Clock Source	Divisor	Baud Rate	Over Sampling	Error(%)
24000000	5000	300	16	0
24000000	2500	600	16	0
24000000	1250	1200	16	0
24000000	625	2400	16	0
24000000	313	4800	16	-0.16
24000000	156	9600	16	0.16
24000000	78	19200	16	0.16
24000000	39	38400	16	0.16
24000000	26	57600	16	0.16
24000000	13	115200	16	0.16
48000000	13	230400	16	0.16
60000000	1	3750000	16	0
75000000	5	921600	16	1.725
48000000	3	1000000	16	0
24000000	1	1500000	16	0
48000000	1	3000000	16	0
80000000	1	5000000	16	0
160000000	1	10000000	16	0

Table 18-20 Errors of Baud Rate in IrDA Mode

Clock source	Divisor	Baud rate	Encoding	Error(%)
24000000	5000	300	3/16	0
24000000	2500	600	3/16	0
24000000	1250	1200	3/16	0
24000000	625	2400	3/16	0
24000000	313	4800	3/16	-0.16
24000000	156	9600	3/16	0.16
24000000	78	19200	3/16	0.16
24000000	39	38400	3/16	0.16
24000000	26	57600	3/16	0.16
24000000	13	115200	3/16	0.16

Table 18-21 Errors of Baud Rate in RS485 Mode

Clock source	Divisor	Baud rate	Encoding	Error(%)
24000000	5000	300	16	0
24000000	2500	600	16	0
24000000	1250	1200	16	0
24000000	625	2400	16	0
24000000	313	4800	16	-0.16
24000000	156	9600	16	0.16

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Clock source	Divisor	Baud rate	Encoding	Error(%)
24000000	78	19200	16	0.16
24000000	39	38400	16	0.16
24000000	26	57600	16	0.16
24000000	13	115200	16	0.16
48000000	13	230400	16	0.16
60000000	1	3750000	16	0
75000000	5	921600	16	1.725
48000000	3	1000000	16	0
24000000	1	1500000	16	0
48000000	1	3000000	16	0
80000000	1	5000000	16	0
160000000	1	10000000	16	0

Table 18-22 Errors of Baud Rate in 19.2M and 26M Clock Source

Clock source	Divisor	Baud rate	Encoding	Error(%)
19200000	125	9600	16	0
26000000	14	115200	16	0.75%

18.10.6.3 DLAB Definition

The DLAB control bit (UART_LCR[7]) is the access control bit of the divisor Latch low/high register.

If DLAB is 0, then the 0x00 offset address is the UART_RBR/UART_THR (RX/TX FIFO) register, and the 0x04 offset address is the UART_IER register.

If DLAB is 1, then the 0x00 offset address is the UART_DLL register, and the 0x04 offset address is the UART_DLH register.

When the UART initializes, the divisor needs to be set. Write 1 to DLAB to configure UART_DLL and UART_DLH, and then write 0 to DLAB to configure UART_RBR/UART_THR.

18.10.6.4 CHCFG_AT_BUSY Definition

The function of the CHCFG_AT_BUSY (UART_HALT [1]) and CHANGE_UPDATE (UART_HALT[2]) are as follows.

CHCFG_AT_BUSY: If this bit is enabled and UART is busy, the software can also set the UART controller, such as the UART_LCR, UART_DLH, UART_DLL register.

CHANGE_UPDATE: If CHCFG_AT_BUSY is enabled, and CHANGE_UPDATE is written to 1, the configuration of the UART controller can be updated. After the update completes, the bit is cleared to 0 automatically.

To set the divisor, write 1 to CHCFG_AT_BUSY, and Write 1 to DLAB to configure UART_DLL and UART_DLH, then Write 1 to CHANGE_UPDATE.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.10.6.5 UART_USR Definition

UART_USR is the BUSY flag, used for indicating the UART controller is busy or not.

When TX is sending data, or RX is receiving data, or TX FIFO/RX FIFO is not null, the UART_USR will be asserted. It indicates the UART controller is busy.

18.10.7 Programming Guidelines

The following takes the UART module in the CPUX domain as an example.

18.10.7.1 Initialization

Step 1 System Initialization

- Configure APB1_CLK_REG in the CCU module to set the APB1 bus clock (The clock is 24MHz by default).
- Set UART_BGR_REG[UARTx_GATING] to 1 to enable the module clock, and set UART_BGR_REG[UARTx_RST] to 1 to de-assert the module.

Step 2 UART Controller Initialization

- IO configuration: Configure GPIO multiplex as UART function, and set UART pins to internal pull-up mode (For detail, see the description in the section GPIO.)
- Baud-rate configuration:
  - Set UART baud-rate (refer to the section Baud and Error Rates);
  - Write UART_FCR [FIFOE] to 1 to enable TX/RX FIFO;
  - Write UART_HALT[HALT_TX] to 1 to disable TX transfer;
  - Set UART_LCR[DLAB] to 1, remain default configuration for other bits; set 0x00 offset address to the UART_DLL register, set 0x04 offset address to the UART_DLH register;
  - Write the high 8-bit of divisor to the UART_DLH register, and write the low 8-bit of divisor to the UART_DLL register;
  - Set UART_LCR[DLAB] to 0, remain default configuration for other bits; set 0x00 offset address to the UART_RBR/UART_THR register, set 0x04 offset address to the UART_IER register;
  - Set UART_HALT[HALT_TX] to 0 to enable TX transfer.

Step 3 Controller Parameter Configuration

- Set data width, stop bits, and even/odd parity type by writing the UART_LCR register.
- Reset, enable FIFO and set FIFO trigger condition by writing the UART_FCR register.
- Set the flow control parameter by writing the UART_MCR register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 4 Interrupt Configuration

- Configure UART interrupt vector number to request UART interrupt (Refer to the section GIC for interrupt vector number).
- In DMA mode, write UART_IER to 0 to disable interrupt; write UART_HSK[Handshake configuration] to 0xE5 to set DMA handshake mode; write UART_FCR[DMAM] to 1 to set DMA transmission/reception mode; set DMA parameter and request DMA interrupt according to DMA configuration process.
- In Interrupt mode, configure UART_IER to enable the corresponding interrupt according to requirements: such as transmit (TX) interrupt, receive (RX) interrupt, receive line status interrupt, RS48 interrupt, etc. (Here TX/RX interrupt is usually used).

18.10.7.2 Transmission in DMA Mode

Step 1 Initialize UART model. Refer to section 18.10.7.1 Initialization for initialization steps.

Step 2 Configure UART baud rate by setting UART_DLL and UART_DLH.

Step 3 Configure UART data format by setting UART_LCR.

Step 4 Initialize UART FIFO by setting UART_FCR and UART_FCC.

Step 5 Set PTE and DMA_PTE_RX by setting UART_HALT.

Step 6 Configure DMAC for UART.

Step 7 Wait for DMA done by checking DMAC status.

18.10.7.3 Transmission in Interrupt Mode

Step 1 Initialize UART model. Refer to section 18.10.7.1 for initialization steps.

Step 2 Configure UART baud rate by setting UART_DLL and UART_DLH.

Step 3 Configure UART data format by setting UART_LCR.

Step 4 Initialize UART FIFO by setting UART_FCR and UART_FCC.

Step 5 Set DRQ trigger level for DMA by setting UART_TFL and UART_RFL than set PTE and DMA_PTE_RX in the UART_HALT.

Step 6 Configure UART interrupt by UART_IER and UART_IIR.

Step 7 Wait for UART Interrupt service done.

18.10.7.4 Transmission in RS485 Mode

Step 1 Initialize UART model. Refer to section 18.10.7.1 for initialization steps.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 2 Configure UART baud rate by setting UART_DLL and UART_DLH.

Step 3 Configure UART data format by setting UART_LCR.

Step 4 Initialize UART FIFO by setting UART_FCR and UART_FCC.

Step 5 Configure UART Mode by setting UART_MCR [7:6].

Step 6 Configure UART RS485 Receive data format by setting UART_485_CTL [1:0].

Step 7 Configure UART RS485 Address Match Register by setting UART_RS485_ADDR_MATCH if chose AAD Receive data mode.

Step 8 IF DMA mode is selected, perform steps 5-7 for DMA mode. If not, perform steps 5-7 for CPU mode.

18.10.7.5 FIFO Test Mode

Step 1 Configure FIFO test mode by setting FIFO_TM.

Step 2 Write data to the txfifo by write UART_THR and read data from the txfifo by read READ_TX_FIFO.

Step 3 Write data to the rxfifo by write WRITE_RX_FIFO and read data from the rxfifo by read READ_RX_FIFO.

18.10.8 Register List

Module Name	Base Address
UART0	0x02500000
UART1	0x02501000
UART2	0x02502000
UART3	0x02503000
UART4	0x02504000
UART5	0x02505000
UART6	0x02506000
S_UART0	0x07080000
S_UART1	0x07081000

Register Name	Offset	Description
UART_RBR	0x0000	UART Receive Buffer Register
UART_THR	0x0000	UART Transmit Holding Register
UART_DLL	0x0000	UART Divisor Latch Low Register
UART_DLH	0x0004	UART Divisor Latch High Register
UART_IER	0x0004	UART Interrupt Enable Register
UART_IIR	0x0008	UART Interrupt Identity Register
UART_FCR	0x0008	UART FIFO Control Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
UART_LCR	0x000C	UART Line Control Register
UART_MCR	0x0010	UART Modem Control Register
UART_LSR	0x0014	UART Line Status Register
UART_MSR	0x0018	UART Modem Status Register
UART_SCH	0x001C	UART Scratch Register
UART_USR	0x007C	UART Status Register
UART_TFL	0x0080	UART Transmit FIFO Level Register
UART_RFL	0x0084	UART Receive FIFO Level Register
UART_HSK	0x0088	UART DMA Handshake Configuration Register
UART_DMA_REQ_EN	0x008C	UART DMA Request Enable Register
UART_HALT	0x00A4	UART Halt TX Register
UART_DBG_DLL	0x00B0	UART Debug DLL Register
UART_DBG_DLH	0x00B4	UART Debug DLH Register
UART_485_CTL	0x00C0	UART RS485 Control Configure and Status Register
UART_RS485_ADDR_MATCH	0x00C4	UART RS485 Address Match Register
BUS_IDLE_CHECK	0x00C8	BUS IDLE CHECK Register
TX_DELAY	0x00CC	TX_DELAY Register
FIFO_TM	0x00D4	FIFO TEST MODE Register
READ_TX_FIFO	0x00D8	READ TX FIFO Register
WRITE_RX_FIFO	0x00DC	WRITE RX FIFO Register
READ_RX_FIFO	0x00E0	READ RX FIFO Register
RTSN_RST_DLY_TIME	0x00E4	RS485 RTSN PULL DOWM DELAY TIME Register
UART_FCC	0x00F0	UART FIFO Clock Control Register

18.10.9 Register Description

18.10.9.1 0x0000 UART Receiver Buffer Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UART_RBR
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: UART_RBR
Bit	Read/Write	Default/Hex	Description
8:0	R	0x0	RBR Receiver Buffer Register Data byte received on the serial input port (sin) in UART mode, or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If in FIFO mode and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an overrun error occurs.

18.10.9.2 0x0000 UART Transmit Holding Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UART_THR
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:0	W	0x0	THR Transmit Holding Register Data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. Any attempt to write data when the FIFO is full results in the write data being lost.

18.10.9.3 0x0000 UART Divisor Latch Low Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UART_DLL
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: UART_DLL
Bit	Read/Write	Default/Hex	Description
7:0	R/W	0x0	DLL Divisor Latch Low Lower 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

18.10.9.4 0x0004 UART Divisor Latch High Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: UART_DLH
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	DLH Divisor Latch High Upper 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.10.9.5 0x0004 UART Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: UART_IER
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	PTIME Programmable THRE Interrupt Mode Enable This is used to enable/disable the generation of THRE Interrupt. 0: Disable 1: Enable
6:5	/	/	/
4	R/W	0x0	RS485_INT_EN RS485 Interrupt Enable 0: Disable 1: Enable
3	R/W	0x0	EDSSI Enable Modem Status Interrupt This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0: Disable 1: Enable
2	R/W	0x0	ELSI Enable Receiver Line Status Interrupt This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0: Disable 1: Enable
1	R/W	0x0	ETBEI Enable Transmit Holding Register Empty Interrupt This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: UART_IER
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	ERBFI Enable Received Data Available Interrupt This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 0: Disable 1: Enable

18.10.9.6 0x0008 UART Interrupt Identity Register (Default Value: 0x0000_0001)

Offset: 0x0008			Register Name: UART_IIR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:6	R	0x0	FEFLAG FIFOs Enable Flag This is used to indicate whether the FIFOs are enabled or disabled. 00: Disable 11: Enable
5:4	/	/	/
3:0	R	0x1	IID Interrupt ID This indicates the highest priority pending interrupt which can be one of the following types: 0000: modem status 0001: no interrupt pending 0010: THR empty 0011:RS485 Interrupt pending by UART_485_CTL[6:5] 0100: received data available 0110: receiver line status 0111: busy detect 1100: character timeout Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Interrupt ID	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset
0001	-	None	None	-
0110	Highest	Receiver line status	Overrun/parity/ framing errors or break interrupt	Reading the line status register
0011	Second	RS485 Interrupt	In RS485 mode, receives address data and match setting address	Writes 1 to addr flag to reset
0100	Third	Received data available	Receiver data available (non-FIFO mode or FIFOs disabled) or RCVR FIFO trigger level reached (FIFO mode and FIFOs enabled)	Reading the receiver buffer register (non-FIFO mode or FIFOs disabled) or the FIFO drops below the trigger level (FIFO mode and FIFOs enabled)
1100	Fourth	Character timeout indication	No characters in or out of the RCVR FIFO during the last 4 character times and there is at least 1character in it during this time	Reading the receiver buffer register
0010	Fifth	Transmit holding register empty	Transmitter holding register empty (Program THRE Mode disabled) or XMIT FIFO at or below threshold (Program THRE Mode enabled)	Reading the IIR register (if source of interrupt); or, writing into THR (FIFOs or THRE Mode not selected or disabled) or XMIT FIFO above threshold (FIFOs and THRE Mode selected and enabled).
0000	Sixth	Modem status	Clear to send or data set ready or ring indicator or data carrier detect. Note that if auto flow control mode is enabled, a change in CTS (that is, DCTS set) does not cause an interrupt.	Reading the Modem status Register
0111	Seventh	Busy detect indication	UART_16550_COMPATIBLE = NO and master has tried to write to the Line Control Register while the UART is busy (USR[0] is set to one).	Reading the UART status register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.10.9.7 0x0008 UART FIFO Control Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: UART_FCR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:6	W	0x0	RT RCVR Trigger This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. In auto flow control mode, it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. 00: 1 character in the FIFO 01: FIFO ¼ full 10: FIFO ½ full 11: FIFO-2 less than full
5:4	W	0x0	TFT TX Empty Trigger This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. It also determines when the dma_tx_req_n signal is asserted when in certain modes of operation. 00: FIFO empty 01: 2 characters in the FIFO 10: FIFO ¼ full 11: FIFO ½ full

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: UART_FCR
Bit	Read/Write	Default/Hex	Description
3	W	0x0	DMAM DMA Mode 0: Mode 0 In this mode, when PTE is high and TX FIFO is enable, the TX DMA request will be set when TFL is less than or equal to FIFO Trigger Level (otherwise it will be cleared). When PTE is high and TX FIFO is disabled, the TX DMA request will be set only if THR is empty. If PTE is low, the TX DMA request will be set only if the TX FIFO (TX FIFO Enabled) or THR (TX FIFO Disabled) is empty. When dma_pte_rx is high and RX FIFO is enabled, the rx drq will be set only if RFL is equal to or more than FIFO Trigger Level, otherwise it will be cleared. 1: Mode 1 In this mode, TX FIFO should be enable. If the PTE is high, the TX DMA request will be set when TFL is less than or equal to FIFO Trigger Level; If PTE is low, the TX DMA request will be set when TX FIFO is empty. Once the request is set, it is cleared only when TX FIFO is full. If RFL is equal to or more than FIFO Trigger Level or there is a character timeout , the rx drq will be set; Once the rx drq is set, it is cleared only when RX FIFO(RX FIFO enabled) or RBR(RX FIFO disabled) is empty.
2	W	0x0	XFIFOR XMIT FIFO Reset This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request. It is 'self-clearing'. It is not necessary to clear this bit.
1	W	0x0	RFIFOR RCVR FIFO Reset This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request. It is 'self-clearing'. It is not necessary to clear this bit.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: UART_FCR
Bit	Read/Write	Default/Hex	Description
0	W	0x0	FIFOE Enable FIFOs This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset.

18.10.9.8 0x000C UART Line Control Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: UART_LCR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	DLAB Divisor Latch Access Bit It is writable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. 0: Select RX Buffer Register (RBR) / TX Holding Register(THR) and Interrupt Enable Register (IER) 1: Select Divisor Latch LS Register (DLL) and Divisor Latch MS Register (DLM)
6	R/W	0x0	BC Break Control Bit This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE = Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x000C			Register Name: UART_LCR
Bit	Read/Write	Default/Hex	Description
5:4	R/W	0x0	EPS Even Parity Select It is writable only when UART is not busy (USR[0] is zero) and always writable readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). Setting the LCR[5] is unset to reverse the LCR[4]. 00: Odd Parity 01: Even Parity
3	R/W	0x0	PEN Parity Enable It is writable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0: Parity disabled 1: Parity enabled Note: When use RS485 mode, PEN(LCR[3]) must be set to 1.
2	R/W	0x0	STOP Number of stop bits It is writable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0: 1 stop bit 1: 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x000C			Register Name: UART_LCR
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x0	DLS Data Length Select It is writable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits Note: When use RS485 mode, DLS must be set to 11.

18.10.9.9 0x0010 UART Modem Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: UART_MCR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:6	R/W	0x0	UART_FUNCTION Select IrDA or RS485 00: UART Mode 01: IrDA SIR Mode 10: RS485 Mode 11: Reversed
5	R/W	0x0	AFCE Auto Flow Control Enable When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled. 0: Auto Flow Control Mode is disabled 1: Auto Flow Control Mode is enabled

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0010			Register Name: UART_MCR
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	LOOP Loop Back Mode 0: Normal Mode 1: Loop Back Mode This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3:2	/	/	/
1	R/W	0x0	RTS Request to Send This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. 0: rts_n de-asserted (logic 1) 1: rts_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0010			Register Name: UART_MCR
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	DTR Data Terminal Ready This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n. 0: dtr_n de-asserted (logic 1) 1: dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.

18.10.9.10 0x0014 UART Line Status Register (Default Value: 0x0000_0060)

Offset: 0x0014			Register Name: UART_LSR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R	0x0	FIFOERR RX Data Error in FIFO When FIFOs are disabled, this bit is always 0. When FIFOs are enabled, this bit is set to 1 when there is at least one PE, FE, or BI in the RX FIFO. It is cleared by a read from the LSR register provided there are no subsequent errors in the FIFO.
6	R	0x1	TEMT Transmitter Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register and the TX Shift Register are empty. If the FIFOs are enabled, this bit is set whenever the TX FIFO and the TX Shift Register are empty. In both cases, this bit is cleared when a byte is written to the TX data channel.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: UART_LSR
Bit	Read/Write	Default/Hex	Description
5	R	0x1	THRE TX Holding Register Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register is empty and ready to accept new data and it is cleared when the CPU writes to the TX Holding Register. If the FIFOs are enabled, this bit is set to "1" whenever the TX FIFO is empty and it is cleared when at least one byte is written to the TX FIFO.
4	R	0x0	BI Break Interrupt This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sir_in, is held in a logic '0' state for longer than the sum of *start time* + *data bits* + *parity* + *stop bits*. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of *start time* + *data bits* + *parity* + *stop bits*. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: UART_LSR
Bit	Read/Write	Default/Hex	Description
3	RC	0x0	FE Framing Error This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0: No framing error 1: Framing error Reading the LSR clears the FE bit.
2	RC	0x0	PE Parity Error This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0: No parity error 1: Parity error Reading the LSR clears the PE bit.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: UART_LSR
Bit	Read/Write	Default/Hex	Description
1	RC	0x0	OE Overrun Error This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0: No overrun error 1: Overrun error Reading the LSR clears the OE bit.
0	R	0x0	DR Data Ready This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0: No data ready 1: Data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

18.10.9.11 0x0018 UART Modem Status Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: UART_MSR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R	0x0	DCD Line State of Data Carrier Detect This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. 0: dcd_n input is de-asserted (logic 1) 1: dcd_n input is asserted (logic 0)

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0018			Register Name: UART_MSR
Bit	Read/Write	Default/Hex	Description
6	R	0x0	RI Line State of Ring Indicator This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. 0: ri_n input is de-asserted (logic 1) 1: ri_n input is asserted (logic 0)
5	R	0x0	DSR Line State of Data Set Ready This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with UART. 0: dsr_n input is de-asserted (logic 1) 1: dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).
4	R	0x0	CTS Line State of Clear To Send This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with UART. 0: cts_n input is de-asserted (logic 1) 1: cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0018			Register Name: UART_MSR
Bit	Read/Write	Default/Hex	Description
3	RC	0x0	DDCD Delta Data Carrier Detect This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. 0: No change on dcd_n since last read of MSR 1: Change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. Note: Ff the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted.
2	RC	0x0	TERI Trailing Edge Ring Indicator This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. 0: No change on ri_n since last read of MSR 1: Change on ri_n since last read of MSR Reading the MSR clears the TERI bit.
1	RC	0x0	DDSR Delta Data Set Ready This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. 0: no change on dsr_n since last read of MSR 1: change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). Note: If the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0018			Register Name: UART_MSR
Bit	Read/Write	Default/Hex	Description
0	RC	0x0	DCTS Delta Clear to Send This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0: No change on ctsdsr_n since last read of MSR 1: Change on ctsdsr_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note: If the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted.

18.10.9.12 0x001C UART Scratch Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: UART_SCH
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	SCRATCH_REG Scratch Register This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART.

18.10.9.13 0x007C UART Status Register (Default Value: 0x0000_0006)

Offset: 0x007C			Register Name: UART_USR
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R	0x0	RFF Receive FIFO Full This is used to indicate that the receive FIFO is completely full. 0: Receive FIFO not full 1: Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x007C			Register Name: UART_USR
Bit	Read/Write	Default/Hex	Description
3	R	0x0	RFNE Receive FIFO Not Empty This is used to indicate that the receive FIFO contains one or more entries. 0: Receive FIFO is empty 1: Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.
2	R	0x1	TFE Transmit FIFO Empty This is used to indicate that the transmit FIFO is completely empty. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.
1	R	0x1	TFNF Transmit FIFO Not Full This is used to indicate that the transmit FIFO in not full. 0: Transmit FIFO is full 1: Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	R	0x0	BUSY UART Busy Bit 0: Idle or inactive 1: Busy

18.10.9.14 0x0080 UART Transmit FIFO Level Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: UART_TFL
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:0	R	0x0	TFL Transmit FIFO Level This is indicates the number of data entries in the transmit FIFO.

18.10.9.15 0x0084 UART Receive FIFO Level Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: UART_RFL
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0084			Register Name: UART_RFL
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:0	R	0x0	RFL Receive FIFO Level This indicates the number of data entries in the receive FIFO.

18.10.9.16 0x0088 UART DMA Handshake Configuration Register (Default Value: 0x0000_00A5)

Offset: 0x0088			Register Name: UART_HSK
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0xA5	Handshake configuration 0xA5: DMA wait cycle mode 0xE5: DMA handshake mode

18.10.9.17 0x008C UART DMA Request Enable Register (Default Value: 0x0000_0003)

Offset: 0x008C			Register Name: UART_DMA_REQ_EN
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	DMA Timeout Enable 0: Disable 1: Enable
1	R/W	0x1	DMA TX REQ Enable 0: Disable 1: Enable
0	R/W	0x1	DMA RX REQ Enable 0: Disable 1: Enable

18.10.9.18 0x00A4 UART Halt TX Register (Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: UART_HALT
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00A4			Register Name: UART_HALT
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	DMA_PTE_RX The sending of RX_DRQ. In DMA1 mode, when RFL is more than or equal to trig or receive timeout, send DRQ. In DMA0 mode, when DMA_PTE_RX = 1 and FIFO on, if RFL is more than or equal to trig, send DRQ, else DRQ is cleared. In other cases, once the receive data is valid, send DRQ.
6	R/W	0x0	PTE The sending of TX_REQ. In DMA1 mode (FIFO on), if PTE is set 1, when TFL is less than or equal to trig, send the DMA request. If PTE is set 0, when FIFO is empty, send the DMA request. The DMA request will stop when FIFO is full. In DMA0 mode, if PTE is set 1 and FIFO on, when TFL is less than or equal to trig, send DMA request. If PTE is set 1 and FIFO off, when THR is empty, send DMA request. If PTE is set 0, when FIFO(FIFO Enable) or THR(FIFO Enable) is empty, send DMA request. Otherwise, DMA request is cleared.
5	R/W	0x0	SIR_RX_INVERT SIR Receiver Pulse Polarity Invert 0: Not invert receiver signal 1: Invert receiver signal
4	R/W	0x0	SIR_TX_INVERT SIR Transmit Pulse Polarity Invert 0: Not invert transmit pulse 1: Invert transmit pulse
3	/	/	/
2	R/WAC	0x0	CHANGE_UPDATE After the user using HALT[1] to change the baudrate or LCR configuration, write 1 to update the configuration and waiting this bit self clear to 0 to finish update process. Write 0 to this bit has no effect. 1: Update trigger, Self clear to 0 when finish update.
1	R/W	0x0	CHCFG_AT_BUSY This is an enable bit for the user to change LCR register configuration and baudrate register (DLH and DLL) when the UART is busy (USB[0] is 1). 1: Enable change when busy

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00A4			Register Name: UART_HALT
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	HALT_TX Halt TX This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 0: Halt TX disabled 1: Halt TX enabled Note: If FIFOs are not enabled, the setting has no effect on operation.

18.10.9.19 0x00B0 UART DBG DLL Register (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: UART_DBG_DLL
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	DEBUG DLL

18.10.9.20 0x00B4 UART DBG DLH Register (Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: UART_DBG_DLH
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	DEBUG DLH

18.10.9.21 0x00C0 UART RS485 Control Configure and Status Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: UART_485_CTL
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	aad_broadcast_mode AAD Mode Receive address detect broadcast mode 0: aad broadcast mode 1: not aad broadcast mode(when use this mode need set UART_485_CTL[1:0] is 01 then set UART_485_CTL[8] is 1)

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00C0			Register Name: UART_485_CTL
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	Add_bit_polarity Address bit polarity 0: The address bit is 1 representative the data is address 1: The address bit is 0 representative the data is address
6	R/W1C	0x0	AAD_ADDR_Detected AAD Mode Receive address detect 0: Receive address is different with set 1: Receive address is same with set
5	R/W1C	0x0	Address_detected RS485 Address detect 0: No address detected 1: address detected
4	R/W	0x0	DUPLEX RS485 transfer mode 0: full duplex 1: half duplex
3:2	/	/	/
1:0	R/W	0x0	RCM RS485 Receive mode This is used to choose the RS485 Receive mode 00: RS_9BITM 01: AAD

18.10.9.22 0x00C4 UART RS485 Address Match Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: UART_RS485_ADDR_MATCH
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	AAD_Receive _ADDR AAD Mode Receive address

18.10.9.23 0x00C8 UART RS485 Bus Idle Check Register (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: BUS_IDLE_CHECK
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00C8			Register Name: BUS_IDLE_CHECK
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	BUS_IDLE_CHK_EN 1: Enable bus idle check function 0: Disable bus idle check function
6	R	0x0	BUS_STATUS The flag of bus status 1: Busy 0: Idle
5:0	R	0x0	ADJ_TIME The idle period of bus. The unit is 8*16*Tclk

18.10.9.24 0x00CC UART TX Delay Register (Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: TX_DELAY
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	DLY The delay time between the last stop bit and the next start bit. The unit is 16*Tclk. It is use to control the space between tow bytes in TX.

18.10.9.25 0x00D4 UART FIFO test mode Register (Default Value: 0x0000_0000)

Offset: 0x00D4			Register Name: FIFO_TM
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	FTM FIFO test mode 0: Normal mode 1: FIFO test mode

18.10.9.26 0x00D8 UART Read TX fifo Register (Default Value: 0x0000_0000)

Offset: 0x00D8			Register Name: READ_TX_FIFO
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:0	R	0x0	R_TXFIFO Read TX FIFO In FIFO test mode, reading the address could read the data from the txfifo.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.10.9.27 0x00DC UART WRITE RX FIFO Register (Default Value: 0x0000_0000)

Offset: 0x00DC			Register Name: WRITE_RX_FIFO
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	W	0x0	W_RXFIFO Write RX FIFO In FIFO test mode, writing the address could write the data to the rxfifo.

18.10.9.28 0x00E0 UART READ RX FIFO Register (Default Value: 0x0000_0000)

Offset: 0x00E0			Register Name: READ_RX_FIFO
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	R_RXFIFO Read RX FIFO In FIFO test mode, read the address could read the data from the rxfifo.

18.10.9.29 0x00E4 RS485 RTSN PULL DOWM DELAY TIME Register (Default Value: 0x0000_0000)

Offset: 0x00E4			Register Name: RTSN_RST_DLY_TIME
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	RTSN_RST_DLYT_TIME_ENABLE Rts_n reset delay time enable 0: Not enable 1: Enable
7:0	R/W	0x0	RTSN_RST_DLYT Rts_n Reset Delay Time Rts_n delay number of BCLK to reset in RS485 auto flow control.

18.10.9.30 0x00F0 UART FIFO Clock Control Register (Default Value: 0x0000_0003)

Offset: 0x00F0			Register Name: UART_FCC
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	FIFO Depth Indicates the depth of TX/RX FIFO
7:3	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00F0			Register Name: UART_FCC
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	RXFIFO Clock Mode 0: Sync mode, R/W clocks use apb clock 1: Sync mode, write clock uses apb clock, read clock uses ahb clock
1	R/W	0x1	TX FIFO Clock Enable 0: Clock disable 1: Clock enable
0	R/W	0x1	RX FIFO Clock Enable 0: Clock disable 1: Clock enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.11 Two Wire Interface (TWI)

18.11.1 Overview

This Two Wire Interface (TWI) Controller is used to connect SoC on the 2-wire bus. It supports all the standard 2-wire bus transfer. Master mode and Slave mode are all supported. The TWI has the following features:

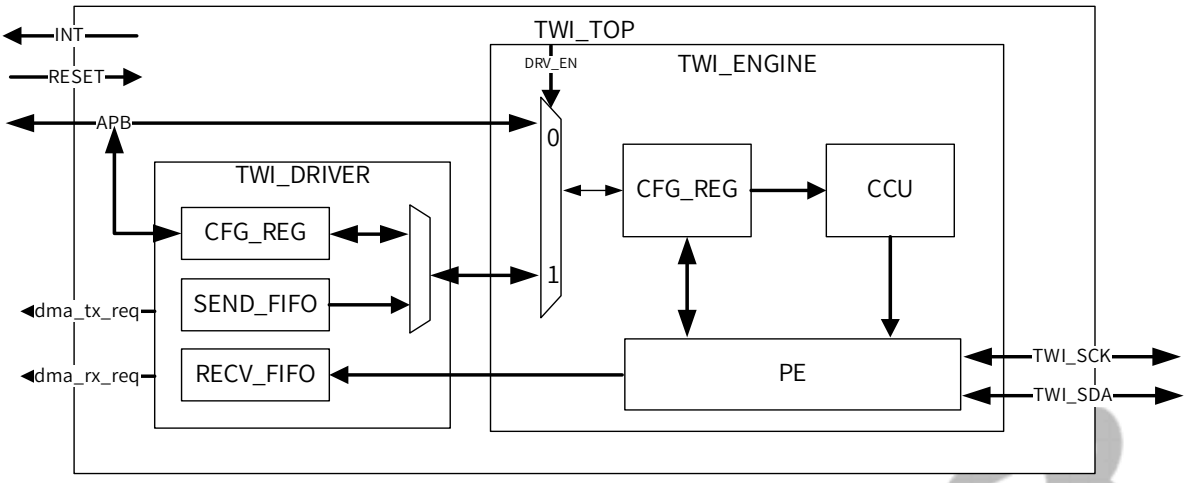
- Up to 16 TWI controllers
  - 13 TWI controllers in CPUX domain: TWI0-12
  - 3 TWI controllers in CPUS domain: S_TWI0-2
- Compliant with I2C bus standard
- Supports master mode or slave mode
- Supports 7-bit standard address and 10-bit extended address.
- Supports standard mode (100 Kbit/s) and high-speed mode (400 Kbit/s).
- Supports general call and start byte.
- Master mode features:
  - Supports the bus arbitration in the case of multiple master devices.
  - Supports clock synchronization and bit and byte waiting.
  - Supports packet transmission and DMA
  - Supports DVFS request adjust voltage
- Salve mode features:
  - Interrupt on address detection

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.11.2 Block Diagram

the following figure shows the block diagram of TWI.

Figure 18-62 TWI Block Diagram



TWI contains the following sub-blocks:

Table 18-23 TWI Sub-blocks

Sub-block	Description
RESET	Module reset signal
INT	Module output interrupt signal
CFG_REG	Module configuration register in TWI
PE	Packet encoding/decoding
CCU	Module clock controller unit
SEND_FIFO	The register address bytes and the written data bytes are buffered in SEND_FIFO
RECV_FIFO	The read data bytes are buffered in RECV_FIFO

The controller includes TWI engine and TWI driver. Each time the TWI engine sends a START signal, a STOP signal, or a BYTE data, or a corresponding ACK, the TWI engine will generate an interrupt, and wait for the CPU to process and clear the interrupt before the next START, STOP, or BYTE, ACK transmission can be performed. Therefore, when a device communication is completed, many interrupts will be generated, and the CPU needs to wait for the previous interrupt before it can configure the next one. The TWI driver defines each communication with the device as a packet transmission. The CPU can directly configure the slave address, register address and data transmission for one or more package transmissions without waiting for interruption, then start the TWI driver, and the TWI driver can control the TWI engine to complete a pre-configured communication, and report an interrupt to the CPU after completion.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.11.3 Clock Sources

Each TWI controller has an input clock source. The following table describes the clock sources for TWI. After selecting a proper clock, users must open the gating of TWI and release the corresponding reset bit.

For more details on the clock setting, configuration, and gating information, see section CCU or PRCM.

Table 18-24 TWI Clock Sources

Module	Clock Sources	Description
TWI	APB	TWI clock source. Refer to CCU for details on APB.
S_TWI	APBS1	TWI clock source. Refer to PRCM for details on APBS1.

18.11.4 External Signals

The following table describes the external signals of the TWI. The TWIn-SCK and TWIn-SDA are bidirectional I/O, when the TWI is configured as a master device, the TWIn-SCK is an output pin; when the TWI is configurable as a slave device, the TWIn-SCK is an input pin. When using TWI, the corresponding PADs are selected as TWI function via section GPIO.

Table 18-25 TWI External Signals

Signal Name	Description	Type
TWI[12:0]-SCK	TWI0 Serial Clock Signal	I/O
TWI[12:0]-SDA	TWI0 Serial Data Signal	I/O
S-TWI[2:0]-SDA	S-TWI0 Serial Data Signal	I/O
S-TWI[2:0]-SCK	S-TWI0 Serial Clock Signal	I/O

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.11.5 Functional Description

18.11.5.1 TWI Engine Master and Slave Mode in TWI Engine

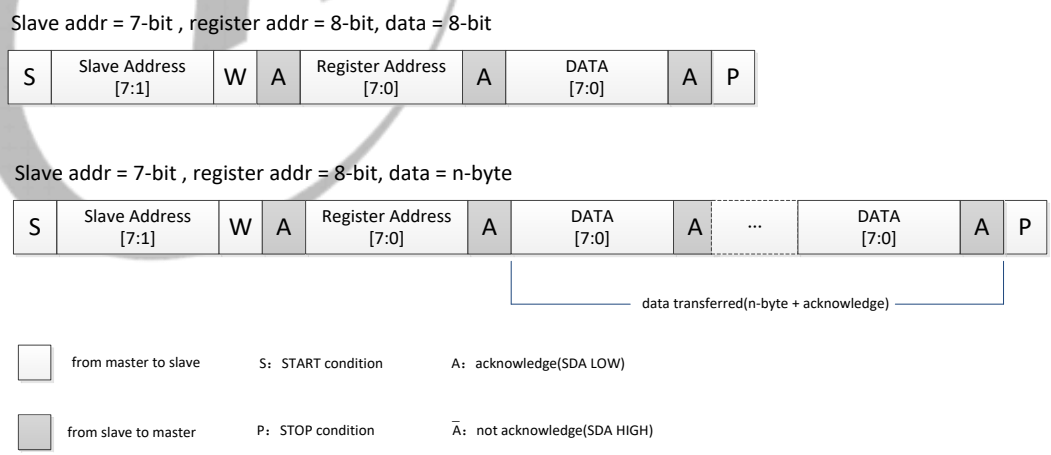
There are four operation modes on the TWI bus which dictates the communications method. They are Master Transmit, Master Receive, Slave Transmit and Slave Receive. In general, CPU host controls TWI Engine by writing commands and data to its registers. TWI Engine transmits an interrupt to CPU when each time a byte transfer is done or a START/STOP conditions is detected. The CPU host can also poll the status register for current status if the interrupt mechanism is not disabled by the CPU host.

When the CPU host wants to start a bus transfer, it initiates a bus START to enter the master mode by setting IM_STA bit in the 2WIRE_CNTR register to high (before it must be low). The TWI Engine will assert INT line and INT_FLAG to indicate a completion for the START condition and each consequent byte transfer. At each interrupt, the micro-processor needs to check the 2WIRE_STAT register for current status. A transfer has to be concluded with STOP condition by setting M_STP bit high.

In Slave Mode, the TWI Engine also constantly samples the bus and looks for its own slave address during addressing cycles. Once a match is found, it is addressed and interrupt the CPU host with the corresponding status. Upon request, the CPU host should read the status, read/write 2WIRE_DATA data register, and set the 2WIRE_CNTR control register. After each byte transfers, a slave device always halts the operation of remote master by holding the next low pulse on SCL line until the microprocessor responds to the status of previous byte transfer or START condition.

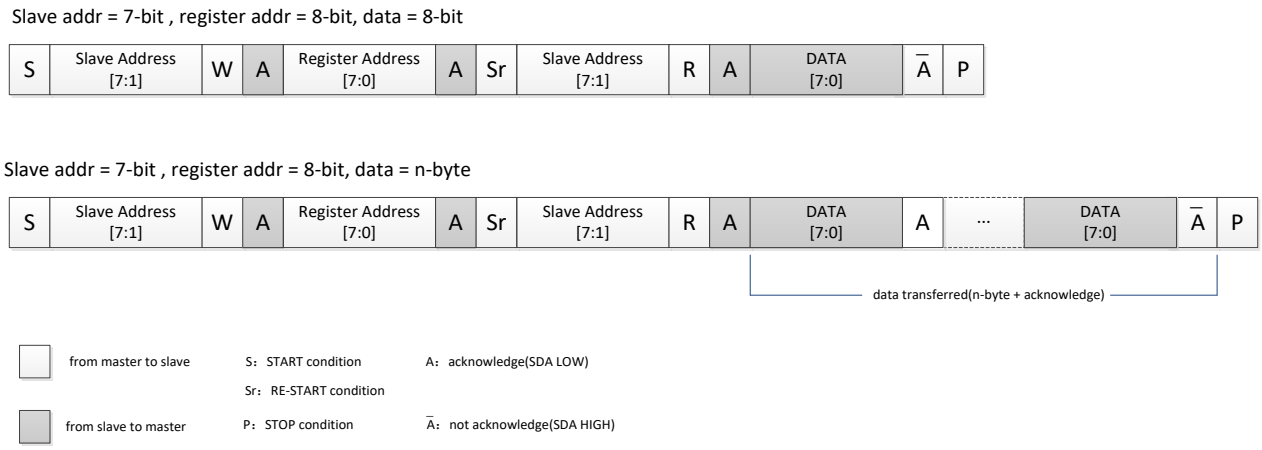
The following figures describes the write/reading timing in 7-bit standard addressing mode.

Figure 18-63 Write Timing in 7-bit Standard Addressing Mode



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 18-64 Read Timing in 7-bit Standard Addressing Mode



The following figures describe the write/read timing in 10-bit extended address mode.

Figure 18-65 Write Timing in 10-bit Extended Addressing Mode

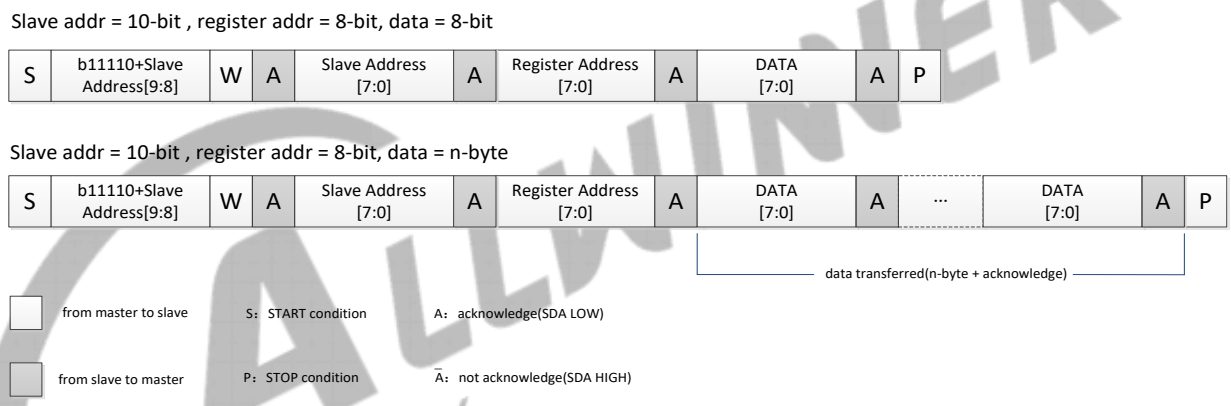
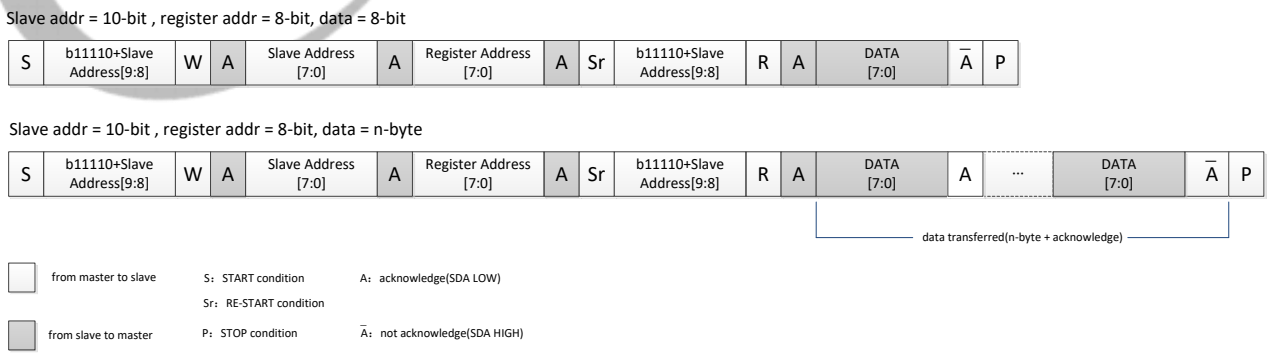


Figure 18-66 Read Timing in 10-bit Extended Addressing Mode

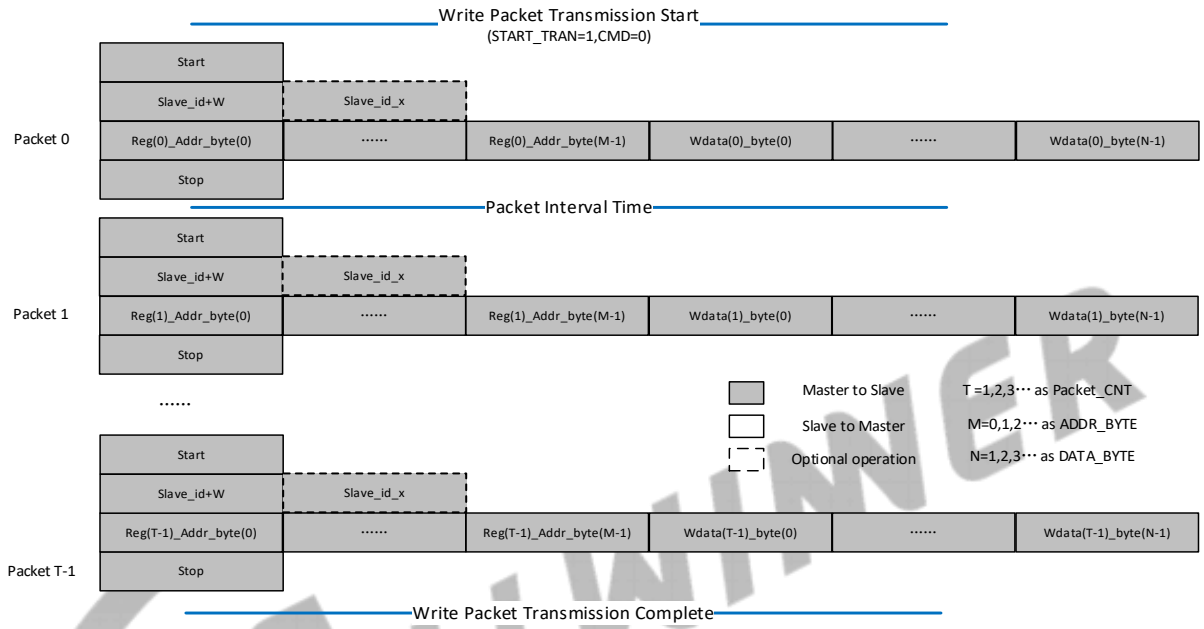


Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.11.5.2 Write/Read Packet Transmission in TWI Driver

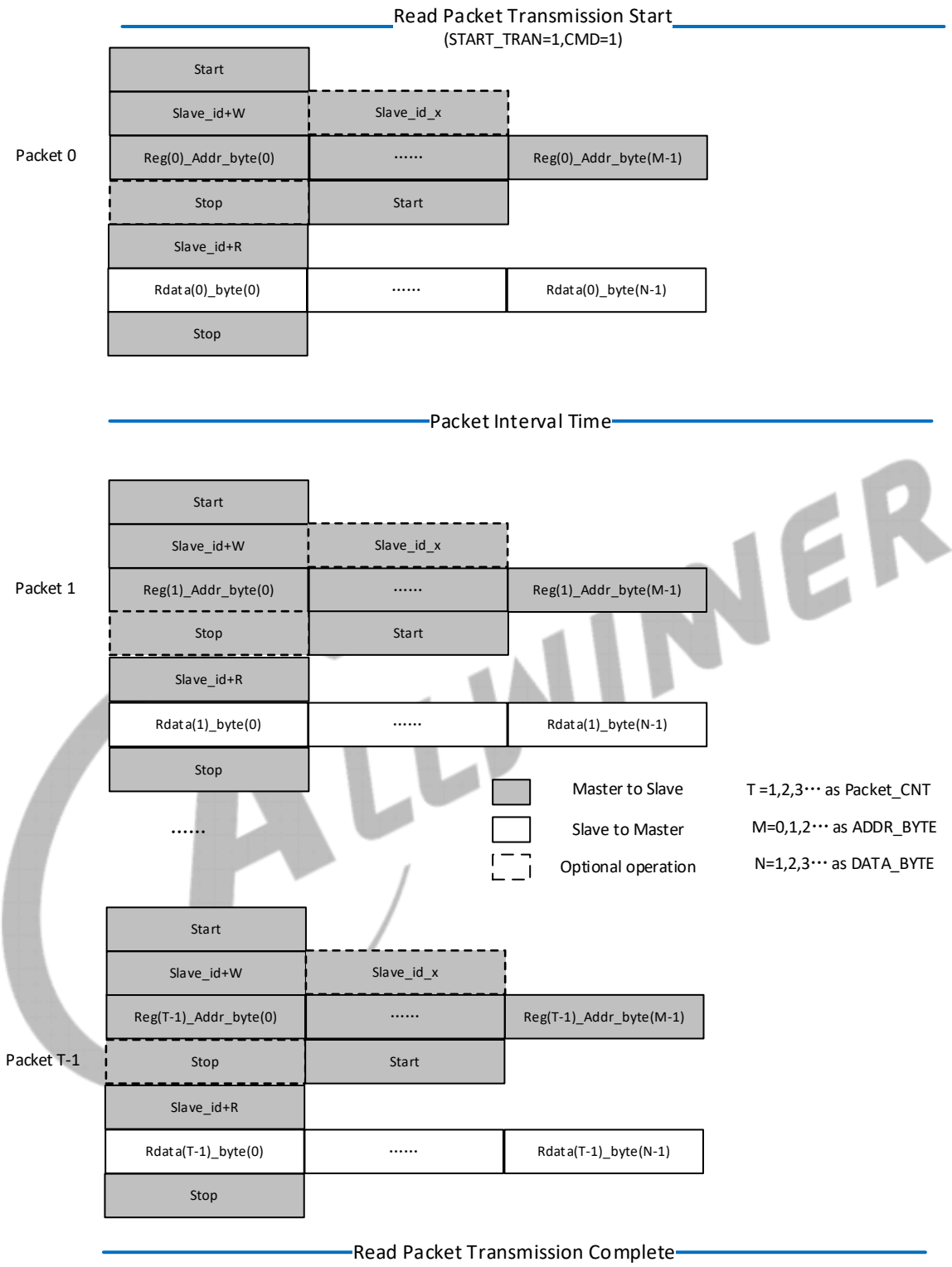
The TWI driver only supports master mode. When the TWI works in master mode, the TWI driver, instead of the CPU host, drives the TWI engine for one or more packet transmission. Packet transmission is defined in the following figures. The register address bytes and the written data bytes are buffered in SEND_FIFO; the read data bytes are buffered in RECV_FIFO.

Figure 18-67 TWI Driver Write Packet Transmission



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 18-68 TWI Driver Read Packet Transmission



18.11.5.3 TWI DVFS

In the master mode, the TWI supports dynamic voltage and frequency scaling (DVFS) request for 8 set of peripherals. Each peripheral has independent interface for communication, which is completed based on the REQ and ACK handshake signals.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

When the peripheral sends the REQ request (REQ=1), TWI will respond to it and transfer the data sent by the peripheral to PMU. After a voltage adjustment finishes, an ACK signal (ACK=1) is sent back. After receiving the high active ACK signal, the peripheral will dis-assert the REQ (REQ=0). Then a voltage adjustment ends.

The primary arbitration is used for arbitrating the REQs simultaneously initiated by multiple peripherals, which can be configured as the poll mode or priority mode.

The secondary arbitration is used for arbitrating the CPU and DVFS device control over the TWI driver, which can be configured as the poll mode.

The read-back function supports configuring whether to read back the transferred data for double check.

The mask function supports configuring the mask bit transferred to PMU. First, initiate the read operation to read back the data, and then mask the corresponding data bit. At last, send out the new data.

18.11.6 Programming Guidelines

The TWI controller operates in an 8-bit data format. The data on the TWI_SDA line is always 8 bits long. At first, the TWI controller sends a start condition. When in the addressing formats of 7-bit, the TWI sends out an 8-bit message which includes 7 MSB slave address and 1 LSB read/write flag. The least significant of the salve address indicates the direction of transmission. When the TWI works in 10-bit slave address mode, the operation will be divided into two steps, for details on the operation, refer to TWI_ADDR and TWI_XADDR.

The following takes the TWI module in the CPUX domain as an example.

18.11.6.1 TWI Engine Initialization

Follow the steps below to initialize the TWI engine.

Step 1 Configure the corresponding GPIO multiplex function as TWI mode.

Step 2 For TWIn, set TWI_BGR_REG [TWIn_GATING] in CCU module to 0 to close TWIn clock.

Step 3 For TWIn, set TWI_BGR_REG [TWIn_RST] in CCU module to 0, then set to 1 to reset TWIn.

Step 4 For TWIn, set TWI_BGR_REG [TWIn_GATING] in CCU module to 1 to open TWIn clock.

Step 5 Configure TWI_CCR[CLK_M] and TWI_CCR[CLK_N] to get the needed rate (The clock source of TWI is from APB1).

Step 6 Configure TWI_CNTR [BUS_EN] and TWI_CNTR [A_ACK]. When using interrupt mode, set TWI_CNTR [INT_EN] to 1, and register the system interrupt through GIC module. In slave mode, configure TWI_ADDR and TWI_XADDR registers to finish TWI initialization configuration.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.11.6.2 Writing Data Operation in TWI Engine

Follow the steps below to write data to the device.

Step 1 Clear TWI_EFR register, and configure TWI_CNTR [M_STA] to 1 to transmit the START signal.

Step 2 After the START signal is transmitted, the first interrupt is triggered, then write device ID to TWI_DATA (For a 10-bit device ID, firstly write the first byte ID, secondly write the second byte ID in the next interrupt).

Step 3 The Interrupt is triggered again after device ID transmission completes, write device data address to be read to TWI_DATA (For a 16-bit address, firstly write the first-byte address, secondly write the second-byte address).

Step 4 Interrupt is triggered after data address transmission completes, write data to be transmitted to TWI_DATA (For consecutive write data operation, every byte transmission completion triggers interrupt, during interrupt write the next byte data to TWI_DATA).

Step 5 After transmission completes, write TWI_CNTR [M_STP] to 1 to transmit the STOP signal and end this write-operation.

18.11.6.3 Reading Data Operation in TWI Engine

Follow the steps below to read data from the device.

Step 1 Clear TWI_EFR register, and set TWI_CNTR [A_ACK] to 1, and configure TWI_CNTR [M_STA] to 1 to transmit the START signal.

Step 2 After the START signal is transmitted, the first interrupt is triggered, then write device ID to TWI_DATA (For a 10-bit device ID, firstly write the first-byte ID, secondly write the second-byte ID in the next interrupt).

Step 3 The Interrupt is triggered again after device ID transmission completes, write device data address to be read to TWI_DATA (For a 16-bit address, firstly write the first-byte address, secondly write the second-byte address).

Step 4 The Interrupt is triggered after data address transmission completes, write TWI_CNTR [M_STA] to 1 to transmit new START signal, and after interrupt triggers, write device ID to TWI_DATA to start read-operation.

Step 5 After device address transmission completes, each receive completion will trigger an interrupt, in turn, read TWI_DATA to get data. When receiving the previous interrupt of the last byte data, clear [A_ACK] to stop acknowledge signal of the last byte.

Step 6 Write TWI_CNTR [M_STP] to 1 to transmit the STOP signal and end this read-operation.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.11.6.4 TWI Driver Initialization

Follow the steps below to initialize the TWI driver.

Step 1 Configure corresponding GPIO multiplex function as TWI mode.

Step 2 For TWIn, set TWI_BGR_REG [TWIn_GATING] in CCU module to 0 to close TWIn clock.

Step 3 For TWIn, set TWI_BGR_REG [TWIn_RST] in CCU module to 0, then set to 1 to reset TWIn.

Step 4 For TWIn, set TWI_BGR_REG [TWIn_GATING] in CCU module to 1 to open TWIn clock.

Step 5 Set TWI_DRV_CTRL [TWI_DRV_EN] to 1 to enable the TWI driver.

Step 6 Configure TWI_DRV_BUS_CTRL [CLK_M] and TWI_DRV_BUS_CTRL [CLK_N] to get the needed rate (The clock source of TWI is from APB1).

Step 7 Set TWI_DRV_CTRL [RESTART_MODE] to 0 and [READ_TRAN_MODE] to 1, and set TWI_DRV_INT_CTRL [TRAN_COM_INT_EN] to 1.

Step 8 When using DMA for data transmission, set TWI_DRV_DMA_CFG [DMA_RX_EN] and TWI_DRV_DMA_CFG [DMA_TX_EN] to 1, and configure TWI_DRV_DMA_CFG [RX_TRIG] and TWI_DRV_DMA_CFG [TX_TRIG] to set the thresholds of RXFIFO and TXFIFO.

To use the DVFS functions, follow the steps below.

Step 1 Configure ADDR_PMU, MASK_EN, and MASK (if needed) of each DVFS device in the TWI_PMU_Dn_CONFIG.

Step 2 Configure the request priority of each DVFS device in the TWI_PMU_ARBITER.

Step 3 Configure the PKT_INTERVAL_PMU, channel enable, readback enable (if needed) in the TWI_PMU_CTL.

Step 4 Set 1 to RR8_Un_ENABLE enable RR8_Un in the TWI_RR8_CTL.

18.11.6.5 Writing Packet Transmission for TWI Driver

Follow the steps below to write package to the device.

Step 1 Configure TWI_DRV_SLV [SLV_ID] to set the device ID, and configure TWI_DRV_SLV [CMD] to 0 to set the write operation.

Step 2 Configure TWI_DRV_FMT [ADDR_BYTE] according to the address width of the device register, and TWI_DRV_FMT [DATA_BYTE] according to the written data count in a packet.

Step 3 Configure TWI_DRV_CFG [PACKET_CNT] to set the written packet number.

Step 4 Configure DMA channel, including TWI TXFIFO, device register address, and the written data.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 5 Set [START_TRAN] to 1 to start TWI Driver transmission.

Step 6 When TWI driver transmission completes, the interrupt is triggered, it indicates that the write packet transmission ends.

18.11.6.6 Reading Packet Transmission for TWI Driver

Step 1 To read package from the device, perform the following steps:

Step 2 Configure TWI_DRV_SLV [SLV_ID] to set the device ID, and configure TWI_DRV_SLV [CMD] to 1 to set the read operation.

Step 3 Configure TWI_DRV_FMT [ADDR_BYTE] according to the address width of the device register, and TWI_DRV_FMT [DATA_BYTE] according to the read data count in a packet.

Step 4 Configure TWI_DRV_CFG [PACKET_CNT] to set the read packet number.

Step 5 Configure DMA channel, including TWI TXFIFO, TWI RXFIFO, device register address and the read data.

Step 6 Set [START_TRAN] to 1 to start TWI Driver transmission.

Step 7 When TWI driver transmission completes, the interrupt is triggered, it indicates that the read packet transmission ends.

18.11.6.7 Slave Mode Configuration

Step 1 Enable A_ACK, BUS_EN, and INT_EN in the TWI_CNTR.

Step 2 Set the TWI_ADDR and TWI_XADDR based on the device address bit width.

18.11.7 TWI0 Register List

Module Name	Base Address	Comments
TWI0	0x02510000	TWI0 register
TWI1	0x02511000	TWI1 register is the same with TWI0
TWI2	0x02512000	TWI2 register is the same with TWI0
TWI3	0x02513000	TWI3 register is the same with TWI0
TWI4	0x02514000	TWI4 register is the same with TWI0
TWI5	0x02515000	TWI5 register is the same with TWI0
TWI6	0x02516000	TWI6 register is the same with TWI0
TWI7	0x02517000	TWI7 register is the same with TWI0
TWI8	0x02518000	TWI8 register is the same with TWI0
TWI9	0x02519000	TWI9 register is the same with TWI0
TWI10	0x0251A000	TWI10 register is the same with TWI0
TWI11	0x0251B000	TWI11 register is the same with TWI0
TWI12	0x0251C000	TWI12 register is the same with TWI0

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Module Name	Base Address	Comments
S_TWI1	0x07084000	S_TWI1 register is the same with TWI0
S_TWI2	0x07085000	S_TWI2 register is the same with TWI0

Register Name	Offset	Description
TWI_ADDR	0x0000	TWI Slave address register
TWI_XADDR	0x0004	TWI Extend address register
TWI_DATA	0x0008	TWI Data register
TWI_CNTR	0x000C	TWI Control register
TWI_STAT	0x0010	TWI Status register
TWI_CCR	0x0014	TWI Clock register
TWI_SRST	0x0018	TWI Soft reset register
TWI_EFR	0x001C	TWI Enhance Feature register
TWI_LCR	0x0020	TWI Line Control register
TWI_DRV_CTRL	0x0200	TWI_DRV Control Register
TWI_DRV_CFG	0x0204	TWI_DRV Transmission Configuration Register
TWI_DRV_SLV	0x0208	TWI_DRV Slave ID Register
TWI_DRV_FMT	0x020C	TWI_DRV Packet Format Register
TWI_DRV_BUS_CTRL	0x0210	TWI_DRV Bus Control Register
TWI_DRV_INT_CTRL	0x0214	TWI_DRV Interrupt Control Register
TWI_DRV_DMA_CFG	0x0218	TWI_DRV DMA Configure Register
TWI_DRV_FIFO_CON	0x021C	TWI_DRV FIFO Content Register
TWI_DRV_SEND_FIFO_ACC	0x0300	TWI_DRV Send Data FIFO Access Register
TWI_DRV_RECV_FIFO_ACC	0x0304	TWI_DRV Receive Data FIFO Access Register

18.11.8 S_TWI0 Register List

Module Name	Base Address	Comments
S_TWI0	0x07083000	S_TWI0 register

Register Name	Offset	Description
TWI_ADDR	0x0000	S_TWI Slave address register
TWI_XADDR	0x0004	S_TWI Extend address register
TWI_DATA	0x0008	S_TWI Data register
TWI_CNTR	0x000C	S_TWI Control register
TWI_STAT	0x0010	S_TWI Status register
TWI_CCR	0x0014	S_TWI Clock register
TWI_SRST	0x0018	S_TWI Soft reset register
TWI_EFR	0x001C	S_TWI Enhance Feature register
TWI_LCR	0x0020	S_TWI Line Control register
TWI_DRV_CTRL	0x0200	S_TWI_DRV Control Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
TWI_DRV_CFG	0x0204	S_TWI_DRV Transmission Configuration Register
TWI_DRV_SLV	0x0208	S_TWI_DRV Slave ID Register
TWI_DRV_FMT	0x020C	S_TWI_DRV Packet Format Register
TWI_DRV_BUS_CTRL	0x0210	S_TWI_DRV Bus Control Register
TWI_DRV_INT_CTRL	0x0214	S_TWI_DRV Interrupt Control Register
TWI_DRV_DMA_CFG	0x0218	S_TWI_DRV DMA Configure Register
TWI_DRV_FIFO_CON	0x021C	S_TWI_DRV FIFO Content Register
TWI_DRV_SEND_FIFO_ACC	0x0300	S_TWI_DRV Send Data FIFO Access Register
TWI_DRV_RECV_FIFO_ACC	0x0304	S_TWI_DRV Receive Data FIFO Access Register
TWI_PMU_CTL	0x0314	S_TWI PMU Control Register
TWI_PMU_INT_CTRL	0x0318	S_TWI PMU Interrupt Control Register
TWI_PMU_INT_STATUS	0x031C	S_TWI PMU Interrupt Status Register
TWI_PMU_ARBITER	0x0320	S_TWI PMU Arbiter Register
TWI_PMU_D0_CONFIG	0x0330	S_TWI PMU Device 0 Configuration Register
TWI_PMU_D1_CONFIG	0x0334	S_TWI PMU Device 1 Configuration Register
TWI_PMU_D2_CONFIG	0x0338	S_TWI PMU Device 2 Configuration Register
TWI_PMU_D3_CONFIG	0x033C	S_TWI PMU Device 3 Configuration Register
TWI_PMU_D4_CONFIG	0x0340	S_TWI PMU Device 4 Configuration Register
TWI_PMU_D5_CONFIG	0x0344	S_TWI PMU Device 5 Configuration Register
TWI_PMU_D6_CONFIG	0x0348	S_TWI PMU Device 6 Configuration Register
TWI_PMU_D7_CONFIG	0x034C	S_TWI PMU Device 7 Configuration Register
TWI_RR8_CTL	0x0380	S_TWI PMU RR8 Control Register

18.11.9 TWI0 Register Description

18.11.9.1 0x0000 TWI0 Slave Address Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TWI_ADDR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:1	R/W	0x0	SLA Slave address 7-bit addressing SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 10-bit addressing 1, 1, 1, 1, 0, SLAX[9:8]
0	R/W	0x0	GCE General call address enable 0: Disable 1: Enable

Notes:

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

For 7-bit addressing:

SLA6 – SLA0 is the 7-bit address of the TWI when is in slave mode. When the TWI receives this address after a START condition, it will generate an interrupt and enter slave mode. (SLA6 corresponds to the first bit received from the TWI bus.) If GCE is set to '1', the TWI will also recognize the general call address (00h).

For 10-bit addressing:

When the address received starts with 11110b, the TWI recognizes this as the first part of a 10-bit address and if the next two bits match ADDR[2:1] (i.e. SLAX9 and SLAX8 of the device's extended address), it sends an ACK. (The device does not generate an interrupt at this point.) If the next byte of the address matches the XADDR register (SLAX7 – SLAX0), the TWI generates an interrupt and goes into slave mode.

18.11.9.2 0x0004 TWI0 Extend Address Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: TWI_XADDR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	SLAX Extend Slave Address SLAX[7:0]

18.11.9.3 0x0008 TWI0 Data Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: TWI_DATA
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	TWI_DATA Data byte for transmitting or received

18.11.9.4 0x000C TWI0 Control Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: TWI_CNTR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	INT_EN Interrupt Enable 0: The interrupt line always low. 1: The interrupt line will go high when INT_FLAG is set.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x000C			Register Name: TWI_CNTR
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	BUS_EN TWI Bus Enable 0: The TWI bus inputs ISDA/ISCL are ignored and the TWI Controller will not respond to any address on the bus. 1: The TWI will respond to calls to its slave address (b) and to the general call address if the GCE bit in the ADDR register is set. **Notes**: In master operation mode, this bit should be set to 1 .
5	R/WAC	0x0	M_STA Master Mode Start When M_STA is set to 1 , TWI Controller will enter master mode and transmit a START condition on the bus when the bus is free. If the M_STA bit is set to 1 when the TWI Controller is already in master mode and one or more bytes have been transmitted, then a repeated START condition will be sent. If the M_STA bit is set to 1 when the TWI is being accessed in slave mode, the TWI will complete the data transfer in slave mode then enter master mode when the bus has been released. The M_STA bit is cleared automatically after a START condition has been sent: writing 0 to this bit has no effect.
4	R/WAC	0x0	M_STP Master Mode Stop If M_STP is set to 1 in master mode, a STOP condition is transmitted on the TWI bus. If the M_STP bit is set to 1 in slave mode, the TWI will behave as if a STOP condition has been received, but no STOP condition will be transmitted on the TWI bus. If both M_STA and M_STP bits are set, the TWI will first transmit the STOP condition (if in master mode) then transmit the START condition. The M_STP bit is cleared automatically: writing a 0 to this bit has no effect.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x000C			Register Name: TWI_CNTR
Bit	Read/Write	Default/Hex	Description
3	R/W1C	0x0	INT_FLAG Interrupt Flag INT_FLAG is automatically set to 1 when any of 28 (out of the possible 29) states is entered (see STAT Register below). The only state that does not set INT_FLAG is state F8h. If the INT_EN bit is set, the interrupt line goes high when IFLG is set to 1 . If the TWI is operating in slave mode, data transfer is suspended when INT_FLAG is set and the low period of the TWI bus clock line (SCL) is stretched until 1 is written to INT_FLAG. The TWI clock line is then released and the interrupt line goes low.
2	R/W	0x0	A_ACK Assert Acknowledge When A_ACK is set to 1 , an Acknowledge (low level on SDA) will be sent during the acknowledge clock pulse on the TWI bus if: 1. Either the whole of a matching 7-bit slave address or the first or the second byte of a matching 10-bit slave address has been received. 2. The general call address has been received and the GCE bit in the ADDR register is set to 1 . 3. A data byte has been received in master or slave mode. When A_ACK is 0 , a Not Acknowledge (high level on SDA) will be sent when a data byte is received in master or slave mode. If A_ACK is cleared to 0 in slave transmitter mode, the byte in the DATA register is assumed to be the last byte . After this byte has been transmitted, the TWI will enter state C8h then return to the idle state (status code F8h) when INT_FLAG is cleared. The TWI will not respond as a slave unless A_ACK is set.
1	/	/	/
0	R/W	0x0	CLK_COUNT_MODE Clock count mode 0: scl clock high period count on oscl 1: scl clock high period count on iscl

Note: For the bits marked with WAC in this register, write 0 to them in case of no operation on these bits.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.11.9.5 0x0010 TWI0 Status Register (Default Value: 0x0000_00F8)

Offset: 0x0010			Register Name: TWI_STAT
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0xF8	STA Status Information Byte Code Status 0x00: Bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK transmitted 0x58: Data byte received in master mode, not ACK transmitted 0x60: Slave address + Write bit received, ACK transmitted 0x68: Arbitration lost in address as master, slave address + Write bit received, ACK transmitted 0x70: General Call address received, ACK transmitted 0x78: Arbitration lost in address as master, General Call address received, ACK transmitted 0x80: Data byte received after slave address received, ACK transmitted 0x88: Data byte received after slave address received, not ACK transmitted 0x90: Data byte received after General Call received, ACK transmitted 0x98: Data byte received after General Call received, not ACK transmitted 0xA0: STOP or repeated START condition received in slave mode 0xA8: Slave address + Read bit received, ACK

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0010			Register Name: TWI_STAT
Bit	Read/Write	Default/Hex	Description
			transmitted 0xB0: Arbitration lost in address as master, slave address + Read bit received, ACK transmitted 0xB8: Data byte transmitted in slave mode, ACK received 0xC0: Data byte transmitted in slave mode, ACK not received 0xC8: Last byte transmitted in slave mode, ACK received 0xD0: Second Address byte + Write bit transmitted, ACK received 0xD8: Second Address byte + Write bit transmitted, ACK not received 0xF8: No relevant status information, INT_FLAG=0 Others: Reserved

18.11.9.6 0x0014 TWI0 Clock Register (Default Value: 0x0000_0080)

Offset: 0x0014			Register Name: TWI_CCR
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	CLK_DUTY_30_EN Enabling duty cycle 30% of Clock as Master 0: bit[7] takes effect 1: 30% Set duty cycle as 30% when the speed reaches 400 Kbit/s.
7	R/W	0x1	CLK_DUTY Setting duty cycle of Clock as Master 0: 50% 1: 40% Set duty cycle as 50% when the speed reaches 100 Kbit/s.
6:3	R/W	0x0	CLK_M Clock M setting

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: TWI_CCR
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x0	CLK_N Clock N setting The TWI bus is sampled by the TWI at the frequency defined by F0: Fsamp = F 0 = Fin / 2^CLK_N The TWI OSCL output frequency, in master mode, is F1 / 10: F1 = F0 / (CLK_M + 1) Foscl = F1 / 10 = Fin / (2^CLK_N * (CLK_M + 1)*10) Specially, Foscl = F1/11 when CLK_M=0 and CLK_DUTY=40% due to the delay of SCL sample debounce. For Example: Fin = 24Mhz (APB clock input) For 400kHz full speed 2Wire, CLK_N = 1, CLK_M=2 F0 = 24M/2^1=12Mhz, F1= F0/(10*(2+1)) = 0.4Mhz For 100Khz standard speed 2Wire, CLK_N=1, CLK_M=11 F0=24M/2^1=12Mhz, F1=F0/(10*(11+1)) = 0.1Mhz

18.11.9.7 0x0018 TWI0 Soft Reset Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: TWI_SRST
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/WAC	0x0	SOFT_RST Soft Reset Write 1 to this bit to reset the TWI and clear to 0 when completing Soft Reset operation.

18.11.9.8 0x001C TWI0 Enhance Feature Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: TWI_EFR
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x001C			Register Name: TWI_EFR
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x0	DBN Data Byte number follow Read Command Control 00: No Data Byte to be written after read command 01: Only 1-byte data to be written after read command 10: Bytes data can be written after read command 11: Bytes data can be written after read command

18.11.9.9 0x0020 TWI0 Line Control Register (Default Value: 0x0000_003A)

Offset: 0x0020			Register Name: TWI_LCR
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R	0x1	SCL_STATE Current state of TWI_SCL 0: Low 1: High
4	R	0x1	SDA_STATE Current state of TWI_SDA 0: Low 1: High
3	R/W	0x1	SCL_CTL TWI_SCL line state control bit When line control mode is enabled (bit[2] set), value of this bit decide the output level of TWI_SCL 0: Output low level 1: Output high level
2	R/W	0x0	SCL_CTL_EN TWI_SCL line state control enable When this bit is set, the state of TWI_SCL is control by the value of bit[3]. 0: Disable TWI_SCL line control mode 1: Enable TWI_SCL line control mode
1	R/W	0x1	SDA_CTL TWI_SDA line state control bit When line control mode is enabled (bit[0] set), value of this bit decide the output level of TWI_SDA 0: Output low level 1: Output high level

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0020			Register Name: TWI_LCR
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	SDA_CTL_EN TWI_SDA line state control enable When this bit is set, the state of TWI_SDA is control by the value of bit[1]. 0: Disable TWI_SDA line control mode 1: Enable TWI_SDA line control mode

18.11.9.10 0x0200 TWI0_DRV Control Register (Default Value: 0x00F8_1000)

Offset: 0x0200			Register Name: TWI_DRV_CTRL
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	START_TRAN Start transmission 0: Transmission idle 1: Start transmission Automatically cleared to 0 when finished. If slave not respond for the expected status over the time defined by TIMEOUT, current transmission will stop. All format setting and data will be loaded from registers and FIFO when transmission start.
30	/	/	/
29	R/W	0x0	RESTART_MODE Restart mode 0: RESTART 1: STOP+START Define the TWI_DRV action after sending register address.
28	R/W	0x0	READ_TRAN_MODE Read transition mode 0: send slave_id+W 1: do not send slave_id+W Setting this bit to 1 if reading from a slave which register width is equal to 0.
27:24	R	0x0	TRAN_RESULT Transition result 000: OK 001: FAIL Other: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0200			Register Name: TWI_DRV_CTRL
Bit	Read/Write	Default/Hex	Description
23:16	R	0xf8	TWI_STA TWI status 0x00: bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK received 0x58: Data byte received in master mode, ACK not received 0x01: Timeout when sending 9th SCL clk Other: Reserved
15:8	R/W	0x10	TIMEOUT_N Timeout number When sending the 9th clock, assert fail signal when slave device did not response after N*F_{SCL} cycles. And software must do a reset to TWI_DRV module and send a stop condition to slave.
7:2	/	/	/
1	R/W	0x0	SOFT_RESET Soft reset 0: Normal 1: reset
0	R/W	0x0	TWI_DRV_EN TWI drive enable 0: Module disable 1: Module enable (only use in TWI Master Mode)

18.11.9.11 0x0204 TWI0_DRV Transmission Configuration Register (Default Value: 0x0000_0001)

Offset: 0x0204	Register Name: TWI_DRV_CFG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PKT_INTERVAL Define the interval between each packet for PKT_INTERVAL F_{SCL} cycles.
15:0	R/W	0x1	PACKET_CNT FIFO data be transmitted as PACKET_CNT packets in current format.

18.11.9.12 0x0208 TWI0_DRV Slave ID Register (Default Value: 0x0000_0000)

Offset: 0x0208			Register Name: TWI_DRV_SLV
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:9	R/W	0x0	SLV_ID Slave device ID 7-bit addressing SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 10-bit addressing 1, 1, 1, 1, 0, SLAX[9:8]
8	R/W	0x0	CMD operation command to slave device 0: write 1: read
7:0	R/W	0x0	SLV_ID_X Slave ID bit 7 to 0 SLAX[7:0], low 8 bits for slave device ID with 10-bit addressing

18.11.9.13 0x020C TWI0_DRV Packet Format Register (Default Value: 0x0001_0001)

Offset: 0x020C			Register Name: TWI_DRV_FMT
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x1	ADDR_BYTE The number of the bytes sent as slave device reg address 0~255
15:0	R/W	0x1	DATA_BYTE The number of the bytes sent or received as data 1~65535

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.11.9.14 0x0210 TWI0_DRV Bus Control Register (Default Value: 0x0000_80C0)

Offset: 0x0210			Register Name: TWI_DRV_BUS_CTRL
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	CLK_DUTY_30_EN Enabling duty cycle 30% of Clock as Master 0: bit[15] takes effect 1: 30% Set duty cycle as 30% when the speed reaches 400 Kbit/s.
16	W	0x0	CLK_COUNT_MODE Clock count mode 0: scl clock high period count on oscl 1: scl clock high period count on iscl
15	R/W	0x1	CLK_DUTY Setting duty cycle of Clock as Master 0: 50% 1: 40% Set duty cycle as 50% when the speed reaches 100 Kbit/s.
14:12	R/W	0x0	CLK_N TWI_DRV bus sampling clock F0 = 24MHz/2^CLK_N
11:8	R/W	0x0	CLK_M TWI_DRV output SCL Frequency is F_{SCL}=F1/10=(F0/(CLK_M+1))/10 Specially, Foscl = F1/11 when CLK_M=0 and CLK_DUTY=40% due to the delay of SCL sample debounce.
7	R	0x1	SCL_STA SCL current status
6	R	0x1	SDA_STA SDA current status
5:4	/	/	/
3	R/W	0x0	SCL_MOV SCL manual output value
2	R/W	0x0	SDA_MOV SDA manual output value
1	R/W	0x0	SCL_MOE SCL manual output en
0	R/W	0x0	SDA_MOE SDA manual output en

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.11.9.15 0x0214 TWI0_DRV Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0214			Register Name: TWI_DRV_INT_CTRL
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19	R/W	0x0	RX_REQ_INT_EN RX request interrupt enable
18	R/W	0x0	TX_REQ_INT_EN TX request interrupt enable
17	R/W	0x0	TRAN_ERR_INT_EN Packet transmission failed interrupt enable
16	R/W	0x0	TRAN_COM_INT_EN Packet transmission completed interrupt enable
15:4	/	/	/
3	R/W1C	0x0	RX_REQ_PD Set when the data byte number in RECV_FIFO reaches RX_TRIG
2	R/W1C	0x0	TX_REQ_PD Set when there is no less than DMA_TX_TRIG empty byte number in SEND_FIFO
1	R/W1C	0x0	TRAN_ERR_PD Packet transmission failed pending
0	R/W1C	0x0	TRAN_COM_PD Packet transmission completed pending

18.11.9.16 0x0218 TWI0_DRV DMA Configure Register (Default Value: 0x0010_0010)

Offset: 0x0218			Register Name: TWI_DRV_DMA_CFG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DMA_RX_EN DMA RX enable
23:22	/	/	/
21:16	R/W	0x10	RX_TRIG RX trigger When DMA_RX_EN set, send DMA RX Req when the data byte number in RECV_FIFO reaches RX_TRIG or Read Packet Transmission completed with RECV_FIFO not empty
15:9	/	/	/
8	R/W	0x0	DMA_TX_EN DMA TX enable
7:6	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0218			Register Name: TWI_DRV_DMA_CFG
Bit	Read/Write	Default/Hex	Description
5:0	R/W	0x10	TX_TRIG TX trigger When DMA_TX_EN set, send DMA TX Req when there is no less than DMA_TX_TRIG empty byte number in SEND_FIFO

18.11.9.17 0x021C TWI0_DRV FIFO Content Register (Default Value: 0x0000_0000)

Offset: 0x021C			Register Name: TWI_DRV_FIFO_CON
Bit	Read/Write	Default/Hex	Description
31:23	/	/	/
22	R/WAC	0x0	RECV_FIFO_CLEAR Set this bit to clear RECV FIFO pointer This bit cleared automatically
21:16	R	0x0	RECV_FIFO_CONTENT The number of data in RECV FIFO
15:7	/	/	/
6	R/WAC	0x0	SEND_FIFO_CLEAR Set this bit to clear SEND_FIFO pointer This bit cleared automatically
5:0	R	0x0	SEND_FIFO_CONTENT The number of data in SEND_FIFO

18.11.9.18 0x0300 TWI0_DRV Send Data FIFO Access Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: TWI_DRV_SEND_FIFO_ACC
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	W	0x0	SEND_DATA_FIFO Data FIFO Address of a 32x8 SEND_FIFO , which stores reg address and data sending to slave device

18.11.9.19 0x0304 TWI0_DRV Receive Data FIFO Access Register (Default Value: 0x0000_0000)

Offset: 0x0304			Register Name: TWI_DRV_RECV_FIFO_ACC
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0304			Register Name: TWI_DRV_RECV_FIFO_ACC
Bit	Read/Write	Default/Hex	Description
7:0	R	0x0	RECV_DATA_FIFO Address of a RECVFIFO which stores data received from slave device

18.11.10 S_TWI0 Register Description

18.11.10.1 0x0000 S_TWI0 Slave Address Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TWI_ADDR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:1	R/W	0x0	SLA Slave address 7-bit addressing SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 10-bit addressing 1, 1, 1, 1, 0, SLAX[9:8]
0	R/W	0x0	GCE General call address enable 0: Disable 1: Enable

Notes:

For 7-bit addressing:

SLA6 – SLA0 is the 7-bit address of the TWI when in slave mode. When the TWI receives this address after a START condition, it will generate an interrupt and enter slave mode. (SLA6 corresponds to the first bit received from the TWI bus.) If GCE is set to '1', the TWI will also recognize the general call address (00h).

For 10-bit addressing:

When the address received starts with 11110b, the TWI recognizes this as the first part of a 10-bit address and if the next two bits match ADDR[2:1] (i.e. SLAX9 and SLAX8 of the device's extended address), it sends an ACK. (The device does not generate an interrupt at this point.) If the next byte of the address matches the XADDR register (SLAX7 – SLAX0), the TWI generates an interrupt and goes into slave mode.

18.11.10.2 0x0004 S_TWI0 Extend Address Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: TWI_XADDR
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: TWI_XADDR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	SLAX Extend Slave Address SLAX[7:0]

18.11.10.3 0x0008 S_TWI0 Data Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: TWI_DATA
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	TWI_DATA Data byte for transmitting or received

18.11.10.4 0x000C S_TWI0 Control Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: TWI_CNTR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	INT_EN Interrupt Enable 0: The interrupt line always low 1: The interrupt line will go high when INT_FLAG is set.
6	R/W	0x0	BUS_EN TWI Bus Enable 0: The TWI bus inputs ISDA/ISCL are ignored and the TWI Controller will not respond to any address on the bus 1: The TWI will respond to calls to its slave address (b) and to the general call address if the GCE bit in the ADDR register is set. Notes: In master operation mode, this bit should be set to 1

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x000C			Register Name: TWI_CNTR
Bit	Read/Write	Default/Hex	Description
5	R/WAC	0x0	M_STA Master Mode Start When M_STA is set to 1 , TWI Controller enters master mode and will transmit a START condition on the bus when the bus is free. If the M_STA bit is set to 1 when the TWI Controller is already in master mode and one or more bytes have been transmitted, then a repeated START condition will be sent. If the M_STA bit is set to 1 when the TWI is being accessed in slave mode, the TWI will complete the data transfer in slave mode then enter master mode when the bus has been released. The M_STA bit is cleared automatically after a START condition has been sent: writing a 0 to this bit has no effect.
4	R/WAC	0x0	M_STP Master Mode Stop If M_STP is set to 1 in master mode, a STOP condition is transmitted on the TWI bus. If the M_STP bit is set to 1 in slave mode, the TWI will behave as if a STOP condition has been received, but no STOP condition will be transmitted on the TWI bus. If both M_STA and M_STP bits are set, the TWI will first transmit the STOP condition (if in master mode) then transmit the START condition. The M_STP bit is cleared automatically: writing a 0 to this bit has no effect.
3	R/W1C	0x0	INT_FLAG Interrupt Flag INT_FLAG is automatically set to 1 when any of 28 (out of the possible 29) states is entered (see STAT Register below). The only state that does not set INT_FLAG is state F8h. If the INT_EN bit is set, the interrupt line goes high when IFLG is set to 1 . If the TWI is operating in slave mode, data transfer is suspended when INT_FLAG is set and the low period of the TWI bus clock line (SCL) is stretched until 1 is written to INT_FLAG. The TWI clock line is then released and the interrupt line goes low.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x000C			Register Name: TWI_CNTR
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	A_ACK Assert Acknowledge When A_ACK is set to 1 , an Acknowledge (low level on SDA) will be sent during the acknowledge clock pulse on the TWI bus if: 1. Either the whole of a matching 7-bit slave address or the first or the second byte of a matching 10-bit slave address has been received. 2. The general call address has been received and the GCE bit in the ADDR register is set to 1 . 3. A data byte has been received in master or slave mode. When A_ACK is 0 , a Not Acknowledge (high level on SDA) will be sent when a data byte is received in master or slave mode. If A_ACK is cleared to 0 in slave transmitter mode, the byte in the DATA register is assumed to be the last byte . After this byte has been transmitted, the TWI will enter state C8h then return to the idle state (status code F8h) when INT_FLAG is cleared. The TWI will not respond as a slave unless A_ACK is set.
1	/	/	/
0	R/W	0x0	CLK_COUNT_MODE Clock count mode 0: scl clock high period count on oscl 1: scl clock high period count on iscl

18.11.10.5 0x0010 S_TWI0 Status Register (Default Value: 0x0000_00F8)

Offset: 0x0010			Register Name: TWI_STAT
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0xF8	STA Status Information Byte Code Status 0x00: Bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0010			Register Name: TWI_STAT
Bit	Read/Write	Default/Hex	Description
			received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK transmitted 0x58: Data byte received in master mode, not ACK transmitted 0x60: Slave address + Write bit received, ACK transmitted 0x68: Arbitration lost in address as master, slave address + Write bit received, ACK transmitted 0x70: General Call address received, ACK transmitted 0x78: Arbitration lost in address as master, General Call address received, ACK transmitted 0x80: Data byte received after slave address received, ACK transmitted 0x88: Data byte received after slave address received, not ACK transmitted 0x90: Data byte received after General Call received, ACK transmitted 0x98: Data byte received after General Call received, not ACK transmitted 0xA0: STOP or repeated START condition received in slave mode 0xA8: Slave address + Read bit received, ACK transmitted 0xB0: Arbitration lost in address as master, slave address + Read bit received, ACK transmitted 0xB8: Data byte transmitted in slave mode, ACK received 0xC0: Data byte transmitted in slave mode, ACK not received 0xC8: Last byte transmitted in slave mode, ACK received 0xD0: Second Address byte + Write bit transmitted, ACK received

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0010			Register Name: TWI_STAT
Bit	Read/Write	Default/Hex	Description
			0xD8: Second Address byte + Write bit transmitted, ACK not received 0xF8: No relevant status information, INT_FLAG=0 Others: Reserved

18.11.10.6 0x0014 S_TWI0 Clock Register (Default Value: 0x0000_0080)

Offset: 0x0014			Register Name: TWI_CCR
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	CLK_DUTY_30_EN Enabling duty cycle 30% of Clock as Master 0: bit[7] takes effect 1: 30% Set duty cycle as 30% when the rate reaches 400 Kbit/s.
7	R/W	0x1	CLK_DUTY Setting duty cycle of Clock as Master 0: 50% 1: 40% Set duty cycle as 50% when the rate reaches 100 Kbit/s.
6:3	R/W	0x0	CLK_M Clock M setting

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: TWI_CCR
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x0	CLK_N Clock N setting The TWI bus is sampled by the TWI at the frequency defined by F0: Fsamp = F 0 = Fin / 2^CLK_N The TWI OSCL output frequency, in master mode, is F1 / 10: F1 = F0 / (CLK_M + 1) Foscl = F1 / 10 = Fin / (2^CLK_N * (CLK_M + 1)*10) Specially, Foscl = F1/11 when CLK_M=0 and CLK_DUTY=40% due to the delay of SCL sample debounce. For Example: Fin = 24Mhz (APB clock input) For 400kHz full speed 2Wire, CLK_N = 1, CLK_M=2 F0 = 24M/2^1=12Mhz, F1= F0/(10*(2+1)) = 0.4Mhz For 100Khz standard speed 2Wire, CLK_N=1, CLK_M=11 F0=24M/2^1=12Mhz, F1=F0/(10*(11+1)) = 0.1Mhz

18.11.10.7 0x0018 S_TWI0 Soft Reset Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: TWI_SRST
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/WAC	0x0	SOFT_RST Soft Reset Write 1 to this bit to reset the TWI and clear to 0 when completing Soft Reset operation.

18.11.10.8 0x001C S_TWI0 Enhance Feature Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: TWI_EFR
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x001C			Register Name: TWI_EFR
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x0	DBN Data Byte number follow Read Command Control 00: No Data Byte to be written after read command 01: Only 1-byte data to be written after read command 10: Bytes data can be written after read command 11: Bytes data can be written after read command

18.11.10.9 0x0020 S_TWI0 Line Control Register (Default Value: 0x0000_003A)

Offset: 0x0020			Register Name: TWI_LCR
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R	0x1	SCL_STATE Current state of TWI_SCL 0: Low 1: High
4	R	0x1	SDA_STATE Current state of TWI_SDA 0: Low 1: High
3	R/W	0x1	SCL_CTL TWI_SCL line state control bit When line control mode is enabled (bit[2] set), value of this bit decide the output level of TWI_SCL 0: Output low level 1: Output high level
2	R/W	0x0	SCL_CTL_EN TWI_SCL line state control enable When this bit is set, the state of TWI_SCL is control by the value of bit[3]. 0: Disable TWI_SCL line control mode 1: Enable TWI_SCL line control mode
1	R/W	0x1	SDA_CTL TWI_SDA line state control bit When line control mode is enabled (bit[0] set), value of this bit decide the output level of TWI_SDA 0: Output low level 1: Output high level

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0020			Register Name: TWI_LCR
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	SDA_CTL_EN TWI_SDA line state control enable When this bit is set, the state of TWI_SDA is control by the value of bit[1]. 0: Disable TWI_SDA line control mode 1: Enable TWI_SDA line control mode

18.11.10.10 0x0200 S_TWI0_DRV Control Register (Default Value: 0x00F8_1000)

Offset: 0x0200			Register Name: TWI_DRV_CTRL
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	START_TRAN Start transmission 0: Transmission idle 1: Start transmission Automatically cleared to 0 when finished. If slave not respond for the expected status over the time defined by TIMEOUT, current transmission will stop. All format setting and data will be loaded from registers and FIFO when transmission start.
30	/	/	/
29	R/W	0x0	RESTART_MODE Restart mode 0: RESTART 1: STOP+START Define the TWI_DRV action after sending register address.
28	R/W	0x0	READ_TRAN_MODE Read transition mode 0: send slave_id+W 1: do not send slave_id+W Setting this bit to 1 if reading from a slave which register width is equal to 0.
27:24	R	0x0	TRAN_RESULT Transition result 000: OK 001: FAIL Other: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0200			Register Name: TWI_DRV_CTRL
Bit	Read/Write	Default/Hex	Description
23:16	R	0xf8	TWI_STA TWI status 0x00: bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK received 0x58: Data byte received in master mode, ACK not received 0x01: Timeout when sending 9th SCL clk Other: Reserved
15:8	R/W	0x10	TIMEOUT_N Timeout number When sending the 9th clock, assert fail signal when slave device did not response after N*F_{SCL} cycles. And software must do a reset to TWI_DRV module and send a stop condition to slave.
7:2	/	/	/
1	R/W	0x0	SOFT_RESET Soft reset 0: Normal 1: reset
0	R/W	0x0	TWI_DRV_EN TWI drive enable 0: Module disable 1: Module enable (only use in TWI Master Mode)

18.11.10.11 0x0204 S_TWI0_DRV Transmission Configuration Register (Default Value: 0x0000_0001)

Offset: 0x0204	Register Name: TWI_DRV_CFG

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PKT_INTERVAL Define the interval between each packet for PKT_INTERVAL F_{SCL} cycles.
15:0	R/W	0x1	PACKET_CNT FIFO data be transmitted as PACKET_CNT packets in current format.

18.11.10.12 0x0208 S_TWI0_DRV Slave ID Register (Default Value: 0x0000_0000)

Offset: 0x0208			Register Name: TWI_DRV_SLV
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:9	R/W	0x0	SLV_ID Slave device ID 7-bit addressing SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 10-bit addressing 1, 1, 1, 1, 0, SLAX[9:8]
8	R/W	0x0	CMD operation command to slave device 0: write 1: read
7:0	R/W	0x0	SLV_ID_X Slave ID bit 7 to 0 SLAX[7:0], low 8 bits for slave device ID with 10-bit addressing

18.11.10.13 0x020C S_TWI0_DRV Packet Format Register (Default Value: 0x0001_0001)

Offset: 0x020C			Register Name: TWI_DRV_FMT
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x1	ADDR_BYTE The number of the bytes sent as slave device reg address 0~255
15:0	R/W	0x1	DATA_BYTE The number of the bytes sent or received as data 1~65535

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.11.10.14 0x0210 S_TWI0_DRV Bus Control Register (Default Value: 0x0000_80C0)

Offset: 0x0210			Register Name: TWI_DRV_BUS_CTRL
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	CLK_DUTY_30_EN Enabling duty cycle 30% of Clock as Master 0: bit[15] takes effect 1: 30% Set duty cycle as 30% when the rate reaches 400 Kbit/s.
16	W	0x0	CLK_COUNT_MODE Clock count mode 0: scl clock high period count on oscl 1: scl clock high period count on iscl
15	R/W	0x1	CLK_DUTY Setting duty cycle of Clock as Master 0: 50% 1: 40% Set duty cycle as 50% when the rate reaches 100 Kbit/s.
14:12	R/W	0x0	CLK_N TWI_DRV bus sampling clock F0 = 24MHz/2^CLK_N
11:8	R/W	0x0	CLK_M TWI_DRV output SCL Frequency is F_{SCL}=F1/10=(F0/(CLK_M+1))/10 Specially, Foscl = F1/11 when CLK_M=0 and CLK_DUTY=40% due to the delay of SCL sample debounce.
7	R	0x1	SCL_STA SCL current status
6	R	0x1	SDA_STA SDA current status
5:4	/	/	/
3	R/W	0x0	SCL_MOV SCL manual output value
2	R/W	0x0	SDA_MOV SDA manual output value
1	R/W	0x0	SCL_MOE SCL manual output en
0	R/W	0x0	SDA_MOE SDA manual output en

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.11.10.15 0x0214 S_TWI0_DRV Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0214			Register Name: TWI_DRV_INT_CTRL
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19	R/W	0x0	RX_REQ_INT_EN RX request interrupt enable
18	R/W	0x0	TX_REQ_INT_EN TX request interrupt enable
17	R/W	0x0	TRAN_ERR_INT_EN Packet transmission failed interrupt enable
16	R/W	0x0	TRAN_COM_INT_EN Packet transmission completed interrupt enable
15:4	/	/	/
3	R/W1C	0x0	RX_REQ_PD Set when the data byte number in RECV_FIFO reaches RX_TRIG
2	R/W1C	0x0	TX_REQ_PD Set when there is no less than DMA_TX_TRIG empty byte number in SEND_FIFO
1	R/W1C	0x0	TRAN_ERR_PD Packet transmission failed pending
0	R/W1C	0x0	TRAN_COM_PD Packet transmission completed pending

18.11.10.16 0x0218 S_TWI0_DRV DMA Configure Register (Default Value: 0x0010_0010)

Offset: 0x0218			Register Name: TWI_DRV_DMA_CFG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DMA_RX_EN DMA RX enable
23:22	/	/	/
21:16	R/W	0x10	RX_TRIG RX trigger When DMA_RX_EN set, send DMA RX Req when the data byte number in RECV_FIFO reaches RX_TRIG or Read Packet Transmission completed with RECV_FIFO not empty
15:9	/	/	/
8	R/W	0x0	DMA_TX_EN DMA TX enable
7:6	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0218			Register Name: TWI_DRV_DMA_CFG
Bit	Read/Write	Default/Hex	Description
5:0	R/W	0x10	TX_TRIG TX trigger When DMA_TX_EN set, send DMA TX Req when there is no less than DMA_TX_TRIG empty byte number in SEND_FIFO

18.11.10.17 0x021C S_TWI0_DRV FIFO Content Register (Default Value: 0x0000_0000)

Offset: 0x021C			Register Name: TWI_DRV_FIFO_CON
Bit	Read/Write	Default/Hex	Description
31:23	/	/	/
22	R/WAC	0x0	RECV_FIFO_CLEAR Set this bit to clear RECV FIFO pointer This bit cleared automatically
21:16	R	0x0	RECV_FIFO_CONTENT The number of data in RECV FIFO
15:7	/	/	/
6	R/WAC	0x0	SEND_FIFO_CLEAR Set this bit to clear SEND_FIFO pointer This bit cleared automatically
5:0	R	0x0	SEND_FIFO_CONTENT The number of data in SEND_FIFO

18.11.10.18 0x0300 S_TWI0_DRV Send Data FIFO Access Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: TWI_DRV_SEND_FIFO_ACC
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	W	0x0	SEND_DATA_FIFO Data FIFO Address of a 32x8 SEND_FIFO , which stores reg address and data sending to slave device

18.11.10.19 0x0304 S_TWI0_DRV Receive Data FIFO Access Register (Default Value: 0x0000_0000)

Offset: 0x0304			Register Name: TWI_DRV_RECV_FIFO_ACC
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0304			Register Name: TWI_DRV_RECV_FIFO_ACC
Bit	Read/Write	Default/Hex	Description
7:0	R	0x0	RECV_DATA_FIFO Address of a RECVFIFO which stores data received from slave device

18.11.10.20 0x0314 S_TWI0 PMU Control Register (Default Value: 0x0000_0000)

Offset: 0x0314			Register Name: TWI_PMU_CTL
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PKT_INTERVAL_PMU Define the interval between each dvfs packet for PKT_INTERVAL_PMU F_{SCL} cycles.
15	R/W	0x0	READ_BACK_D7_ENABLE The enable bit of read back function of Device 7 0: Disable 1: Enable If this bit is set to 1, TWI will read back the values of corresponding registers when it transfers a data package to PMU. The read-back values are used for confirm whether the data package transfer succeeds or not.
14	R/W	0x0	READ_BACK_D6_ENABLE The enable bit of read back function of Device 6 0: Disable 1: Enable
13	R/W	0x0	READ_BACK_D5_ENABLE The enable bit of read back function of Device 5 0: Disable 1: Enable
12	R/W	0x0	READ_BACK_D4_ENABLE The enable bit of read back function of Device 4 0: Disable 1: Enable
11	R/W	0x0	READ_BACK_D3_ENABLE The enable bit of read back function of Device 3 0: Disable 1: Enable
10	R/W	0x0	READ_BACK_D2_ENABLE The enable bit of read back function of Device 2 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0314			Register Name: TWI_PMU_CTL
Bit	Read/Write	Default/Hex	Description
9	R/W	0x0	READ_BACK_D1_ENABLE The enable bit of read back function of Device 1 0: Disable 1: Enable
8	R/W	0x0	READ_BACK_D0_ENABLE The enable bit of read back function of Device 0 0: Disable 1: Enable
7	R/W	0x0	D7_EN Device 7 Enable 0: Disable 1: Enable Disabling Device 7 will close its DVFS function.
6	R/W	0x0	D6_EN Device 6 Enable 0: Disable 1: Enable Disabling Device 6 will close its DVFS function.
5	R/W	0x0	D5_EN Device 5 Enable 0: Disable 1: Enable Disabling Device 5 will close its DVFS function.
4	R/W	0x0	D4_EN Device 4 Enable 0: Disable 1: Enable Disabling Device 4 will close its DVFS function.
3	R/W	0x0	D3_EN Device 3 Enable 0: Disable 1: Enable Disabling Device 3 will close its DVFS function.
2	R/W	0x0	D2_EN Device 2 Enable 0: Disable 1: Enable Disabling Device 2 will close its DVFS function.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0314			Register Name: TWI_PMU_CTL
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	D1_EN Device 1 Enable 0: Disable 1: Enable Disabling Device 1 will close its DVFS function.
0	R/W	0x0	D0_EN Device 0 Enable 0: Disable 1: Enable Disabling Device 0 will close its DVFS function.

18.11.10.21 0x0318 S_TWI0 PMU Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0318			Register Name: TWI_PMU_INT_CTRL
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	RECV_ERR_INT_EN_PMU7 Packet receive failed interrupt enable This bit only takes effect when it is set to 1.
22	R/W	0x0	RECV_ERR_INT_EN_PMU6 Packet receive failed interrupt enable This bit only takes effect when it is set to 1.
21	R/W	0x0	RECV_ERR_INT_EN_PMU5 Packet receive failed interrupt enable This bit only takes effect when it is set to 1.
20	R/W	0x0	RECV_ERR_INT_EN_PMU4 Packet receive failed interrupt enable This bit only takes effect when it is set to 1.
19	R/W	0x0	RECV_ERR_INT_EN_PMU3 Packet receive failed interrupt enable This bit only takes effect when it is set to 1.
18	R/W	0x0	RECV_ERR_INT_EN_PMU2 Packet receive failed interrupt enable This bit only takes effect when it is set to 1.
17	R/W	0x0	RECV_ERR_INT_EN_PMU1 Packet receive failed interrupt enable This bit only takes effect when it is set to 1.
16	R/W	0x0	RECV_ERR_INT_EN_PMU0 Packet receive failed interrupt enable This bit only takes effect when it is set to 1.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0318			Register Name: TWI_PMU_INT_CTRL
Bit	Read/Write	Default/Hex	Description
15	R/W	0x0	TRAN_OK_INT_EN_PMU7 Packet transmit completed interrupt enable This bit only takes effect when it is set to 1.
14	R/W	0x0	TRAN_OK_INT_EN_PMU6 Packet transmit completed interrupt enable This bit only takes effect when it is set to 1.
13	R/W	0x0	TRAN_OK_INT_EN_PMU5 Packet transmit completed interrupt enable This bit only takes effect when it is set to 1.
12	R/W	0x0	TRAN_OK_INT_EN_PMU4 Packet transmit completed interrupt enable This bit only takes effect when it is set to 1.
11	R/W	0x0	TRAN_OK_INT_EN_PMU3 Packet transmit completed interrupt enable This bit only takes effect when it is set to 1.
10	R/W	0x0	TRAN_OK_INT_EN_PMU2 Packet transmit completed interrupt enable This bit only takes effect when it is set to 1.
9	R/W	0x0	TRAN_OK_INT_EN_PMU1 Packet transmit completed interrupt enable This bit only takes effect when it is set to 1.
8	R/W	0x0	TRAN_OK_INT_EN_PMU0 Packet transmit completed interrupt enable This bit only takes effect when it is set to 1.
7	R/W	0x0	TRAN_ERR_INT_EN_PMU7 Packet transmit failed interrupt enable This bit only takes effect when it is set to 1.
6	R/W	0x0	TRAN_ERR_INT_EN_PMU6 Packet transmit failed interrupt enable This bit only takes effect when it is set to 1.
5	R/W	0x0	TRAN_ERR_INT_EN_PMU5 Packet transmit failed interrupt enable This bit only takes effect when it is set to 1.
4	R/W	0x0	TRAN_ERR_INT_EN_PMU4 Packet transmit failed interrupt enable This bit only takes effect when it is set to 1.
3	R/W	0x0	TRAN_ERR_INT_EN_PMU3 Packet transmit failed interrupt enable This bit only takes effect when it is set to 1.
2	R/W	0x0	TRAN_ERR_INT_EN_PMU2 Packet transmit failed interrupt enable This bit only takes effect when it is set to 1.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0318			Register Name: TWI_PMU_INT_CTRL
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	TRAN_ERR_INT_EN_PMU1 Packet transmit failed interrupt enable This bit only takes effect when it is set to 1.
0	R/W	0x0	TRAN_ERR_INT_EN_PMU0 Packet transmit failed interrupt enable This bit only takes effect when it is set to 1.

18.11.10.22 0x031C S_TWI0 PMU Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x031C			Register Name: TWI_PMU_INT_STATUS
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W1C	0x0	RECV_ERR_PD_PMU7 Packet receive failed pending of PMU device 7
22	R/W1C	0x0	RECV_ERR_PD_PMU6 Packet receive failed pending of PMU device 6
21	R/W1C	0x0	RECV_ERR_PD_PMU5 Packet receive failed pending of PMU device 5
20	R/W1C	0x0	RECV_ERR_PD_PMU4 Packet receive failed pending of PMU device 4
19	R/W1C	0x0	RECV_ERR_PD_PMU3 Packet receive failed pending of PMU device 3
18	R/W1C	0x0	RECV_ERR_PD_PMU2 Packet receive failed pending of PMU device 2
17	R/W1C	0x0	RECV_ERR_PD_PMU1 Packet receive failed pending of PMU device 1
16	R/W1C	0x0	RECV_ERR_PD_PMU0 Packet receive failed pending of PMU device 0
15	R/W1C	0x0	TRAN_OK_PD_PMU7 Packet transmit completed pending of PMU device 7
14	R/W1C	0x0	TRAN_OK_PD_PMU6 Packet transmit completed pending of PMU device 6
13	R/W1C	0x0	TRAN_OK_PD_PMU5 Packet transmit completed pending of PMU device 5
12	R/W1C	0x0	TRAN_OK_PD_PMU4 Packet transmit completed pending of PMU device 4
11	R/W1C	0x0	TRAN_OK_PD_PMU3 Packet transmit completed pending of PMU device 3
10	R/W1C	0x0	TRAN_OK_PD_PMU2 Packet transmit completed pending of PMU device 2

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x031C			Register Name: TWI_PMU_INT_STATUS
Bit	Read/Write	Default/Hex	Description
9	R/W1C	0x0	TRAN_OK_PD_PMU1 Packet transmit completed pending of PMU device 1
8	R/W1C	0x0	TRAN_OK_PD_PMU0 Packet transmit completed pending of PMU device 0
7	R/W1C	0x0	TRAN_ERR_PD_PMU7 Packet transmit failed pending of PMU device 7
6	R/W1C	0x0	TRAN_ERR_PD_PMU6 Packet transmit failed pending of PMU device 6
5	R/W1C	0x0	TRAN_ERR_PD_PMU5 Packet transmit failed pending of PMU device 5
4	R/W1C	0x0	TRAN_ERR_PD_PMU4 Packet transmit failed pending of PMU device 4
3	R/W1C	0x0	TRAN_ERR_PD_PMU3 Packet transmit failed pending of PMU device 3
2	R/W1C	0x0	TRAN_ERR_PD_PMU2 Packet transmit failed pending of PMU device 2
1	R/W1C	0x0	TRAN_ERR_PD_PMU1 Packet transmit failed pending of PMU device 1
0	R/W1C	0x0	TRAN_ERR_PD_PMU0 Packet transmit failed pending of PMU device 0

18.11.10.23 0x0320 S_TWI0 PMU Arbiter Register (Default Value: 0x0000_0000)

Offset: 0x0320			Register Name: TWI_PMU_ARBITER
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	PRIORITY_7 Priority of Device 7 The higher value indicates the higher priority of device 7. The configuration value ranges from 0 to 2. If the value is larger than 2, the priority of device 7 is equal to that when the value is 2.
27:24	R/W	0x0	PRIORITY_6 Priority of Device 6 The higher the of this value, the higher the priority of device 6 The configuration value ranges from 0 to 2. If the value is larger than 2, the priority of device 6 is equal to that when the value is 2.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0320			Register Name: TWI_PMU_ARBITER
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0x0	PRIORITY_5 Priority of Device 5 The higher the of this value, the higher the priority of device 5 The configuration value ranges from 0 to 2. If the value is larger than 2, the priority of device 5 is equal to that when the value is 2.
19:16	R/W	0x0	PRIORITY_4 Priority of Device 4 The higher the of this value, the higher the priority of device 4 The configuration value ranges from 0 to 2. If the value is larger than 2, the priority of device 4 is equal to that when the value is 2.
15:12	R/W	0x0	PRIORITY_3 Priority of Device 3 The higher the of this value, the higher the priority of device 3 The configuration value ranges from 0 to 2. If the value is larger than 2, the priority of device 3 is equal to that when the value is 2.
11:8	R/W	0x0	PRIORITY_2 Priority of Device 2 The higher the of this value, the higher the priority of device 2 The configuration value ranges from 0 to 2. If the value is larger than 2, the priority of device 2 is equal to that when the value is 2.
7:4	R/W	0x0	PRIORITY_1 Priority of Device 1 The higher the of this value, the higher the priority of device 1 The configuration value ranges from 0 to 2. If the value is larger than 2, the priority of device 1 is equal to that when the value is 2.
3:0	R/W	0x0	PRIORITY_0 Priority of Device 0 The higher the of this value, the higher the priority of device 0 The configuration value ranges from 0 to 2. If the value is larger than 2, the priority of device 0 is equal to that when the value is 2.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.11.10.24 0x0330 S_TWI0 PMU Device 0 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0330			Register Name: TWI_PMU_D0_CONFIG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MUSK_EN0 Musk function enable of Device 0 0: Disable 1: Enable
30:16	/	/	/
15:8	R/W	0x0	MUSK0 Musk field of Device 0 Musk
7:0	R/W	0x0	ADDR_PMU0 Register Address of Device 0 in PMU

18.11.10.25 0x0334 S_TWI0 PMU Device 1 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0334			Register Name: TWI_PMU_D1_CONFIG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MUSK_EN1 Musk function enable of Device 1 0: Disable 1: Enable
30:16	/	/	/
15:8	R/W	0x0	MUSK1 Musk field of Device 1 Musk
7:0	R/W	0x0	ADDR_PMU1 Register Address of Device 1 in PMU

18.11.10.26 0x0338 S_TWI0 PMU Device 2 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0338			Register Name: TWI_PMU_D2_CONFIG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MUSK_EN2 Musk function enable of Device 2 0: Disable 1: Enable
30:16	/	/	/
15:8	R/W	0x0	MUSK2 Musk field of Device 2 Musk

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0338			Register Name: TWI_PMU_D2_CONFIG
Bit	Read/Write	Default/Hex	Description
7:0	R/W	0x0	ADDR_PMU2 Register Address of Device 2 in PMU

18.11.10.27 0x033C S_TWI0 PMU Device 3 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x033C			Register Name: TWI_PMU_D3_CONFIG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MUSK_EN3 Musk function enable of Device 3 0: Disable 1: Enable
30:16	/	/	/
15:8	R/W	0x0	MUSK3 Musk field of Device 3 Musk
7:0	R/W	0x0	ADDR_PMU3 Register Address of Device 3 in PMU

18.11.10.28 0x0340 S_TWI0 PMU Device 4 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: TWI_PMU_D4_CONFIG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MUSK_EN4 Musk function enable of Device 4 0: Disable 1: Enable
30:16	/	/	/
15:8	R/W	0x0	MUSK4 Musk field of Device 4 Musk
7:0	R/W	0x0	ADDR_PMU4 Register Address of Device 4 in PMU

18.11.10.29 0x0344 S_TWI0 PMU Device 5 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0344			Register Name: TWI_PMU_D5_CONFIG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0344			Register Name: TWI_PMU_D5_CONFIG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MUSK_EN5 Musk function enable of Device 5 0: Disable 1: Enable
30:16	/	/	/
15:8	R/W	0x0	MUSK5 Musk field of Device 5 Musk
7:0	R/W	0x0	ADDR_PMU5 Register Address of Device 5 in PMU

18.11.10.30 0x0348 S_TWI0 PMU Device 6 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0348			Register Name: TWI_PMU_D6_CONFIG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MUSK_EN6 Musk function enable of Device 6 0: Disable 1: Enable
30:16	/	/	/
15:8	R/W	0x0	MUSK6 Musk field of Device 6 Musk
7:0	R/W	0x0	ADDR_PMU6 Register Address of Device 6 in PMU

18.11.10.31 0x034C S_TWI0 PMU Device 7 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x034C			Register Name: TWI_PMU_D7_CONFIG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MUSK_EN7 Musk function enable of Device 7 0: Disable 1: Enable
30:16	/	/	/
15:8	R/W	0x0	MUSK7 Musk field of Device 7 Musk
7:0	R/W	0x0	ADDR_PMU7 Register Address of Device 7 in PMU

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.11.10.32 0x0380 S_TWI0 PMU RR8 Control Register (Default Value: 0x0000_0000)

Offset: 0x0380			Register Name: TWI_RR8_CTL
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	RR8_U2_ENABLE The enable bit of function of RR8_U2 0: Disable 1: Enable
1	R/W	0x0	RR8_U1_ENABLE The enable bit of function of RR8_U1 0: Disable 1: Enable
0	R/W	0x0	RR8_U0_ENABLE The enable bit of function of RR8_U0 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.12 General Purpose ADC (GPADC)

18.12.1 Overview

The General Purpose ADC (GPADC) can convert the external signal into a certain proportion of digital value, to realize the measurement of analog signal, which can be applied to power detection and key detection.

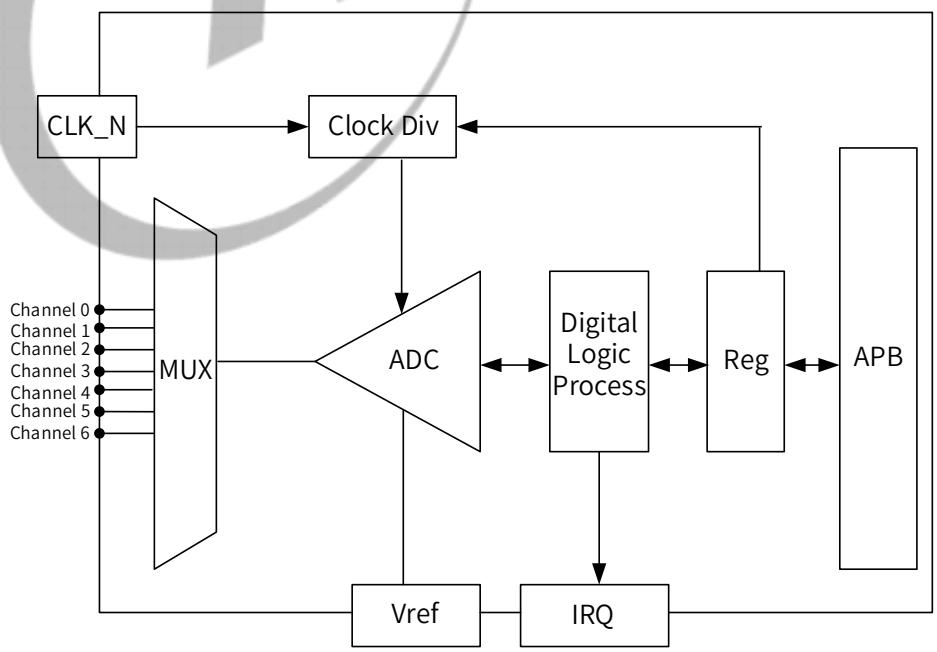
The GPADC has the following features:

- 12-bit successive-approximation register ADC (SAR ADC) with 7 pads
  - 4 for boot detection
  - 3for analog voltage input detection
- 64 FIFO depth of data register
- 12-bit sampling resolution
- Up to 1 MHz sampling frequency
- Input voltage: 0 V to 1.8 V
- Three operation modes: single conversion mode, continuous conversion mode, and burst conversion mode

18.12.2 Block Diagram

The following table shows the block diagram of the GPADC.

Figure 18-69 GPADC Block Diagram



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.12.3 Clock Sources

The following table describes the clock sources of GPADC. For clock setting, configurations, and gating information, refer to the section CCU.

Module	Clock Sources	Description
GPADC	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.
	DCXO	The external high-frequency crystal oscillator. Its frequency is 26 MHz.

18.12.4 External Signals

The following table describes the external signals of the GPADC.

Table 18-26 GPADC External Signals

Signal Name	Description	Type
BOOT-SEL-GPADC 0-0	General Purpose ADC Input Channel 0 for BOOT SELECT	AI
BOARD-ID-GPADC 0-1	General Purpose ADC Input Channel 1 for BOARD ID	AI
BOARD-ID-GPADC 0-2	General Purpose ADC Input Channel 2 for BOARD ID	AI
GPADC0-3	General Purpose ADC Input Channel 3	AI
GPADC0-4	General Purpose ADC Input Channel 4	AI
GPADC0-5	General Purpose ADC Input Channel 5	AI
GPADC0-6	General Purpose ADC Input Channel 6	AI
VCM-ADC	GPADC Reference Voltage 0.9V	AI
VREFP-ADC	GPADC Reference Voltage 1.8V	P
VREFN-ADC	GPADC Reference Ground	G

18.12.5 Functional Description

18.12.5.1 Operation Mode

- Single conversion mode

The GPADC samples and converts once in a specified channel, and then the converted data is updated at the data registers of the corresponding channels.

- Continuous conversion mode

The GPADC keeps sampling and converting in a specified channel until the ADC is disabled, and then the converted data is updated at the data registers of the corresponding channels.

- Burst conversion mode

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

The GPADC keeps sampling and converting in a specified channel until the ADC is disabled, and then the converted data is sequentially stored at the FIFO.

18.12.5.2 Clock and Timing Requirements

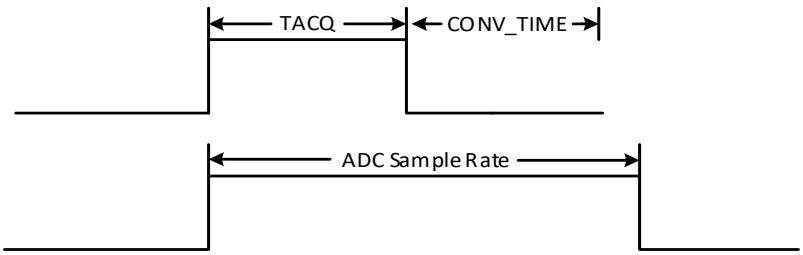
CLK_IN = 24 MHz

CONV_TIME (Conversion Time) = 1/(24MHz/13Cycles) =0.542 (us)

TACQ (ADC acquiring time) > 10RC (R is output resistor of ADC sample circuit, C = 6.4 pF)

ADC Sample Frequency > TACQ+CONV_TIME+3

Figure 18-70 GPADC Timing Requirement

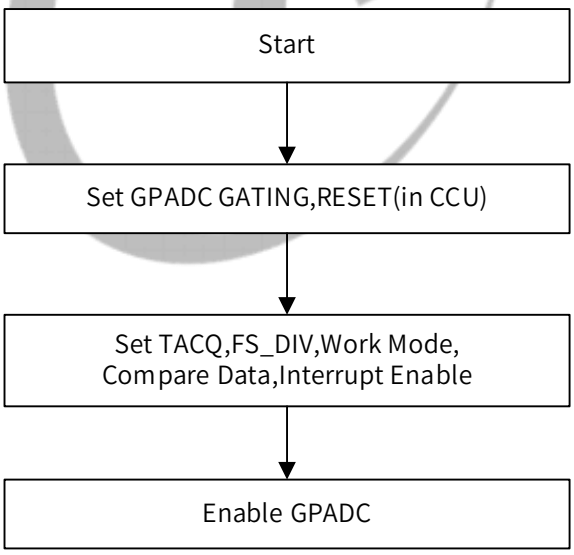


18.12.6 Programming Guidelines

18.12.6.1 Initialization

The GPADC initial process is as follows.

Figure 18-71 GPADC Initial Process



Query Mode

Take channel0 for example:

Step 1 Write 0x1 to the bit [16] of GPADC0_BGR_REG to de-assert reset.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 2 Write 0x1 to the bit [0] of GPADC0_BGR_REG to enable the GPADC clock.

Step 3 Write 0x2F to the bit [15:0] of GP_SR_CON to set the acquiring time of ADC.

Step 4 Write 0x1DF to the bit [31:16] of GP_SR_CON to set the ADC sample frequency divider.

Step 5 Write 0x2 to the bit [19:18] of GP_CTRL to set the continuous conversion mode.

Step 6 (Optional) If you need to configure the sampling frequency for each channel, follow these steps:

a) Configure GP_SMP_TMS (offset: 0x00C0) register to set GP_SMP_TMS value. The initial sampling frequency set in step4 is multiplied by this value to get the actual sampling frequency. For detailed configuration information, please refer to the section Sampling Frequency.

b) Configure the GP_CH_SMP_BYP bit (bit {0}) of GP_SMP_BYP (offset: 0x00D0) register as 0.

Step 7 Write 0x1 to the bit [0] of GP_CS_EN to enable the analog input channel.

Step 8 Write 0x1 to the bit [16] of GP_CTRL to enable the ADC function.

Step 9 Read the bit [0] of GP_DATA_INTS. If the bit is 1, then data conversion is complete.

Step 10 Read the bit [11:0] of GP_CH0_DATA, and calculate voltage value based on GPADC formula.

Interrupt Mode

Take channel0 for example:

Step 1 Write 0x1 to the bit [16] of GPADC0_BGR_REG to de-assert reset.

Step 2 Write 0x1 to the bit [0] of GPADC0_BGR_REG to enable the GPADC clock.

Step 3 Write 0x2F to the bit [15:0] of GP_SR_CON to set the acquiring time of ADC.

Step 4 Write 0x1DF to the bit [31:16] of GP_SR_CON to set the ADC sample frequency divider.

Step 5 Write 0x2 to the bit [19:18] of GP_CTRL to set the continuous conversion mode.

Step 6 (Optional) If you need to configure the sampling frequency for each channel, follow these steps:

a) Configure GP_SMP_TMS (offset: 0x00C0) register to set GP_SMP_TMS value. The initial sampling frequency set in step4 is multiplied by this value to get the actual sampling frequency. For detailed configuration information, please refer to section Sampling Frequency.

b) Configure the GP_CH_SMP_BYP bit (bit {0}) of GP_SMP_BYP (offset: 0x00D0) register as 0. Write 0x1 to the bit [0] of GP_CS_EN to enable the analog input channel.

Step 7 Write 0x1 to the bit [0] of GP_DATA_INTC to enable the GPADC data interrupt.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 8 Set the GIC module based on the IRQ 93.

Step 9 Put interrupt handler address into interrupt vector table based on the IRQ 93.

Step 10 Write 0x1 to the bit16 of GP_CTRL to enable the ADC function.

Step 11 Read the bit [11:0] of GP_CH0_DATA from the interrupt handler, calculate voltage value based on GPADC formula.

18.12.6.2 Sampling Frequency Configuration

The sampling frequency is only configurable in continue conversion mode. The sampling frequency for each channel can be configured as a multiple of 32 kHz and the total sampling frequency of all channels should be less than or equal to 1 MHz.

The sampling frequency configuration steps are as follows.

Step 1 After setting GP_SMP_TMS0/1/2/3 and GP_SMP_BYP as 0, configure the ADC_EN bit (bit [16]) of GP_CTRL (offset: 0x0004) register to disable ADC function.

Step 2 Configure the FS_DIV bit (bit [31:16]) of GP_SR_CON (offset: 0x0000) register to set the initial sampling frequency of each channel.

Step 3 Configure GP_SMP_TMS (offset: 0x00C0) register to set GP_SMP_TMS value. The initial sampling frequency is multiplied by this value to get the actual sampling frequency.

NOTE

All GPADC channels should be configured simultaneously.

The following are the all available sampling frequencies for each channel and corresponding GP_SMP_TMS values.

Table 18-27 GP_SMP_TMS Value Corresponding to Each Sampling Frequency

Sampling frequency	GP_SMP_TMS Value	Sampling frequency	GP_SMP_TMS Value
32 kHz	1	544 kHz	17
64 kHz	2	576 kHz	18
96 kHz	3	608 kHz	19
128 kHz	4	640 kHz	20
160 kHz	5	672 kHz	21
192 kHz	6	704 kHz	22
224 kHz	7	736 kHz	23
256 kHz	8	768 kHz	24
288 kHz	9	800 kHz	25
320 kHz	10	832 kHz	26
352 kHz	11	864 kHz	27

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Sampling frequency	GP_SMP_TMS Value	Sampling frequency	GP_SMP_TMS Value
384 kHz	12	896 kHz	28
416 kHz	13	928 kHz	29
448 kHz	14	960 kHz	30
480 kHz	15	992 kHz	31
512 kHz	16	/	/

Step 4 Configure the GP_CH_SMP_BYP bit (bit {0}) of GP_SMP_BYP (offset: 0x00D0) register as 0.

Step 5 Configure the ADC_EN bit (bit [16]) of GP_CTRL (offset: 0x0004) register to enable ADC function.

18.12.6.3 In-phase Amplifier Configuration

In the use of forward amplifier, the amplification factor needs to be configured in the registers GP_OPA_TUNE0 and GP_OPA_TUNE1. The final magnification values are shown in the figure below.

Table 18-28 Magnification Value Configuration

Magnification Value	GP_OPA_TUNE0/ GP_OPA_TUNE0
1	0000
2	0001
3	0010
4	0011
5	0100
6	0101
7	0110
8	0111
9	1000
10	1001
11	1010
12	1011
13	1100
14	1101
15	1110
16	1111

18.12.7 Register List

Module Name	Base Address
GPADC	0x02521000

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
GP_SR_CON	0x0000	GPADC Sample Rate Configure Register
GP_CTRL	0x0004	GPADC Control Register
GP_CS_EN	0x0008	GPADC Compare and Select Enable Register
GP_FIFO_INTC	0x000C	GPADC FIFO Interrupt Control Register
GP_FIFO_INTS	0x0010	GPADC FIFO Interrupt Status Register
GP_FIFO_DATA	0x0014	GPADC FIFO Data Register
GP_CDATA	0x0018	GPADC Calibration Data Register
GP_DATAL_INTC	0x0020	GPADC Data Low Interrupt Configure Register
GP_DATAH_INTC	0x0024	GPADC Data High Interrupt Configure Register
GP_DATA_INTC	0x0028	GPADC Data Interrupt Configure Register
GP_DATAL_INTS	0x0030	GPADC Data Low Interrupt Status Register
GP_DATAH_INTS	0x0034	GPADC Data High Interrupt Status Register
GP_DATA_INTS	0x0038	GPADC Data Interrupt Status Register
GP_CH0_CMP_DATA	0x0040	GPADC CH0 Compare Data Register
GP_CH1_CMP_DATA	0x0044	GPADC CH1 Compare Data Register
GP_CH2_CMP_DATA	0x0048	GPADC CH2 Compare Data Register
GP_CH3_CMP_DATA	0x004C	GPADC CH3 Compare Data Register
GP_CH4_CMP_DATA	0x0050	GPADC CH4 Compare Data Register
GP_CH5_CMP_DATA	0x0054	GPADC CH5 Compare Data Register
GP_CH6_CMP_DATA	0x0058	GPADC CH6 Compare Data Register
GP_CH0_DATA	0x0080	GPADC CH0 Data Register
GP_CH1_DATA	0x0084	GPADC CH1 Data Register
GP_CH2_DATA	0x0088	GPADC CH2 Data Register
GP_CH3_DATA	0x008C	GPADC CH3 Data Register
GP_CH4_DATA	0x0090	GPADC CH4 Data Register
GP_CH5_DATA	0x0094	GPADC CH5 Data Register
GP_CH6_DATA	0x0098	GPADC CH6 Data Register
GP_SMP_TMS0	0x00C0	GPADC Sampling Times0 Register
GP_SMP_TMS1	0x00C4	GPADC Sampling Times1 Register
GP_SMP_BYP	0x00D0	GPADC Channel Sample Rate Setting Bypass Register
GP_ADC_SEL_EN	0x00DC	GPADC ADC SELECT Enable Register
GP_OPA_EN	0x00F0	GPADC OPAMP Enable Register
GP_OPA_TUNE0	0x00F4	GPADC OPAMP Tune0 Register
GP_RVLT_SEL	0x00FC	GPADC Reference Voltage Source Select Register

18.12.8 Register Description

18.12.8.1 0x0000 GPADC Sample Rate Configure Register (Default Value: 0x01DF_002F)

Offset: 0x0000			Register Name: GP_SR_CON
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: GP_SR_CON
Bit	Read/Write	Default/Hex	Description
31: 16	R/W	0x1DF	FS_DIV ADC Sample Frequency Divider CLK_IN/(n+1) Default value: 50K
15:0	R/W	0x2F	TACQ ADC Acquiring Time (n+1)/CLK_IN Default value: 2 us

18.12.8.2 0x0004 GPADC Control Register (Default Value: 0x0080_0000)

Offset: 0x0004			Register Name: GP_CTRL
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	ADC_FIRST_DLY ADC First Convert Delay setting ADC conversion of each channel is delayed by N samples.
23	R/W	0x1	ADC_AUTOCALI_EN ADC Auto Calibration
22	/	/	/
21:20	R/W	0x0	ADC_OP_BIAS ADC OP Bias Adjust the bandwidth of the ADC amplifier.
19:18	R/W	0x0	GP_MODE GPADC Work Mode 00: Single conversion mode 01: Single-cycle conversion mode 10: Continuous conversion mode 11: Burst conversion mode
17	R/W	0x0	ADC_CALI_EN ADC Calibration 1: start Calibration, it is cleared to 0 after calibration

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: GP_CTRL
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	ADC_EN ADC Function Enable Before the bit is enabled, configure ADC parameters including the work mode and channel number, etc. 0: Disable 1: Enable When selecting a single conversion mode, the bit can be cleared automatically after the switch is completed.
15:0	/	/	/

18.12.8.3 0x0008 GPADC Compare and Select Enable Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: GP_CS_EN
Bit	Read/Write	Default/Hex	Description
31:23	/	/	/
22	R/W	0x0	ADC_CH6_CMP_EN Channel 6 Compare Enable 0: Disable 1: Enable
21	R/W	0x0	ADC_CH5_CMP_EN Channel 5 Compare Enable 0: Disable 1: Enable
20	R/W	0x0	ADC_CH4_CMP_EN Channel 4 Compare Enable 0: Disable 1: Enable
19	R/W	0x0	ADC_CH3_CMP_EN Channel 3 Compare Enable 0: Disable 1: Enable
18	R/W	0x0	ADC_CH2_CMP_EN Channel 2 Compare Enable 0: Disable 1: Enable
17	R/W	0x0	ADC_CH1_CMP_EN Channel 1 Compare Enable 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: GP_CS_EN
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	ADC_CH0_CMP_EN Channel 0 Compare Enable 0: Disable 1: Enable
15:6	/	/	/
6	R/W	0x0	ADC_CH6_SELECT. Analog input channel 6 Select 0: Disable 1: Enable
5	R/W	0x0	ADC_CH5_SELECT. Analog input channel 5 Select 0: Disable 1: Enable
4	R/W	0x0	ADC_CH4_SELECT. Analog input channel 4 Select 0: Disable 1: Enable
3	R/W	0x0	ADC_CH3_SELECT. Analog input channel 3 Select 0: Disable 1: Enable
2	R/W	0x0	ADC_CH2_SELECT. Analog input channel 2 Select 0: Disable 1: Enable
1	R/W	0x0	ADC_CH1_SELECT. Analog input channel 1 Select 0: Disable 1: Enable
0	R/W	0x0	ADC_CH0_SELECT. Analog input channel 0 Select 0: Disable 1: Enable

18.12.8.4 0x000C GPADC FIFO Interrupt Control Register (Default Value: 0x0000_1F00)

Offset: 0x000C			Register Name: GP_FIFO_INTC
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x000C			Register Name: GP_FIFO_INTC
Bit	Read/Write	Default/Hex	Description
18	R/W	0x0	FIFO_DATA_DRQ_EN ADC FIFO Date DRQ Enable 0: Disable 1: Enable
17	R/W	0x0	FIFO_OVERRUN_IRQ_EN ADC FIFO Over Run IRQ Enable 0: Disable 1: Enable
16	R/W	0x0	FIFO_DATA_IRQ_EN ADC FIFO Data Available IRQ Enable 0: Disable 1: Enable
15:14	/	/	/
13:8	R/W	0x1F	FIFO_TRIG_LEVEL Interrupt trigger level for ADC Trigger Level = TXTL + 1
7:5	/	/	/
4	R/WAC	0x0	FIFO_FLUSH ADC FIFO Flush Write 1 to flush TX FIFO, self-clear to 0 .
3:0	/	/	/

18.12.8.5 0x0010 GPADC FIFO Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: GP_FIFO_INTS
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W1C	0x0	FIFO_OVERRUN_PENDING. ADC FIFO Over Run IRQ pending 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write 1 to clear this interrupt
16	R/W1C	0x0	FIFO_DATA_PENDING. ADC FIFO Data Available Pending Bit 0: NO Pending IRQ 1: FIFO Available Pending IRQ Write 1 to clear this interrupt
15	/	/	/
14:8	R	0x0	RXA_CNT ADC FIFO available Sample Word Counter
7:0	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.12.8.6 0x0014 GPADC FIFO Data Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: GP_FIFO_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x0	GP_FIFO_DATA GPADC Data in FIFO

18.12.8.7 0x0018 GPADC Calibration Data Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: GP_CDATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x000	GP_CDATA GPADC Calibration Data

18.12.8.8 0x0020 GPADC Data Low Interrupt Configure Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: GP_DATAL_INTC
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x0	CH6_LOW_IRQ_EN Channel 6 Voltage Low Available Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	CH5_LOW_IRQ_EN Channel 5 Voltage Low Available Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	CH4_LOW_IRQ_EN Channel 4 Voltage Low Available Interrupt Enable 0: Disable 1: Enable
3	R/W	0x0	CH3_LOW_IRQ_EN Channel 3 Voltage Low Available Interrupt Enable 0: Disable 1: Enable
2	R/W	0x0	CH2_LOW_IRQ_EN Channel 2 Voltage Low Available Interrupt Enable 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0020			Register Name: GP_DATAL_INTC
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	CH1_LOW_IRQ_EN Channel 1 Voltage Low Available Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	CH0_LOW_IRQ_EN Channel 0 Voltage Low Available Interrupt Enable 0: Disable 1: Enable

18.12.8.9 0x0024 GPADC Data High Interrupt Configure Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: GP_DATAH_INTC
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x0	CH6_HIG_IRQ_EN Channel 6 Voltage High Available Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	CH5_HIG_IRQ_EN Channel 5 Voltage High Available Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	CH4_HIG_IRQ_EN Channel 4 Voltage High Available Interrupt Enable 0: Disable 1: Enable
3	R/W	0x0	CH3_HIG_IRQ_EN Channel 3 Voltage High Available Interrupt Enable 0: Disable 1: Enable
2	R/W	0x0	CH2_HIG_IRQ_EN Channel 2 Voltage High Available Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	CH1_HIG_IRQ_EN Channel 1 Voltage High Available Interrupt Enable 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0024			Register Name: GP_DATAH_INTC
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	CH0_HIG_IRQ_EN Channel 0 Voltage High Available Interrupt Enable 0: Disable 1: Enable

18.12.8.10 0x0028 GPADC Data Interrupt Configure Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: GP_DATA_INTC
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x0	CH6_DATA_IRQ_EN Channel 6 Data Available Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	CH5_DATA_IRQ_EN Channel 5 Data Available Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	CH4_DATA_IRQ_EN Channel 4 Data Available Interrupt Enable 0: Disable 1: Enable
3	R/W	0x0	CH3_DATA_IRQ_EN Channel 3 Data Available Interrupt Enable 0: Disable 1: Enable
2	R/W	0x0	CH2_DATA_IRQ_EN Channel 2 Data Available Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	CH1_DATA_IRQ_EN Channel 1 Data Available Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	CH0_DATA_IRQ_EN Channel 0 Data Available Interrupt Enable 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.12.8.11 0x0030 GPADC Data Low Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: GP_DATAL_INTS
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W1C	0x0	CH6_LOW_PENGDING Channel 6 Voltage Low Available Interrupt Status 0: NO Pending IRQ 1: Channel 2 Voltage Low Available Pending IRQ Write 1 to clear this interrupt or automatic clear if interrupt condition fails
5	R/W1C	0x0	CH5_LOW_PENGDING Channel 5 Voltage Low Available Interrupt Status 0: NO Pending IRQ 1: Channel 1 Voltage Low Available Pending IRQ Write 1 to clear this interrupt or automatic clear if interrupt condition fails
4	R/W1C	0x0	CH4_LOW_PENGDING Channel 4 Voltage Low Available Interrupt Status 0: NO Pending IRQ 1: Channel 0 Voltage Low Available Pending IRQ Write 1 to clear this interrupt or automatic clear if interrupt condition fails
3	R/W1C	0x0	CH3_LOW_PENGDING Channel 3 Voltage Low Available Interrupt Status 0: NO Pending IRQ 1: Channel 3 Voltage Low Available Pending IRQ Write 1 to clear this interrupt or automatic clear if interrupt condition fails
2	R/W1C	0x0	CH2_LOW_PENGDING Channel 2 Voltage Low Available Interrupt Status 0: NO Pending IRQ 1: Channel 2 Voltage Low Available Pending IRQ Write 1 to clear this interrupt or automatic clear if interrupt condition fails
1	R/W1C	0x0	CH1_LOW_PENGDING Channel 1 Voltage Low Available Interrupt Status 0: NO Pending IRQ 1: Channel 1 Voltage Low Available Pending IRQ Write 1 to clear this interrupt or automatic clear if interrupt condition fails

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0030			Register Name: GP_DATAL_INTS
Bit	Read/Write	Default/Hex	Description
0	R/W1C	0x0	CH0_LOW_PENGDING Channel 0 Voltage Low Available Interrupt Status 0: NO Pending IRQ 1: Channel 0 Voltage Low Available Pending IRQ Write 1 to clear this interrupt or automatic clear if interrupt condition fails

18.12.8.12 0x0034 GPADC Data High Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: GP_DATAH_INTS
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W1C	0x0	CH6_HIG_PENGDING Channel 6 Voltage High Available Interrupt Status 0: NO Pending IRQ 1: Channel 6 Voltage High Available Pending IRQ Write 1 to clear this interrupt or automatic clear if interrupt condition fails
5	R/W1C	0x0	CH5_HIG_PENGDING Channel 5 Voltage High Available Interrupt Status 0: NO Pending IRQ 1: Channel 5 Voltage High Available Pending IRQ Write 1 to clear this interrupt or automatic clear if interrupt condition fails
4	R/W1C	0x0	CH4_HIG_PENGDING Channel 4 Voltage High Available Interrupt Status 0: NO Pending IRQ 1: Channel 4 Voltage High Available Pending IRQ Write 1 to clear this interrupt or automatic clear if interrupt condition fails
3	R/W1C	0x0	CH3_HIG_PENGDING Channel 3 Voltage High Available Interrupt Status 0: NO Pending IRQ 1: Channel 3 Voltage High Available Pending IRQ Write 1 to clear this interrupt or automatic clear if interrupt condition fails

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0034			Register Name: GP_DATAH_INTS
Bit	Read/Write	Default/Hex	Description
2	R/W1C	0x0	CH2_HIG_PENGDING Channel 2 Voltage High Available Interrupt Status 0: NO Pending IRQ 1: Channel 2 Voltage High Available Pending IRQ Write 1 to clear this interrupt or automatic clear if interrupt condition fails
1	R/W1C	0x0	CH1_HIG_PENGDING Channel 1 Voltage High Available Interrupt Status 0: NO Pending IRQ 1: Channel 1 Voltage High Available Pending IRQ Write 1 to clear this interrupt or automatic clear if interrupt condition fails
0	R/W1C	0x0	CH0_HIG_PENGDING Channel 0 Voltage High Available Interrupt Status 0: NO Pending IRQ 1: Channel 0 Voltage High Available Pending IRQ Write 1 to clear this interrupt or automatic clear if interrupt condition fails

18.12.8.13 0x0038 GPADC Data Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: GP_DATA_INTS
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W1C	0x0	CH6_DATA_PENGDING Channel 6 Data Available Interrupt Status 0: NO Pending IRQ 1: Channel 6 Data Available Pending IRQ Write 1 to clear this interrupt or automatic clear if interrupt condition fails
5	R/W1C	0x0	CH5_DATA_PENGDING Channel 5 Data Available Interrupt Status 0: NO Pending IRQ 1: Channel 5 Data Available Pending IRQ Write 1 to clear this interrupt or automatic clear if interrupt condition fails

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0038			Register Name: GP_DATA_INTS
Bit	Read/Write	Default/Hex	Description
4	R/W1C	0x0	CH4_DATA_PENGDING Channel 4 Data Available Interrupt Status 0: NO Pending IRQ 1: Channel 4 Data Available Pending IRQ Write 1 to clear this interrupt or automatic clear if interrupt condition fails
3	R/W1C	0x0	CH3_DATA_PENGDING Channel 3 Data Available Interrupt Status 0: NO Pending IRQ 1: Channel 3 Data Available Pending IRQ Write 1 to clear this interrupt or automatic clear if interrupt condition fails
2	R/W1C	0x0	CH2_DATA_PENGDING Channel 2 Data Available Interrupt Status 0: NO Pending IRQ 1: Channel 2 Data Available Pending IRQ Write 1 to clear this interrupt or automatic clear if interrupt condition fails
1	R/W1C	0x0	CH1_DATA_PENGDING Channel 1 Data Available Interrupt Status 0: NO Pending IRQ 1: Channel 1 Data Available Pending IRQ Write 1 to clear this interrupt or automatic clear if interrupt condition fails
0	R/W1C	0x0	CH0_DATA_PENGDING Channel 0 Data Available Interrupt Status 0: NO Pending IRQ 1: Channel 0 Data Available Pending IRQ Write 1 to clear this interrupt or automatic clear if interrupt condition fails

18.12.8.14 0x0040 GPADC CH0 Compare Data Register (Default Value: 0x0BFF_0400)

Offset: 0x0040			Register Name: GP_CH0_CMP_DATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xBFF	CH0_CMP_HIG_DATA Channel 0 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH0_CMP_LOW_DATA Channel 0 Voltage Low Value

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.12.8.15 0x0044 GPADC CH1 Compare Data Register (Default Value: 0x0BFF_0400)

Offset: 0x0044			Register Name: GP_CH1_CMP_DATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xBFF	CH1_CMP_HIG_DATA Channel 1 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH1_CMP_LOW_DATA Channel 1 Voltage Low Value

18.12.8.16 0x0048 GPADC CH2 Compare Data Register (Default Value: 0x0BFF_0400)

Offset: 0x0048			Register Name: GP_CH2_CMP_DATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xBFF	CH2_CMP_HIG_DATA Channel 2 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH2_CMP_LOW_DATA Channel 2 Voltage Low Value

18.12.8.17 0x004C GPADC CH3 Compare Data Register (Default Value: 0x0BFF_0400)

Offset: 0x004C			Register Name: GP_CH3_CMP_DATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xBFF	CH3_CMP_HIG_DATA Channel 3 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH3_CMP_LOW_DATA Channel 3 Voltage Low Value

18.12.8.18 0x0050 GPADC CH4 Compare Data Register (Default Value: 0x0BFF_0400)

Offset: 0x0050			Register Name: GP_CH4_CMP_DATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xBFF	CH4_CMP_HIG_DATA Channel 4 Voltage High Value
15:12	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0050			Register Name: GP_CH4_CMP_DATA
Bit	Read/Write	Default/Hex	Description
11:0	R/W	0x400	CH4_CMP_LOW_DATA Channel 4 Voltage Low Value

18.12.8.19 0x0054 GPADC CH5 Compare Data Register (Default Value: 0x0BFF_0400)

Offset: 0x0054			Register Name: GP_CH5_CMP_DATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xBFF	CH5_CMP_HIG_DATA Channel 5 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH5_CMP_LOW_DATA Channel 5 Voltage Low Value

18.12.8.20 0x0058 GPADC CH6 Compare Data Register (Default Value: 0x0BFF_0400)

Offset: 0x0058			Register Name: GP_CH6_CMP_DATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xBFF	CH6_CMP_HIG_DATA Channel 6 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH6_CMP_LOW_DATA Channel 6 Voltage Low Value

18.12.8.21 0x0080 GPADC CH0 Data Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: GP_CH0_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH0_DATA Channel 0 Data

18.12.8.22 0x0084 GPADC CH1 Data Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: GP_CH1_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0084			Register Name: GP_CH1_DATA
Bit	Read/Write	Default/Hex	Description
11:0	R	0x000	GP_CH1_DATA Channel 1 Data

18.12.8.23 0x0088 GPADC CH2 Data Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: GP_CH2_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH2_DATA Channel 2 Data

18.12.8.24 0x008C GPADC CH3 Data Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: GP_CH3_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH3_DATA Channel 3 Data

18.12.8.25 0x0090 GPADC CH4 Data Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: GP_CH4_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH4_DATA Channel 4 Data

18.12.8.26 0x0094 GPADC CH5 Data Register (Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: GP_CH5_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH5_DATA Channel 5 Data

18.12.8.27 0x0098 GPADC CH6 Data Register (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: GP_CH6_DATA
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0098			Register Name: GP_CH6_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH6_DATA Channel 6 Data

18.12.8.28 0x00C0 GPADC Sampling Times0 Register (Default Value 0x0000_0000)

Offset: 0x00C0			Register Name: GP_SMP_TMS0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:24	R/W	0x0	GP_ CH3_SMP_TMS GPADC Channel 3 Sampling Times Register 0x0: 0 (channel disable) 0x1: 1 (p) 0x1f: 31 Other: Reserved
23: 22	/	/	/
21:16	R/W	0x0	GP_ CH2_SMP_TMS GPADC Channel 2 Sampling Times Register 0x0: 0 (channel disable) 0x1: 1 (p) 0x1f: 31 Other: Reserved
15: 14	/	/	/
13:8	R/W	0x0	GP_ CH1_SMP_TMS GPADC Channel 1 Sampling Times Register 0x0: 0 (channel disable) 0x1: 1 (p) 0x1f: 31 Other: Reserved
7:6	/	/	/
5:0	R/W	0x0	GP_ CH0_SMP_TMS GPADC Channel 0 Sampling Times Register 0x0: 0 (channel disable) 0x1: 1 (p) 0x1f: 31 Other: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.12.8.29 0x00C4 GPADC Sampling Times1 Register (Default Value 0x0000_0000)

Offset: 0x00C4			Register Name: GP_SMP_TMS1
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:16	R/W	0x0	GP_ CH6_SMP_TMS GPADC Channel 6 Sampling Times Register 0x0: 0 (channel disable) 0x1: 1 (p) 0x1f: 31 Other: Reserved
15: 14	/	/	/
13:8	R/W	0x0	GP_ CH5_SMP_TMS GPADC Channel 5 Sampling Times Register 0x0: 0 (channel disable) 0x1: 1 (p) 0x1f: 31 Other: Reserved
7:6	/	/	/
5:0	R/W	0x0	GP_ CH4_SMP_TMS GPADC Channel 4 Sampling Times Register 0x0: 0 (channel disable) 0x1: 1 (p) 0x1f: 31 Other: Reserved

18.12.8.30 0x00D0 GPADC Channel Sample Rate Setting Bypass Register (Default Value 0x0000_0001)

Offset: 0x00D0			Register Name: GP_SMP_BYP
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	GP_ CH_SMP_BYP GPADC Channel Sample Rate Setting Bypass 0: Enable sampling rate setting 1: Disable sampling rate setting

18.12.8.31 0x00DC GPADC ADC SELECT Enable Register (Default Value: 0x0000_0000)

Offset: 0x00DC	Register Name: GP_ADC_SEL_EN

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	GP_ADC_SEL_EN GPADC ADC SELECT ENABLE 0: Select normal ADC 1: Select test ADC

18.12.8.32 0x00F0 GPADC OPAMP Enable Register (Default Value: 0x0000_0000)

Offset: 0x00F0			Register Name: GP_OPA_EN
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
22	R/W	0x0	GP_CH6_OPA_SEL 0: ADC input bypass operation amplifier 1: ADC input from operation amplifier
21	R/W	0x0	GP_CH5_OPA_SEL 0: ADC input bypass operation amplifier 1: ADC input from operation amplifier
20	R/W	0x0	GP_CH4_OPA_SEL 0: ADC input bypass operation amplifier 1: ADC input from operation amplifier
19	R/W	0x0	GP_CH3_OPA_SEL 0: ADC input bypass operation amplifier 1: ADC input from operation amplifier
18	R/W	0x0	GP_CH2_OPA_SEL 0: ADC input bypass operation amplifier 1: ADC input from operation amplifier
17	R/W	0x0	GP_CH1_OPA_SEL 0: ADC input bypass operation amplifier 1: ADC input from operation amplifier
16	R/W	0x0	GP_CH0_OPA_SEL 0: ADC input bypass operation amplifier 1: ADC input from operation amplifier
15:7	/	/	/
6	R/W	0x0	GP_CH6_OPA_EN Operation Amplifier for GPADC Channel 6 0: Disable 1: Enable
5	R/W	0x0	GP_CH5_OPA_EN Operation Amplifier for GPADC Channel 5 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00F0			Register Name: GP_OPA_EN
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	GP_CH4_OPA_EN Operation Amplifier for GPADC Channel 4 0: Disable 1: Enable
3	R/W	0x0	GP_CH3_OPA_EN Operation Amplifier for GPADC Channel 3 0: Disable 1: Enable
2	R/W	0x0	GP_CH2_OPA_EN Operation Amplifier for GPADC Channel 2 0: Disable 1: Enable
1	R/W	0x0	GP_CH1_OPA_EN Operation Amplifier for GPADC Channel 1 0: Disable 1: Enable
0	R/W	0x0	GP_CH0_OPA_EN Operation Amplifier for GPADC Channel 0 0: Disable 1: Enable

18.12.8.33 0x00F4 GPADC OPAMP Tune0 Register (Default Value 0x8888_8888)

Offset: 0x00F4			Register Name: GP_OPA_TUNE0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x8	GP_CH7_OPA_TUNE Indicates the magnification of operation amplifier for GPADC Channel 7 0x0: 1 times 0x1: 2 times (p)(p) 0xf: 16 times
27:24	R/W	0x8	GP_CH6_OPA_TUNE Indicates the magnification of operation amplifier for GPADC Channel 6 0x0: 1 times 0x1: 2 times (p)(p) 0xf: 16 times

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00F4			Register Name: GP_OPA_TUNE0
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0x8	GP_CH5_OPA_TUNE Indicates the magnification of operation amplifier for GPADC Channel 5 0x0: 1 times 0x1: 2 times (p)(p) 0xf: 16 times
19:16	R/W	0x8	GP_CH4_OPA_TUNE Indicates the magnification of operation amplifier for GPADC Channel 4 0x0: 1 times 0x1: 2 times (p)(p) 0xf: 16 times
15:12	R/W	0x8	GP_CH3_OPA_TUNE Indicates the magnification of operation amplifier for GPADC Channel 3 0x0: 1 times 0x1: 2 times (p)(p) 0xf: 16 times
11:8	R/W	0x8	GP_CH2_OPA_TUNE Indicates the magnification of operation amplifier for GPADC Channel 2 0x0: 1 times 0x1: 2 times (p)(p) 0xf: 16 times
7:4	R/W	0x8	GP_CH1_OPA_TUNE Indicates the magnification of operation amplifier for GPADC Channel 1 0x0: 1 times 0x1: 2 times (p)(p) 0xf: 16 times
3:0	R/W	0x8	GP_CH0_OPA_TUNE Indicates the magnification of operation amplifier for GPADC Channel 0 0x0: 1 times 0x1: 2 times (p)(p) 0xf: 16 times

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.12.8.34 0x00FC GPADC Reference Voltage Source Select Register (Default Value 0x0000_0001)

Offset: 0x00FC			Register Name: GP_RVLT_SEL
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	GP_RVLT_SEL GPADC Reference Voltage Source Selector 0: External LDO 1: Internal LDO

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.13 Low Rate ADC (LRADC)

18.13.1 Overview

The low rate analog-to-digital converter (LRADC) can convert the external signal into a certain proportion of digital value, to realize the measurement of analog signal, which can be applied to power detection and key detection.

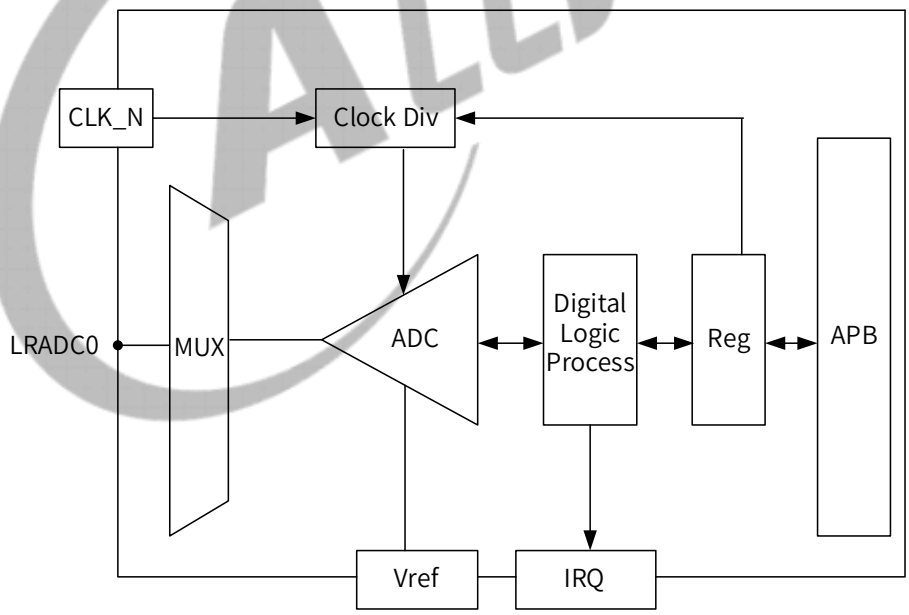
The LRADC has the following features:

- 6-bit sampling resolution
- Up to 2 KHz sampling frequency
- Input voltage: 0 V to 1.35 V; power supply voltage:1.8V
- Supports hold key and general key
- Supports interrupt control
- Three operation modes: single mode, continuous mode, and normal mode

18.13.2 Block Diagram

The following figure shows the block diagram of the LRADC.

Figure 18-72 LRADC Block Diagram



18.13.3 Clock Sources

The following table describes the clock sources of LRADC. For clock setting, configurations, and gating information, refer to the section CCU.

Module	Clock Sources	Description
LRADC	RTC_32K	Its frequency is 32.768 KHz by default.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.13.4 External Signals

The following table describes the external signals of the LRADC. The LRADC pin is the analog input signal.

Table 18-29 LRADC External Signals

Signal Name	Description	Type
LRADC0-0	Low Rate ADC	AI

18.13.5 Functional Description

18.13.5.1 Operation Mode

- Normal Mode

The LRADC gathers and averages 8 samples to obtain a data, then updates it to the data register and asserts a data interrupt flag. Sampling is repeated in this manner until the LRADC is disabled.

- Continuous Mode

The LRADC gathers and averages 8 samples every 8*(N+1) sample cycle, then updates it to the data register and asserts a data interrupt flag. (N is defined in the bit [19:16] of LRADC_CTRL).

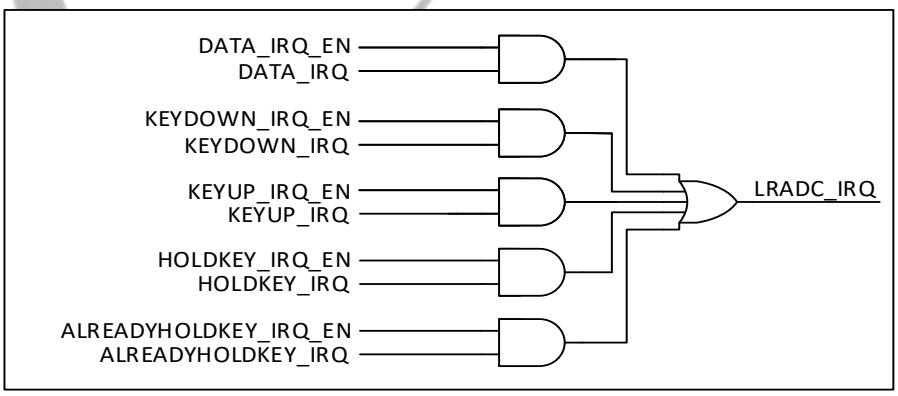
- Single Mode

The LRADC gathers and averages 8 samples to obtain a data, then updates it to the data register and asserts a data interrupt flag. Then, the LRADC stops sampling.

18.13.5.2 Interrupt Control

Each LRADC channel has five interrupt sources and five interrupt enable controls.

Figure 18-73 LRADC Interrupt



When the input voltage is between LEVEL A (1.35 V) and LEVEL B (control by the bit [5:4] of LRADC_CTRL), the IRQ1 will be generated. When the input voltage is lower than LEVEL B, the IRQ2 will be generated.

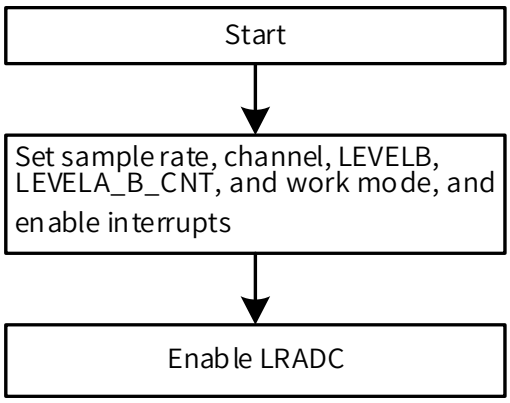
If the controller receives IRQ1 but does not receive IRQ2 in a certain time, the controller will generate Hold Key Pending, or Data IRQ Pending.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

The Hold KEY is usually used for the self-locking key. When the self-locking key stays in the locked status, the controller receives the IRQ2, then the controller will generate Already Hold Pending.

18.13.6 Programming Guidelines

18.13.6.1 Initialization



18.13.6.2 Normal Mode

Perform the following steps for normal mode:

Step 1 Configure LRADC_BGR_REG [LRADC_GATING] to 0 to disable the clock of LRADC.

Step 2 Configure LRADC_BGR_REG [LRADC_RST] to 1 to de-assert the reset of LRADC.

Step 3 Configure LRADC_BGR_REG [LRADC_GATING] to 1 to enable the clock of LRADC.

Step 4 Configure LRADC_CTRL[LRADC_SAMPLE_RATE] to set the appropriate sampling frequency.

Step 5 Configure LRADC_CTRL[LEVELB_VOL] to set the appropriate voltage threshold.

Step 6 Configure LRADC_CTRL[FIRST_CONVER_DLY] and LRADC_CTRL[LEVELA_B_CNT] to set the appropriate debounce value.

Step 7 Configure LRADC_CTRL[LRADC_HOLD_KEY_EN] to 1.

Step 8 Configure LRADC_CTRL[KEY_MODE_SELECT] to 0 to set the normal mode.

Step 9 Configure LRADC_INTC to enable the corresponding interrupt.

Step 10 Configure LRADC_CTRL[LRADC_HOLD_KEY_EN] to 1.

Step 11 Read the corresponding key voltage value from LRADC_DATA when the CPU receives the LRADC interrupt.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.13.6.3 Single Mode

Perform the following steps for the single mode:

Step 1 ConfigureLRADC_BGR_REG [LRADC_GATING] to 0 to disable the clock of LRADC.

Step 2 ConfigureLRADC_BGR_REG [LRADC_RST] to 1 to de-assert the reset of LRADC.

Step 3 ConfigureLRADC_BGR_REG [LRADC_GATING] to 1 to enable the clock of LRADC.

Step 4 Configure LRADC_CTRL[LRADC_SAMPLE_RATE] to set the appropriate sampling frequency.

Step 5 Configure LRADC_CTRL[LEVELB_VOL] to set the appropriate voltage threshold.

Step 6 Configure LRADC_CTRL[FIRST_CONVER_DLY] and LRADC_CTRL[LEVELA_B_CNT] to set the appropriate debounce value.

Step 7 Configure LRADC_CTRL[LRADC_HOLD_KEY_EN] to 1.

Step 8 Configure LRADC_CTRL[KEY_MODE_SELECT] to 1 to set the single mode.

Step 9 Configure LRADC_INTC to enable the corresponding interrupt.

Step 10 Configure LRADC_CTRL[LRADC_HOLD_KEY_EN] to 1.

Step 11 Read the corresponding key voltage value from LRADC_DATA when the CPU receives the LRADC interrupt.

18.13.6.4 Continuous Mode

Perform the following steps for continuous mode:

Step 1 Configure LRADC_BGR_REG [LRADC_GATING] to 0 to disable the clock of LRADC.

Step 2 ConfigureLRADC_BGR_REG [LRADC_RST] to 1 to de-assert the reset of LRADC.

Step 3 Configure LRADC_BGR_REG [LRADC_GATING] to 1 to enable the clock of LRADC.

Step 4 Configure LRADC_CTRL[LRADC_SAMPLE_RATE] to set the appropriate sampling frequency.

Step 5 Configure LRADC_CTRL[LEVELB_VOL] to set the appropriate voltage threshold.

Step 6 Configure LRADC_CTRL[FIRST_CONVER_DLY] and LRADC_CTRL[LEVELA_B_CNT] to set the appropriate debounce value.

Step 7 Configure LRADC_CTRL[LRADC_HOLD_KEY_EN] to 1.

Step 8 Configure LRADC_CTRL[KEY_MODE_SELECT] to 2 to set the continuous mode, and configure LRADC_CTRL[CONTINUE_TIME_SELECT] to set a sampling interval.

Step 9 Configure LRADC_INTC to enable the corresponding interrupt.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 10 Configure LRADC_CTRL[LRADC_HOLD_KEY_EN] to 1.

Step 11 Read the corresponding key voltage value from LRADC_DATA when the CPU receives the LRADC interrupt.

18.13.6.5 Calculation Formula

Calculation formula: LRADC_DATA = Vin/VREF*63, VREF=1.35 V

18.13.7 Register List

Module Name	Base Address
LRADC	0x02524000

Register Name	Offset	Description
LRADC_CTRL	0x0000	LRADC Control Register
LRADC_INTC	0x0004	LRADC Interrupt Control Register
LRADC_INTS	0x0008	LRADC Interrupt Status Register
LRADC_DATA0	0x000C	LRADC Data Register0
LRADC_DATA1	0x0010	LRADC Data Register1

18.13.8 Register Description

18.13.8.1 0x0000 LRADC Control Register (Default Value: 0x0100_0168)

Offset: 0x0000			Register Name: LRADC_CTRL
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x1	FIRST_CONVERT_DLY ADC First Convert Delay Setting ADC conversion is delayed by n samples.
23:22	R/W	0x0	CHANNEL_SEL Select the channel that be enabled 00: channel 0 only 01: channel 1 only 10: channel 1 and channel 0
21:20	/	/	/
19:16	R/W	0x0	CONTINUE_TIME_SELECT Continuous Mode Time Select One of 8*(N+1) sample as a valuable sample data.
15:14	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: LRADC_CTRL
Bit	Read/Write	Default/Hex	Description
13:12	R/W	0x0	KEY_MODE_SELECT Key Mode Select 00: Normal Mode 01: Single Mode 10: Continuous Mode
11:8	R/W	0x1	LEVELA_B_CNT Level A to Level B time threshold select Judge the ADC convert value from level A to level B in n+1 samples.
7	R/W	0x0	LRADC_HOLD_KEY_EN LRADC Hold KEY Enable 0: Disable 1: Enable
6	R/W	0x1	LRADC_CHANNEL_EN LRADC Channel Enable 0: Disable 1: Enable
5:4	R/W	0x2	LEVELB_VOL Level B Corresponding Data Value setting (the real voltage value) 00: 0x3C (1.286 V) 01: 0x39 (1.221 V) 10: 0x36 (1.157 V) 11: 0x33 (1.093 V)
3:2	R/W	0x2	LRADC_SAMPLE_RATE LRADC Sample Rate 00: 2 kHz 01: 1 kHz 10: 500 Hz 11: 250 Hz
1	/	/	/
0	R/W	0x0	LRADC_EN LRADC Enable 0: Disable 1: Enable

18.13.8.2 0x0004 LRADC Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: LRADC_INTC
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: LRADC_INTC
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	ADC1_KEYUP_IRQ_EN ADC1 Key Up IRQ Enable 0: Disable 1: Enable
11	R/W	0x0	ADC1_ALRDY_HOLD_IRQ_EN ADC1 Already Hold Key IRQ Enable 0: Disable 1: Enable
10	R/W	0x0	ADC1_HOLD_IRQ_EN ADC1 Hold Key IRQ Enable 0: Disable 1: Enable
9	R/W	0x0	ADC1_KEYDOWN_EN ADC1 Key Down Enable 0: Disable 1: Enable
8	R/W	0x0	ADC1_DATA_IRQ_EN ADC1 Data IRQ Enable 0: Disable 1: Enable
7:5	/	/	/
4	R/W	0x0	ADC0_KEYUP_IRQ_EN ADC0 Key Up IRQ Enable 0: Disable 1: Enable
3	R/W	0x0	ADC0_ALRDY_HOLD_IRQ_EN ADC0 Already Hold Key IRQ Enable 0: Disable 1: Enable
2	R/W	0x0	ADC0_HOLD_IRQ_EN ADC0 Hold Key IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	ADC0_KEYDOWN_EN ADC0 Key Down Enable 0: Disable 1: Enable
0	R/W	0x0	ADC0_DATA_IRQ_EN ADC0 Data IRQ Enable 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.13.8.3 0x0008 LRADC Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: LRADC_INTS
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W1C	0x0	ADC1_KEYUP_PENDING ADC1 Key up pending Bit When general Key pull up, the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
11	R/W1C	0x0	ADC1_ALRDY_HOLD_PENDING ADC1 Already Hold Pending Bit When hold Key is pulled down, pull the general key down if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
10	R/W1C	0x0	ADC1_HOLDKEY_PENDING ADC1 Hold Key Pending Bit When Hold Key is pulled down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: NO IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
9	R/W1C	0x0	ADC1_KEYDOWN_PENDING ADC1 Key Down IRQ Pending Bit When General Key is pulled down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: LRADC_INTS
Bit	Read/Write	Default/Hex	Description
8	R/W1C	0x0	ADC1_DATA_PENDING ADC1 Data IRQ Pending Bit 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
7:5	/	/	/
4	R/W1C	0x0	ADC0_KEYUP_PENDING ADC0 Key up Pending Bit When the general key is pulled up, and the corresponding interrupt is enabled, the status bit will be set. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
3	R/W1C	0x0	ADC0_ALRDY_HOLD_PENDING ADC0 Already Hold Pending Bit When the hold key is pulled down and the general key is pulled down, and the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
2	R/W1C	0x0	ADC0_HOLDKEY_PENDING ADC0 Hold Key Pending Bit When the hold key is pulled down, and the corresponding interrupt is enabled, the status bit is set and the interrupt line is set. 0: NO IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: LRADC_INTS
Bit	Read/Write	Default/Hex	Description
1	R/W1C	0x0	ADC0_KEYDOWN_PENDING ADC0 Key Down IRQ Pending Bit When the general key is pulled down, and the corresponding interrupt is enabled, the status bit is set and the interrupt line is set. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
0	R/W1C	0x0	ADC0_DATA_PENDING ADC0 Data IRQ Pending Bit 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.

18.13.8.4 0x000C LRADC Data Register0 (Default Value: 0x0000_003F)

Offset: 0x000C			Register Name: LRADC_DATA0
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5:0	R	0x3F	LRADC0_DATA LRADC0 Data

18.13.8.5 0x0010 LRADC Data Register1 (Default Value: 0x0000_003F)

Offset: 0x0010			Register Name: LRADC_DATA1
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5:0	R	0x3F	LRADC1_DATA LRADC1 Data

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.14 GPIO

18.14.1 Overview

The general purpose input/output (GPIO) is one of the blocks controlling the chip multiplexing pins. Each pin can be configured as input or output and these pins are used to generate input signals or output signals for special purposes.

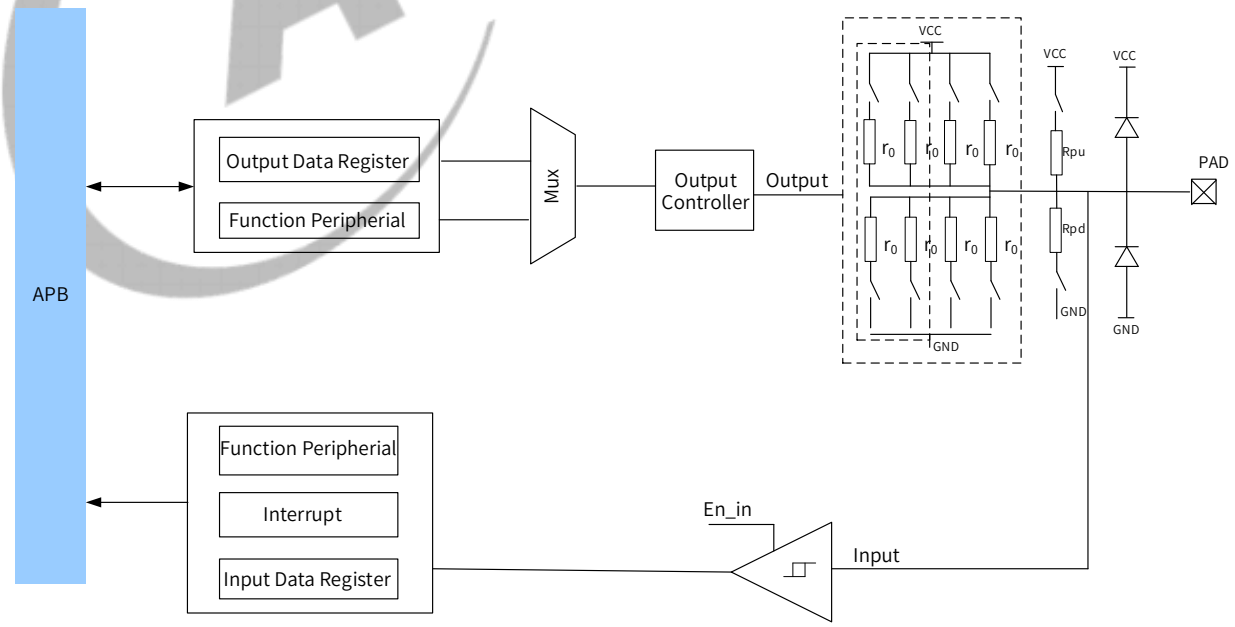
The GPIO has the following features:

- 11 groups of ports (PB, PC, PD, PE, PF, PG, PH, PJ, PK, PL, PM)
- Software control for each signal pin
- Each GPIO peripheral can produce an interrupt
- Pull-up/Pull-down/no-Pull register control
- Control the direction of every signal
- 4 drive strengths in each operating mode
- Up to 159 interrupts
- Configurable interrupt edges

18.14.2 Block Diagram

The following figure shows the block diagram of the GPIO.

Figure 18-74 GPIO Block Diagram



The overall I/O ports consists of the digital part (GPIO, peripheral interfaces) and IO analog part (output buffer, pull up/down, pad). The output of digital part can be selected by MUX, and the analog part can be used to configure pull-up/pull-down registers, driving strengths and so on.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

When in the read operation, read the current pin level to the APB bus. When not in the read operation, the external pins aren t connected to the APB bus, which is called the high-impedance state.

18.14.3 Functional Description

18.14.3.1 Multi-Functional Port

A733 includes 159 multi-functional input/output port pins. There are 11 ports as listed below.

Port Name	Number of I/O Pins	Input Driver	Output Driver	Multiplex I/O Pins	Typical Power Supply
PB	11	Schmitt	CMOS	UART/TWI/OWA/SPI/I2S/JTAG /LCD/PWM/FANOUT/HDMI	3.3V
PC	17	Schmitt	CMOS	NAND/SDC/SPI/SPIF	3.3V/1.8V
PD	24	Schmitt	CMOS	LCD/PWM/LVDS/DSI/EINK/SPI/UA RT/TWI/PCIE	3.3V/1.8V
PE	16	Schmitt	CMOS	MCSI/TWI/FANOUT/CSI/NCSI/HD MI/TCON/SPI/LEDC/I2S/IR_RX/P WM/UART/PCIE	3.3V/1.8V
PF	7	Schmitt	CMOS	SDC/JTAG/UART/TWI	3.3V/1.8V
PG	15	Schmitt	CMOS	SDC/UART/I2S/FANOUT/LCD/TWI /DMIC/HDMI/PWM	3.3V/1.8V
PH	17	Schmitt	CMOS	TWI/UART/DMIC/IR_TX/SPI/I2S/L EDC/RGMII	3.3V/1.8V
PJ	6	Schmitt	CMOS	LCD/PWM/SPI/UART/TWI	3.3V/1.8V
PK	26	Schmitt	CMOS	MCSI/TWI/UART/I2S/PWM/HDMI/ SPI/NCSI/JTAG/PCIE	3.3V/1.8V
PL	14	Schmitt	CMOS	S_TWI/S_UART/S_JTAG/S_IR_RX/ S_SPI/S_PWM	3.3V/1.8V
PM	6	Schmitt	CMOS	S_JTAG/S_PWM/S_IR_RX/S_SPI/ S_TWI/S_UART	3.3V/1.8V

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

The following tables show the multiplex function pins.

NOTE

For each GPIO, Function0 is input function; Function1 is output function; Function10 to Function13 are reserved.

Table 18-30 Port B Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PB0	I/O	UART2-TX	UART0-TX	SPI2-CS0	DSI-TRIG-LCD-TE1	LCD0-D0	JTAG-MS			PB-EINT0
PB1	I/O	UART2-RX	UART0-RX	SPI2-CLK		LCD0-D1	JTAG-CK			PB-EINT1
PB2	I/O	UART2-RTS		SPI2-MOSI	HDMI-SCL	LCD0-D8	JTAG-DO	TWI0-SCK		PB-EINT2
PB3	I/O	UART2-CTS		SPI2-MISO	HDMI-SDA	LCD0-D9	JTAG-DI	TWI0-SDA		PB-EINT3
PB4	I/O	PWM0-0	I2S0-MCLK	SPI2-CS1	HDMI-CEC	LCD0-D16		TWI1-SCK		PB-EINT4
PB5	I/O		I2S0-BCLK	SPI2-CS2	PWM0-1	LCD0-D17		TWI1-SDA		PB-EINT5
PB6	I/O	CLK-FANOUT1	I2S0-LRCK	SPI2-CS3	PWM0-2	PWM0-8				PB-EINT6
PB7	I/O	CLK-FANOUT2	I2S0-DOUT0	I2S0-DIN1	PWM0-9	OWA0-IN		TWI1-SCK		PB-EINT7
PB8	I/O	CLK-FANOUT3	I2S0-DIN0	I2S0-DOUT1	PWM1-0	OWA0-OUT		TWI1-SDA		PB-EINT8
PB9	I/O	UART0-TX	I2S0-DIN2	I2S0-DOUT2	PWM1-1	WATCHDOG-SIG	LCD0-D16	TWI8-SCK	TWI0-SCK	PB-EINT9
PB10	I/O	UART0-RX	I2S0-DIN3	I2S0-DOUT3	PWM1-2		LCD0-D17	TWI8-SDA	TWI0-SDA	PB-EINT10

Table 18-31 Port C Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PC0	I/O	NAND-WE	SDC2-DS	SDC3-DS						PC-EINT0
PC1	I/O	NAND-ALE	SDC2-RST	SDC3-RST						PC-EINT1
PC2	I/O	NAND-CLE			SPI0-MOSI	SPIF0-MOSI				PC-EINT2
PC3	I/O	NAND-CE1			SPI0-CS0	SPIF0-CS0				PC-EINT3
PC4	I/O	NAND-CE0			SPI0-MISO	SPIF0-MISO				PC-EINT4
PC5	I/O	NAND-RE	SDC2-CLK	SDC3-CLK						PC-EINT5
PC6	I/O	NAND-RB0	SDC2-CMD	SDC3-CMD						PC-EINT6
PC7	I/O	NAND-RB1			SPI0-CS1	SPIF0-DQS				PC-EINT7
PC8	I/O	NAND-DQ7	SDC2-D3	SDC3-D3		SPIF0-D7				PC-EINT8
PC9	I/O	NAND-DQ6	SDC2-D4	SDC3-D4		SPIF0-D6				PC-EINT9
PC10	I/O	NAND-DQ5	SDC2-D0	SDC3-D0		SPIF0-D5				PC-EINT10
PC11	I/O	NAND-DQ4	SDC2-D5	SDC3-D5		SPIF0-D4				PC-EINT11
PC12	I/O	NAND-DQS			SPI0-CLK	SPIF0-CLK				PC-EINT12
PC13	I/O	NAND-DQ3	SDC2-D1	SDC3-D1						PC-EINT13
PC14	I/O	NAND-DQ2	SDC2-D6	SDC3-D6						PC-EINT14
PC15	I/O	NAND-DQ1	SDC2-D2	SDC3-D2	SPI0-WP	SPIF0-WP/SPIF0-D2				PC-EINT15
PC16	I/O	NAND-DQ0	SDC2-D7	SDC3-D7	SPI0-HOLD	SPIF0-HOLD/SPIF0-D3				PC-EINT16

Table 18-32 Port D Multiplex Function

Pin Name	IO Type	Function2	Function3	Function 4	Function5	Function6	Function7	Function 8	Function 9	Function1 4
PD0	I/O	LCD0-D2	LVDS0-D0P	DSI0-D0P	EINK-D0		PWM0-0			PD-EINT0
PD1	I/O	LCD0-D3	LVDS0-D0N	DSI0-D0N	EINK-D1		PWM0-1			PD-EINT1
PD2	I/O	LCD0-D4	LVDS0-D1P	DSI0-D1P	EINK-D2		PWM0-2			PD-EINT2
PD3	I/O	LCD0-D5	LVDS0-D1N	DSI0-D1N	EINK-D3		PWM0-3			PD-EINT3
PD4	I/O	LCD0-D6	LVDS0-D2P	DSI0-CKP	EINK-D4		PWM0-4			PD-EINT4
PD5	I/O	LCD0-D7	LVDS0-D2N	DSI0-CKN	EINK-D5		PWM0-5			PD-EINT5
PD6	I/O	LCD0-D10	LVDS0-CKP	DSI0-D2P	EINK-D6		PWM0-6			PD-EINT6
PD7	I/O	LCD0-D11	LVDS0-CKN	DSI0-D2N	EINK-D7		PWM0-7			PD-EINT7
PD8	I/O	LCD0-D12	LVDS0-D3P	DSI0-D3P	EINK-D8		PWM0-8			PD-EINT8
PD9	I/O	LCD0-D13	LVDS0-D3N	DSI0-D3N	EINK-D9		PWM0-9			PD-EINT9
PD10	I/O	LCD0-D14	LVDS1-D0P	DSI1-D0P	EINK-D10	SPI1-CS0/DBI-CSX	PWM1-0			PD-EINT10
PD11	I/O	LCD0-D15	LVDS1-D0N	DSI1-D0N	EINK-D11	SPI1-CLK/DBI-SCLK	PWM1-1			PD-EINT11

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PD12	I/O	LCD0-D18	LVDS1-D1P	DSI1-D1P	EINK-D12	SPI1-MOSI/DBI-SDO	PWM1-2			PD-EINT12
PD13	I/O	LCD0-D19	LVDS1-D1N	DSI1-D1N	EINK-D13	SPI1-MISO/DBI-SDI/DBI-TE/DBI-DCX	PWM1-3			PD-EINT13
PD14	I/O	LCD0-D20	LVDS1-D2P	DSI1-CKP	EINK-D14	SPI1-HOLD/DBI-DCX/DBI-WRX	UART3-RTS			PD-EINT14
PD15	I/O	LCD0-D21	LVDS1-D2N	DSI1-CKN	EINK-D15	SPI1-CS1	UART3-CTS			PD-EINT15
PD16	I/O	LCD0-D22	LVDS1-CKP	DSI1-D2P	EINK-OEH	TWI2-SCK	UART3-TX			PD-EINT16
PD17	I/O	LCD0-D23	LVDS1-CKN	DSI1-D2N	EINK-LEH	TWI2-SDA	UART3-RX			PD-EINT17
PD18	I/O	LCD0-CLK	LVDS1-D3P	DSI1-D3P	EINK-CKH	SPI1-WP/DBI-TE	UART4-RTS			PD-EINT18
PD19	I/O	LCD0-DE	LVDS1-D3N	DSI1-D3N	EINK-STH	PWM1-5	UART4-CTS			PD-EINT19
PD20	I/O	LCD0-HSYNC	DSI-TRIG-LCD-TE1	TWI0-SCK	EINK-CKV	PCIE-CLKREQN	UART4-TX	TWI3-SCK	PWM0-2	PD-EINT20
PD21	I/O	LCD0-VSYNC		TWI0-SDA	EINK-MODE	PCIE-WAKEN	UART4-RX	TWI3-SDA	PWM0-3	PD-EINT21
PD22	I/O	PWM0-4			EINK-STV	PCIE-PERSTN	TWI0-SCK	TWI2-SCK	PWM1-4	PD-EINT22
PD23	I/O	PWM0-5				PCIE-CLKREQN	TWI0-SDA	TWI2-SDA	PWM1-5	PD-EINT23

Table 18-33 Port E Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PE0	I/O	MCSI0-MCLK	CSI0-XHS		SPI3-CS0		NCSI0-HSYNC	UART6-TX		PE-EINT0
PE1	OD	TWI2-SCK	CSI1-XHS		SPI3-CLK		NCSI0-VSYNC	UART6-RX		PE-EINT1
PE2	I/O	TWI2-SDA	CSI0-XVS-FSYNC		SPI3-MOSI		NCSI0-PCLK	UART6-RTS		PE-EINT2
PE3	I/O	TWI3-SCK	CSI1-XVS-FSYNC	PWM0-0	SPI3-MISO		NCSI0-D1	UART6-CTS		PE-EINT3
PE4	OD	TWI3-SDA	LEDC	PWM0-1	SPI3-CS1		NCSI0-D0	UART6-DCD		PE-EINT4
PE5	I/O	MCSI1-MCLK			PWM0-2		NCSI0-MCLK	UART6-DSR		PE-EINT5
PE6	I/O	CLK-FANOUT1	HDMI-CEC	I2S3-DIN0<MUX-HDMI-EDP>	I2S3-DOUT1<MUX-HDMI-EDP>		NCSI0-D2	UART6-DTR		PE-EINT6
PE7	I/O	CLK-FANOUT2	HDMI-SCL	I2S3-BCLK<MUX-HDMI-EDP>			NCSI0-D3	TWI11-SCK		PE-EINT7
PE8	I/O	CLK-FANOUT3	HDMI-SDA	I2S3-LRCK<MUX-HDMI-EDP>			NCSI0-D4	TWI11-SDA		PE-EINT8
PE9	I/O	MCSI2-MCLK	TCON-FSYNC0	I2S3-MCLK<MUX-HDMI-EDP>			NCSI0-D5	UART6-RI		PE-EINT9
PE10	I/O	TWI4-SCK	TCON-FSYNC1	I2S3-DIN3<MUX-HDMI-EDP>	I2S3-DOUT3<MUX-HDMI-EDP>		NCSI0-D6	UART1-RTS		PE-EINT10
PE11	I/O	TWI4-SDA	SPI3-MISO	I2S3-DIN2<MUX-HDMI-EDP>	I2S3-DOUT2<MUX-HDMI-EDP>	PCIE-CLKREQN	NCSI0-D7	UART1-CTS		PE-EINT11
PE12	I/O		SPI3-CS0	I2S3-DOUT0<MUX-HDMI-EDP>	I2S3-DIN1<MUX-HDMI-EDP>	PCIE-WAKEN		UART1-TX		PE-EINT12
PE13	I/O		SPI3-CLK			PCIE-PERSTN		UART1-RX		PE-EINT13
PE14	I/O		SPI3-MOSI		PWM1-8	PCIE-CLKREQN	IR-RX	TWI9-SCK		PE-EINT14
PE15	I/O		SPI3-CS1		PWM1-9	IR-RX		TWI9-SDA		PE-EINT15

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Table 18-34 Port F Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PF0	I/O	SDC0-D1	JTAG-MS		UART5-RTS	TWI2-SCK				PF-EINT0
PF1	I/O	SDC0-CMD	JTAG-DO							PF-EINT1
PF2	I/O	SDC0-CLK	UART0-TX							PF-EINT2
PF3	I/O	SDC0-D0	JTAG-DI		UART5-CTS	TWI2-SDA				PF-EINT3
PF4	I/O	SDC0-D3	UART0-RX		UART5-RX					PF-EINT4
PF5	I/O	SDC0-D2	JTAG-CK		UART5-TX					PF-EINT5
PF6	I/O									PF-EINT6

Table 18-35 Port G Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PG0	I/O	SDC1-CLK	LCD0-D0	PWM1-1						PG-EINT0
PG1	I/O	SDC1-CMD	LCD0-D1	PWM1-2						PG-EINT1
PG2	I/O	SDC1-D0	LCD0-D8	PWM1-3						PG-EINT2
PG3	I/O	SDC1-D1	LCD0-D9	PWM1-4						PG-EINT3
PG4	I/O	SDC1-D2	LCD0-D16	PWM1-5						PG-EINT4
PG5	I/O	SDC1-D3	LCD0-D17	PWM1-6						PG-EINT5
PG6	I/O	UART1-TX	UART4-TX	PWM1-7						PG-EINT6
PG7	I/O	UART1-RX	UART4-RX	PWM1-8						PG-EINT7
PG8	I/O	UART1-RTS	UART4-RTS	UART5-TX		TWI0-SCK				PG-EINT8
PG9	I/O	UART1-CTS	UART4-CTS	UART5-RX		TWI0-SDA				PG-EINT9
PG10	I/O	I2S1-MCLK	CLK-FANOUT0	PWM1-9		DMIC-CLK				PG-EINT10
PG11	I/O	I2S1-BCLK	TWI12-SCK	TWI9-SCK		DMIC-DATA3	HDMI-CEC			PG-EINT11
PG12	I/O	I2S1-LRCK	TWI12-SDA	TWI9-SDA		DMIC-DATA2	HDMI-SCL			PG-EINT12
PG13	I/O	I2S1-DOUT0	I2S1-DIN1	TWI6-SCK		DMIC-DATA1	HDMI-SDA			PG-EINT13
PG14	I/O	I2S1-DIN0	I2S1-DOUT1	TWI6-SDA		DMIC-DATA0				PG-EINT14

Table 18-36 Port H Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PH0	I/O	TWI0-SCK	I2S2-DOUT2	I2S2-DIN2	RGMII0-RXD1/RMII0-RXD1	TWI3-SCK	SPI1-HOLD			PH-EINT0
PH1	I/O	TWI0-SDA	I2S2-DOUT3	I2S2-DIN3	RGMII0-RXD0/RMII0-RXD0	TWI3-SDA	SPI1-WP			PH-EINT1
PH2	I/O	TWI1-SCK		I2S2-MCLK	RGMII0-RXCTL/RMII0-CRS-DV		SPI1-CS1			PH-EINT2
PH3	I/O	TWI1-SDA		I2S2-BCLK	RGMII0-CLKIN/RMII0-RXER		SPI1-MISO			PH-EINT3
PH4	I/O	UART3-TX	SPI2-CS3	I2S2-LRCK	RGMII0-TXD1/RMII0-TXD1		SPI1-CS0			PH-EINT4
PH5	I/O	UART3-RX	I2S2-DIN1	I2S2-DOUT0	RGMII0-TXD0/RMII0-TXD0		SPI1-MOSI			PH-EINT5
PH6	I/O	UART3-RTS	I2S2-DOUT1	I2S2-DIN0	RGMII0-TXCK/RMII0-TXCK		SPI1-CLK			PH-EINT6
PH7	I/O	UART3-CTS	SPI2-CS2	DSI-TRIG-LCD-TE1	RGMII0-TXCTL/RMII0-TXEN					PH-EINT7
PH8	I/O	DMIC-CLK	SPI2-CLK		RGMII0-MDC					PH-EINT8
PH9	I/O	DMIC-DATA0	SPI2-CS0		RGMII0-MDIO					PH-EINT9
PH10	I/O	DMIC-DATA1	SPI2-MOSI		RGMII0-RXD3/RMII0-NULL					PH-EINT10
PH11	I/O	DMIC-DATA2	SPI2-MISO		RGMII0-RXD2/RMII0-NULL					PH-EINT11
PH12	I/O	DMIC-DATA3	SPI2-CS1		RGMII0-RXCK/RMII0-NULL					PH-EINT12
PH13	I/O	UART5-TX			RGMII0-TXD3/RMII0-NULL	TWI7-SDA				PH-EINT13
PH14	I/O	UART5-RX			RGMII0-TXD2/RMII0-NULL	TWI7-SCK				PH-EINT14
PH15	I/O	UART5-RTS	LEDC	DSI-TRIG-LCD-TE1	RGMII0-EPHY-25/50M					PH-EINT15
PH16	I/O	UART5-CTS			IR-TX					PH-EINT16

Table 18-37 Port J Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PJ22	I/O		PWM1-4	UART3-TX	UART2-RTS	TWI7-SCK	TWI3-SCK	TWI11-SCK	LCD0-D8	PJ-EINT22
PJ23	I/O		PWM1-5	UART3-RX	UART2-CTS	TWI7-SDA	TWI3-SDA	TWI11-SDA	LCD0-D9	PJ-EINT23
PJ24	I/O		PWM1-6	UART4-TX			TWI4-SCK	SPI3-CLK		PJ-EINT24

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PJ25	I/O		PWM1-7	UART4-RX			TWI4-SDA	SPI3-MOSI		PJ-EINT25
PJ26	I/O		PWM1-8	UART4-RTS	UART2-TX		TWI5-SCK	SPI3-MISO	LCD0-D16	PJ-EINT26
PJ27	I/O		PWM1-9	UART4-CTS	UART2-RX	DSI-TRIG-LCD-TE1	TWI5-SDA	SPI3-CS0	LCD0-D17	PJ-EINT27

Table 18-38 Port K Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PK0	I/O	MCSIA-D0N	UART6-DCD	I2S4-BCLK<MUX-EDP>	HDMI-CEC	TWI1-SDA	NCSI1-HSYNC			PK-EINT0
PK1	I/O	MCSIA-D0P	UART6-DSR	I2S4-MCLK<MUX-EDP>	HDMI-SCL	TWI1-SCK	NCSI1-VSYNC			PK-EINT1
PK2	I/O	MCSIA-D1N	UART6-DTR	I2S4-LRCK<MUX-EDP>	HDMI-SDA	TWI5-SDA	NCSI1-PCLK			PK-EINT2
PK3	I/O	MCSIA-D1P	UART6-RI	I2S4-DIN0<MUX-EDP>	I2S4-DOUT1<MUX-EDP>	TWI5-SCK	NCSI1-MCLK			PK-EINT3
PK4	I/O	MCSIA-CKN	PCIE-WAKEN	I2S4-DOUT0<MUX-EDP>	I2S4-DIN1<MUX-EDP>	SPI3-CS0	NCSI1-D15			PK-EINT4
PK5	I/O	MCSIA-CKP	PCIE-CLKREQN	PWM1-8	PWM1-9	SPI3-CLK	NCSI1-D14			PK-EINT5
PK6	I/O	MCSIA-D2N	TWI2-SCK	UART4-TX	UART2-RTS	SPI3-MOSI	NCSI1-D13			PK-EINT6
PK7	I/O	MCSIA-D2P	TWI2-SDA	UART4-RX	UART2-CTS	SPI3-MISO	NCSI1-D12			PK-EINT7
PK8	I/O	MCSIA-D3N	MCSI0-MCLK	UART4-RTS	UART2-TX	SPI3-CS1	NCSI1-D11			PK-EINT8
PK9	I/O	MCSIA-D3P	MCSI2-MCLK	UART4-CTS	UART2-RX		NCSI1-D10			PK-EINT9
PK10	I/O	MCSIB-D0N	UART6-TX		PWM0-3		NCSI1-D9			PK-EINT10
PK11	I/O	MCSIB-D0P	UART6-RX		PWM0-4		NCSI1-D8			PK-EINT11
PK12	I/O	MCSIB-D1N	UART6-RTS		PWM0-5		NCSI1-D7			PK-EINT12
PK13	I/O	MCSIB-D1P	UART6-CTS		PWM0-6		NCSI1-D6			PK-EINT13
PK14	I/O	MCSIB-CKN	PCIE-PERSTN		PWM0-7		NCSI1-D5			PK-EINT14
PK15	I/O	MCSIB-CKP			PWM0-8		NCSI1-D4			PK-EINT15
PK16	I/O	MCSIB-D2N	TWI3-SCK	UART2-TX	PWM0-9		NCSI1-D3			PK-EINT16
PK17	I/O	MCSIB-D2P	TWI3-SDA	UART2-RX	PWM1-0		NCSI1-D2			PK-EINT17
PK18	I/O	MCSIB-D3N	MCSI1-MCLK	UART2-RTS	PWM1-1		NCSI1-D1	TWI9-SCK		PK-EINT18
PK19	I/O	MCSIB-D3P	MCSI2-MCLK	UART2-CTS	PWM1-2		NCSI1-D0	TWI9-SDA		PK-EINT19
PK20	I/O	MCSIC-D0N	TWI2-SCK	UART3-TX	PWM0-1		NCSI1-PCLK	UART1-RTS		PK-EINT20
PK21	I/O	MCSIC-D0P	TWI2-SDA	UART3-RX	PWM0-2		NCSI1-MCLK	UART1-CTS		PK-EINT21
PK22	I/O	MCSIC-D1N	TWI3-SCK	UART3-RTS	PWM1-6		NCSI1-HSYNC	UART1-TX		PK-EINT22
PK23	I/O	MCSIC-D1P	TWI3-SDA	UART3-CTS	PWM1-7		NCSI1-VSYNC	UART1-RX		PK-EINT23
PK24	I/O	MCSIC-CKN	MCSI0-MCLK	PWM0-6	TWI12-SCK			TWI10-SDA		PK-EINT24
PK25	I/O	MCSIC-CKP	MCSI1-MCLK	PWM0-7	TWI12-SDA			TWI10-SCK		PK-EINT25

Table 18-39 Port L Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PL0	I/O	S-TWI0-SCK	S-TWI1-SCK	S-TWI2-SCK						PL-EINT0

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PL1	I/O	S-TWI0-SDA	S-TWI1-SDA	S-TWI2-SDA	S-IR-RX					PL-EINT1
PL2	I/O	S-UART1-TX	S-UART0-TX	S-TWI1-SDA		S-PWM0-0				PL-EINT2
PL3	I/O	S-UART1-RX	S-UART0-RX	S-TWI1-SCK	S-IR-RX	S-PWM0-1				PL-EINT3
PL4	I/O	S-JTAG-MS	S-TWI2-SCK	S-SPI0-CS0	S-IR-RX	S-PWM0-2				PL-EINT4
PL5	I/O	S-JTAG-CK	S-TWI2-SDA	S-SPI0-CLK		S-PWM0-3				PL-EINT5
PL6	I/O	S-JTAG-DO	S-UART0-TX	S-SPI0-MOSI	S-IR-RX	S-PWM0-4				PL-EINT6
PL7	I/O	S-JTAG-DI	S-UART0-RX	S-SPI0-MISO		S-PWM0-5				PL-EINT7
PL8	I/O	S-TWI1-SCK	S-UART1-TX	S-TWI0-SCK	S-TWI2-SCK	S-PWM0-6				PL-EINT8
PL9	I/O	S-TWI1-SDA	S-UART1-RX	S-TWI0-SDA	S-TWI2-SDA	S-PWM0-7				PL-EINT9
PL10	I/O	S-UART0-TX	S-TWI2-SCK	S-UART1-TX		S-PWM0-8				PL-EINT10
PL11	I/O	S-UART0-RX	S-TWI2-SDA	S-UART1-RX	S-IR-RX	S-PWM0-9				PL-EINT11
PL12	I/O	S-UART1-TX	S-TWI1-SCK	S-TWI2-SCK	S-IR-RX					PL-EINT12
PL13	I/O	S-UART1-RX	S-TWI1-SDA	S-TWI2-SDA						PL-EINT13

Table 18-40 Port M Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PM0	I/O	S-JTAG-MS	S-SPI0-CS0	S-RJTAG-MS	S-TWI1-SCK	S-PWM0-2	S-IR-RX			PM-EINT0
PM1	I/O	S-JTAG-CK	S-SPI0-CLK	S-RJTAG-CK	S-TWI1-SDA	S-PWM0-3				PM-EINT1
PM2	I/O	S-JTAG-DO	S-SPI0-MOSI	S-UART0-TX	S-UART1-TX	S-PWM0-4				PM-EINT2
PM3	I/O	S-JTAG-DI	S-SPI0-MISO	S-UART0-RX	S-UART1-RX	S-PWM0-5				PM-EINT3
PM4	I/O	S-UART0-TX	S-TWI2-SCK	S-TWI1-SCK	S-UART1-TX	S-PWM0-0	S-IR-RX			PM-EINT4
PM5	I/O	S-UART0-RX	S-TWI2-SDA	S-TWI1-SDA	S-UART1-RX	S-PWM0-1	S-IR-RX			PM-EINT5

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.14.3.2 Port Function

The Port Controller supports 11 GPIOs, and each can be configured as Input, Output, Function Peripheral, I/O disable or Interrupt function. Their configuration instruction are as follows.

Table 18-41 Port Function

Category	Function	Buffer Strength	Pull Up	Pull Down
Input	GPIO/Multiplexing Input	/	X	X
Output	GPIO/Multiplexing Output	Y	X	X
Disable	Pull Up	/	Y	N
	Pull Down	/	N	Y
Interrupt	Trigger	/	X	X

NOTE

/: Configuration is unnecessary and invalid.

Y: Configuration is necessary. If no configuration, it will be configured to the default status.

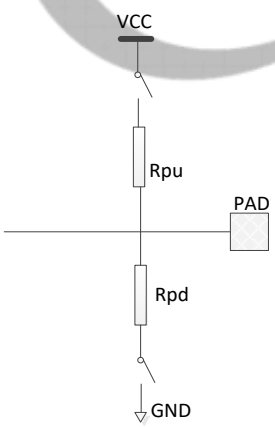
X: Configuration is selected according to the actual situation

N: Configuration is forbidden.

18.14.3.3 Pull-up, Pull-down, and High-impedance Input

Each IO can be configured as the internal pull-up, pull-down, or high-impedance input mode.

Figure 18-75 Pull-up, Pull-down, and High-impedance Input Mode



High-impedance: The output port is in the floating status. All the drives are turned off, and their levels are depended by the external levels.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Pull-up: The uncertain signals are pulled high by resistors, which performs the current-limiting function. In pull-up status, the IO is pulled up to VCC by Rpu.

Pull-down: The uncertain signals are pulled low by resistors. In pull-down status, the IO is pulled down to GND by Rpd.

NOTE

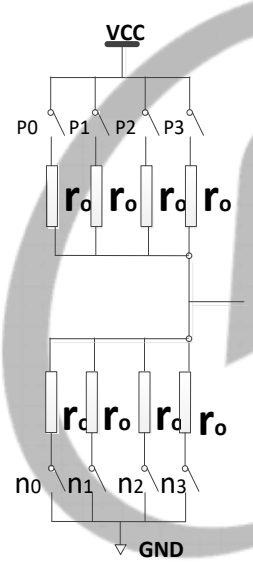
The pull-up/down resistor value of each IO is around 100K.

Whether pull-down, pull-up or high-impedance input is decided by the external circuit.

18.14.3.4 Output Driving Strength

Each IO can be set as different output driving strength. The IO driving strength diagram is as follows.

Figure 18-76 IO Buffer Strength Diagram



High Level Output

In the process of high level output, the n0, n1, n2, n3 of NMOS is off, and the p0, p1, p2, p3 of PMOS is on.

When the driving strength is set to 0, only the p0 is turned on, during which the output impedance is maximum, that is, the driving capability is the weakest. The output impedance is the turned-on r0.

When the driving strength is set to 1, only the p0 and p1 are turned on. The output impedance is r0/2, equivalent to the parallel-connected two r0.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

When the driving strength is set to 2, three MOS of p0-p3 are turned on. The output impedance is r0/3, equivalent to the parallel-connected three p0.

When the driving strength is set to 3, p0-p3 are turned on. The output impedance is r0/4, equivalent to the parallel-connected four p0.

Low Level Output

In the process of low level output, the p0, p1, p2, p3 of PMOS is off, and the n0, n1, n2, n3 of NMOS is on.

When the driving strength is set to 0, only the n0 is turned on, during which the output impedance is maximum, that is, the driving capability is the weakest. The output impedance is the turned-on r0.

When the driving strength is set to 1, only the n0 and n1 are turned on. The output impedance is r0/2, equivalent to the parallel-connected two r0.

When the driving strength is set to 2, three MOS of n0-n3 are turned on. The output impedance is r0/3, equivalent to the parallel-connected three r0.

When the driving strength is set to 3, n0-n3 are turned on. The output impedance is r0/4, equivalent to the parallel-connected four r0.

NOTE

a) No matter what kind of driver strength it is, r0 typical value is 200Ω when voltage is 3.3V and it is 100Ω when voltage is 1.8V.

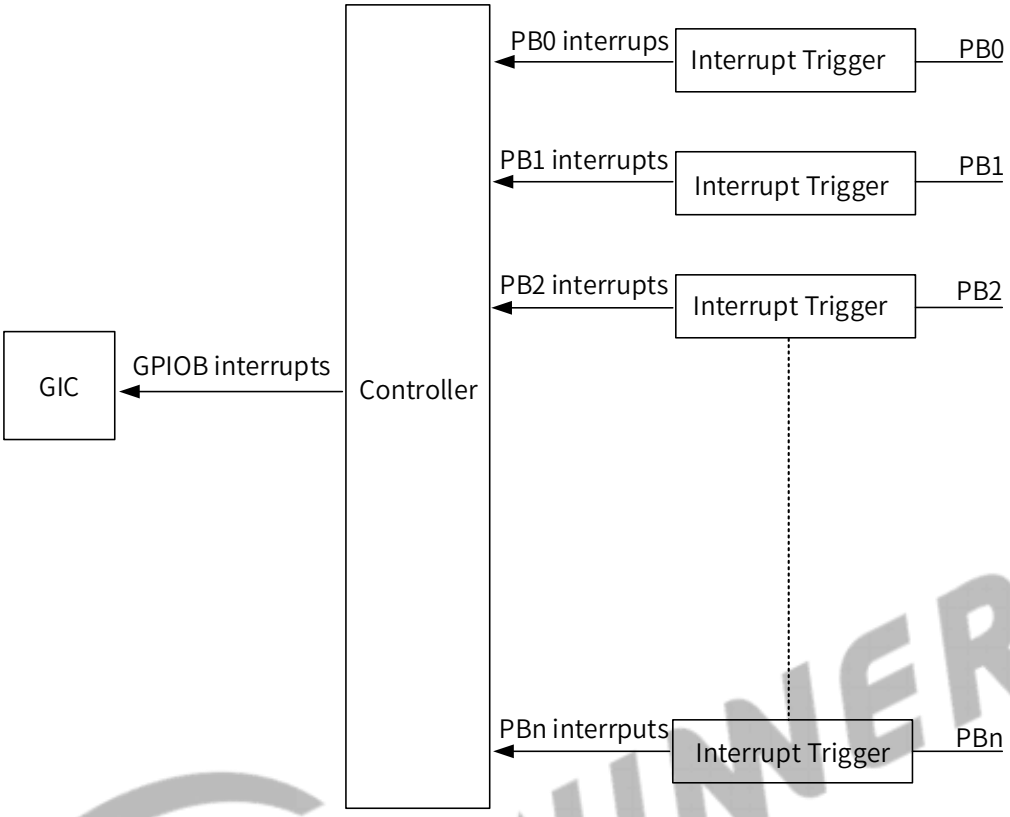
b) When GPIO is configured as input or interrupt functions, the output driver circuit is unconnected to port. Then, driver configuration is invalid.

18.14.3.5 Interrupts

There is an interrupt number for each group of IO, in which all IOs share one interrupt number. When an IO generates interrupts, the collector will send interrupt request to GIC. The user can query which IO generates interrupt in the external interrupt status registers. The following interrupt diagram takes PB as an example.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 18-77 GPIOB Interrupt Diagram



The interrupt trigger of GPIO supports the following trigger types.

- **Positive Edge**: When a low level changes to a high level, the IO will generate interrupts.
- **Negative Edge**: When a high level changes to a low level, the IO will generate interrupts.
- **High Level**: The IO will generate interrupts in the high level.
- **Low Level**: The IO will generate interrupts in the low level.
- **Double Edge**: The IO will generate interrupts both in the positive edge and negative edge.

The interrupt trigger types can be configured in the external interrupt configure registers.

The GPIO interrupts support hardware debounce function configuration in the external interrupt debounce Registers. In this way, the trigger signal will be sampled with a lower-frequency sample clock. As the dither frequency of signals is higher than their sample frequency, the debounce effect is reached.

The sample clock source can be set in the GPIO_INT_CLK_SELECT, and the prescale factor can be set in DEB_CLK_PRE_SCALE.

18.14.3.6 GPIO Group Withstand Voltage

Before using GPIO, you need to read the voltage in the GPIO Group Power Value Register. If it is 1, the power supply is 3.3V; in this condition, no voltage setting is needed. If it is 0, the power

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

supply is 1.8V; in this condition, the withstand voltage needs to be set in the GPIO Group Power Voltage Select Control Register.

If it is 0 in the GPIO Group Power Voltage Select Control Register, the GPIO group power supply will be set as 1.8V.

If it is 1 in the GPIO Group Power Voltage Select Control Register, the GPIO group power supply will be set as 3.3V.

If it is 2 in the GPIO Group Power Voltage Select Control Register, the GPIO group enters the adaptive mode. Their withstand voltage will be auto adjusted based on the detected GPIO voltage.

18.14.4 Programming Guidelines

18.14.4.1 Disabling I/O Pins

To disable I/O pins, follow the steps as below.

Step 1 Write 1111 to the Px_SELECT of the Px_CFG register to disable the I/O pins.

Step 2 If needed, set the pull-up/pull-down status of the I/O pins by setting the Px_PULL register. In the pull-up status, the pin level is 1 by default; in the pull-down status, the pin level is 0 by default.

18.14.4.2 Input Configuration

To configure I/O pins as the general input pins, follow the steps as below.

Step 1 Write 0 to the Px_SELECT of the Px_CFG register to enable input function.

Step 2 If needed, set the pull-up/pull-down status of the I/O pins by setting the Px_PULL register. When the I/O pins are externally driven, the external input value can be read; When the I/O pins are not externally driven, the pin statuses are 1 (pull-up) or 0 (pull-down).

Step 3 Read the pin status in the Px_DAT register.

18.14.4.3 Output Configuration

To configure I/O pins as the general output pins, follow the steps as below.

Step 1 Write 1 to the Px_SELECT of the Px_CFG register to enable output function.

Step 2 If needed, configure the Px_DRV register to set the output driving strength. When it is set as 11, the driving strength is maximum; when it is set as 0, the driving strength is minimum. It is set as 1 by default.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 3 If needed, configure the Px_PULL register to set the pull-up and pull-down status. When the output function is enabled, the I/O pin status are the same as the output signals; when the output function is disabled, the pin statuses are 1 (pull-up) or 0 (pull-down).

Step 4 Write to Px_DAT register or output 1 or 0 to I/O pins through atomic operation.

Step 5 During the atomic operation, write 1 to the corresponding bits in Px_DAT_SET. Writing 1 to corresponding bits in Px_DAT_CLR will clear them.

18.14.4.4 Interrupt Configuration

To configure I/O pins as the interrupt pins, follow the steps as below.

Step 1 Write 1110 to the Px_SELECT of the Px_CFG register to enable the interrupt function.

Step 2 If needed, set the pull-up/pull-down status of the I/O pins by setting the Px_PULL register. In the pull-up status, the interrupt input level is 1 by default in case of no driving strength. In the pull-down status, the interrupt input level is 0 by default in case of no driving strength.

Step 3 Set the interrupt trigger types in the Px_INT_CFG register.

Step 4 Set the debounce clock in the Px_INT_CFG register.

Step 5 Clear the IRQ pending status in the Px_INT_STA register.

Step 6 Enable external interrupts in the Px_INT_CTL register.

Step 7 After receiving interrupts, CPU will handle them. After that, the pending status of interrupts can be cleared in the Px_INT_STA register.

Step 8 Disable external interrupts in the Px_INT_CTL register in case no interrupts are needed.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

NOTE

a) It is not recommended to switch functions through PX_CFG in the interrupt mode. As the pins are in the input state, their input levels can be read in the PX_DAT.

b) Disable the interrupts in the PX_INT_CTL before configuring new functions during the function switches. Before switching back to the interrupt functions, clear the pending states in the PX_INT_STA.

c) If the interrupts aren t disabled in the course of function switches, an interrupt will be mistakenly triggered.

18.14.4.5 Multi-Function Configuration

To configure I/O pins as the multiplexing function pins, follow the steps as below.

Step 1 Set the pin as the needed function through the Px_SELECT bit of the Px_CFG register.

Step 2 Set the driving strength in the Px_DRV register according to the selected function.

Step 3 Set the pull-up/down status in the Px_PLL register according to the selected function. When the I/O pins are driven, the I/O pin status are the same as the output signals; when the output function are not driven, the pin statuses are 1 (pull-up) or 0 (pull-down).

18.14.4.6 Power Configuration

Configuring Group Power Voltage

The SoC only supports setting group power voltage in PF ports, which is able to be set as 3.3 V or 1.8V by configuring GPIO_POW_VAL_SET_CTL. The group power voltage in other ports is unconfigurable and depended on peripheral circuits.

Configuring Group Withstand Voltage

Configuring group withstand voltage intends to ensure that the internal withstand circuit voltage is consistent with group voltage. There are two modes, adaptive mode and manual mode, for users. In the SoC, the GPIO groups are configured as adaptive mode by default. When the power-up completes, the groups can be re-configured.

The following steps describe how to configure group withstand voltage.

- **Adaptive Mode**

In adaptive mode, each bit is set as 10 in GPIO_POW_MOD_SEL. The internal withstand circuit will adjust group withstand mode automatically depending on the detected GPIO voltage.

- **Manual Mode**

Step 4 Read the GPIO_POW_VAL to obtain the voltage statuses of GPIO group.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 5 Configure the GPIO_POW_MOD_SEL to keep the voltage statuses of corresponding bits consistent with the those of GPIO groups. Specifically, when the voltage value of GPIO group is 1.8V, configure the corresponding bit as 0; when the voltage value of GPIO group is 3.3V, configure the corresponding bit as 1.

18.14.5 Register List

18.14.5.1 GPIO Register List

Module Name	Base Address
GPIO	0x02000000

Register Name	Offset	Description
GPIO_POW_MOD_SEL	0x0040	GPIO Group Withstand Voltage Mode Select Register
GPIO_POW_VAL	0x0048	GPIO Group Power Value Register
GPIO_POW_VAL_SET_CTL	0x0070	GPIO Group Power Voltage Select Control Register
PB_CFG0	0x0100	PB Configure Register 0
PB_CFG1	0x0104	PB Configure Register 1
PB_DAT	0x0110	PB Data Register
PB_DAT_SET	0x0114	PB Data Set Register
PB_DAT_CLR	0x0118	PB Data Clear Register
PB_DRV0	0x0120	PB Multi-driving Register 0
PB_DRV1	0x0124	PB Multi-driving Register 1
PB_PUL0	0x0130	PB Pull Register 0
PB_INT_CFG0	0x0140	PB External Interrupt Configure Register 0
PB_INT_CFG1	0x0144	PB External Interrupt Configure Register 1
PB_INT_CTL	0x0150	PB External Interrupt Control Register
PB_INT_STA	0x0154	PB External Interrupt Status Register
PB_INT_DEB	0x0158	PB External Debounce Configure Register
PB_SECURE	0x0170	PB SECURE Configure Register
PC_CFG0	0x0180	PC Configure Register 0
PC_CFG1	0x0184	PC Configure Register 1
PC_CFG2	0x0188	PC Configure Register 2
PC_DAT	0x0190	PC Data Register
PC_DAT_SET	0x0194	PC Data Set Register
PC_DAT_CLR	0x0198	PC Data Clear Register
PC_DRV0	0x01A0	PC Multi-driving Register 0
PC_DRV1	0x01A4	PC Multi-driving Register 1
PC_DRV2	0x01A8	PC Multi-driving Register 2
PC_PUL0	0x01B0	PC Pull Register 0
PC_PUL1	0x01B4	PC Pull Register 1
PC_INT_CFG0	0x01C0	PC External Interrupt Configure Register 0

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
PC_INT_CFG1	0x01C4	PC External Interrupt Configure Register 1
PC_INT_CFG2	0x01C8	PC External Interrupt Configure Register 2
PC_INT_CTL	0x01D0	PC External Interrupt Control Register
PC_INT_STA	0x01D4	PC External Interrupt Status Register
PC_INT_DEB	0x01D8	PC External Debounce Configure Register
PC_SECURE	0x01F0	PC SECURE Configure Register
PD_CFG0	0x0200	PD Configure Register 0
PD_CFG1	0x0204	PD Configure Register 1
PD_CFG2	0x0208	PD Configure Register 2
PD_DAT	0x0210	PD Data Register
PD_DAT_SET	0x0214	PD Data Set Register
PD_DAT_CLR	0x0218	PD Data Clear Register
PD_DRV0	0x0220	PD Multi-driving Register 0
PD_DRV1	0x0224	PD Multi-driving Register 1
PD_DRV2	0x0228	PD Multi-driving Register 2
PD_PUL0	0x0230	PD Pull Register 0
PD_PUL1	0x0234	PD Pull Register 1
PD_INT_CFG0	0x0240	PD External Interrupt Configure Register 0
PD_INT_CFG1	0x0244	PD External Interrupt Configure Register 1
PD_INT_CFG2	0x0248	PD External Interrupt Configure Register 2
PD_INT_CTL	0x0250	PD External Interrupt Control Register
PD_INT_STA	0x0254	PD External Interrupt Status Register
PD_INT_DEB	0x0258	PD External Debounce Configure Register
PD_SECURE	0x0270	PD SECURE Configure Register
PE_CFG0	0x0280	PE Configure Register 0
PE_CFG1	0x0284	PE Configure Register 1
PE_DAT	0x0290	PE Data Register
PE_DAT_SET	0x0294	PE Data Set Register
PE_DAT_CLR	0x0298	PE Data Clear Register
PE_DRV0	0x02A0	PE Multi-driving Register 0
PE_DRV1	0x02A4	PE Multi-driving Register 1
PE_PUL0	0x02B0	PE Pull Register 0
PE_INT_CFG0	0x02C0	PE External Interrupt Configure Register 0
PE_INT_CFG1	0x02C4	PE External Interrupt Configure Register 1
PE_INT_CTL	0x02D0	PE External Interrupt Control Register
PE_INT_STA	0x02D4	PE External Interrupt Status Register
PE_INT_DEB	0x02D8	PE External Debounce Configure Register
PE_SECURE	0x02F0	PE SECURE Configure Register
PF_CFG0	0x0300	PF Configure Register 0
PF_DAT	0x0310	PF Data Register
PF_DAT_SET	0x0314	PF Data Set Register
PF_DAT_CLR	0x0318	PF Data Clear Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
PF_DRV0	0x0320	PF Multi-driving Register 0
PF_PUL0	0x0330	PF Pull Register 0
PF_INT_CFG0	0x0340	PF External Interrupt Configure Register 0
PF_INT_CTL	0x0350	PF External Interrupt Control Register
PF_INT_STA	0x0354	PF External Interrupt Status Register
PF_INT_DEB	0x0358	PF External Debounce Configure Register
PF_SECURE	0x0370	PF SECURE Configure Register
PG_CFG0	0x0380	PG Configure Register 0
PG_CFG1	0x0384	PG Configure Register 1
PG_DAT	0x0390	PG Data Register
PG_DAT_SET	0x0394	PG Data Set Register
PG_DAT_CLR	0x0398	PG Data Clear Register
PG_DRV0	0x03A0	PG Multi-driving Register 0
PG_DRV1	0x03A4	PG Multi-driving Register 1
PG_PUL0	0x03B0	PG Pull Register 0
PG_INT_CFG0	0x03C0	PG External Interrupt Configure Register 0
PG_INT_CFG1	0x03C4	PG External Interrupt Configure Register 1
PG_INT_CTL	0x03D0	PG External Interrupt Control Register
PG_INT_STA	0x03D4	PG External Interrupt Status Register
PG_INT_DEB	0x03D8	PG External Debounce Configure Register
PG_SECURE	0x03F0	PG SECURE Configure Register
PH_CFG0	0x0400	PH Configure Register 0
PH_CFG1	0x0404	PH Configure Register 1
PH_CFG2	0x0408	PH Configure Register 2
PH_DAT	0x0410	PH Data Register
PH_DAT_SET	0x0414	PH Data Set Register
PH_DAT_CLR	0x0418	PH Data Clear Register
PH_DRV0	0x0420	PH Multi-driving Register 0
PH_DRV1	0x0424	PH Multi-driving Register 1
PH_DRV2	0x0428	PH Multi-driving Register 2
PH_PUL0	0x0430	PH Pull Register 0
PH_PUL1	0x0434	PH Pull Register 1
PH_INT_CFG0	0x0440	PH External Interrupt Configure Register 0
PH_INT_CFG1	0x0444	PH External Interrupt Configure Register 1
PH_INT_CFG2	0x0448	PH External Interrupt Configure Register 2
PH_INT_CTL	0x0450	PH External Interrupt Control Register
PH_INT_STA	0x0454	PH External Interrupt Status Register
PH_INT_DEB	0x0458	PH External Debounce Configure Register
PH_SECURE	0x0470	PH SECURE Configure Register
PJ_CFG0	0x0500	PJ Configure Register 0
PJ_CFG1	0x0504	PJ Configure Register 1
PJ_CFG2	0x0508	PJ Configure Register 2

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
PJ_CFG3	0x050C	PJ Configure Register 3
PJ_DAT	0x0510	PJ Data Register
PJ_DAT_SET	0x0514	PJ Data Set Register
PJ_DAT_CLR	0x0518	PJ Data Clear Register
PJ_DRV0	0x0520	PJ Multi-driving Register 0
PJ_DRV1	0x0524	PJ Multi-driving Register 1
PJ_DRV2	0x0528	PJ Multi-driving Register 2
PJ_DRV3	0x052C	PJ Multi-driving Register 3
PJ_PUL0	0x0530	PJ Pull Register 0
PJ_PUL1	0x0534	PJ Pull Register 1
PJ_INT_CFG0	0x0540	PJ External Interrupt Configure Register 0
PJ_INT_CFG1	0x0544	PJ External Interrupt Configure Register 1
PJ_INT_CFG2	0x0548	PJ External Interrupt Configure Register 2
PJ_INT_CFG3	0x054C	PJ External Interrupt Configure Register 3
PJ_INT_CTL	0x0550	PJ External Interrupt Control Register
PJ_INT_STA	0x0554	PJ External Interrupt Status Register
PJ_INT_DEB	0x0558	PJ External Debounce Configure Register
PJ_SECURE	0x0570	PJ SECURE Configure Register
PK_CFG0	0x0580	PK Configure Register 0
PK_CFG1	0x0584	PK Configure Register 1
PK_CFG2	0x0588	PK Configure Register 2
PK_CFG3	0x058C	PK Configure Register 3
PK_DAT	0x0590	PK Data Register
PK_DAT_SET	0x0594	PK Data Set Register
PK_DAT_CLR	0x0598	PK Data Clear Register
PK_DRV0	0x05A0	PK Multi-driving Register 0
PK_DRV1	0x05A4	PK Multi-driving Register 1
PK_DRV2	0x05A8	PK Multi-driving Register 2
PK_DRV3	0x05AC	PK Multi-driving Register 3
PK_PUL0	0x05B0	PK Pull Register 0
PK_PUL1	0x05B4	PK Pull Register 1
PK_INT_CFG0	0x05C0	PK External Interrupt Configure Register 0
PK_INT_CFG1	0x05C4	PK External Interrupt Configure Register 1
PK_INT_CFG2	0x05C8	PK External Interrupt Configure Register 2
PK_INT_CFG3	0x05CC	PK External Interrupt Configure Register 3
PK_INT_CTL	0x05D0	PK External Interrupt Control Register
PK_INT_STA	0x05D4	PK External Interrupt Status Register
PK_INT_DEB	0x05D8	PK External Debounce Configure Register
PK_SECURE	0x05F0	PK SECURE Configure Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.14.5.2 S_GPIO Register List

Module Name	Base Address
S_GPIO	0x0702_5000

Register Name	Offset	Description
PL_CFG0	0x0000	PL Configure Register 0
PL_CFG1	0x0004	PL Configure Register 1
PL_DAT	0x0010	PL Data Register
PL_DRV0	0x0014	PL Multi-driving Register 0
PL_DRV1	0x0018	PL Multi-driving Register 1
PL_PUL0	0x0024	PL Pull Register 0
PM_CFG0	0x0030	PM Configure Register 0
PM_DAT	0x0040	PM Data Register
PM_DRV0	0x0044	PM Multi-driving Register 0
PM_PUL0	0x0054	PM Pull Register 0
PL_INT_CFG0	0x0200	PL External Interrupt Configure Register 0
PL_INT_CFG1	0x0204	PL External Interrupt Configure Register 1
PL_INT_CTL	0x0210	PL External Interrupt Control Register
PL_INT_STA	0x0214	PL External Interrupt Status Register
PL_INT_DEB	0x0218	PL External Debounce Configure Register
PM_INT_CFG0	0x0220	PM External Interrupt Configure Register 0
PM_INT_CTL	0x0230	PM External Interrupt Control Register
PM_INT_STA	0x0234	PM External Interrupt Status Register
PM_INT_DEB	0x0238	PM External Debounce Configure Register
GPIO_POW_MOD_SEL	0x0340	GPIO Group Withstand Voltage Mode Select Register
GPIO_POW_VAL	0x0348	GPIO Group Power Value Register
PL_SECURE	0x0400	PL SECURE Configure Register
PM_SECURE	0x0404	PM SECURE Configure Register

18.14.6 GPIO Register Description

18.14.6.1 0x0040 GPIO Group Withstand Voltage Mode Select Register (Default Value: 0x022A_AAA0)

Offset: 0x0040			Register Name: GPIO_POW_MOD_SEL
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0040			Register Name: GPIO_POW_MOD_SEL
Bit	Read/Write	Default/Hex	Description
25:24	R/W	0x2	VCCIO_PWR_MOD_SEL. VCC_IO POWER MODE Select. 00: 3.3V 01: auto 10: 3.3V 11: 1.8V
23:22	/	/	/
21:20	R/W	0x2	PK_PWR_MOD_SEL PK_POWER MODE Select. 00: 3.3V 01: auto 10: 3.3V 11: 1.8V
19:18	R/W	0x2	PJ_PWR_MOD_SEL PJ_POWER MODE Select. 00: 3.3V 01: auto 10: 3.3V 11: 1.8V
17:16	/	0x2	Reserved
15:14	R/W	0x2	PH_PWR_MOD_SEL PH_POWER MODE Select. 00: 3.3V 01: auto 10: 3.3V 11: 1.8V
13:12	R/W	0x2	PG_PWR_MOD_SEL PG_POWER MODE Select. 00: 3.3V 01: auto 10: 3.3V 11: 1.8V
11:10	R/W	0x2	PF_PWR_MOD_SEL PF_POWER MODE Select. 00: 3.3V 01: auto 10: 3.3V 11: 1.8V

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0040			Register Name: GPIO_POW_MOD_SEL
Bit	Read/Write	Default/Hex	Description
9:8	R/W	0x2	PE_PWR_MOD_SEL PE_POWER MODE Select. 00: 3.3V 01: auto 10: 3.3V 11: 1.8V
7:6	R/W	0x2	PD_PWR_MOD_SEL PD_POWER MODE Select. 00: 3.3V 01: auto 10: 3.3V 11: 1.8V
5:4	R/W	0x2	PC_PWR_MOD_SEL PC_POWER MODE Select. 00: 3.3V 01: auto 10: 3.3V 11: 1.8V
3:0	/	/	/

18.14.6.2 0x0048 GPIO Group Power Value Register (Default Value: 0x0115_5550)

Offset: 0x0048			Register Name: GPIO_POW_VAL
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R	0x1	VCCIO_PWR_VAL VCC_IO Power Value. 00: Invalid 01: Invalid 10: 3.3V 11: 1.8V
23:22	/	/	/
21:20	R	0x1	PK_PWR_VAL PK_Port Power Value. 00: Invalid 01: Invalid 10: 3.3V 11: 1.8V

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0048			Register Name: GPIO_POW_VAL
Bit	Read/Write	Default/Hex	Description
19:18	R	0x1	PJ_PWR_VAL PJ_Port Power Value. 00: Invalid 01: Invalid 10: 3.3V 11: 1.8V
17:16	/	0x1	Reserved
15:14	R	0x1	PH_PWR_VAL PH_Port Power Value. 00: Invalid 01: Invalid 10: 3.3V 11: 1.8V
13:12	R	0x1	PG_PWR_VAL PG_Port Power Value. 00: Invalid 01: Invalid 10: 3.3V 11: 1.8V
11:10	R	0x1	PF_PWR_VAL PF_Port Power Value. 00: Invalid 01: Invalid 10: 3.3V 11: 1.8V
9:8	R	0x1	PE_PWR_VAL PE_Port Power Value. 00: Invalid 01: Invalid 10: 3.3V 11: 1.8V
7:6	R	0x1	PD_PWR_VAL PD_Port Power Value. 00: Invalid 01: Invalid 10: 3.3V 11: 1.8V

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0048			Register Name: GPIO_POW_VAL
Bit	Read/Write	Default/Hex	Description
5:4	R	0x1	PC_PWR_VAL PC_Port Power Value. 00: Invalid 01: Invalid 10: 3.3V 11: 1.8V
3:0	/	/	/

18.14.6.3 0x0070 GPIO Group Power Voltage Select Control Register (Default Value: 0x0000_0001)

Offset: 0x0070			Register Name: GPIO_POW_VAL_SET_CTL
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	VCC_PF_PWR_VOL_SEL VCC_PF Power Voltage Select Control. 0: 1.8V 1: 3.3V

18.14.6.4 0x0100 PB Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0100			Register Name: PB_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PB7_SELECT PB7 Select. 0000: Input 0001: Output 0010: CLK-FANOUT2 0011: I2S0-DOUT0 0100: I2S0-DIN1 0101: PWM0-9 0110: OWA0-IN 0111: Reserved 1000: TWI1-SCK 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT7 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0100			Register Name: PB_CFG0
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0xF	PB6_SELECT PB6 Select. 0000: Input 0001: Output 0010: CLK-FANOUT1 0011: I2S0-LRCK 0100: SPI2-CS3 0101: PWM0-2 0110: PWM0-8 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT6 1111: IO Disable
23:20	R/W	0xF	PB5_SELECT PB5 Select. 0000: Input 0001: Output 0010: Reserved 0011: I2S0-BCLK 0100: SPI2-CS2 0101: PWM0-1 0110: LCD0-D17 0111: Reserved 1000: TWI1-SDA 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT5 1111: IO Disable
19:16	R/W	0xF	PB4_SELECT PB4 Select. 0000: Input 0001: Output 0010: PWM0-0 0011: I2S0-MCLK 0100: SPI2-CS1 0101: HDMI-CEC 0110: LCD0-D16 0111: Reserved 1000: TWI1-SCK 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT4 1111: IO Disable
15:12	R/W	0xF	PB3_SELECT PB3 Select. 0000: Input 0001: Output 0010: UART2-CTS 0011: Reserved 0100: SPI2-MISO 0101: HDMI-SDA 0110: LCD0-D9 0111: JTAG-DI 1000: TWI0-SDA 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT3 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0100			Register Name: PB_CFG0
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0xF	PB2_SELECT PB2 Select. 0000: Input 0001: Output 0010: UART2-RTS 0011: Reserved 0100: SPI2-MOSI 0101: HDMI-SCL 0110: LCD0-D8 0111: JTAG-DO 1000: TWI0-SCK 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT2 1111: IO Disable
7:4	R/W	0xF	PB1_SELECT PB1 Select. 0000: Input 0001: Output 0010: UART2-RX 0011: UART0-RX 0100: SPI2-CLK 0101: Reserved 0110: LCD0-D1 0111: JTAG-CK 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT1 1111: IO Disable
3:0	R/W	0xF	PB0_SELECT PB0 Select. 0000: Input 0001: Output 0010: UART2-TX 0011: UART0-TX 0100: SPI2-CS0 0101: DSI-TRIG-LCD-TE1 0110: LCD0-D0 0111: JTAG-MS 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT0 1111: IO Disable

18.14.6.5 0x0104 PB Configure Register 1 (Default Value: 0x0000_0FFF)

Offset: 0x0104			Register Name: PB_CFG1
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0104			Register Name: PB_CFG1
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0xF	PB10_SELECT PB10 Select. 0000: Input 0001: Output 0010: UART0-RX 0011: I2S0-DIN3 0100: I2S0-DOUT3 0101: PWM1-2 0110: Reserved 0111: LCD0-D17 1000: TWI8-SDA 1001: TWI0-SDA 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT10 1111: IO Disable
7:4	R/W	0xF	PB9_SELECT PB9 Select. 0000: Input 0001: Output 0010: UART0-TX 0011: I2S0-DIN2 0100: I2S0-DOUT2 0101: PWM1-1 0110: WATCHDOG-SIG 0111: LCD0-D16 1000: TWI8-SCK 1001: TWI0-SCK 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT9 1111: IO Disable
3:0	R/W	0xF	PB8_SELECT PB8 Select. 0000: Input 0001: Output 0010: CLK-FANOUT3 0011: I2S0-DIN0 0100: I2S0-DOUT1 0101: PWM1-0 0110: OWA0-OUT 0111: Reserved 1000: TWI1-SDA 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT8 1111: IO Disable

18.14.6.6 0x0110 PB Data Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: PB_DAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0110			Register Name: PB_DAT
Bit	Read/Write	Default/Hex	Description
10:0	R/W	0	PB_DAT PB Data. If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

18.14.6.7 0x0114 PB Data Set Register (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: PB_DAT_SET
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10	R/W1S	0x0	PORT10_DAT_SET Writing 1 to this bit can set bit 10 in the PB_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 10 in PB_DAT register.
9	R/W1S	0x0	PORT9_DAT_SET Writing 1 to this bit can set bit 9 in the PB_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 9 in PB_DAT register.
8	R/W1S	0x0	PORT8_DAT_SET Writing 1 to this bit can set bit 8 in the PB_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 8 in PB_DAT register.
7	R/W1S	0x0	PORT7_DAT_SET Writing 1 to this bit can set bit 7 in the PB_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 7 in PB_DAT register.
6	R/W1S	0x0	PORT6_DAT_SET Writing 1 to this bit can set bit 6 in the PB_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 6 in PB_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0114			Register Name: PB_DAT_SET
Bit	Read/Write	Default/Hex	Description
5	R/W1S	0x0	PORT5_DAT_SET Writing 1 to this bit can set bit 5 in the PB_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 5 in PB_DAT register.
4	R/W1S	0x0	PORT4_DAT_SET Writing 1 to this bit can set bit 4 in the PB_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 4 in PB_DAT register.
3	R/W1S	0x0	PORT3_DAT_SET Writing 1 to this bit can set bit 3 in the PB_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 3 in PB_DAT register.
2	R/W1S	0x0	PORT2_DAT_SET Writing 1 to this bit can set bit 2 in the PB_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 2 in PB_DAT register.
1	R/W1S	0x0	PORT1_DAT_SET Writing 1 to this bit can set bit 1 in the PB_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 1 in PB_DAT register.
0	R/W1S	0x0	PORT0_DAT_SET Writing 1 to this bit can set bit 0 in the PB_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 0 in PB_DAT register.

18.14.6.8 0x0118 PB Data Clear Register (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: PB_DAT_CLR
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10	R/W1C	0x0	PORT10_DAT_CLR Writing 1 to this bit clear bit 10 in the PB_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 10 in PB_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0118			Register Name: PB_DAT_CLR
Bit	Read/Write	Default/Hex	Description
9	R/W1C	0x0	PORT9_DAT_CLR Writing 1 to this bit clear bit 9 in the PB_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 9 in PB_DAT register.
8	R/W1C	0x0	PORT8_DAT_CLR Writing 1 to this bit clear bit 8 in the PB_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 8 in PB_DAT register.
7	R/W1C	0x0	PORT7_DAT_CLR Writing 1 to this bit clear bit 7 in the PB_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 7 in PB_DAT register.
6	R/W1C	0x0	PORT6_DAT_CLR Writing 1 to this bit clear bit 6 in the PB_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 6 in PB_DAT register.
5	R/W1C	0x0	PORT5_DAT_CLR Writing 1 to this bit clear bit 5 in the PB_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 5 in PB_DAT register.
4	R/W1C	0x0	PORT4_DAT_CLR Writing 1 to this bit clear bit 4 in the PB_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 4 in PB_DAT register.
3	R/W1C	0x0	PORT3_DAT_CLR Writing 1 to this bit clear bit 3 in the PB_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 3 in PB_DAT register.
2	R/W1C	0x0	PORT2_DAT_CLR Writing 1 to this bit clear bit 2 in the PB_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 2 in PB_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0118			Register Name: PB_DAT_CLR
Bit	Read/Write	Default/Hex	Description
1	R/W1C	0x0	PORT1_DAT_CLR Writing 1 to this bit clear bit 1 in the PB_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 1 in PB_DAT register.
0	R/W1C	0x0	PORT0_DAT_CLR Writing 1 to this bit clear bit 0 in the PB_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 0 in PB_DAT register.

18.14.6.9 0x0120 PB Multi-Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x0120			Register Name: PB_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PB7_DRV PB7 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PB6_DRV PB6 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PB5_DRV PB5 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PB4_DRV PB4 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PB3_DRV PB3 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0120			Register Name: PB_DRV0
Bit	Read/Write	Default/Hex	Description
9:8	R/W	0x1	PB2_DRV PB2 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PB1_DRV PB1 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PB0_DRV PB0 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

18.14.6.10 0x0124 PB Multi-Driving Register 1 (Default Value: 0x0000_0111)

Offset: 0x0124			Register Name: PB_DRV1
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:8	R/W	0x1	PB10_DRV PB10 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PB9_DRV PB9 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PB8_DRV PB8 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

18.14.6.11 0x0130 PB Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: PB_PUL0
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0130			Register Name: PB_PUL0
Bit	Read/Write	Default/Hex	Description
21:20	R/W	0x0	PB10_PULL PB10 Pull_up or down Select. 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PB9_PULL PB9 Pull_up or down Select. 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PB8_PULL PB8 Pull_up or down Select. 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PB7_PULL PB7 Pull_up or down Select. 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PB6_PULL PB6 Pull_up or down Select. 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PB5_PULL PB5 Pull_up or down Select. 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PB4_PULL PB4 Pull_up or down Select. 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PB3_PULL PB3 Pull_up or down Select. 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PB2_PULL PB2 Pull_up or down Select. 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PB1_PULL PB1 Pull_up or down Select. 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0130			Register Name: PB_PUL0
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x0	PB0_PULL PB0 Pull_up or down Select. 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved

18.14.6.12 0x0140 PB External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0140			Register Name: PB_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0140			Register Name: PB_INT_CFG0
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT3_CFG External INT3 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

18.14.6.13 0x0144 PB External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0144			Register Name: PB_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0144			Register Name: PB_INT_CFG1
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0x0	EINT10_CFG External INT10 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

18.14.6.14 0x0150 PB External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: PB_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10	R/W	0x0	EINT10_CTL External INT10 Enable. 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0150			Register Name: PB_INT_CTL
Bit	Read/Write	Default/Hex	Description
8	R/W	0x0	EINT8_CTL External INT8 Enable. 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable. 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable. 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable. 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable. 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable. 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable. 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable. 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable. 0: Disable 1: Enable

18.14.6.15 0x0154 PB External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0154			Register Name: PB_INT_STA
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0154			Register Name: PB_INT_STA
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10	R/W1C	0x0	EINT10_STATUS External INT10 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W1C	0x0	EINT9_STATUS External INT9 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W1C	0x0	EINT8_STATUS External INT8 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W1C	0x0	EINT7_STATUS External INT7 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0154			Register Name: PB_INT_STA
Bit	Read/Write	Default/Hex	Description
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

18.14.6.16 0x0158 PB External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0158			Register Name: PB_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n. The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select. 0: RTC_32K 1: SYS_CLK24M

18.14.6.17 0x0170 PB SECURE Configure Register (Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: PB_SECURE
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PORT31_SEC_SEL Port31 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0170			Register Name: PB_SECURE
Bit	Read/Write	Default/Hex	Description
30	R/W	0x0	PORT30_SEC_SEL Port30 secure select. 0: Not secure 1: Secure
29	R/W	0x0	PORT29_SEC_SEL Port29 secure select. 0: Not secure 1: Secure
28	R/W	0x0	PORT28_SEC_SEL Port28 secure select. 0: Not secure 1: Secure
27	R/W	0x0	PORT27_SEC_SEL Port27 secure select. 0: Not secure 1: Secure
26	R/W	0x0	PORT26_SEC_SEL Port26 secure select. 0: Not secure 1: Secure
25	R/W	0x0	PORT25_SEC_SEL Port25 secure select. 0: Not secure 1: Secure
24	R/W	0x0	PORT24_SEC_SEL Port24 secure select. 0: Not secure 1: Secure
23	R/W	0x0	PORT23_SEC_SEL Port23 secure select. 0: Not secure 1: Secure
22	R/W	0x0	PORT22_SEC_SEL Port22 secure select. 0: Not secure 1: Secure
21	R/W	0x0	PORT21_SEC_SEL Port21 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0170			Register Name: PB_SECURE
Bit	Read/Write	Default/Hex	Description
20	R/W	0x0	PORT20_SEC_SEL Port20 secure select. 0: Not secure 1: Secure
19	R/W	0x0	PORT19_SEC_SEL Port19 secure select. 0: Not secure 1: Secure
18	R/W	0x0	PORT18_SEC_SEL Port18 secure select. 0: Not secure 1: Secure
17	R/W	0x0	PORT17_SEC_SEL Port17 secure select. 0: Not secure 1: Secure
16	R/W	0x0	PORT16_SEC_SEL Port16 secure select. 0: Not secure 1: Secure
15	R/W	0x0	PORT15_SEC_SEL Port15 secure select. 0: Not secure 1: Secure
14	R/W	0x0	PORT14_SEC_SEL Port14 secure select. 0: Not secure 1: Secure
13	R/W	0x0	PORT13_SEC_SEL Port13 secure select. 0: Not secure 1: Secure
12	R/W	0x0	PORT12_SEC_SEL Port12 secure select. 0: Not secure 1: Secure
11	R/W	0x0	PORT11_SEC_SEL Port11 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0170			Register Name: PB_SECURE
Bit	Read/Write	Default/Hex	Description
10	R/W	0x0	PORT10_SEC_SEL Port10 secure select. 0: Not secure 1: Secure
9	R/W	0x0	PORT9_SEC_SEL Port9 secure select. 0: Not secure 1: Secure
8	R/W	0x0	PORT8_SEC_SEL Port8 secure select. 0: Not secure 1: Secure
7	R/W	0x0	PORT7_SEC_SEL Port7 secure select. 0: Not secure 1: Secure
6	R/W	0x0	PORT6_SEC_SEL Port6 secure select. 0: Not secure 1: Secure
5	R/W	0x0	PORT5_SEC_SEL Port5 secure select. 0: Not secure 1: Secure
4	R/W	0x0	PORT4_SEC_SEL Port4 secure select. 0: Not secure 1: Secure
3	R/W	0x0	PORT3_SEC_SEL Port3 secure select. 0: Not secure 1: Secure
2	R/W	0x0	PORT2_SEC_SEL Port2 secure select. 0: Not secure 1: Secure
1	R/W	0x0	PORT1_SEC_SEL Port1 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0170			Register Name: PB_SECURE
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	PORT0_SEC_SEL Port0 secure select. 0: Not secure 1: Secure

18.14.6.18 0x0180 PC Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0180			Register Name: PC_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PC7_SELECT PC7 Select. 0000: Input 0001: Output 0010: NAND-RB1 0011: Reserved 0100: Reserved 0101: SPI0-CS1 0110: SPIF0-DQS 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT7 1111: IO Disable
27:24	R/W	0xF	PC6_SELECT PC6 Select. 0000: Input 0001: Output 0010: NAND-RB0 0011: SDC2-CMD 0100: SDC3-CMD 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT6 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0180			Register Name: PC_CFG0
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0xF	PC5_SELECT PC5 Select. 0000: Input 0001: Output 0010: NAND-RE 0011: SDC2-CLK 0100: SDC3-CLK 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT5 1111: IO Disable
19:16	R/W	0xF	PC4_SELECT PC4 Select. 0000: Input 0001: Output 0010: NAND-CE0 0011: Reserved 0100: Reserved 0101: SPI0-MISO 0110: SPIF0-MISO 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT4 1111: IO Disable
15:12	R/W	0xF	PC3_SELECT PC3 Select. 0000: Input 0001: Output 0010: NAND-CE1 0011: Reserved 0100: Reserved 0101: SPI0-CS0 0110: SPIF0-CS0 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT3 1111: IO Disable
11:8	R/W	0xF	PC2_SELECT PC2 Select. 0000: Input 0001: Output 0010: NAND-CLE 0011: Reserved 0100: Reserved 0101: SPI0-MOSI 0110: SPIF0-MOSI 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT2 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0180			Register Name: PC_CFG0
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0xF	PC1_SELECT PC1 Select. 0000: Input 0001: Output 0010: NAND-ALE 0011: SDC2-RST 0100: SDC3-RST 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT1 1111: IO Disable
3:0	R/W	0xF	PC0_SELECT PC0 Select. 0000: Input 0001: Output 0010: NAND-WE 0011: SDC2-DS 0100: SDC3-DS 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT0 1111: IO Disable

18.14.6.19 0x0184 PC Configure Register 1 (Default Value: 0xFFFF_FFFF)

Offset: 0x0184			Register Name: PC_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PC15_SELECT PC15 Select. 0000: Input 0001: Output 0010: NAND-DQ1 0011: SDC2-D2 0100: SDC3-D2 0101: SPI0-WP 0110: SPIF0-WP/SPIF0-D2 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT15 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0184			Register Name: PC_CFG1
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0xF	PC14_SELECT PC14 Select. 0000: Input 0001: Output 0010: NAND-DQ2 0011: SDC2-D6 0100: SDC3-D6 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT14 1111: IO Disable
23:20	R/W	0xF	PC13_SELECT PC13 Select. 0000: Input 0001: Output 0010: NAND-DQ3 0011: SDC2-D1 0100: SDC3-D1 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT13 1111: IO Disable
19:16	R/W	0xF	PC12_SELECT PC12 Select. 0000: Input 0001: Output 0010: NAND-DQS 0011: Reserved 0100: Reserved 0101: SPI0-CLK 0110: SPIF0-CLK 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT12 1111: IO Disable
15:12	R/W	0xF	PC11_SELECT PC11 Select. 0000: Input 0001: Output 0010: NAND-DQ4 0011: SDC2-D5 0100: SDC3-D5 0101: Reserved 0110: SPIF0-D4 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT11 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0184			Register Name: PC_CFG1
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0xF	PC10_SELECT PC10 Select. 0000: Input 0001: Output 0010: NAND-DQ5 0011: SDC2-D0 0100: SDC3-D0 0101: Reserved 0110: SPIF0-D5 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT10 1111: IO Disable
7:4	R/W	0xF	PC9_SELECT PC9 Select. 0000: Input 0001: Output 0010: NAND-DQ6 0011: SDC2-D4 0100: SDC3-D4 0101: Reserved 0110: SPIF0-D6 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT9 1111: IO Disable
3:0	R/W	0xF	PC8_SELECT PC8 Select. 0000: Input 0001: Output 0010: NAND-DQ7 0011: SDC2-D3 0100: SDC3-D3 0101: Reserved 0110: SPIF0-D7 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT8 1111: IO Disable

18.14.6.20 0x0188 PC Configure Register 2 (Default Value: 0x0000_000F)

Offset: 0x0188			Register Name: PC_CFG2
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0188			Register Name: PC_CFG2
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xF	PC16_SELECT PC16 Select. 0000: Input 0001: Output 0010: NAND-DQ0 0011: SDC2-D7 0100: SDC3-D7 0101: SPI0-HOLD 0110: SPIF0-HOLD/SPIF0-D3 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT16 1111: IO Disable

18.14.6.21 0x0190 PC Data Register (Default Value: 0x0000_0000)

Offset: 0x0190			Register Name: PC_DAT
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16:0	R/W	0	PC_DAT PC Data. If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

18.14.6.22 0x0194 PC Data Set Register (Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: PC_DAT_SET
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W1S	0x0	PORT16_DAT_SET Writing 1 to this bit can set bit 16 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 16 in PC_DAT register.
15	R/W1S	0x0	PORT15_DAT_SET Writing 1 to this bit can set bit 15 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 15 in PC_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0194			Register Name: PC_DAT_SET
Bit	Read/Write	Default/Hex	Description
14	R/W1S	0x0	PORT14_DAT_SET Writing 1 to this bit can set bit 14 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 14 in PC_DAT register.
13	R/W1S	0x0	PORT13_DAT_SET Writing 1 to this bit can set bit 13 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 13 in PC_DAT register.
12	R/W1S	0x0	PORT12_DAT_SET Writing 1 to this bit can set bit 12 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 12 in PC_DAT register.
11	R/W1S	0x0	PORT11_DAT_SET Writing 1 to this bit can set bit 11 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 11 in PC_DAT register.
10	R/W1S	0x0	PORT10_DAT_SET Writing 1 to this bit can set bit 10 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 10 in PC_DAT register.
9	R/W1S	0x0	PORT9_DAT_SET Writing 1 to this bit can set bit 9 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 9 in PC_DAT register.
8	R/W1S	0x0	PORT8_DAT_SET Writing 1 to this bit can set bit 8 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 8 in PC_DAT register.
7	R/W1S	0x0	PORT7_DAT_SET Writing 1 to this bit can set bit 7 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 7 in PC_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0194			Register Name: PC_DAT_SET
Bit	Read/Write	Default/Hex	Description
6	R/W1S	0x0	PORT6_DAT_SET Writing 1 to this bit can set bit 6 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 6 in PC_DAT register.
5	R/W1S	0x0	PORT5_DAT_SET Writing 1 to this bit can set bit 5 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 5 in PC_DAT register.
4	R/W1S	0x0	PORT4_DAT_SET Writing 1 to this bit can set bit 4 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 4 in PC_DAT register.
3	R/W1S	0x0	PORT3_DAT_SET Writing 1 to this bit can set bit 3 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 3 in PC_DAT register.
2	R/W1S	0x0	PORT2_DAT_SET Writing 1 to this bit can set bit 2 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 2 in PC_DAT register.
1	R/W1S	0x0	PORT1_DAT_SET Writing 1 to this bit can set bit 1 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 1 in PC_DAT register.
0	R/W1S	0x0	PORT0_DAT_SET Writing 1 to this bit can set bit 0 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 0 in PC_DAT register.

18.14.6.23 0x0198 PC Data Clear Register (Default Value: 0x0000_0000)

Offset: 0x0198			Register Name: PC_DAT_CLR
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0198			Register Name: PC_DAT_CLR
Bit	Read/Write	Default/Hex	Description
16	R/W1C	0x0	PORT16_DAT_CLR Writing 1 to this bit clear bit 16 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 16 in PC_DAT register.
15	R/W1C	0x0	PORT15_DAT_CLR Writing 1 to this bit clear bit 15 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 15 in PC_DAT register.
14	R/W1C	0x0	PORT14_DAT_CLR Writing 1 to this bit clear bit 14 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 14 in PC_DAT register.
13	R/W1C	0x0	PORT13_DAT_CLR Writing 1 to this bit clear bit 13 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 13 in PC_DAT register.
12	R/W1C	0x0	PORT12_DAT_CLR Writing 1 to this bit clear bit 12 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 12 in PC_DAT register.
11	R/W1C	0x0	PORT11_DAT_CLR Writing 1 to this bit clear bit 11 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 11 in PC_DAT register.
10	R/W1C	0x0	PORT10_DAT_CLR Writing 1 to this bit clear bit 10 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 10 in PC_DAT register.
9	R/W1C	0x0	PORT9_DAT_CLR Writing 1 to this bit clear bit 9 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 9 in PC_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0198			Register Name: PC_DAT_CLR
Bit	Read/Write	Default/Hex	Description
8	R/W1C	0x0	PORT8_DAT_CLR Writing 1 to this bit clear bit 8 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 8 in PC_DAT register.
7	R/W1C	0x0	PORT7_DAT_CLR Writing 1 to this bit clear bit 7 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 7 in PC_DAT register.
6	R/W1C	0x0	PORT6_DAT_CLR Writing 1 to this bit clear bit 6 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 6 in PC_DAT register.
5	R/W1C	0x0	PORT5_DAT_CLR Writing 1 to this bit clear bit 5 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 5 in PC_DAT register.
4	R/W1C	0x0	PORT4_DAT_CLR Writing 1 to this bit clear bit 4 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 4 in PC_DAT register.
3	R/W1C	0x0	PORT3_DAT_CLR Writing 1 to this bit clear bit 3 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 3 in PC_DAT register.
2	R/W1C	0x0	PORT2_DAT_CLR Writing 1 to this bit clear bit 2 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 2 in PC_DAT register.
1	R/W1C	0x0	PORT1_DAT_CLR Writing 1 to this bit clear bit 1 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 1 in PC_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0198			Register Name: PC_DAT_CLR
Bit	Read/Write	Default/Hex	Description
0	R/W1C	0x0	PORT0_DAT_CLR Writing 1 to this bit clear bit 0 in the PC_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 0 in PC_DAT register.

18.14.6.24 0x01A0 PC Multi-Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x01A0			Register Name: PC_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PC7_DRV PC7 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PC6_DRV PC6 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PC5_DRV PC5 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PC4_DRV PC4 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PC3_DRV PC3 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PC2_DRV PC2 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x01A0			Register Name: PC_DRV0
Bit	Read/Write	Default/Hex	Description
5:4	R/W	0x1	PC1_DRV PC1 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PC0_DRV PC0 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

18.14.6.25 0x01A4 PC Multi-Driving Register 1 (Default Value: 0x1111_1111)

Offset: 0x01A4			Register Name: PC_DRV1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PC15_DRV PC15 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PC14_DRV PC14 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PC13_DRV PC13 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PC12_DRV PC12 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PC11_DRV PC11 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x01A4			Register Name: PC_DRV1
Bit	Read/Write	Default/Hex	Description
9:8	R/W	0x1	PC10_DRV PC10 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PC9_DRV PC9 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PC8_DRV PC8 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

18.14.6.26 0x01A8 PC Multi-Driving Register 2 (Default Value: 0x0000_0001)

Offset: 0x01A8			Register Name: PC_DRV2
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x1	PC16_DRV PC16 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

18.14.6.27 0x01B0 PC Pull Register 0 (Default Value: 0x0000_5140)

Offset: 0x01B0			Register Name: PC_PUL0
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	PC15_PULL PC15 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
29:28	R/W	0x0	PC14_PULL PC14 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x01B0			Register Name: PC_PUL0
Bit	Read/Write	Default/Hex	Description
27:26	R/W	0x0	PC13_PULL PC13 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PC12_PULL PC12 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PC11_PULL PC11 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PC10_PULL PC10 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PC9_PULL PC9 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PC8_PULL PC8 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x1	PC7_PULL PC7 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x1	PC6_PULL PC6 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PC5_PULL PC5 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x1	PC4_PULL PC4 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x01B0			Register Name: PC_PUL0
Bit	Read/Write	Default/Hex	Description
7:6	R/W	0x1	PC3_PULL PC3 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PC2_PULL PC2 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PC1_PULL PC1 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PC0_PULL PC0 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

18.14.6.28 0x01B4 PC Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x01B4			Register Name: PC_PUL1
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	PC16_PULL PC16 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

18.14.6.29 0x01C0 PC External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x01C0			Register Name: PC_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x01C0			Register Name: PC_INT_CFG0
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0x0	EINT6_CFG External INT6 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x01C0			Register Name: PC_INT_CFG0
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0x0	EINT1_CFG External INT1 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

18.14.6.30 0x01C4 PC External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x01C4			Register Name: PC_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT15_CFG External INT15 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x01C4			Register Name: PC_INT_CFG1
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0x0	EINT13_CFG External INT13 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x01C4			Register Name: PC_INT_CFG1
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	EINT8_CFG External INT8 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

18.14.6.31 0x01C8 PC External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x01C8			Register Name: PC_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	EINT16_CFG External INT16 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

18.14.6.32 0x01D0 PC External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x01D0			Register Name: PC_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	EINT16_CTL External INT16 Enable. 0: Disable 1: Enable
15	R/W	0x0	EINT15_CTL External INT15 Enable. 0: Disable 1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x01D0			Register Name: PC_INT_CTL
Bit	Read/Write	Default/Hex	Description
13	R/W	0x0	EINT13_CTL External INT13 Enable. 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable. 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable. 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable. 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable. 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable. 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable. 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable. 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable. 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x01D0			Register Name: PC_INT_CTL
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	EINT3_CTL External INT3 Enable. 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable. 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable. 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable. 0: Disable 1: Enable

18.14.6.33 0x01D4 PC External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x01D4			Register Name: PC_INT_STA
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W1C	0x0	EINT16_STATUS External INT16 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
15	R/W1C	0x0	EINT15_STATUS External INT15 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W1C	0x0	EINT14_STATUS External INT14 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x01D4			Register Name: PC_INT_STA
Bit	Read/Write	Default/Hex	Description
13	R/W1C	0x0	EINT13_STATUS External INT13 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W1C	0x0	EINT12_STATUS External INT12 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W1C	0x0	EINT11_STATUS External INT11 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W1C	0x0	EINT10_STATUS External INT10 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W1C	0x0	EINT9_STATUS External INT9 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W1C	0x0	EINT8_STATUS External INT8 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W1C	0x0	EINT7_STATUS External INT7 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x01D4			Register Name: PC_INT_STA
Bit	Read/Write	Default/Hex	Description
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

18.14.6.34 0x01D8 PC External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x01D8			Register Name: PC_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n. The selected clock source is prescaled by 2^n
3:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x01D8			Register Name: PC_INT_DEB
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select. 0: RTC_32K 1: SYS_CLK24M

18.14.6.35 0x01F0 PC SECURE Configure Register (Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: PC_SECURE
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PORT31_SEC_SEL Port31 secure select. 0: Not secure 1: Secure
30	R/W	0x0	PORT30_SEC_SEL Port30 secure select. 0: Not secure 1: Secure
29	R/W	0x0	PORT29_SEC_SEL Port29 secure select. 0: Not secure 1: Secure
28	R/W	0x0	PORT28_SEC_SEL Port28 secure select. 0: Not secure 1: Secure
27	R/W	0x0	PORT27_SEC_SEL Port27 secure select. 0: Not secure 1: Secure
26	R/W	0x0	PORT26_SEC_SEL Port26 secure select. 0: Not secure 1: Secure
25	R/W	0x0	PORT25_SEC_SEL Port25 secure select. 0: Not secure 1: Secure
24	R/W	0x0	PORT24_SEC_SEL Port24 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x01F0			Register Name: PC_SECURE
Bit	Read/Write	Default/Hex	Description
23	R/W	0x0	PORT23_SEC_SEL Port23 secure select. 0: Not secure 1: Secure
22	R/W	0x0	PORT22_SEC_SEL Port22 secure select. 0: Not secure 1: Secure
21	R/W	0x0	PORT21_SEC_SEL Port21 secure select. 0: Not secure 1: Secure
20	R/W	0x0	PORT20_SEC_SEL Port20 secure select. 0: Not secure 1: Secure
19	R/W	0x0	PORT19_SEC_SEL Port19 secure select. 0: Not secure 1: Secure
18	R/W	0x0	PORT18_SEC_SEL Port18 secure select. 0: Not secure 1: Secure
17	R/W	0x0	PORT17_SEC_SEL Port17 secure select. 0: Not secure 1: Secure
16	R/W	0x0	PORT16_SEC_SEL Port16 secure select. 0: Not secure 1: Secure
15	R/W	0x0	PORT15_SEC_SEL Port15 secure select. 0: Not secure 1: Secure
14	R/W	0x0	PORT14_SEC_SEL Port14 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x01F0			Register Name: PC_SECURE
Bit	Read/Write	Default/Hex	Description
13	R/W	0x0	PORT13_SEC_SEL Port13 secure select. 0: Not secure 1: Secure
12	R/W	0x0	PORT12_SEC_SEL Port12 secure select. 0: Not secure 1: Secure
11	R/W	0x0	PORT11_SEC_SEL Port11 secure select. 0: Not secure 1: Secure
10	R/W	0x0	PORT10_SEC_SEL Port10 secure select. 0: Not secure 1: Secure
9	R/W	0x0	PORT9_SEC_SEL Port9 secure select. 0: Not secure 1: Secure
8	R/W	0x0	PORT8_SEC_SEL Port8 secure select. 0: Not secure 1: Secure
7	R/W	0x0	PORT7_SEC_SEL Port7 secure select. 0: Not secure 1: Secure
6	R/W	0x0	PORT6_SEC_SEL Port6 secure select. 0: Not secure 1: Secure
5	R/W	0x0	PORT5_SEC_SEL Port5 secure select. 0: Not secure 1: Secure
4	R/W	0x0	PORT4_SEC_SEL Port4 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x01F0			Register Name: PC_SECURE
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	PORT3_SEC_SEL Port3 secure select. 0: Not secure 1: Secure
2	R/W	0x0	PORT2_SEC_SEL Port2 secure select. 0: Not secure 1: Secure
1	R/W	0x0	PORT1_SEC_SEL Port1 secure select. 0: Not secure 1: Secure
0	R/W	0x0	PORT0_SEC_SEL Port0 secure select. 0: Not secure 1: Secure

18.14.6.36 0x0200 PD Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0200			Register Name: PD_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PD7_SELECT PD7 Select. 0000: Input 0001: Output 0010: LCD0-D11 0011: LVDS0-CKN 0100: DSI0-D2N 0101: EINK-D7 0110: Reserved 0111: PWM0-7 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT7 1111: IO Disable
27:24	R/W	0xF	PD6_SELECT PD6 Select. 0000: Input 0001: Output 0010: LCD0-D10 0011: LVDS0-CKP 0100: DSI0-D2P 0101: EINK-D6 0110: Reserved 0111: PWM0-6 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT6 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0200			Register Name: PD_CFG0
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0xF	PD5_SELECT PD5 Select. 0000: Input 0001: Output 0010: LCD0-D7 0011: LVDS0-D2N 0100: DSI0-CKN 0101: EINK-D5 0110: Reserved 0111: PWM0-5 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT5 1111: IO Disable
19:16	R/W	0xF	PD4_SELECT PD4 Select. 0000: Input 0001: Output 0010: LCD0-D6 0011: LVDS0-D2P 0100: DSI0-CKP 0101: EINK-D4 0110: Reserved 0111: PWM0-4 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT4 1111: IO Disable
15:12	R/W	0xF	PD3_SELECT PD3 Select. 0000: Input 0001: Output 0010: LCD0-D5 0011: LVDS0-D1N 0100: DSI0-D1N 0101: EINK-D3 0110: Reserved 0111: PWM0-3 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT3 1111: IO Disable
11:8	R/W	0xF	PD2_SELECT PD2 Select. 0000: Input 0001: Output 0010: LCD0-D4 0011: LVDS0-D1P 0100: DSI0-D1P 0101: EINK-D2 0110: Reserved 0111: PWM0-2 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT2 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0200			Register Name: PD_CFG0
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0xF	PD1_SELECT PD1 Select. 0000: Input 0001: Output 0010: LCD0-D3 0011: LVDS0-D0N 0100: DSI0-D0N 0101: EINK-D1 0110: Reserved 0111: PWM0-1 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT1 1111: IO Disable
3:0	R/W	0xF	PD0_SELECT PD0 Select. 0000: Input 0001: Output 0010: LCD0-D2 0011: LVDS0-D0P 0100: DSI0-D0P 0101: EINK-D0 0110: Reserved 0111: PWM0-0 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT0 1111: IO Disable

18.14.6.37 0x0204 PD Configure Register 1 (Default Value: 0xFFFF_FFFF)

Offset: 0x0204			Register Name: PD_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PD15_SELECT PD15 Select. 0000: Input 0001: Output 0010: LCD0-D21 0011: LVDS1-D2N 0100: DSI1-CKN 0101: EINK-D15 0110: SPI1-CS1 0111: UART3-CTS 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT15 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0204			Register Name: PD_CFG1
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0xF	PD14_SELECT PD14 Select. 0000: Input 0001: Output 0010: LCD0-D20 0011: LVDS1-D2P 0100: DSI1-CKP 0101: EINK-D14 0110: SPI1-HOLD/DBI-DCX/DBI-WRX 0111: UART3-RTS 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT14 1111: IO Disable
23:20	R/W	0xF	PD13_SELECT PD13 Select. 0000: Input 0001: Output 0010: LCD0-D19 0011: LVDS1-D1N 0100: DSI1-D1N 0101: EINK-D13 0110: SPI1-MISO/DBI-SDI/DBI-TE/DBI-DCX 0111: PWM1-3 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT13 1111: IO Disable
19:16	R/W	0xF	PD12_SELECT PD12 Select. 0000: Input 0001: Output 0010: LCD0-D18 0011: LVDS1-D1P 0100: DSI1-D1P 0101: EINK-D12 0110: SPI1-MOSI/DBI-SDO 0111: PWM1-2 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT12 1111: IO Disable
15:12	R/W	0xF	PD11_SELECT PD11 Select. 0000: Input 0001: Output 0010: LCD0-D15 0011: LVDS1-D0N 0100: DSI1-D0N 0101: EINK-D11 0110: SPI1-CLK/DBI-SCLK 0111: PWM1-1 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT11 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0204			Register Name: PD_CFG1
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0xF	PD10_SELECT PD10 Select. 0000: Input 0001: Output 0010: LCD0-D14 0011: LVDS1-D0P 0100: DSI1-D0P 0101: EINK-D10 0110: SPI1-CS0/DBI-CSX 0111: PWM1-0 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT10 1111: IO Disable
7:4	R/W	0xF	PD9_SELECT PD9 Select. 0000: Input 0001: Output 0010: LCD0-D13 0011: LVDS0-D3N 0100: DSI0-D3N 0101: EINK-D9 0110: Reserved 0111: PWM0-9 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT9 1111: IO Disable
3:0	R/W	0xF	PD8_SELECT PD8 Select. 0000: Input 0001: Output 0010: LCD0-D12 0011: LVDS0-D3P 0100: DSI0-D3P 0101: EINK-D8 0110: Reserved 0111: PWM0-8 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT8 1111: IO Disable

18.14.6.38 0x0208 PD Configure Register 2 (Default Value: 0xFFFF_FFFF)

Offset: 0x0208			Register Name: PD_CFG2
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0208			Register Name: PD_CFG2
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PD23_SELECT PD23 Select. 0000: Input 0001: Output 0010: PWM0-5 0011: Reserved 0100: Reserved 0101: Reserved 0110: PCIE-CLKREQN 0111: TWI0-SDA 1000: TWI2-SDA 1001: PWM1-5 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT23 1111: IO Disable
27:24	R/W	0xF	PD22_SELECT PD22 Select. 0000: Input 0001: Output 0010: PWM0-4 0011: Reserved 0100: Reserved 0101: EINK-STV 0110: PCIE-PERSTN 0111: TWI0-SCK 1000: TWI2-SCK 1001: PWM1-4 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT22 1111: IO Disable
23:20	R/W	0xF	PD21_SELECT PD21 Select. 0000: Input 0001: Output 0010: LCD0-VSYNC 0011: Reserved 0100: TWI0-SDA 0101: EINK-MODE 0110: PCIE-WAKEN 0111: UART4-RX 1000: TWI3-SDA 1001: PWM0-3 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT21 1111: IO Disable
19:16	R/W	0xF	PD20_SELECT PD20 Select. 0000: Input 0001: Output 0010: LCD0-HSYNC 0011: DSI-TRIG-LCD-TE1 0100: TWI0-SCK 0101: EINK-CKV 0110: PCIE-CLKREQN 0111: UART4-TX 1000: TWI3-SCK 1001: PWM0-2 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT20 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0208			Register Name: PD_CFG2
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0xF	PD19_SELECT PD19 Select. 0000: Input 0001: Output 0010: LCD0-DE 0011: LVDS1-D3N 0100: DSI1-D3N 0101: EINK-STH 0110: PWM1-5 0111: UART4-CTS 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT19 1111: IO Disable
11:8	R/W	0xF	PD18_SELECT PD18 Select. 0000: Input 0001: Output 0010: LCD0-CLK 0011: LVDS1-D3P 0100: DSI1-D3P 0101: EINK-CKH 0110: SPI1-WP/DBI-TE 0111: UART4-RTS 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT18 1111: IO Disable
7:4	R/W	0xF	PD17_SELECT PD17 Select. 0000: Input 0001: Output 0010: LCD0-D23 0011: LVDS1-CKN 0100: DSI1-D2N 0101: EINK-LEH 0110: TWI2-SDA 0111: UART3-RX 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT17 1111: IO Disable
3:0	R/W	0xF	PD16_SELECT PD16 Select. 0000: Input 0001: Output 0010: LCD0-D22 0011: LVDS1-CKP 0100: DSI1-D2P 0101: EINK-OEH 0110: TWI2-SCK 0111: UART3-TX 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT16 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.14.6.39 0x0210 PD Data Register (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: PD_DAT
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0	PD_DAT PD Data. If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

18.14.6.40 0x0214 PD Data Set Register (Default Value: 0x0000_0000)

Offset: 0x0214			Register Name: PD_DAT_SET
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W1S	0x0	PORT23_DAT_SET Writing 1 to this bit can set bit 23 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 23 in PD_DAT register.
22	R/W1S	0x0	PORT22_DAT_SET Writing 1 to this bit can set bit 22 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 22 in PD_DAT register.
21	R/W1S	0x0	PORT21_DAT_SET Writing 1 to this bit can set bit 21 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 21 in PD_DAT register.
20	R/W1S	0x0	PORT20_DAT_SET Writing 1 to this bit can set bit 20 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 20 in PD_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0214			Register Name: PD_DAT_SET
Bit	Read/Write	Default/Hex	Description
19	R/W1S	0x0	PORT19_DAT_SET Writing 1 to this bit can set bit 19 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 19 in PD_DAT register.
18	R/W1S	0x0	PORT18_DAT_SET Writing 1 to this bit can set bit 18 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 18 in PD_DAT register.
17	R/W1S	0x0	PORT17_DAT_SET Writing 1 to this bit can set bit 17 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 17 in PD_DAT register.
16	R/W1S	0x0	PORT16_DAT_SET Writing 1 to this bit can set bit 16 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 16 in PD_DAT register.
15	R/W1S	0x0	PORT15_DAT_SET Writing 1 to this bit can set bit 15 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 15 in PD_DAT register.
14	R/W1S	0x0	PORT14_DAT_SET Writing 1 to this bit can set bit 14 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 14 in PD_DAT register.
13	R/W1S	0x0	PORT13_DAT_SET Writing 1 to this bit can set bit 13 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 13 in PD_DAT register.
12	R/W1S	0x0	PORT12_DAT_SET Writing 1 to this bit can set bit 12 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 12 in PD_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0214			Register Name: PD_DAT_SET
Bit	Read/Write	Default/Hex	Description
11	R/W1S	0x0	PORT11_DAT_SET Writing 1 to this bit can set bit 11 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 11 in PD_DAT register.
10	R/W1S	0x0	PORT10_DAT_SET Writing 1 to this bit can set bit 10 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 10 in PD_DAT register.
9	R/W1S	0x0	PORT9_DAT_SET Writing 1 to this bit can set bit 9 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 9 in PD_DAT register.
8	R/W1S	0x0	PORT8_DAT_SET Writing 1 to this bit can set bit 8 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 8 in PD_DAT register.
7	R/W1S	0x0	PORT7_DAT_SET Writing 1 to this bit can set bit 7 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 7 in PD_DAT register.
6	R/W1S	0x0	PORT6_DAT_SET Writing 1 to this bit can set bit 6 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 6 in PD_DAT register.
5	R/W1S	0x0	PORT5_DAT_SET Writing 1 to this bit can set bit 5 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 5 in PD_DAT register.
4	R/W1S	0x0	PORT4_DAT_SET Writing 1 to this bit can set bit 4 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 4 in PD_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0214			Register Name: PD_DAT_SET
Bit	Read/Write	Default/Hex	Description
3	R/W1S	0x0	PORT3_DAT_SET Writing 1 to this bit can set bit 3 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 3 in PD_DAT register.
2	R/W1S	0x0	PORT2_DAT_SET Writing 1 to this bit can set bit 2 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 2 in PD_DAT register.
1	R/W1S	0x0	PORT1_DAT_SET Writing 1 to this bit can set bit 1 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 1 in PD_DAT register.
0	R/W1S	0x0	PORT0_DAT_SET Writing 1 to this bit can set bit 0 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 0 in PD_DAT register.

18.14.6.41 0x0218 PD Data Clear Register (Default Value: 0x0000_0000)

Offset: 0x0218			Register Name: PD_DAT_CLR
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W1C	0x0	PORT23_DAT_CLR Writing 1 to this bit clear bit 23 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 23 in PD_DAT register.
22	R/W1C	0x0	PORT22_DAT_CLR Writing 1 to this bit clear bit 22 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 22 in PD_DAT register.
21	R/W1C	0x0	PORT21_DAT_CLR Writing 1 to this bit clear bit 21 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 21 in PD_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0218			Register Name: PD_DAT_CLR
Bit	Read/Write	Default/Hex	Description
20	R/W1C	0x0	PORT20_DAT_CLR Writing 1 to this bit clear bit 20 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 20 in PD_DAT register.
19	R/W1C	0x0	PORT19_DAT_CLR Writing 1 to this bit clear bit 19 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 19 in PD_DAT register.
18	R/W1C	0x0	PORT18_DAT_CLR Writing 1 to this bit clear bit 18 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 18 in PD_DAT register.
17	R/W1C	0x0	PORT17_DAT_CLR Writing 1 to this bit clear bit 17 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 17 in PD_DAT register.
16	R/W1C	0x0	PORT16_DAT_CLR Writing 1 to this bit clear bit 16 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 16 in PD_DAT register.
15	R/W1C	0x0	PORT15_DAT_CLR Writing 1 to this bit clear bit 15 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 15 in PD_DAT register.
14	R/W1C	0x0	PORT14_DAT_CLR Writing 1 to this bit clear bit 14 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 14 in PD_DAT register.
13	R/W1C	0x0	PORT13_DAT_CLR Writing 1 to this bit clear bit 13 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 13 in PD_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0218			Register Name: PD_DAT_CLR
Bit	Read/Write	Default/Hex	Description
12	R/W1C	0x0	PORT12_DAT_CLR Writing 1 to this bit clear bit 12 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 12 in PD_DAT register.
11	R/W1C	0x0	PORT11_DAT_CLR Writing 1 to this bit clear bit 11 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 11 in PD_DAT register.
10	R/W1C	0x0	PORT10_DAT_CLR Writing 1 to this bit clear bit 10 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 10 in PD_DAT register.
9	R/W1C	0x0	PORT9_DAT_CLR Writing 1 to this bit clear bit 9 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 9 in PD_DAT register.
8	R/W1C	0x0	PORT8_DAT_CLR Writing 1 to this bit clear bit 8 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 8 in PD_DAT register.
7	R/W1C	0x0	PORT7_DAT_CLR Writing 1 to this bit clear bit 7 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 7 in PD_DAT register.
6	R/W1C	0x0	PORT6_DAT_CLR Writing 1 to this bit clear bit 6 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 6 in PD_DAT register.
5	R/W1C	0x0	PORT5_DAT_CLR Writing 1 to this bit clear bit 5 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 5 in PD_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0218			Register Name: PD_DAT_CLR
Bit	Read/Write	Default/Hex	Description
4	R/W1C	0x0	PORT4_DAT_CLR Writing 1 to this bit clear bit 4 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 4 in PD_DAT register.
3	R/W1C	0x0	PORT3_DAT_CLR Writing 1 to this bit clear bit 3 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 3 in PD_DAT register.
2	R/W1C	0x0	PORT2_DAT_CLR Writing 1 to this bit clear bit 2 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 2 in PD_DAT register.
1	R/W1C	0x0	PORT1_DAT_CLR Writing 1 to this bit clear bit 1 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 1 in PD_DAT register.
0	R/W1C	0x0	PORT0_DAT_CLR Writing 1 to this bit clear bit 0 in the PD_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 0 in PD_DAT register.

18.14.6.42 0x0220 PD Multi-Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x0220			Register Name: PD_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PD7_DRV PD7 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PD6_DRV PD6 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0220			Register Name: PD_DRV0
Bit	Read/Write	Default/Hex	Description
21:20	R/W	0x1	PD5_DRV PD5 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PD4_DRV PD4 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PD3_DRV PD3 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PD2_DRV PD2 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PD1_DRV PD1 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PD0_DRV PD0 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

18.14.6.43 0x0224 PD Multi-Driving Register 1 (Default Value: 0x1111_1111)

Offset: 0x0224			Register Name: PD_DRV1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PD15_DRV PD15 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0224			Register Name: PD_DRV1
Bit	Read/Write	Default/Hex	Description
25:24	R/W	0x1	PD14_DRV PD14 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PD13_DRV PD13 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PD12_DRV PD12 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PD11_DRV PD11 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PD10_DRV PD10 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PD9_DRV PD9 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PD8_DRV PD8 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

18.14.6.44 0x0228 PD Multi-Driving Register 2 (Default Value: 0x1111_1111)

Offset: 0x0228			Register Name: PD_DRV2
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0228			Register Name: PD_DRV2
Bit	Read/Write	Default/Hex	Description
29:28	R/W	0x1	PD23_DRV PD23 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PD22_DRV PD22 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PD21_DRV PD21 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PD20_DRV PD20 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PD19_DRV PD19 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PD18_DRV PD18 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PD17_DRV PD17 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PD16_DRV PD16 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.14.6.45 0x0230 PD Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: PD_PUL0
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	PD15_PULL PD15 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
29:28	R/W	0x0	PD14_PULL PD14 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
27:26	R/W	0x0	PD13_PULL PD13 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PD12_PULL PD12 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PD11_PULL PD11 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PD10_PULL PD10 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PD9_PULL PD9 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PD8_PULL PD8 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PD7_PULL PD7 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PD6_PULL PD6 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0230			Register Name: PD_PUL0
Bit	Read/Write	Default/Hex	Description
11:10	R/W	0x0	PD5_PULL PD5 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PD4_PULL PD4 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PD3_PULL PD3 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PD2_PULL PD2 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PD1_PULL PD1 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PD0_PULL PD0 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

18.14.6.46 0x0234 PD Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: PD_PUL1
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:14	R/W	0x0	PD23_PULL PD23 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PD22_PULL PD22 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0234			Register Name: PD_PUL1
Bit	Read/Write	Default/Hex	Description
11:10	R/W	0x0	PD21_PULL PD21 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PD20_PULL PD20 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PD19_PULL PD19 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PD18_PULL PD18 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PD17_PULL PD17 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PD16_PULL PD16 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

18.14.6.47 0x0240 PD External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0240			Register Name: PD_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0240			Register Name: PD_INT_CFG0
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0x0	EINT6_CFG External INT6 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0240			Register Name: PD_INT_CFG0
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0x0	EINT1_CFG External INT1 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

18.14.6.48 0x0244 PD External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0244			Register Name: PD_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT15_CFG External INT15 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0244			Register Name: PD_INT_CFG1
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0x0	EINT13_CFG External INT13 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0244			Register Name: PD_INT_CFG1
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	EINT8_CFG External INT8 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

18.14.6.49 0x0248 PD External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0248			Register Name: PD_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT23_CFG External INT23 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT22_CFG External INT22 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT21_CFG External INT21 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0248			Register Name: PD_INT_CFG2
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0x0	EINT20_CFG External INT20 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT19_CFG External INT19 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT18_CFG External INT18 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT17_CFG External INT17 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT16_CFG External INT16 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.14.6.50 0x0250 PD External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0250			Register Name: PD_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	EINT23_CTL External INT23 Enable. 0: Disable 1: Enable
22	R/W	0x0	EINT22_CTL External INT22 Enable. 0: Disable 1: Enable
21	R/W	0x0	EINT21_CTL External INT21 Enable. 0: Disable 1: Enable
20	R/W	0x0	EINT20_CTL External INT20 Enable. 0: Disable 1: Enable
19	R/W	0x0	EINT19_CTL External INT19 Enable. 0: Disable 1: Enable
18	R/W	0x0	EINT18_CTL External INT18 Enable. 0: Disable 1: Enable
17	R/W	0x0	EINT17_CTL External INT17 Enable. 0: Disable 1: Enable
16	R/W	0x0	EINT16_CTL External INT16 Enable. 0: Disable 1: Enable
15	R/W	0x0	EINT15_CTL External INT15 Enable. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0250			Register Name: PD_INT_CTL
Bit	Read/Write	Default/Hex	Description
14	R/W	0x0	EINT14_CTL External INT14 Enable. 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable. 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable. 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable. 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable. 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable. 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable. 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable. 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable. 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0250			Register Name: PD_INT_CTL
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	EINT4_CTL External INT4 Enable. 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable. 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable. 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable. 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable. 0: Disable 1: Enable

18.14.6.51 0x0254 PD External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0254			Register Name: PD_INT_STA
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W1C	0x0	EINT23_STATUS External INT23 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
22	R/W1C	0x0	EINT22_STATUS External INT22 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
21	R/W1C	0x0	EINT21_STATUS External INT21 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0254			Register Name: PD_INT_STA
Bit	Read/Write	Default/Hex	Description
20	R/W1C	0x0	EINT20_STATUS External INT20 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
19	R/W1C	0x0	EINT19_STATUS External INT19 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
18	R/W1C	0x0	EINT18_STATUS External INT18 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
17	R/W1C	0x0	EINT17_STATUS External INT17 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
16	R/W1C	0x0	EINT16_STATUS External INT16 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
15	R/W1C	0x0	EINT15_STATUS External INT15 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W1C	0x0	EINT14_STATUS External INT14 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W1C	0x0	EINT13_STATUS External INT13 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0254			Register Name: PD_INT_STA
Bit	Read/Write	Default/Hex	Description
12	R/W1C	0x0	EINT12_STATUS External INT12 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W1C	0x0	EINT11_STATUS External INT11 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W1C	0x0	EINT10_STATUS External INT10 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W1C	0x0	EINT9_STATUS External INT9 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W1C	0x0	EINT8_STATUS External INT8 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W1C	0x0	EINT7_STATUS External INT7 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0254			Register Name: PD_INT_STA
Bit	Read/Write	Default/Hex	Description
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

18.14.6.52 0x0258 PD External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0258			Register Name: PD_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n. The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select. 0: RTC_32K 1: SYS_CLK24M

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.14.6.53 0x0270 PD SECURE Configure Register (Default Value: 0x0000_0000)

Offset: 0x0270			Register Name: PD_SECURE
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PORT31_SEC_SEL Port31 secure select. 0: Not secure 1: Secure
30	R/W	0x0	PORT30_SEC_SEL Port30 secure select. 0: Not secure 1: Secure
29	R/W	0x0	PORT29_SEC_SEL Port29 secure select. 0: Not secure 1: Secure
28	R/W	0x0	PORT28_SEC_SEL Port28 secure select. 0: Not secure 1: Secure
27	R/W	0x0	PORT27_SEC_SEL Port27 secure select. 0: Not secure 1: Secure
26	R/W	0x0	PORT26_SEC_SEL Port26 secure select. 0: Not secure 1: Secure
25	R/W	0x0	PORT25_SEC_SEL Port25 secure select. 0: Not secure 1: Secure
24	R/W	0x0	PORT24_SEC_SEL Port24 secure select. 0: Not secure 1: Secure
23	R/W	0x0	PORT23_SEC_SEL Port23 secure select. 0: Not secure 1: Secure
22	R/W	0x0	PORT22_SEC_SEL Port22 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0270			Register Name: PD_SECURE
Bit	Read/Write	Default/Hex	Description
21	R/W	0x0	PORT21_SEC_SEL Port21 secure select. 0: Not secure 1: Secure
20	R/W	0x0	PORT20_SEC_SEL Port20 secure select. 0: Not secure 1: Secure
19	R/W	0x0	PORT19_SEC_SEL Port19 secure select. 0: Not secure 1: Secure
18	R/W	0x0	PORT18_SEC_SEL Port18 secure select. 0: Not secure 1: Secure
17	R/W	0x0	PORT17_SEC_SEL Port17 secure select. 0: Not secure 1: Secure
16	R/W	0x0	PORT16_SEC_SEL Port16 secure select. 0: Not secure 1: Secure
15	R/W	0x0	PORT15_SEC_SEL Port15 secure select. 0: Not secure 1: Secure
14	R/W	0x0	PORT14_SEC_SEL Port14 secure select. 0: Not secure 1: Secure
13	R/W	0x0	PORT13_SEC_SEL Port13 secure select. 0: Not secure 1: Secure
12	R/W	0x0	PORT12_SEC_SEL Port12 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0270			Register Name: PD_SECURE
Bit	Read/Write	Default/Hex	Description
11	R/W	0x0	PORT11_SEC_SEL Port11 secure select. 0: Not secure 1: Secure
10	R/W	0x0	PORT10_SEC_SEL Port10 secure select. 0: Not secure 1: Secure
9	R/W	0x0	PORT9_SEC_SEL Port9 secure select. 0: Not secure 1: Secure
8	R/W	0x0	PORT8_SEC_SEL Port8 secure select. 0: Not secure 1: Secure
7	R/W	0x0	PORT7_SEC_SEL Port7 secure select. 0: Not secure 1: Secure
6	R/W	0x0	PORT6_SEC_SEL Port6 secure select. 0: Not secure 1: Secure
5	R/W	0x0	PORT5_SEC_SEL Port5 secure select. 0: Not secure 1: Secure
4	R/W	0x0	PORT4_SEC_SEL Port4 secure select. 0: Not secure 1: Secure
3	R/W	0x0	PORT3_SEC_SEL Port3 secure select. 0: Not secure 1: Secure
2	R/W	0x0	PORT2_SEC_SEL Port2 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0270			Register Name: PD_SECURE
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	PORT1_SEC_SEL Port1 secure select. 0: Not secure 1: Secure
0	R/W	0x0	PORT0_SEC_SEL Port0 secure select. 0: Not secure 1: Secure

18.14.6.54 0x0280 PE Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0280			Register Name: PE_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PE7_SELECT PE7 Select. 0000: Input 0001: Output 0010: CLK-FANOUT2 0011: HDMI-SCL 0100: I2S3-BCLK<MUX-HDMI-EDP> 0101: Reserved 0110: Reserved 0111: NCSI0-D3 1000: TWI11-SCK 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT7 1111: IO Disable
27:24	R/W	0xF	PE6_SELECT PE6 Select. 0000: Input 0001: Output 0010: CLK-FANOUT1 0011: HDMI-CEC 0100: I2S3-DIN0<MUX-HDMI-EDP> 0101: I2S3-DOUT1<MUX-HDMI-EDP> 0110: Reserved 0111: NCSI0-D2 1000: UART6-DTR 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT6 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0280			Register Name: PE_CFG0
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0xF	PE5_SELECT PE5 Select. 0000: Input 0001: Output 0010: MCSI1-MCLK 0011: Reserved 0100: Reserved 0101: PWM0-2 0110: Reserved 0111: NCSI0-MCLK 1000: UART6-DSR 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT5 1111: IO Disable
19:16	R/W	0xF	PE4_SELECT PE4 Select. 0000: Input 0001: Output 0010: TWI3-SDA 0011: LEDC 0100: PWM0-1 0101: SPI3-CS1 0110: Reserved 0111: NCSI0-D0 1000: UART6-DCD 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT4 1111: IO Disable
15:12	R/W	0xF	PE3_SELECT PE3 Select. 0000: Input 0001: Output 0010: TWI3-SCK 0011: CSI1-XVS-FSYNC 0100: PWM0-0 0101: SPI3-MISO 0110: Reserved 0111: NCSI0-D1 1000: UART6-CTS 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT3 1111: IO Disable
11:8	R/W	0xF	PE2_SELECT PE2 Select. 0000: Input 0001: Output 0010: TWI2-SDA 0011: CSI0-XVS-FSYNC 0100: Reserved 0101: SPI3-MOSI 0110: Reserved 0111: NCSI0-PCLK 1000: UART6-RTS 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT2 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0280			Register Name: PE_CFG0
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0xF	PE1_SELECT PE1 Select. 0000: Input 0001: Output 0010: TWI2-SCK 0011: CSI1-XHS 0100: Reserved 0101: SPI3-CLK 0110: Reserved 0111: NCSI0-VSYNC 1000: UART6-RX 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT1 1111: IO Disable
3:0	R/W	0xF	PE0_SELECT PE0 Select. 0000: Input 0001: Output 0010: MCSI0-MCLK 0011: CSI0-XHS 0100: Reserved 0101: SPI3-CS0 0110: Reserved 0111: NCSI0-HSYNC 1000: UART6-TX 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT0 1111: IO Disable

18.14.6.55 0x0284 PE Configure Register 1 (Default Value: 0xFFFF_FFFF)

Offset: 0x0284			Register Name: PE_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PE15_SELECT PE15 Select. 0000: Input 0001: Output 0010: Reserved 0011: SPI3-CS1 0100: Reserved 0101: PWM1-9 0110: IR-RX 0111: Reserved 1000: TWI9-SDA 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT15 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0284			Register Name: PE_CFG1
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0xF	PE14_SELECT PE14 Select. 0000: Input 0001: Output 0010: Reserved 0011: SPI3-MOSI 0100: Reserved 0101: PWM1-8 0110: PCIE-CLKREQN 0111: IR-RX 1000: TWI9-SCK 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT14 1111: IO Disable
23:20	R/W	0xF	PE13_SELECT PE13 Select. 0000: Input 0001: Output 0010: Reserved 0011: SPI3-CLK 0100: Reserved 0101: Reserved 0110: PCIE-PERSTN 0111: Reserved 1000: UART1-RX 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT13 1111: IO Disable
19:16	R/W	0xF	PE12_SELECT PE12 Select. 0000: Input 0001: Output 0010: Reserved 0011: SPI3-CS0 0100: I2S3-DOUT0<MUX-HDMI-EDP> 0101: I2S3-DIN1<MUX-HDMI-EDP> 0110: PCIE-WAKEN 0111: Reserved 1000: UART1-TX 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT12 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0284			Register Name: PE_CFG1
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0xF	PE11_SELECT PE11 Select. 0000: Input 0001: Output 0010: TWI4-SDA 0011: SPI3-MISO 0100: I2S3-DIN2<MUX-HDMI-EDP> 0101: I2S3-DOUT2<MUX-HDMI-EDP> 0110: PCIE-CLKREQN 0111: NCSI0-D7 1000: UART1-CTS 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT11 1111: IO Disable
11:8	R/W	0xF	PE10_SELECT PE10 Select. 0000: Input 0001: Output 0010: TWI4-SCK 0011: TCON-FSYNC1 0100: I2S3-DIN3<MUX-HDMI-EDP> 0101: I2S3-DOUT3<MUX-HDMI-EDP> 0110: Reserved 0111: NCSI0-D6 1000: UART1-RTS 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT10 1111: IO Disable
7:4	R/W	0xF	PE9_SELECT PE9 Select. 0000: Input 0001: Output 0010: MCSI2-MCLK 0011: TCON-FSYNC0 0100: I2S3-MCLK 0101: Reserved 0110: Reserved 0111: NCSI0-D5 1000: UART6-RI 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT9 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0284			Register Name: PE_CFG1
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xF	PE8_SELECT PE8 Select. 0000: Input 0001: Output 0010: CLK-FANOUT3 0011: HDMI-SDA 0100: I2S3-LRCK<MUX-HDMI-EDP> 0101: Reserved 0110: Reserved 0111: NCSI0-D4 1000: TWI11-SDA 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT8 1111: IO Disable

18.14.6.56 0x0290 PE Data Register (Default Value: 0x0000_0000)

Offset: 0x0290			Register Name: PE_DAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0	PE_DAT PE Data. If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

18.14.6.57 0x0294 PE Data Set Register (Default Value: 0x0000_0000)

Offset: 0x0294			Register Name: PE_DAT_SET
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W1S	0x0	PORT15_DAT_SET Writing 1 to this bit can set bit 15 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 15 in PE_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0294			Register Name: PE_DAT_SET
Bit	Read/Write	Default/Hex	Description
14	R/W1S	0x0	PORT14_DAT_SET Writing 1 to this bit can set bit 14 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 14 in PE_DAT register.
13	R/W1S	0x0	PORT13_DAT_SET Writing 1 to this bit can set bit 13 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 13 in PE_DAT register.
12	R/W1S	0x0	PORT12_DAT_SET Writing 1 to this bit can set bit 12 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 12 in PE_DAT register.
11	R/W1S	0x0	PORT11_DAT_SET Writing 1 to this bit can set bit 11 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 11 in PE_DAT register.
10	R/W1S	0x0	PORT10_DAT_SET Writing 1 to this bit can set bit 10 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 10 in PE_DAT register.
9	R/W1S	0x0	PORT9_DAT_SET Writing 1 to this bit can set bit 9 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 9 in PE_DAT register.
8	R/W1S	0x0	PORT8_DAT_SET Writing 1 to this bit can set bit 8 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 8 in PE_DAT register.
7	R/W1S	0x0	PORT7_DAT_SET Writing 1 to this bit can set bit 7 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 7 in PE_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0294			Register Name: PE_DAT_SET
Bit	Read/Write	Default/Hex	Description
6	R/W1S	0x0	PORT6_DAT_SET Writing 1 to this bit can set bit 6 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 6 in PE_DAT register.
5	R/W1S	0x0	PORT5_DAT_SET Writing 1 to this bit can set bit 5 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 5 in PE_DAT register.
4	R/W1S	0x0	PORT4_DAT_SET Writing 1 to this bit can set bit 4 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 4 in PE_DAT register.
3	R/W1S	0x0	PORT3_DAT_SET Writing 1 to this bit can set bit 3 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 3 in PE_DAT register.
2	R/W1S	0x0	PORT2_DAT_SET Writing 1 to this bit can set bit 2 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 2 in PE_DAT register.
1	R/W1S	0x0	PORT1_DAT_SET Writing 1 to this bit can set bit 1 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 1 in PE_DAT register.
0	R/W1S	0x0	PORT0_DAT_SET Writing 1 to this bit can set bit 0 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 0 in PE_DAT register.

18.14.6.58 0x0298 PE Data Clear Register (Default Value: 0x0000_0000)

Offset: 0x0298			Register Name: PE_DAT_CLR
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0298			Register Name: PE_DAT_CLR
Bit	Read/Write	Default/Hex	Description
15	R/W1C	0x0	PORT15_DAT_CLR Writing 1 to this bit clear bit 15 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 15 in PE_DAT register.
14	R/W1C	0x0	PORT14_DAT_CLR Writing 1 to this bit clear bit 14 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 14 in PE_DAT register.
13	R/W1C	0x0	PORT13_DAT_CLR Writing 1 to this bit clear bit 13 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 13 in PE_DAT register.
12	R/W1C	0x0	PORT12_DAT_CLR Writing 1 to this bit clear bit 12 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 12 in PE_DAT register.
11	R/W1C	0x0	PORT11_DAT_CLR Writing 1 to this bit clear bit 11 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 11 in PE_DAT register.
10	R/W1C	0x0	PORT10_DAT_CLR Writing 1 to this bit clear bit 10 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 10 in PE_DAT register.
9	R/W1C	0x0	PORT9_DAT_CLR Writing 1 to this bit clear bit 9 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 9 in PE_DAT register.
8	R/W1C	0x0	PORT8_DAT_CLR Writing 1 to this bit clear bit 8 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 8 in PE_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0298			Register Name: PE_DAT_CLR
Bit	Read/Write	Default/Hex	Description
7	R/W1C	0x0	PORT7_DAT_CLR Writing 1 to this bit clear bit 7 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 7 in PE_DAT register.
6	R/W1C	0x0	PORT6_DAT_CLR Writing 1 to this bit clear bit 6 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 6 in PE_DAT register.
5	R/W1C	0x0	PORT5_DAT_CLR Writing 1 to this bit clear bit 5 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 5 in PE_DAT register.
4	R/W1C	0x0	PORT4_DAT_CLR Writing 1 to this bit clear bit 4 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 4 in PE_DAT register.
3	R/W1C	0x0	PORT3_DAT_CLR Writing 1 to this bit clear bit 3 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 3 in PE_DAT register.
2	R/W1C	0x0	PORT2_DAT_CLR Writing 1 to this bit clear bit 2 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 2 in PE_DAT register.
1	R/W1C	0x0	PORT1_DAT_CLR Writing 1 to this bit clear bit 1 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 1 in PE_DAT register.
0	R/W1C	0x0	PORT0_DAT_CLR Writing 1 to this bit clear bit 0 in the PE_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 0 in PE_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.14.6.59 0x02A0 PE Multi-Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x02A0			Register Name: PE_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PE7_DRV PE7 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PE6_DRV PE6 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PE5_DRV PE5 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PE4_DRV PE4 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PE3_DRV PE3 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PE2_DRV PE2 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PE1_DRV PE1 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PE0_DRV PE0 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.14.6.60 0x02A4 PE Multi-Driving Register 1 (Default Value: 0x1111_1111)

Offset: 0x02A4			Register Name: PE_DRV1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PE15_DRV PE15 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PE14_DRV PE14 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PE13_DRV PE13 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PE12_DRV PE12 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PE11_DRV PE11 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PE10_DRV PE10 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PE9_DRV PE9 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PE8_DRV PE8 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.14.6.61 0x02B0 PE Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x02B0			Register Name: PE_PUL0
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	PE15_PULL PE15 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
29:28	R/W	0x0	PE14_PULL PE14 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
27:26	R/W	0x0	PE13_PULL PE13 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PE12_PULL PE12 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PE11_PULL PE11 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PE10_PULL PE10 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PE9_PULL PE9 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PE8_PULL PE8 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PE7_PULL PE7 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PE6_PULL PE6 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x02B0			Register Name: PE_PUL0
Bit	Read/Write	Default/Hex	Description
11:10	R/W	0x0	PE5_PULL PE5 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PE4_PULL PE4 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PE3_PULL PE3 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PE2_PULL PE2 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PE1_PULL PE1 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PE0_PULL PE0 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

18.14.6.62 0x02C0 PE External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x02C0			Register Name: PE_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x02C0			Register Name: PE_INT_CFG0
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0x0	EINT6_CFG External INT6 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x02C0			Register Name: PE_INT_CFG0
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0x0	EINT1_CFG External INT1 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

18.14.6.63 0x02C4 PE External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x02C4			Register Name: PE_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT15_CFG External INT15 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x02C4			Register Name: PE_INT_CFG1
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0x0	EINT13_CFG External INT13 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x02C4			Register Name: PE_INT_CFG1
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	EINT8_CFG External INT8 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

18.14.6.64 00x02D0 PE External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02D0			Register Name: PE_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x0	EINT15_CTL External INT15 Enable. 0: Disable 1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable. 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable. 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable. 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable. 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x02D0			Register Name: PE_INT_CTL
Bit	Read/Write	Default/Hex	Description
9	R/W	0x0	EINT9_CTL External INT9 Enable. 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable. 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable. 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable. 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable. 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable. 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable. 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable. 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable. 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.14.6.65 0x02D4 PE External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02D4			Register Name: PE_INT_STA
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W1C	0x0	EINT15_STATUS External INT15 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W1C	0x0	EINT14_STATUS External INT14 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W1C	0x0	EINT13_STATUS External INT13 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W1C	0x0	EINT12_STATUS External INT12 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W1C	0x0	EINT11_STATUS External INT11 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W1C	0x0	EINT10_STATUS External INT10 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W1C	0x0	EINT9_STATUS External INT9 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x02D4			Register Name: PE_INT_STA
Bit	Read/Write	Default/Hex	Description
8	R/W1C	0x0	EINT8_STATUS External INT8 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W1C	0x0	EINT7_STATUS External INT7 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x02D4			Register Name: PE_INT_STA
Bit	Read/Write	Default/Hex	Description
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

18.14.6.66 0x02D8 PE External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x02D8			Register Name: PE_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n. The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select. 0: RTC_32K 1: SYS_CLK24M

18.14.6.67 0x02F0 PE SECURE Configure Register (Default Value: 0x0000_0000)

Offset: 0x02F0			Register Name: PE_SECURE
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PORT31_SEC_SEL Port31 secure select. 0: Not secure 1: Secure
30	R/W	0x0	PORT30_SEC_SEL Port30 secure select. 0: Not secure 1: Secure
29	R/W	0x0	PORT29_SEC_SEL Port29 secure select. 0: Not secure 1: Secure
28	R/W	0x0	PORT28_SEC_SEL Port28 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x02F0			Register Name: PE_SECURE
Bit	Read/Write	Default/Hex	Description
27	R/W	0x0	PORT27_SEC_SEL Port27 secure select. 0: Not secure 1: Secure
26	R/W	0x0	PORT26_SEC_SEL Port26 secure select. 0: Not secure 1: Secure
25	R/W	0x0	PORT25_SEC_SEL Port25 secure select. 0: Not secure 1: Secure
24	R/W	0x0	PORT24_SEC_SEL Port24 secure select. 0: Not secure 1: Secure
23	R/W	0x0	PORT23_SEC_SEL Port23 secure select. 0: Not secure 1: Secure
22	R/W	0x0	PORT22_SEC_SEL Port22 secure select. 0: Not secure 1: Secure
21	R/W	0x0	PORT21_SEC_SEL Port21 secure select. 0: Not secure 1: Secure
20	R/W	0x0	PORT20_SEC_SEL Port20 secure select. 0: Not secure 1: Secure
19	R/W	0x0	PORT19_SEC_SEL Port19 secure select. 0: Not secure 1: Secure
18	R/W	0x0	PORT18_SEC_SEL Port18 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x02F0			Register Name: PE_SECURE
Bit	Read/Write	Default/Hex	Description
17	R/W	0x0	PORT17_SEC_SEL Port17 secure select. 0: Not secure 1: Secure
16	R/W	0x0	PORT16_SEC_SEL Port16 secure select. 0: Not secure 1: Secure
15	R/W	0x0	PORT15_SEC_SEL Port15 secure select. 0: Not secure 1: Secure
14	R/W	0x0	PORT14_SEC_SEL Port14 secure select. 0: Not secure 1: Secure
13	R/W	0x0	PORT13_SEC_SEL Port13 secure select. 0: Not secure 1: Secure
12	R/W	0x0	PORT12_SEC_SEL Port12 secure select. 0: Not secure 1: Secure
11	R/W	0x0	PORT11_SEC_SEL Port11 secure select. 0: Not secure 1: Secure
10	R/W	0x0	PORT10_SEC_SEL Port10 secure select. 0: Not secure 1: Secure
9	R/W	0x0	PORT9_SEC_SEL Port9 secure select. 0: Not secure 1: Secure
8	R/W	0x0	PORT8_SEC_SEL Port8 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x02F0			Register Name: PE_SECURE
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	PORT7_SEC_SEL Port7 secure select. 0: Not secure 1: Secure
6	R/W	0x0	PORT6_SEC_SEL Port6 secure select. 0: Not secure 1: Secure
5	R/W	0x0	PORT5_SEC_SEL Port5 secure select. 0: Not secure 1: Secure
4	R/W	0x0	PORT4_SEC_SEL Port4 secure select. 0: Not secure 1: Secure
3	R/W	0x0	PORT3_SEC_SEL Port3 secure select. 0: Not secure 1: Secure
2	R/W	0x0	PORT2_SEC_SEL Port2 secure select. 0: Not secure 1: Secure
1	R/W	0x0	PORT1_SEC_SEL Port1 secure select. 0: Not secure 1: Secure
0	R/W	0x0	PORT0_SEC_SEL Port0 secure select. 0: Not secure 1: Secure

18.14.6.68 0x0300 PF Configure Register 0 (Default Value: 0x0FFF_FFFF)

Offset: 0x0300			Register Name: PF_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0300			Register Name: PF_CFG0
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0xF	PF6-SELECT PF6 Select. 0000: Input 0001: Output 0010: Reserved 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PF-EINT6 1111: IO Disable
23:20	R/W	0xF	PF5-SELECT PF5 Select. 0000: Input 0001: Output 0010: SDC0-D2 0011: JTAG-CK 0100: Reserved 0101: UART5-TX 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PF-EINT5 1111: IO Disable
19:16	R/W	0xF	PF4-SELECT PF4 Select. 0000: Input 0001: Output 0010: SDC0-D3 0011: UART0-RX 0100: Reserved 0101: UART5-RX 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PF-EINT4 1111: IO Disable
15:12	R/W	0xF	PF3-SELECT PF3 Select. 0000: Input 0001: Output 0010: SDC0-D0 0011: JTAG-DI 0100: Reserved 0101: UART5-CTS 0110: TWI2-SDA 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PF-EINT3 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0300			Register Name: PF_CFG0
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0xF	PF2-SELECT PF2 Select. 0000: Input 0001: Output 0010: SDC0-CLK 0011: UART0-TX 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PF-EINT2 1111: IO Disable
7:4	R/W	0xF	PF1-SELECT PF1 Select. 0000: Input 0001: Output 0010: SDC0-CMD 0011: JTAG-DO 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PF-EINT1 1111: IO Disable
3:0	R/W	0xF	PF0-SELECT PF0 Select. 0000: Input 0001: Output 0010: SDC0-D1 0011: JTAG-MS 0100: Reserved 0101: UART5-RTS 0110: TWI2-SCK 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PF-EINT0 1111: IO Disable

18.14.6.69 0x0310 PF Data Register (Default Value: 0x0000_0000)

Offset: 0x0310			Register Name: PF_DAT
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0310			Register Name: PF_DAT
Bit	Read/Write	Default/Hex	Description
6:0	R/W	0	PF_DAT PF Data. If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

18.14.6.70 0x0314 PF Data Set Register (Default Value: 0x0000_0000)

Offset: 0x0314			Register Name: PF_DAT_SET
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W1S	0x0	PORT6_DAT_SET Writing 1 to this bit can set bit 6 in the PF_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 6 in PF_DAT register.
5	R/W1S	0x0	PORT5_DAT_SET Writing 1 to this bit can set bit 5 in the PF_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 5 in PF_DAT register.
4	R/W1S	0x0	PORT4_DAT_SET Writing 1 to this bit can set bit 4 in the PF_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 4 in PF_DAT register.
3	R/W1S	0x0	PORT3_DAT_SET Writing 1 to this bit can set bit 3 in the PF_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 3 in PF_DAT register.
2	R/W1S	0x0	PORT2_DAT_SET Writing 1 to this bit can set bit 2 in the PF_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 2 in PF_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0314			Register Name: PF_DAT_SET
Bit	Read/Write	Default/Hex	Description
1	R/W1S	0x0	PORT1_DAT_SET Writing 1 to this bit can set bit 1 in the PF_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 1 in PF_DAT register.
0	R/W1S	0x0	PORT0_DAT_SET Writing 1 to this bit can set bit 0 in the PF_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 0 in PF_DAT register.

18.14.6.71 0x0318 PF Data Clear Register (Default Value: 0x0000_0000)

Offset: 0x0318			Register Name: PF_DAT_CLR
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W1C	0x0	PORT6_DAT_CLR Writing 1 to this bit clear bit 6 in the PF_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 6 in PF_DAT register.
5	R/W1C	0x0	PORT5_DAT_CLR Writing 1 to this bit clear bit 5 in the PF_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 5 in PF_DAT register.
4	R/W1C	0x0	PORT4_DAT_CLR Writing 1 to this bit clear bit 4 in the PF_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 4 in PF_DAT register.
3	R/W1C	0x0	PORT3_DAT_CLR Writing 1 to this bit clear bit 3 in the PF_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 3 in PF_DAT register.
2	R/W1C	0x0	PORT2_DAT_CLR Writing 1 to this bit clear bit 2 in the PF_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 2 in PF_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0318			Register Name: PF_DAT_CLR
Bit	Read/Write	Default/Hex	Description
1	R/W1C	0x0	PORT1_DAT_CLR Writing 1 to this bit clear bit 1 in the PF_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 1 in PF_DAT register.
0	R/W1C	0x0	PORT0_DAT_CLR Writing 1 to this bit clear bit 0 in the PF_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 0 in PF_DAT register.

18.14.6.72 0x0320 PF Multi-Driving Register 0 (Default Value: 0x0111_1111)

Offset: 0x0320			Register Name: PF_DRV0
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x1	PF6_DRV PF6 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PF5_DRV PF5 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PF4_DRV PF4 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PF3_DRV PF3 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PF2_DRV PF2 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0320			Register Name: PF_DRV0
Bit	Read/Write	Default/Hex	Description
5:4	R/W	0x1	PF1_DRV PF1 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PF0_DRV PF0 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

18.14.6.73 0x0330 PF Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0330			Register Name: PF_PUL0
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:12	R/W	0x0	PF6_PULL PF6 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PF5_PULL PF5 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PF4_PULL PF4 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PF3_PULL PF3 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PF2_PULL PF2 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PF1_PULL PF1 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0330			Register Name: PF_PUL0
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x0	PF0_PULL PF0 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

18.14.6.74 0x0340 PF External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: PF_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0x0	EINT6_CFG External INT6 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0340			Register Name: PF_INT_CFG0
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT3_CFG External INT3 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

18.14.6.75 0x0350 PF External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0350			Register Name: PF_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0350			Register Name: PF_INT_CTL
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	EINT6_CTL External INT6 Enable. 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable. 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable. 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable. 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable. 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable. 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable. 0: Disable 1: Enable

18.14.6.76 0x0354 PF External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0354			Register Name: PF_INT_STA
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0354			Register Name: PF_INT_STA
Bit	Read/Write	Default/Hex	Description
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

18.14.6.77 0x0358 PF External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0358			Register Name: PF_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n. The selected clock source is prescaled by 2^n
3:1	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0358			Register Name: PF_INT_DEB
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select. 0: RTC_32K 1: SYS_CLK24M

18.14.6.78 0x0370 PF SECURE Configure Register (Default Value: 0x0000_0000)

Offset: 0x0370			Register Name: PF_SECURE
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PORT31_SEC_SEL Port31 secure select. 0: Not secure 1: Secure
30	R/W	0x0	PORT30_SEC_SEL Port30 secure select. 0: Not secure 1: Secure
29	R/W	0x0	PORT29_SEC_SEL Port29 secure select. 0: Not secure 1: Secure
28	R/W	0x0	PORT28_SEC_SEL Port28 secure select. 0: Not secure 1: Secure
27	R/W	0x0	PORT27_SEC_SEL Port27 secure select. 0: Not secure 1: Secure
26	R/W	0x0	PORT26_SEC_SEL Port26 secure select. 0: Not secure 1: Secure
25	R/W	0x0	PORT25_SEC_SEL Port25 secure select. 0: Not secure 1: Secure
24	R/W	0x0	PORT24_SEC_SEL Port24 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0370			Register Name: PF_SECURE
Bit	Read/Write	Default/Hex	Description
23	R/W	0x0	PORT23_SEC_SEL Port23 secure select. 0: Not secure 1: Secure
22	R/W	0x0	PORT22_SEC_SEL Port22 secure select. 0: Not secure 1: Secure
21	R/W	0x0	PORT21_SEC_SEL Port21 secure select. 0: Not secure 1: Secure
20	R/W	0x0	PORT20_SEC_SEL Port20 secure select. 0: Not secure 1: Secure
19	R/W	0x0	PORT19_SEC_SEL Port19 secure select. 0: Not secure 1: Secure
18	R/W	0x0	PORT18_SEC_SEL Port18 secure select. 0: Not secure 1: Secure
17	R/W	0x0	PORT17_SEC_SEL Port17 secure select. 0: Not secure 1: Secure
16	R/W	0x0	PORT16_SEC_SEL Port16 secure select. 0: Not secure 1: Secure
15	R/W	0x0	PORT15_SEC_SEL Port15 secure select. 0: Not secure 1: Secure
14	R/W	0x0	PORT14_SEC_SEL Port14 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0370			Register Name: PF_SECURE
Bit	Read/Write	Default/Hex	Description
13	R/W	0x0	PORT13_SEC_SEL Port13 secure select. 0: Not secure 1: Secure
12	R/W	0x0	PORT12_SEC_SEL Port12 secure select. 0: Not secure 1: Secure
11	R/W	0x0	PORT11_SEC_SEL Port11 secure select. 0: Not secure 1: Secure
10	R/W	0x0	PORT10_SEC_SEL Port10 secure select. 0: Not secure 1: Secure
9	R/W	0x0	PORT9_SEC_SEL Port9 secure select. 0: Not secure 1: Secure
8	R/W	0x0	PORT8_SEC_SEL Port8 secure select. 0: Not secure 1: Secure
7	R/W	0x0	PORT7_SEC_SEL Port7 secure select. 0: Not secure 1: Secure
6	R/W	0x0	PORT6_SEC_SEL Port6 secure select. 0: Not secure 1: Secure
5	R/W	0x0	PORT5_SEC_SEL Port5 secure select. 0: Not secure 1: Secure
4	R/W	0x0	PORT4_SEC_SEL Port4 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0370			Register Name: PF_SECURE
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	PORT3_SEC_SEL Port3 secure select. 0: Not secure 1: Secure
2	R/W	0x0	PORT2_SEC_SEL Port2 secure select. 0: Not secure 1: Secure
1	R/W	0x0	PORT1_SEC_SEL Port1 secure select. 0: Not secure 1: Secure
0	R/W	0x0	PORT0_SEC_SEL Port0 secure select. 0: Not secure 1: Secure

18.14.6.79 0x0380 PG Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0380			Register Name: PG_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PG7_SELECT PG7 Select. 0000: Input 0001: Output 0010: UART1-RX 0011: UART4-RX 0100: PWM1-8 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT7 1111: IO Disable
27:24	R/W	0xF	PG6_SELECT PG6 Select. 0000: Input 0001: Output 0010: UART1-TX 0011: UART4-TX 0100: PWM1-7 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT6 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0380			Register Name: PG_CFG0
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0xF	PG5_SELECT PG5 Select. 0000: Input 0001: Output 0010: SDC1-D3 0011: LCD0-D17 0100: PWM1-6 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT5 1111: IO Disable
19:16	R/W	0xF	PG4_SELECT PG4 Select. 0000: Input 0001: Output 0010: SDC1-D2 0011: LCD0-D16 0100: PWM1-5 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT4 1111: IO Disable
15:12	R/W	0xF	PG3_SELECT PG3 Select. 0000: Input 0001: Output 0010: SDC1-D1 0011: LCD0-D9 0100: PWM1-4 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT3 1111: IO Disable
11:8	R/W	0xF	PG2_SELECT PG2 Select. 0000: Input 0001: Output 0010: SDC1-D0 0011: LCD0-D8 0100: PWM1-3 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT2 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0380			Register Name: PG_CFG0
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0xF	PG1_SELECT PG1 Select. 0000: Input 0001: Output 0010: SDC1-CMD 0011: LCD0-D1 0100: PWM1-2 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT1 1111: IO Disable
3:0	R/W	0xF	PG0_SELECT PG0 Select. 0000: Input 0001: Output 0010: SDC1-CLK 0011: LCD0-D0 0100: PWM1-1 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT0 1111: IO Disable

18.14.6.80 0x0384 PG Configure Register 1 (Default Value: 0x0FFF_FFFF)

Offset: 0x0384			Register Name: PG_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0xF	PG14_SELECT PG14 Select. 0000: Input 0001: Output 0010: I2S1-DIN0 0011: I2S1-DOUT1 0100: TWI6-SDA 0101: Reserved 0110: DMIC-DATA0 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT14 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0384			Register Name: PG_CFG1
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0xF	PG13_SELECT PG13 Select. 0000: Input 0001: Output 0010: I2S1-DOUT0 0011: I2S1-DIN1 0100: TWI6-SCK 0101: Reserved 0110: DMIC-DATA1 0111: HDMI-SDA 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT13 1111: IO Disable
19:16	R/W	0xF	PG12_SELECT PG12 Select. 0000: Input 0001: Output 0010: I2S1-LRCK 0011: TWI12-SDA 0100: TWI9-SDA 0101: Reserved 0110: DMIC-DATA2 0111: HDMI-SCL 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT12 1111: IO Disable
15:12	R/W	0xF	PG11_SELECT PG11 Select. 0000: Input 0001: Output 0010: I2S1-BCLK 0011: TWI12-SCK 0100: TWI9-SCK 0101: Reserved 0110: DMIC-DATA3 0111: HDMI-CEC 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT11 1111: IO Disable
11:8	R/W	0xF	PG10_SELECT PG10 Select. 0000: Input 0001: Output 0010: I2S1-MCLK 0011: CLK-FANOUT0 0100: PWM1-9 0101: Reserved 0110: DMIC-CLK 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT10 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0384			Register Name: PG_CFG1
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0xF	PG9_SELECT PG9 Select. 0000: Input 0001: Output 0010: UART1-CTS 0011: UART4-CTS 0100: UART5-RX 0101: Reserved 0110: TWI0-SDA 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT9 1111: IO Disable
3:0	R/W	0xF	PG8_SELECT PG8 Select. 0000: Input 0001: Output 0010: UART1-RTS 0011: UART4-RTS 0100: UART5-TX 0101: Reserved 0110: TWI0-SCK 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT8 1111: IO Disable

18.14.6.81 0x0390 PG Data Register (Default Value: 0x0000_0000)

Offset: 0x0390			Register Name: PG_DAT
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14:0	R/W	0	PG_DAT PG Data. If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

18.14.6.82 0x0394 PG Data Set Register (Default Value: 0x0000_0000)

Offset: 0x0394			Register Name: PG_DAT_SET
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0394			Register Name: PG_DAT_SET
Bit	Read/Write	Default/Hex	Description
14	R/W1S	0x0	PORT14_DAT_SET Writing 1 to this bit can set bit 14 in the PG_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 14 in PG_DAT register.
13	R/W1S	0x0	PORT13_DAT_SET Writing 1 to this bit can set bit 13 in the PG_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 13 in PG_DAT register.
12	R/W1S	0x0	PORT12_DAT_SET Writing 1 to this bit can set bit 12 in the PG_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 12 in PG_DAT register.
11	R/W1S	0x0	PORT11_DAT_SET Writing 1 to this bit can set bit 11 in the PG_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 11 in PG_DAT register.
10	R/W1S	0x0	PORT10_DAT_SET Writing 1 to this bit can set bit 10 in the PG_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 10 in PG_DAT register.
9	R/W1S	0x0	PORT9_DAT_SET Writing 1 to this bit can set bit 9 in the PG_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 9 in PG_DAT register.
8	R/W1S	0x0	PORT8_DAT_SET Writing 1 to this bit can set bit 8 in the PG_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 8 in PG_DAT register.
7	R/W1S	0x0	PORT7_DAT_SET Writing 1 to this bit can set bit 7 in the PG_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 7 in PG_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0394			Register Name: PG_DAT_SET
Bit	Read/Write	Default/Hex	Description
6	R/W1S	0x0	PORT6_DAT_SET Writing 1 to this bit can set bit 6 in the PG_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 6 in PG_DAT register.
5	R/W1S	0x0	PORT5_DAT_SET Writing 1 to this bit can set bit 5 in the PG_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 5 in PG_DAT register.
4	R/W1S	0x0	PORT4_DAT_SET Writing 1 to this bit can set bit 4 in the PG_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 4 in PG_DAT register.
3	R/W1S	0x0	PORT3_DAT_SET Writing 1 to this bit can set bit 3 in the PG_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 3 in PG_DAT register.
2	R/W1S	0x0	PORT2_DAT_SET Writing 1 to this bit can set bit 2 in the PG_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 2 in PG_DAT register.
1	R/W1S	0x0	PORT1_DAT_SET Writing 1 to this bit can set bit 1 in the PG_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 1 in PG_DAT register.
0	R/W1S	0x0	PORT0_DAT_SET Writing 1 to this bit can set bit 0 in the PG_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 0 in PG_DAT register.

18.14.6.83 0x0398 PG Data Clear Register (Default Value: 0x0000_0000)

Offset: 0x0398			Register Name: PG_DAT_CLR
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0398			Register Name: PG_DAT_CLR
Bit	Read/Write	Default/Hex	Description
14	R/W1C	0x0	PORT14_DAT_CLR Writing 1 to this bit clear corresponding bit in the PG_DAT register; write 0 have no effect. A read of this bit returns the value of corresponding bit in PG_DAT register
13	R/W1C	0x0	PORT13_DAT_CLR Writing 1 to this bit clear corresponding bit in the PG_DAT register; write 0 have no effect. A read of this bit returns the value of corresponding bit in PG_DAT register
12	R/W1C	0x0	PORT12_DAT_CLR Writing 1 to this bit clear corresponding bit in the PG_DAT register; write 0 have no effect. A read of this bit returns the value of corresponding bit in PG_DAT register
11	R/W1C	0x0	PORT11_DAT_CLR Writing 1 to this bit clear corresponding bit in the PG_DAT register; write 0 have no effect. A read of this bit returns the value of corresponding bit in PG_DAT register
10	R/W1C	0x0	PORT10_DAT_CLR Writing 1 to this bit clear corresponding bit in the PG_DAT register; write 0 have no effect. A read of this bit returns the value of corresponding bit in PG_DAT register
9	R/W1C	0x0	PORT9_DAT_CLR Writing 1 to this bit clear corresponding bit in the PG_DAT register; write 0 have no effect. A read of this bit returns the value of corresponding bit in PG_DAT register
8	R/W1C	0x0	PORT8_DAT_CLR Writing 1 to this bit clear corresponding bit in the PG_DAT register; write 0 have no effect. A read of this bit returns the value of corresponding bit in PG_DAT register
7	R/W1C	0x0	PORT7_DAT_CLR Writing 1 to this bit clear corresponding bit in the PG_DAT register; write 0 have no effect. A read of this bit returns the value of corresponding bit in PG_DAT register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0398			Register Name: PG_DAT_CLR
Bit	Read/Write	Default/Hex	Description
6	R/W1C	0x0	PORT6_DAT_CLR Writing 1 to this bit clear corresponding bit in the PG_DAT register; write 0 have no effect. A read of this bit returns the value of corresponding bit in PG_DAT register
5	R/W1C	0x0	PORT5_DAT_CLR Writing 1 to this bit clear corresponding bit in the PG_DAT register; write 0 have no effect. A read of this bit returns the value of corresponding bit in PG_DAT register
4	R/W1C	0x0	PORT4_DAT_CLR Writing 1 to this bit clear corresponding bit in the PG_DAT register; write 0 have no effect. A read of this bit returns the value of corresponding bit in PG_DAT register
3	R/W1C	0x0	PORT3_DAT_CLR Writing 1 to this bit clear corresponding bit in the PG_DAT register; write 0 have no effect. A read of this bit returns the value of corresponding bit in PG_DAT register
2	R/W1C	0x0	PORT2_DAT_CLR Writing 1 to this bit clear corresponding bit in the PG_DAT register; write 0 have no effect. A read of this bit returns the value of corresponding bit in PG_DAT register
1	R/W1C	0x0	PORT1_DAT_CLR Writing 1 to this bit clear corresponding bit in the PG_DAT register; write 0 have no effect. A read of this bit returns the value of corresponding bit in PG_DAT register
0	R/W1C	0x0	PORT0_DAT_CLR Writing 1 to this bit clear corresponding bit in the PG_DAT register; write 0 have no effect. A read of this bit returns the value of corresponding bit in PG_DAT register

18.14.6.84 0x03A0 PG Multi-Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x03A0			Register Name: PG_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x03A0			Register Name: PG_DRV0
Bit	Read/Write	Default/Hex	Description
29:28	R/W	0x1	PG7_DRV PG7 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PG6_DRV PG6 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PG5_DRV PG5 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PG4_DRV PG4 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PG3_DRV PG3 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PG2_DRV PG2 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PG1_DRV PG1 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PG0_DRV PG0 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.14.6.85 0x03A4 PG Multi-Driving Register 1 (Default Value: 0x0111_1111)

Offset: 0x03A4			Register Name: PG_DRV1
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x1	PG14_DRV PG14 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PG13_DRV PG13 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PG12_DRV PG12 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PG11_DRV PG11 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PG10_DRV PG10 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PG9_DRV PG9 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PG8_DRV PG8 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

18.14.6.86 0x03B0 PG Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x03B0	Register Name: PG_PUL0

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	PG14_PULL PG14 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
27:26	R/W	0x0	PG13_PULL PG13 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PG12_PULL PG12 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PG11_PULL PG11 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PG10_PULL PG10 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PG9_PULL PG9 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PG8_PULL PG8 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PG7_PULL PG7 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PG6_PULL PG6 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PG5_PULL PG5 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

9:8	R/W	0x0	PG4_PULL PG4 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PG3_PULL PG3 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PG2_PULL PG2 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PG1_PULL PG1 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PG0_PULL PG0 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

18.14.6.87 0x03C0 PG External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x03C0			Register Name: PG_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x03C0			Register Name: PG_INT_CFG0
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0x0	EINT5_CFG External INT5 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x03C0			Register Name: PG_INT_CFG0
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	EINT0_CFG External INT0 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

18.14.6.88 0x03C4 PG External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x03C4			Register Name: PG_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0x0	EINT14_CFG External INT14 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x03C4			Register Name: PG_INT_CFG1
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT11_CFG External INT11 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

18.14.6.89 0x03D0 PG External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x03D0			Register Name: PG_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x03D0			Register Name: PG_INT_CTL
Bit	Read/Write	Default/Hex	Description
14	R/W	0x0	EINT14_CTL External INT14 Enable. 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable. 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable. 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable. 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable. 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable. 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable. 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable. 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable. 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x03D0			Register Name: PG_INT_CTL
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	EINT4_CTL External INT4 Enable. 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable. 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable. 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable. 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable. 0: Disable 1: Enable

18.14.6.90 0x03D4 PG External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x03D4			Register Name: PG_INT_STA
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14	R/W1C	0x0	EINT14_STATUS External INT14 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W1C	0x0	EINT13_STATUS External INT13 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W1C	0x0	EINT12_STATUS External INT12 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x03D4			Register Name: PG_INT_STA
Bit	Read/Write	Default/Hex	Description
11	R/W1C	0x0	EINT11_STATUS External INT11 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W1C	0x0	EINT10_STATUS External INT10 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W1C	0x0	EINT9_STATUS External INT9 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W1C	0x0	EINT8_STATUS External INT8 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W1C	0x0	EINT7_STATUS External INT7 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x03D4			Register Name: PG_INT_STA
Bit	Read/Write	Default/Hex	Description
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

18.14.6.91 0x03D8 PG External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x03D8			Register Name: PG_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n. The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select. 0: RTC_32K 1: SYS_CLK24M

18.14.6.92 0x03F0 PG SECURE Configure Register (Default Value: 0x0000_0000)

Offset: 0x03F0			Register Name: PG_SECURE
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x03F0			Register Name: PG_SECURE
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PORT31_SEC_SEL Port31 secure select. 0: Not secure 1: Secure
30	R/W	0x0	PORT30_SEC_SEL Port30 secure select. 0: Not secure 1: Secure
29	R/W	0x0	PORT29_SEC_SEL Port29 secure select. 0: Not secure 1: Secure
28	R/W	0x0	PORT28_SEC_SEL Port28 secure select. 0: Not secure 1: Secure
27	R/W	0x0	PORT27_SEC_SEL Port27 secure select. 0: Not secure 1: Secure
26	R/W	0x0	PORT26_SEC_SEL Port26 secure select. 0: Not secure 1: Secure
25	R/W	0x0	PORT25_SEC_SEL Port25 secure select. 0: Not secure 1: Secure
24	R/W	0x0	PORT24_SEC_SEL Port24 secure select. 0: Not secure 1: Secure
23	R/W	0x0	PORT23_SEC_SEL Port23 secure select. 0: Not secure 1: Secure
22	R/W	0x0	PORT22_SEC_SEL Port22 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x03F0			Register Name: PG_SECURE
Bit	Read/Write	Default/Hex	Description
21	R/W	0x0	PORT21_SEC_SEL Port21 secure select. 0: Not secure 1: Secure
20	R/W	0x0	PORT20_SEC_SEL Port20 secure select. 0: Not secure 1: Secure
19	R/W	0x0	PORT19_SEC_SEL Port19 secure select. 0: Not secure 1: Secure
18	R/W	0x0	PORT18_SEC_SEL Port18 secure select. 0: Not secure 1: Secure
17	R/W	0x0	PORT17_SEC_SEL Port17 secure select. 0: Not secure 1: Secure
16	R/W	0x0	PORT16_SEC_SEL Port16 secure select. 0: Not secure 1: Secure
15	R/W	0x0	PORT15_SEC_SEL Port15 secure select. 0: Not secure 1: Secure
14	R/W	0x0	PORT14_SEC_SEL Port14 secure select. 0: Not secure 1: Secure
13	R/W	0x0	PORT13_SEC_SEL Port13 secure select. 0: Not secure 1: Secure
12	R/W	0x0	PORT12_SEC_SEL Port12 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x03F0			Register Name: PG_SECURE
Bit	Read/Write	Default/Hex	Description
11	R/W	0x0	PORT11_SEC_SEL Port11 secure select. 0: Not secure 1: Secure
10	R/W	0x0	PORT10_SEC_SEL Port10 secure select. 0: Not secure 1: Secure
9	R/W	0x0	PORT9_SEC_SEL Port9 secure select. 0: Not secure 1: Secure
8	R/W	0x0	PORT8_SEC_SEL Port8 secure select. 0: Not secure 1: Secure
7	R/W	0x0	PORT7_SEC_SEL Port7 secure select. 0: Not secure 1: Secure
6	R/W	0x0	PORT6_SEC_SEL Port6 secure select. 0: Not secure 1: Secure
5	R/W	0x0	PORT5_SEC_SEL Port5 secure select. 0: Not secure 1: Secure
4	R/W	0x0	PORT4_SEC_SEL Port4 secure select. 0: Not secure 1: Secure
3	R/W	0x0	PORT3_SEC_SEL Port3 secure select. 0: Not secure 1: Secure
2	R/W	0x0	PORT2_SEC_SEL Port2 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x03F0			Register Name: PG_SECURE
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	PORT1_SEC_SEL Port1 secure select. 0: Not secure 1: Secure
0	R/W	0x0	PORT0_SEC_SEL Port0 secure select. 0: Not secure 1: Secure

18.14.6.93 0x0400 PH Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0400			Register Name: PH_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PH7_SELECT PH7 Select. 0000: Input 0001: Output 0010: UART3-CTS 0011: SPI2-CS2 0100: DSI-TRIG-LCD-TE1 0101: RGMII0-TXCTL/RMII0-TXEN 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT7 1111: IO Disable
27:24	R/W	0xF	PH6_SELECT PH6 Select. 0000: Input 0001: Output 0010: UART3-RTS 0011: I2S2-DOUT1 0100: I2S2-DIN0 0101: RGMII0-TXCK/RMII0-TXCK 0110: Reserved 0111: SPI1-CLK 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT6 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0400			Register Name: PH_CFG0
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0xF	PH5_SELECT PH5 Select. 0000: Input 0001: Output 0010: UART3-RX 0011: I2S2-DIN1 0100: I2S2-DOUT0 0101: RGMII0-TXD0/RMII0-TXD0 0110: Reserved 0111: SPI1-MOSI 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT5 1111: IO Disable
19:16	R/W	0xF	PH4_SELECT PH4 Select. 0000: Input 0001: Output 0010: UART3-TX 0011: SPI2-CS3 0100: I2S2-LRCK 0101: RGMII0-TXD1/RMII0-TXD1 0110: Reserved 0111: SPI1-CS0 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT4 1111: IO Disable
15:12	R/W	0xF	PH3_SELECT PH3 Select. 0000: Input 0001: Output 0010: TWI1-SDA 0011: Reserved 0100: I2S2-BCLK 0101: RGMII0-CLKIN/RMII0-RXER 0110: Reserved 0111: SPI1-MISO 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT3 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0400			Register Name: PH_CFG0
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0xF	PH2_SELECT PH2 Select. 0000: Input 0001: Output 0010: TWI1-SCK 0011: Reserved 0100: I2S2-MCLK 0101: RGMII0-RXCTL/RMII0-CRS-DV 0110: Reserved 0111: SPI1-CS1 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT2 1111: IO Disable
7:4	R/W	0xF	PH1_SELECT PH1 Select. 0000: Input 0001: Output 0010: TWI0-SDA 0011: I2S2-DOUT3 0100: I2S2-DIN3 0101: RGMII0-RXD0/RMII0-RXD0 0110: TWI3-SDA 0111: SPI1-WP 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT1 1111: IO Disable
3:0	R/W	0xF	PH0_SELECT PH0 Select. 0000: Input 0001: Output 0010: TWI0-SCK 0011: I2S2-DOUT2 0100: I2S2-DIN2 0101: RGMII0-RXD1/RMII0-RXD1 0110: TWI3-SCK 0111: SPI1-HOLD 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT0 1111: IO Disable

18.14.6.94 0x0404 PH Configure Register 1 (Default Value: 0xFFFF_FFFF)

Offset: 0x0404			Register Name: PH_CFG1
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0404			Register Name: PH_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PH15_SELECT PH15 Select. 0000: Input 0001: Output 0010: UART5-RTS 0011: LEDC 0100: DSI-TRIG-LCD-TE1 0101: RGMII0-EPHY-25/50M 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT15 1111: IO Disable
27:24	R/W	0xF	PH14_SELECT PH14 Select. 0000: Input 0001: Output 0010: UART5-RX 0011: Reserved 0100: Reserved 0101: RGMII0-TXD2/RMII0-NULL 0110: TWI7-SCK 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT14 1111: IO Disable
23:20	R/W	0xF	PH13_SELECT PH13 Select. 0000: Input 0001: Output 0010: UART5-TX 0011: Reserved 0100: Reserved 0101: RGMII0-TXD3/RMII0-NULL 0110: TWI7-SDA 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT13 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0404			Register Name: PH_CFG1
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0xF	PH12_SELECT PH12 Select. 0000: Input 0001: Output 0010: DMIC-DATA3 0011: SPI2-CS1 0100: Reserved 0101: RGMII0-RXCK/RMII0-NULL 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT12 1111: IO Disable
15:12	R/W	0xF	PH11_SELECT PH11 Select. 0000: Input 0001: Output 0010: DMIC-DATA2 0011: SPI2-MISO 0100: Reserved 0101: RGMII0-RXD2/RMII0-NULL 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT11 1111: IO Disable
11:8	R/W	0xF	PH10_SELECT PH10 Select. 0000: Input 0001: Output 0010: DMIC-DATA1 0011: SPI2-MOSI 0100: Reserved 0101: RGMII0-RXD3/RMII0-NULL 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT10 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0404			Register Name: PH_CFG1
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0xF	PH9_SELECT PH9 Select. 0000: Input 0001: Output 0010: DMIC-DATA0 0011: SPI2-CS0 0100: Reserved 0101: RGMII0-MDIO 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT9 1111: IO Disable
3:0	R/W	0xF	PH8_SELECT PH8 Select. 0000: Input 0001: Output 0010: DMIC-CLK 0011: SPI2-CLK 0100: Reserved 0101: RGMII0-MDC 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT8 1111: IO Disable

18.14.6.95 0x0408 PH Configure Register 2 (Default Value: 0x0000_FFFF)

Offset: 0x0408			Register Name: PH_CFG2
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0xF	PH16_SELECT PH16 Select. 0000: Input 0001: Output 0010: UART5-CTS 0011: Reserved 0100: SPI2-CLK 0101: IR-TX 0110: TWI5-SCK 0111: TWI6-SCK 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT16 1111: IO Disable

18.14.6.96 0x0410 PH Data Register (Default Value: 0x0000_0000)

Offset: 0x0410			Register Name: PH_DAT
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0410			Register Name: PH_DAT
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16:0	R/W	0	PH_DAT PH Data. If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

18.14.6.97 0x0414 PH Data Set Register (Default Value: 0x0000_0000)

Offset: 0x0414			Register Name: PH_DAT_SET
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W1S	0x0	PORT16_DAT_SET Writing 1 to this bit set bit 16 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 16 in PH_DAT register.
15	R/W1S	0x0	PORT15_DAT_SET Writing 1 to this bit set bit 15 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 15 in PH_DAT register.
14	R/W1S	0x0	PORT14_DAT_SET Writing 1 to this bit set bit 14 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 14 in PH_DAT register.
13	R/W1S	0x0	PORT13_DAT_SET Writing 1 to this bit set bit 13 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 13 in PH_DAT register.
12	R/W1S	0x0	PORT12_DAT_SET Writing 1 to this bit set bit 12 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 12 in PH_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0414			Register Name: PH_DAT_SET
Bit	Read/Write	Default/Hex	Description
11	R/W1S	0x0	PORT11_DAT_SET Writing 1 to this bit set bit 11 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 11 in PH_DAT register.
10	R/W1S	0x0	PORT10_DAT_SET Writing 1 to this bit set bit 10 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 10 in PH_DAT register.
9	R/W1S	0x0	PORT9_DAT_SET Writing 1 to this bit set bit 9 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 9 in PH_DAT register.
8	R/W1S	0x0	PORT8_DAT_SET Writing 1 to this bit set bit 8 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 8 in PH_DAT register.
7	R/W1S	0x0	PORT7_DAT_SET Writing 1 to this bit set bit 7 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 7 in PH_DAT register.
6	R/W1S	0x0	PORT6_DAT_SET Writing 1 to this bit set bit 6 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 6 in PH_DAT register.
5	R/W1S	0x0	PORT5_DAT_SET Writing 1 to this bit set bit 5 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 5 in PH_DAT register.
4	R/W1S	0x0	PORT4_DAT_SET Writing 1 to this bit set bit 4 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 4 in PH_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0414			Register Name: PH_DAT_SET
Bit	Read/Write	Default/Hex	Description
3	R/W1S	0x0	PORT3_DAT_SET Writing 1 to this bit set bit 3 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 3 in PH_DAT register.
2	R/W1S	0x0	PORT2_DAT_SET Writing 1 to this bit set bit 2 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 2 in PH_DAT register.
1	R/W1S	0x0	PORT1_DAT_SET Writing 1 to this bit set bit 1 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 1 in PH_DAT register.
0	R/W1S	0x0	PORT0_DAT_SET Writing 1 to this bit set bit 0 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 0 in PH_DAT register.

18.14.6.98 0x0418 PH Data Clear Register (Default Value: 0x0000_0000)

Offset: 0x0418			Register Name: PH_DAT_CLR
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W1C	0x0	PORT16_DAT_CLR Writing 1 to this bit clear bit 16 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 16 in PH_DAT register.
15	R/W1C	0x0	PORT15_DAT_CLR Writing 1 to this bit clear bit 15 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 15 in PH_DAT register.
14	R/W1C	0x0	PORT14_DAT_CLR Writing 1 to this bit clear bit 14 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 14 in PH_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0418			Register Name: PH_DAT_CLR
Bit	Read/Write	Default/Hex	Description
13	R/W1C	0x0	PORT13_DAT_CLR Writing 1 to this bit clear bit 13 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 13 in PH_DAT register.
12	R/W1C	0x0	PORT12_DAT_CLR Writing 1 to this bit clear bit 12 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 12 in PH_DAT register.
11	R/W1C	0x0	PORT11_DAT_CLR Writing 1 to this bit clear bit 11 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 11 in PH_DAT register.
10	R/W1C	0x0	PORT10_DAT_CLR Writing 1 to this bit clear bit 10 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 10 in PH_DAT register.
9	R/W1C	0x0	PORT9_DAT_CLR Writing 1 to this bit clear bit 9 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 9 in PH_DAT register.
8	R/W1C	0x0	PORT8_DAT_CLR Writing 1 to this bit clear bit 8 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 8 in PH_DAT register.
7	R/W1C	0x0	PORT7_DAT_CLR Writing 1 to this bit clear bit 7 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 7 in PH_DAT register.
6	R/W1C	0x0	PORT6_DAT_CLR Writing 1 to this bit clear bit 6 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 6 in PH_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0418			Register Name: PH_DAT_CLR
Bit	Read/Write	Default/Hex	Description
5	R/W1C	0x0	PORT5_DAT_CLR Writing 1 to this bit clear bit 5 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 5 in PH_DAT register.
4	R/W1C	0x0	PORT4_DAT_CLR Writing 1 to this bit clear bit 4 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 4 in PH_DAT register.
3	R/W1C	0x0	PORT3_DAT_CLR Writing 1 to this bit clear bit 3 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 3 in PH_DAT register.
2	R/W1C	0x0	PORT2_DAT_CLR Writing 1 to this bit clear bit 2 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 2 in PH_DAT register.
1	R/W1C	0x0	PORT1_DAT_CLR Writing 1 to this bit clear bit 1 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 1 in PH_DAT register.
0	R/W1C	0x0	PORT0_DAT_CLR Writing 1 to this bit clear bit 0 in the PH_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 0 in PH_DAT register.

18.14.6.99 0x0420 PH Multi-Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x0420			Register Name: PH_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PH7_DRV PH7 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0420			Register Name: PH_DRV0
Bit	Read/Write	Default/Hex	Description
25:24	R/W	0x1	PH6_DRV PH6 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PH5_DRV PH5 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PH4_DRV PH4 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PH3_DRV PH3 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PH2_DRV PH2 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PH1_DRV PH1 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PH0_DRV PH0 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

18.14.6.100 0x0424 PH Multi-Driving Register 1 (Default Value: 0x1111_1111)

Offset: 0x0424			Register Name: PH_DRV1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0424			Register Name: PH_DRV1
Bit	Read/Write	Default/Hex	Description
29:28	R/W	0x1	PH15_DRV PH15 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PH14_DRV PH14 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PH13_DRV PH13 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PH12_DRV PH12 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PH11_DRV PH11 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PH10_DRV PH10 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PH9_DRV PH9 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PH8_DRV PH8 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.14.6.101 0x0428 PH Multi-Driving Register 2 (Default Value: 0x0000_1111)

Offset: 0x0428			Register Name: PH_DRV2
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x1	PH16_DRV PH16 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

18.14.6.102 0x0430 PH Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0430			Register Name: PH_PUL0
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	PH15_PULL PH15 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
29:28	R/W	0x0	PH14_PULL PH14 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
27:26	R/W	0x0	PH13_PULL PH13 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PH12_PULL PH12 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PH11_PULL PH11 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PH10_PULL PH10 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PH9_PULL PH9 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0430			Register Name: PH_PUL0
Bit	Read/Write	Default/Hex	Description
17:16	R/W	0x0	PH8_PULL PH8 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PH7_PULL PH7 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PH6_PULL PH6 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PH5_PULL PH5 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PH4_PULL PH4 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PH3_PULL PH3 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PH2_PULL PH2 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PH1_PULL PH1 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PH0_PULL PH0 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

18.14.6.103 0x0434 PH Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0434			Register Name: PH_PUL1
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0434			Register Name: PH_PUL1
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	PH16_PULL PH16 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

18.14.6.104 0x0440 PH External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0440			Register Name: PH_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0440			Register Name: PH_INT_CFG0
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0x0	EINT4_CFG External INT4 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.14.6.105 0x0444 PH External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0444			Register Name: PH_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT15_CFG External INT15 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0444			Register Name: PH_INT_CFG1
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0x0	EINT10_CFG External INT10 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

18.14.6.106 0x0448 PH External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0448			Register Name: PH_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	EINT16_CFG External INT16 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.14.6.107 0x0450 PH External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0450			Register Name: PH_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	EINT16_CTL External INT16 Enable. 0: Disable 1: Enable
15	R/W	0x0	EINT15_CTL External INT15 Enable. 0: Disable 1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable. 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable. 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable. 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable. 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable. 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable. 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0450			Register Name: PH_INT_CTL
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	EINT7_CTL External INT7 Enable. 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable. 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable. 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable. 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable. 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable. 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable. 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable. 0: Disable 1: Enable

18.14.6.108 0x0454 PH External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0454			Register Name: PH_INT_STA
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0454			Register Name: PH_INT_STA
Bit	Read/Write	Default/Hex	Description
16	R/W1C	0x0	EINT16_STATUS External INT16 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
15	R/W1C	0x0	EINT15_STATUS External INT15 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W1C	0x0	EINT14_STATUS External INT14 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W1C	0x0	EINT13_STATUS External INT13 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W1C	0x0	EINT12_STATUS External INT12 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W1C	0x0	EINT11_STATUS External INT11 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W1C	0x0	EINT10_STATUS External INT10 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W1C	0x0	EINT9_STATUS External INT9 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0454			Register Name: PH_INT_STA
Bit	Read/Write	Default/Hex	Description
8	R/W1C	0x0	EINT8_STATUS External INT8 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W1C	0x0	EINT7_STATUS External INT7 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0454			Register Name: PH_INT_STA
Bit	Read/Write	Default/Hex	Description
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

18.14.6.109 0x0458 PH External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0458			Register Name: PH_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n. The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select. 0: RTC_32K 1: SYS_CLK24M

18.14.6.110 0x0470 PH SECURE Configure Register (Default Value: 0x0000_0000)

Offset: 0x0470			Register Name: PH_SECURE
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	PORT16_SEC_SEL Port16 secure select. 0: Not secure 1: Secure
15	R/W	0x0	PORT15_SEC_SEL Port15 secure select. 0: Not secure 1: Secure
14	R/W	0x0	PORT14_SEC_SEL Port14 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0470			Register Name: PH_SECURE
Bit	Read/Write	Default/Hex	Description
13	R/W	0x0	PORT13_SEC_SEL Port13 secure select. 0: Not secure 1: Secure
12	R/W	0x0	PORT12_SEC_SEL Port12 secure select. 0: Not secure 1: Secure
11	R/W	0x0	PORT11_SEC_SEL Port11 secure select. 0: Not secure 1: Secure
10	R/W	0x0	PORT10_SEC_SEL Port10 secure select. 0: Not secure 1: Secure
9	R/W	0x0	PORT9_SEC_SEL Port9 secure select. 0: Not secure 1: Secure
8	R/W	0x0	PORT8_SEC_SEL Port8 secure select. 0: Not secure 1: Secure
7	R/W	0x0	PORT7_SEC_SEL Port7 secure select. 0: Not secure 1: Secure
6	R/W	0x0	PORT6_SEC_SEL Port6 secure select. 0: Not secure 1: Secure
5	R/W	0x0	PORT5_SEC_SEL Port5 secure select. 0: Not secure 1: Secure
4	R/W	0x0	PORT4_SEC_SEL Port4 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0470			Register Name: PH_SECURE
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	PORT3_SEC_SEL Port3 secure select. 0: Not secure 1: Secure
2	R/W	0x0	PORT2_SEC_SEL Port2 secure select. 0: Not secure 1: Secure
1	R/W	0x0	PORT1_SEC_SEL Port1 secure select. 0: Not secure 1: Secure
0	R/W	0x0	PORT0_SEC_SEL Port0 secure select. 0: Not secure 1: Secure

18.14.6.111 0x0508 PJ Configure Register 2 (Default Value: 0xFFFF_FFFF)

Offset: 0x0508			Register Name: PJ_CFG2
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PJ23_SELECT PJ23 Select. 0000: Input 0001: Output 0010: LCD1-D23 0011: PWM1-5 0100: UART3-RX 0101: UART2-CTS 0110: TWI7-SDA 0111: TWI3-SDA 1000: TWI11-SDA 1001: LCD0-D9 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT23 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0508			Register Name: PJ_CFG2
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0xF	PJ22_SELECT PJ22 Select. 0000: Input 0001: Output 0010: LCD1-D22 0011: PWM1-4 0100: UART3-TX 0101: UART2-RTS 0110: TWI7-SCK 0111: TWI3-SCK 1000: TWI11-SCK 1001: LCD0-D8 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT22 1111: IO Disable
23:0	/	/	/

18.14.6.112 0x050C PJ Configure Register 3 (Default Value: 0x0000_FFFF)

Offset: 0x050C			Register Name: PJ_CFG3
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:12	R/W	0xF	PJ27_SELECT PJ27 Select. 0000: Input 0001: Output 0010: LCD1-VSYNC 0011: PWM1-9 0100: UART4-CTS 0101: UART2-RX 0110: DSI-TRIG-LCD-TE1 0111: TWI5-SDA 1000: SPI3-CS0 1001: LCD0-D17 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT27 1111: IO Disable
11:8	R/W	0xF	PJ26_SELECT PJ26 Select. 0000: Input 0001: Output 0010: LCD1-HSYNC 0011: PWM1-8 0100: UART4-RTS 0101: UART2-TX 0110: Reserved 0111: TWI5-SCK 1000: SPI3-MISO 1001: LCD0-D16 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT26 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x050C			Register Name: PJ_CFG3
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0xF	PJ25_SELECT PJ25 Select. 0000: Input 0001: Output 0010: LCD1-DE 0011: PWM1-7 0100: UART4-RX 0101: Reserved 0110: Reserved 0111: TWI4-SDA 1000: SPI3-MOSI 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT25 1111: IO Disable
3:0	R/W	0xF	PJ24_SELECT PJ24 Select. 0000: Input 0001: Output 0010: LCD1-CLK 0011: PWM1-6 0100: UART4-TX 0101: Reserved 0110: Reserved 0111: TWI4-SCK 1000: SPI3-CLK 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PJ-EINT24 1111: IO Disable

18.14.6.113 0x0510 PJ Data Register (Default Value: 0x0000_0000)

Offset: 0x0510			Register Name: PJ_DAT
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:22	R/W	0	PJ_DAT PJ Data. If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.
21:0	/	/	/

18.14.6.114 0x0514 PJ Data Set Register (Default Value: 0x0000_0000)

Offset: 0x0514			Register Name: PJ_DAT_SET
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0514			Register Name: PJ_DAT_SET
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R/W1S	0x0	PORT27_DAT_SET Writing 1 to this bit sets bit 27 in the PJ_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 27 in PJ_DAT register.
26	R/W1S	0x0	PORT26_DAT_SET Writing 1 to this bit sets bit 26 in the PJ_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 26 in PJ_DAT register.
25	R/W1S	0x0	PORT25_DAT_SET Writing 1 to this bit sets bit 25 in the PJ_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 25 in PJ_DAT register.
24	R/W1S	0x0	PORT24_DAT_SET Writing 1 to this bit sets bit 24 in the PJ_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 24 in PJ_DAT register.
23	R/W1S	0x0	PORT23_DAT_SET Writing 1 to this bit sets bit 23 in the PJ_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 23 in PJ_DAT register.
22	R/W1S	0x0	PORT22_DAT_SET Writing 1 to this bit sets bit 22 in the PJ_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 22 in PJ_DAT register.
21:0	/	/	/

18.14.6.115 0x0518 PJ Data Clear Register (Default Value: 0x0000_0000)

Offset: 0x0518			Register Name: PJ_DAT_CLR
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0518			Register Name: PJ_DAT_CLR
Bit	Read/Write	Default/Hex	Description
27	R/W1C	0x0	PORT27_DAT_CLR Writing 1 to this bit clear bit 27 in the PJ_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 27 in PJ_DAT register.
26	R/W1C	0x0	PORT26_DAT_CLR Writing 1 to this bit clear bit 26 in the PJ_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 26 in PJ_DAT register.
25	R/W1C	0x0	PORT25_DAT_CLR Writing 1 to this bit clear bit 25 in the PJ_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 25 in PJ_DAT register.
24	R/W1C	0x0	PORT24_DAT_CLR Writing 1 to this bit clear bit 24 in the PJ_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 24 in PJ_DAT register.
23	R/W1C	0x0	PORT23_DAT_CLR Writing 1 to this bit clear bit 23 in the PJ_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 23 in PJ_DAT register.
22	R/W1C	0x0	PORT22_DAT_CLR Writing 1 to this bit clear bit 22 in the PJ_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 22 in PJ_DAT register.
21:0	/	/	/

18.14.6.116 0x0528 PJ Multi-Driving Register 2 (Default Value: 0x1111_1111)

Offset: 0x0528			Register Name: PJ_DRV2
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PJ23_DRV PJ23 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0528			Register Name: PJ_DRV2
Bit	Read/Write	Default/Hex	Description
27:26	/	/	/
25:24	R/W	0x1	PJ22_DRV PJ22 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:0	/	/	/

18.14.6.117 0x052C PJ Multi-Driving Register 3 (Default Value: 0x0000_1111)

Offset: 0x052C			Register Name: PJ_DRV3
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:12	R/W	0x1	PJ27_DRV PJ27 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PJ26_DRV PJ26 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PJ25_DRV PJ25 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PJ24_DRV PJ24 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

18.14.6.118 0x0534 PJ Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0534			Register Name: PJ_PUL1
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0534			Register Name: PJ_PUL1
Bit	Read/Write	Default/Hex	Description
23:22	R/W	0x0	PJ27_PULL PJ27 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PJ26_PULL PJ26 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PJ25_PULL PJ25 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PJ24_PULL PJ24 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PJ23_PULL PJ23 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PJ22_PULL PJ22 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:0	/	/	/

18.14.6.119 0x0548 PJ External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0548			Register Name: PJ_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT23_CFG External INT23 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0548			Register Name: PJ_INT_CFG2
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0x0	EINT22_CFG External INT22 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
23:0	/	/	/

18.14.6.120 0x054C PJ External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x054C			Register Name: PJ_INT_CFG3
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:12	R/W	0x0	EINT27_CFG External INT27 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT26_CFG External INT26 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT25_CFG External INT25 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x054C			Register Name: PJ_INT_CFG3
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	EINT24_CFG External INT24 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

18.14.6.121 0x0550 PJ External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0550			Register Name: PJ_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R/W	0x0	EINT27_CTL External INT27 Enable. 0: Disable 1: Enable
26	R/W	0x0	EINT26_CTL External INT26 Enable. 0: Disable 1: Enable
25	R/W	0x0	EINT25_CTL External INT25 Enable. 0: Disable 1: Enable
24	R/W	0x0	EINT24_CTL External INT24 Enable. 0: Disable 1: Enable
23	R/W	0x0	EINT23_CTL External INT23 Enable. 0: Disable 1: Enable
22	R/W	0x0	EINT22_CTL External INT22 Enable. 0: Disable 1: Enable
21:0	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.14.6.122 0x0554 PJ External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0554			Register Name: PJ_INT_STA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R/W1C	0x0	EINT27_STATUS External INT27 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
26	R/W1C	0x0	EINT26_STATUS External INT26 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
25	R/W1C	0x0	EINT25_STATUS External INT25 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
24	R/W1C	0x0	EINT24_STATUS External INT24 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
23	R/W1C	0x0	EINT23_STATUS External INT23 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
22	R/W1C	0x0	EINT22_STATUS External INT22 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
21	/	/	/

18.14.6.123 0x0558 PJ External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0558			Register Name: PJ_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0558			Register Name: PJ_INT_DEB
Bit	Read/Write	Default/Hex	Description
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n. The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select. 0: RTC_32K 1: SYS_CLK24M

18.14.6.124 0x0570 PJ SECURE Configure Register (Default Value: 0x0000_0000)

Offset: 0x0570			Register Name: PJ_SECURE
Bit	Read/Write	Default/Hex	Description
31	/	/	/
27	R/W	0x0	PORT27_SEC_SEL Port27 secure select. 0: Not secure 1: Secure
26	R/W	0x0	PORT26_SEC_SEL Port26 secure select. 0: Not secure 1: Secure
25	R/W	0x0	PORT25_SEC_SEL Port25 secure select. 0: Not secure 1: Secure
24	R/W	0x0	PORT24_SEC_SEL Port24 secure select. 0: Not secure 1: Secure
23	R/W	0x0	PORT23_SEC_SEL Port23 secure select. 0: Not secure 1: Secure
22	R/W	0x0	PORT22_SEC_SEL Port22 secure select. 0: Not secure 1: Secure
21:0	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.14.6.125 0x0580 PK Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0580			Register Name: PK_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PK7_SELECT PK7 Select. 0000: Input 0001: Output 0010: MCSIA-D2P 0011: TWI2-SDA 0100: UART4-RX 0101: UART2-CTS 0110: SPI3-MISO 0111: NCSI1-D12 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT7 1111: IO Disable
27:24	R/W	0xF	PK6_SELECT PK6 Select. 0000: Input 0001: Output 0010: MCSIA-D2N 0011: TWI2-SCK 0100: UART4-TX 0101: UART2-RTS 0110: SPI3-MOSI 0111: NCSI1-D13 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT6 1111: IO Disable
23:20	R/W	0xF	PK5_SELECT PK5 Select. 0000: Input 0001: Output 0010: MCSIA-CKP 0011: PCIE-CLKREQN 0100: PWM1-8 0101: PWM1-9 0110: SPI3-CLK 0111: NCSI1-D14 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT5 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0580			Register Name: PK_CFG0
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0xF	PK4_SELECT PK4 Select. 0000: Input 0001: Output 0010: MCSIA-CKN 0011: PCIE-WAKEN 0100: I2S4-DOUT0<MUX-HDMI-EDP> 0101: I2S4-DIN1<MUX-HDMI-EDP> 0110: SPI3-CS0 0111: NCSI1-D15 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT4 1111: IO Disable
15:12	R/W	0xF	PK3_SELECT PK3 Select. 0000: Input 0001: Output 0010: MCSIA-D1P 0011: UART6-RI 0100: I2S4-DIN0<MUX-HDMI-EDP> 0101: I2S4-DOUT1<MUX-HDMI-EDP> 0110: TWI5-SCK 0111: NCSI1-MCLK 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT3 1111: IO Disable
11:8	R/W	0xF	PK2_SELECT PK2 Select. 0000: Input 0001: Output 0010: MCSIA-D1N 0011: UART6-DTR 0100: I2S4-LRCK<MUX-HDMI-EDP> 0101: HDMI-SDA 0110: TWI5-SDA 0111: NCSI1-PCLK 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT2 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0580			Register Name: PK_CFG0
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0xF	PK1_SELECT PK1 Select. 0000: Input 0001: Output 0010: MCSIA-D0P 0011: UART6-DSR 0100: I2S4-MCLK<MUX-HDMI-EDP> 0101: HDMI-SCL 0110: TWI1-SCK 0111: NCSI1-VSYNC 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT1 1111: IO Disable
3:0	R/W	0xF	PK0_SELECT PK0 Select. 0000: Input 0001: Output 0010: MCSIA-D0N 0011: UART6-DCD 0100: I2S4-BCLK<MUX-HDMI-EDP> 0101: HDMI-CEC 0110: TWI1-SDA 0111: NCSI1-HSYNC 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT0 1111: IO Disable

18.14.6.126 0x0584 PK Configure Register 1 (Default Value: 0xFFFF-FFFF)

Offset: 0x0584			Register Name: PK_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PK15_SELECT PK15 Select. 0000: Input 0001: Output 0010: MCSIB-CKP 0011: Reserved 0100: Reserved 0101: PWM0-8 0110: Reserved 0111: NCSI1-D4 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT15 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0584			Register Name: PK_CFG1
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0xF	PK14_SELECT PK14 Select. 0000: Input 0001: Output 0010: MCSIB-CKN 0011: PCIE-PERSTN 0100: Reserved 0101: PWM0-7 0110: Reserved 0111: NCSI1-D5 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT14 1111: IO Disable
23:20	R/W	0xF	PK13_SELECT PK13 Select. 0000: Input 0001: Output 0010: MCSIB-D1P 0011: UART6-CTS 0100: Reserved 0101: PWM0-6 0110: Reserved 0111: NCSI1-D6 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT13 1111: IO Disable
19:16	R/W	0xF	PK12_SELECT PK12 Select. 0000: Input 0001: Output 0010: MCSIB-D1N 0011: UART6-RTS 0100: Reserved 0101: PWM0-5 0110: Reserved 0111: NCSI1-D7 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT12 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0584			Register Name: PK_CFG1
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0xF	PK11_SELECT PK11 Select. 0000: Input 0001: Output 0010: MCSIB-D0P 0011: UART6-RX 0100: Reserved 0101: PWM0-4 0110: Reserved 0111: NCSI1-D8 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT11 1111: IO Disable
11:8	R/W	0xF	PK10_SELECT PK10 Select. 0000: Input 0001: Output 0010: MCSIB-D0N 0011: UART6-TX 0100: Reserved 0101: PWM0-3 0110: Reserved 0111: NCSI1-D9 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT10 1111: IO Disable
7:4	R/W	0xF	PK9_SELECT PK9 Select. 0000: Input 0001: Output 0010: MCSIA-D3P 0011: MCSI2-MCLK 0100: UART4-CTS 0101: UART2-RX 0110: Reserved 0111: NCSI1-D10 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT9 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0584			Register Name: PK_CFG1
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xF	PK8_SELECT PK8 Select. 0000: Input 0001: Output 0010: MCSIA-D3N 0011: MCSI0-MCLK 0100: UART4-RTS 0101: UART2-TX 0110: SPI3-CS1 0111: NCSI1-D11 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT8 1111: IO Disable

18.14.6.127 0x0588 PK Configure Register 2 (Default Value: 0xFFFF-FFFF)

Offset: 0x0588			Register Name: PK_CFG2
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PK23_SELECT PK23 Select. 0000: Input 0001: Output 0010: MCSIC-D1P 0011: TWI3-SDA 0100: UART3-CTS 0101: PWM1-7 0110: Reserved 0111: NCSI1-VSYNC 1000: UART1-RX 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT23 1111: IO Disable
27:24	R/W	0xF	PK22_SELECT PK22 Select. 0000: Input 0001: Output 0010: MCSIC-D1N 0011: TWI3-SCK 0100: UART3-RTS 0101: PWM1-6 0110: Reserved 0111: NCSI1-HSYNC 1000: UART1-TX 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT22 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0588			Register Name: PK_CFG2
Bit	Read/Write	Default/Hex	Description
23:20	R/W	0xF	PK21_SELECT PK21 Select. 0000: Input 0001: Output 0010: MCSIC-D0P 0011: TWI2-SDA 0100: UART3-RX 0101: PWM0-2 0110: Reserved 0111: NCSI1-MCLK 1000: UART1-CTS 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT21 1111: IO Disable
19:16	R/W	0xF	PK20_SELECT PK20 Select. 0000: Input 0001: Output 0010: MCSIC-D0N 0011: TWI2-SCK 0100: UART3-TX 0101: PWM0-1 0110: Reserved 0111: NCSI1-PCLK 1000: UART1-RTS 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT20 1111: IO Disable
15:12	R/W	0xF	PK19_SELECT PK19 Select. 0000: Input 0001: Output 0010: MCSIB-D3P 0011: MCSI2-MCLK 0100: UART2-CTS 0101: PWM1-2 0110: Reserved 0111: NCSI1-D0 1000: TWI9-SDA 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT19 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0588			Register Name: PK_CFG2
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0xF	PK18_SELECT PK18 Select. 0000: Input 0001: Output 0010: MCSIB-D3N 0011: MCSI1-MCLK 0100: UART2-RTS 0101: PWM1-1 0110: Reserved 0111: NCSI1-D1 1000: TWI9-SCK 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT18 1111: IO Disable
7:4	R/W	0xF	PK17_SELECT PK17 Select. 0000: Input 0001: Output 0010: MCSIB-D2P 0011: TWI3-SDA 0100: UART2-RX 0101: PWM1-0 0110: Reserved 0111: NCSI1-D2 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT17 1111: IO Disable
3:0	R/W	0xF	PK16_SELECT PK16 Select. 0000: Input 0001: Output 0010: MCSIB-D2N 0011: TWI3-SCK 0100: UART2-TX 0101: PWM0-9 0110: Reserved 0111: NCSI1-D3 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT16 1111: IO Disable

18.14.6.128 0x058C PK Configure Register 3 (Default Value: 0x0000-00FF)

Offset: 0x058C			Register Name: PK_CFG3
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x058C			Register Name: PK_CFG3
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0xF	PK25_SELECT PK25 Select. 0000: Input 0001: Output 0010: MCSIC-CKP 0011: MCSI1-MCLK 0100: PWM0-7 0101: TWI12-SDA 0110: Reserved 0111: Reserved 1000: TWI10-SCK 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT25 1111: IO Disable
3:0	R/W	0xF	PK24_SELECT PK24 Select. 0000: Input 0001: Output 0010: MCSIC-CKN 0011: MCSI0-MCLK 0100: PWM0-6 0101: TWI12-SCK 0110: Reserved 0111: Reserved 1000: TWI10-SDA 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT24 1111: IO Disable

18.14.6.129 0x0590 PK Data Register (Default Value: 0x0000_0000)

Offset: 0x0590			Register Name: PK_DAT
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:0	R/W	0	PK_DAT PK Data. If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.14.6.130 0x0594 PK Data Set Register (Default Value: 0x0000_0000)

Offset: 0x0594			Register Name: PK_DAT_SET
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25	R/W1S	0x0	PORT25_DAT_SET Writing 1 to this bit sets bit 25 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 25 in PK_DAT register.
24	R/W1S	0x0	PORT24_DAT_SET Writing 1 to this bit sets bit 24 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 24 in PK_DAT register.
23	R/W1S	0x0	PORT23_DAT_SET Writing 1 to this bit sets bit 23 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 23 in PK_DAT register.
22	R/W1S	0x0	PORT22_DAT_SET Writing 1 to this bit sets bit 22 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 22 in PK_DAT register.
21	R/W1S	0x0	PORT21_DAT_SET Writing 1 to this bit sets bit 21 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 21 in PK_DAT register.
20	R/W1S	0x0	PORT20_DAT_SET Writing 1 to this bit sets bit 20 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 20 in PK_DAT register.
19	R/W1S	0x0	PORT19_DAT_SET Writing 1 to this bit sets bit 19 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 19 in PK_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0594			Register Name: PK_DAT_SET
Bit	Read/Write	Default/Hex	Description
18	R/W1S	0x0	PORT18_DAT_SET Writing 1 to this bit sets bit 18 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 18 in PK_DAT register.
17	R/W1S	0x0	PORT17_DAT_SET Writing 1 to this bit sets bit 17 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 17 in PK_DAT register.
16	R/W1S	0x0	PORT16_DAT_SET Writing 1 to this bit sets bit 16 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 16 in PK_DAT register.
15	R/W1S	0x0	PORT15_DAT_SET Writing 1 to this bit sets bit 15 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 15 in PK_DAT register.
14	R/W1S	0x0	PORT14_DAT_SET Writing 1 to this bit sets bit 14 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 14 in PK_DAT register.
13	R/W1S	0x0	PORT13_DAT_SET Writing 1 to this bit sets bit 13 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 13 in PK_DAT register.
12	R/W1S	0x0	PORT12_DAT_SET Writing 1 to this bit sets bit 12 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 12 in PK_DAT register.
11	R/W1S	0x0	PORT11_DAT_SET Writing 1 to this bit sets bit 11 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 11 in PK_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0594			Register Name: PK_DAT_SET
Bit	Read/Write	Default/Hex	Description
10	R/W1S	0x0	PORT10_DAT_SET Writing 1 to this bit sets bit 10 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 10 in PK_DAT register.
9	R/W1S	0x0	PORT9_DAT_SET Writing 1 to this bit sets bit 9 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 9 in PK_DAT register.
8	R/W1S	0x0	PORT8_DAT_SET Writing 1 to this bit sets bit 8 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 8 in PK_DAT register.
7	R/W1S	0x0	PORT7_DAT_SET Writing 1 to this bit sets bit 7 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 7 in PK_DAT register.
6	R/W1S	0x0	PORT6_DAT_SET Writing 1 to this bit sets bit 6 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 6 in PK_DAT register.
5	R/W1S	0x0	PORT5_DAT_SET Writing 1 to this bit sets bit 5 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 5 in PK_DAT register.
4	R/W1S	0x0	PORT4_DAT_SET Writing 1 to this bit sets bit 4 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 4 in PK_DAT register.
3	R/W1S	0x0	PORT3_DAT_SET Writing 1 to this bit sets bit 3 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 3 in PK_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0594			Register Name: PK_DAT_SET
Bit	Read/Write	Default/Hex	Description
2	R/W1S	0x0	PORT2_DAT_SET Writing 1 to this bit sets bit 2 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 2 in PK_DAT register.
1	R/W1S	0x0	PORT1_DAT_SET Writing 1 to this bit sets bit 1 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 1 in PK_DAT register.
0	R/W1S	0x0	PORT0_DAT_SET Writing 1 to this bit sets bit 0 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 0 in PK_DAT register.

18.14.6.131 0x0598 PK Data Clear Register (Default Value: 0x0000_0000)

Offset: 0x0598			Register Name: PK_DAT_CLR
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25	R/W1C	0x0	PORT25_DAT_CLR Writing 1 to this bit clears bit 25 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 25 in PK_DAT register.
24	R/W1C	0x0	PORT24_DAT_CLR Writing 1 to this bit clears bit 24 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 24 in PK_DAT register.
23	R/W1C	0x0	PORT23_DAT_CLR Writing 1 to this bit clears bit 23 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 23 in PK_DAT register.
22	R/W1C	0x0	PORT22_DAT_CLR Writing 1 to this bit clears bit 22 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 22 in PK_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0598			Register Name: PK_DAT_CLR
Bit	Read/Write	Default/Hex	Description
21	R/W1C	0x0	PORT21_DAT_CLR Writing 1 to this bit clears bit 21 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 21 in PK_DAT register.
20	R/W1C	0x0	PORT20_DAT_CLR Writing 1 to this bit clears bit 20 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 20 in PK_DAT register.
19	R/W1C	0x0	PORT19_DAT_CLR Writing 1 to this bit clears bit 19 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 19 in PK_DAT register.
18	R/W1C	0x0	PORT18_DAT_CLR Writing 1 to this bit clears bit 18 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 18 in PK_DAT register.
17	R/W1C	0x0	PORT17_DAT_CLR Writing 1 to this bit clears bit 17 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 17 in PK_DAT register.
16	R/W1C	0x0	PORT16_DAT_CLR Writing 1 to this bit clears bit 16 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 16 in PK_DAT register.
15	R/W1C	0x0	PORT15_DAT_CLR Writing 1 to this bit clears bit 15 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 15 in PK_DAT register.
14	R/W1C	0x0	PORT14_DAT_CLR Writing 1 to this bit clears bit 14 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 14 in PK_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0598			Register Name: PK_DAT_CLR
Bit	Read/Write	Default/Hex	Description
13	R/W1C	0x0	PORT13_DAT_CLR Writing 1 to this bit clears bit 13 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 13 in PK_DAT register.
12	R/W1C	0x0	PORT12_DAT_CLR Writing 1 to this bit clears bit 12 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 12 in PK_DAT register.
11	R/W1C	0x0	PORT11_DAT_CLR Writing 1 to this bit clears bit 11 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 11 in PK_DAT register.
10	R/W1C	0x0	PORT10_DAT_CLR Writing 1 to this bit clears bit 10 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 10 in PK_DAT register.
9	R/W1C	0x0	PORT9_DAT_CLR Writing 1 to this bit clears bit 9 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 9 in PK_DAT register.
8	R/W1C	0x0	PORT8_DAT_CLR Writing 1 to this bit clears bit 8 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 8 in PK_DAT register.
7	R/W1C	0x0	PORT7_DAT_CLR Writing 1 to this bit clears bit 7 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 7 in PK_DAT register.
6	R/W1C	0x0	PORT6_DAT_CLR Writing 1 to this bit clears bit 6 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 6 in PK_DAT register.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0598			Register Name: PK_DAT_CLR
Bit	Read/Write	Default/Hex	Description
5	R/W1C	0x0	PORT5_DAT_CLR Writing 1 to this bit clears bit 5 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 5 in PK_DAT register.
4	R/W1C	0x0	PORT4_DAT_CLR Writing 1 to this bit clears bit 4 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 4 in PK_DAT register.
3	R/W1C	0x0	PORT3_DAT_CLR Writing 1 to this bit clears bit 3 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 3 in PK_DAT register.
2	R/W1C	0x0	PORT2_DAT_CLR Writing 1 to this bit clears bit 2 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 2 in PK_DAT register.
1	R/W1C	0x0	PORT1_DAT_CLR Writing 1 to this bit clears bit 1 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 1 in PK_DAT register.
0	R/W1C	0x0	PORT0_DAT_CLR Writing 1 to this bit clears bit 0 in the PK_DAT register; writing 0 has no effect. A read of this bit returns the value of bit 0 in PK_DAT register.

18.14.6.132 0x05A0 PK Multi-Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x05A0			Register Name: PK_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PK7_DRV PK7 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x05A0			Register Name: PK_DRV0
Bit	Read/Write	Default/Hex	Description
25:24	R/W	0x1	PK6_DRV PK6 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PK5_DRV PK5 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PK4_DRV PK4 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PK3_DRV PK3 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PK2_DRV PK2 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PK1_DRV PK1 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PK0_DRV PK0 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

18.14.6.133 0x05A4 PK Multi-Driving Register 1 (Default Value: 0x1111_1111)

Offset: 0x05A4			Register Name: PK_DRV1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x05A4			Register Name: PK_DRV1
Bit	Read/Write	Default/Hex	Description
29:28	R/W	0x1	PK15_DRV PK15 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PK14_DRV PK14 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PK13_DRV PK13 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PK12_DRV PK12 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PK11_DRV PK11 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PK10_DRV PK10 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PK9_DRV PK9 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PK8_DRV PK8 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.14.6.134 0x05A8 PK Multi-Driving Register 2 (Default Value: 0x1111_1111)

Offset: 0x05A8			Register Name: PK_DRV2
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PK23_DRV PK23 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PK22_DRV PK22 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PK21_DRV PK21 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PK20_DRV PK20 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PK19_DRV PK19 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PK18_DRV PK18 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PK17_DRV PK17 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PK16_DRV PK16 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.14.6.135 0x05AC PK Multi-Driving Register 3 (Default Value: 0x0000_0011)

Offset: 0x05AC			Register Name: PK_DRV3
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5:4	R/W	0x1	PK25_DRV PK25 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PK24_DRV PK24 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

18.14.6.136 0x05B0 PK Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x05B0			Register Name: PK_PUL0
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	PK15_PULL PK15 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
29:28	R/W	0x0	PK14_PULL PK14 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
27:26	R/W	0x0	PK13_PULL PK13 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PK12_PULL PK12 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PK11_PULL PK11 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PK10_PULL PK10 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x05B0			Register Name: PK_PUL0
Bit	Read/Write	Default/Hex	Description
19:18	R/W	0x0	PK9_PULL PK9 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PK8_PULL PK8 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PK7_PULL PK7 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PK6_PULL PK6 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PK5_PULL PK5 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PK4_PULL PK4 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PK3_PULL PK3 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PK2_PULL PK2 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PK1_PULL PK1 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PK0_PULL PK0 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.14.6.137 0x05B4 PK Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x05B4			Register Name: PK_PUL1
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:18	R/W	0x0	PK25_PULL PK25 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PK24_PULL PK24 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PK23_PULL PK23 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PK22_PULL PK22 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PK21_PULL PK21 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PK20_PULL PK20 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PK19_PULL PK19 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PK18_PULL PK18 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PK17_PULL PK17 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x05B4			Register Name: PK_PUL1
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x0	PK16_PULL PK16 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

18.14.6.138 0x05C0 PK External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x05C0			Register Name: PK_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x05C0			Register Name: PK_INT_CFG0
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0x0	EINT3_CFG External INT3 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

18.14.6.139 0x05C4 PK External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x05C4			Register Name: PK_INT_CFG1
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x05C4			Register Name: PK_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT15_CFG External INT15 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x05C4			Register Name: PK_INT_CFG1
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0x0	EINT10_CFG External INT10 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

18.14.6.140 0x05C8 PK External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x05C8			Register Name: PK_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT23_CFG External INT23 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x05C8			Register Name: PK_INT_CFG2
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0x0	EINT22_CFG External INT22 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT21_CFG External INT21 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT20_CFG External INT20 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT19_CFG External INT19 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT18_CFG External INT18 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x05C8			Register Name: PK_INT_CFG2
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0x0	EINT17_CFG External INT17 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT16_CFG External INT16 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

18.14.6.141 0x05CC PK External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x05CC			Register Name: PK_INT_CFG3
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:4	R/W	0x0	EINT25_CFG External INT25 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT24_CFG External INT24 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.14.6.142 0x05D0 PK External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x05D0			Register Name: PK_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25	R/W	0x0	EINT25_CTL External INT25 Enable. 0: Disable 1: Enable
24	R/W	0x0	EINT24_CTL External INT24 Enable. 0: Disable 1: Enable
23	R/W	0x0	EINT23_CTL External INT23 Enable. 0: Disable 1: Enable
22	R/W	0x0	EINT22_CTL External INT22 Enable. 0: Disable 1: Enable
21	R/W	0x0	EINT21_CTL External INT21 Enable. 0: Disable 1: Enable
20	R/W	0x0	EINT20_CTL External INT20 Enable. 0: Disable 1: Enable
19	R/W	0x0	EINT19_CTL External INT19 Enable. 0: Disable 1: Enable
18	R/W	0x0	EINT18_CTL External INT18 Enable. 0: Disable 1: Enable
17	R/W	0x0	EINT17_CTL External INT17 Enable. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x05D0			Register Name: PK_INT_CTL
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	EINT16_CTL External INT16 Enable. 0: Disable 1: Enable
15	R/W	0x0	EINT15_CTL External INT15 Enable. 0: Disable 1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable. 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable. 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable. 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable. 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable. 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable. 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable. 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x05D0			Register Name: PK_INT_CTL
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	EINT6_CTL External INT6 Enable. 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable. 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable. 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable. 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable. 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable. 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable. 0: Disable 1: Enable

18.14.6.143 0x05D4 PK External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x05D4			Register Name: PK_INT_STA
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25	R/W1C	0x0	EINT25_STATUS External INT25 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x05D4			Register Name: PK_INT_STA
Bit	Read/Write	Default/Hex	Description
24	R/W1C	0x0	EINT24_STATUS External INT24 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
23	R/W1C	0x0	EINT23_STATUS External INT23 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
22	R/W1C	0x0	EINT22_STATUS External INT22 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
21	R/W1C	0x0	EINT21_STATUS External INT21 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
20	R/W1C	0x0	EINT20_STATUS External INT20 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
19	R/W1C	0x0	EINT19_STATUS External INT19 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
18	R/W1C	0x0	EINT18_STATUS External INT18 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
17	R/W1C	0x0	EINT17_STATUS External INT17 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x05D4			Register Name: PK_INT_STA
Bit	Read/Write	Default/Hex	Description
16	R/W1C	0x0	EINT16_STATUS External INT16 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
15	R/W1C	0x0	EINT15_STATUS External INT15 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W1C	0x0	EINT14_STATUS External INT14 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W1C	0x0	EINT13_STATUS External INT13 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W1C	0x0	EINT12_STATUS External INT12 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W1C	0x0	EINT11_STATUS External INT11 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W1C	0x0	EINT10_STATUS External INT10 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W1C	0x0	EINT9_STATUS External INT9 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x05D4			Register Name: PK_INT_STA
Bit	Read/Write	Default/Hex	Description
8	R/W1C	0x0	EINT8_STATUS External INT8 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W1C	0x0	EINT7_STATUS External INT7 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x05D4			Register Name: PK_INT_STA
Bit	Read/Write	Default/Hex	Description
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

18.14.6.144 0x05D8 PK External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x05D8			Register Name: PK_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n. The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select. 0: RTC_32K 1: SYS_CLK24M

18.14.6.145 0x05F0 PK SECURE Configure Register (Default Value: 0x0000_0000)

Offset: 0x05F0			Register Name: PK_SECURE
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PORT31_SEC_SEL Port31 secure select. 0: Not secure 1: Secure
30	R/W	0x0	PORT30_SEC_SEL Port30 secure select. 0: Not secure 1: Secure
29	R/W	0x0	PORT29_SEC_SEL Port29 secure select. 0: Not secure 1: Secure
28	R/W	0x0	PORT28_SEC_SEL Port28 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x05F0			Register Name: PK_SECURE
Bit	Read/Write	Default/Hex	Description
27	R/W	0x0	PORT27_SEC_SEL Port27 secure select. 0: Not secure 1: Secure
26	R/W	0x0	PORT26_SEC_SEL Port26 secure select. 0: Not secure 1: Secure
25	R/W	0x0	PORT25_SEC_SEL Port25 secure select. 0: Not secure 1: Secure
24	R/W	0x0	PORT24_SEC_SEL Port24 secure select. 0: Not secure 1: Secure
23	R/W	0x0	PORT23_SEC_SEL Port23 secure select. 0: Not secure 1: Secure
22	R/W	0x0	PORT22_SEC_SEL Port22 secure select. 0: Not secure 1: Secure
21	R/W	0x0	PORT21_SEC_SEL Port21 secure select. 0: Not secure 1: Secure
20	R/W	0x0	PORT20_SEC_SEL Port20 secure select. 0: Not secure 1: Secure
19	R/W	0x0	PORT19_SEC_SEL Port19 secure select. 0: Not secure 1: Secure
18	R/W	0x0	PORT18_SEC_SEL Port18 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x05F0			Register Name: PK_SECURE
Bit	Read/Write	Default/Hex	Description
17	R/W	0x0	PORT17_SEC_SEL Port17 secure select. 0: Not secure 1: Secure
16	R/W	0x0	PORT16_SEC_SEL Port16 secure select. 0: Not secure 1: Secure
15	R/W	0x0	PORT15_SEC_SEL Port15 secure select. 0: Not secure 1: Secure
14	R/W	0x0	PORT14_SEC_SEL Port14 secure select. 0: Not secure 1: Secure
13	R/W	0x0	PORT13_SEC_SEL Port13 secure select. 0: Not secure 1: Secure
12	R/W	0x0	PORT12_SEC_SEL Port12 secure select. 0: Not secure 1: Secure
11	R/W	0x0	PORT11_SEC_SEL Port11 secure select. 0: Not secure 1: Secure
10	R/W	0x0	PORT10_SEC_SEL Port10 secure select. 0: Not secure 1: Secure
9	R/W	0x0	PORT9_SEC_SEL Port9 secure select. 0: Not secure 1: Secure
8	R/W	0x0	PORT8_SEC_SEL Port8 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x05F0			Register Name: PK_SECURE
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	PORT7_SEC_SEL Port7 secure select. 0: Not secure 1: Secure
6	R/W	0x0	PORT6_SEC_SEL Port6 secure select. 0: Not secure 1: Secure
5	R/W	0x0	PORT5_SEC_SEL Port5 secure select. 0: Not secure 1: Secure
4	R/W	0x0	PORT4_SEC_SEL Port4 secure select. 0: Not secure 1: Secure
3	R/W	0x0	PORT3_SEC_SEL Port3 secure select. 0: Not secure 1: Secure
2	R/W	0x0	PORT2_SEC_SEL Port2 secure select. 0: Not secure 1: Secure
1	R/W	0x0	PORT1_SEC_SEL Port1 secure select. 0: Not secure 1: Secure
0	R/W	0x0	PORT0_SEC_SEL Port0 secure select. 0: Not secure 1: Secure

18.14.7 S_GPIO Register Description

18.14.7.1 0x0000 PL Configure Register 0 (Default Value: 0xFFFF-FFFF)

Offset: 0x0000			Register Name: PL_CFG0
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: PL_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PL7_SELECT PL7 Select. 0000: Input 0001: Output 0010: S-JTAG-DI 0011: S-UART0-RX 0100: S-SPI0-MISO 0101: Reserved 0110: S-PWM0-5 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT7 1111: IO Disable
27:24	R/W	0xF	PL6_SELECT PL6 Select. 0000: Input 0001: Output 0010: S-JTAG-DO 0011: S-UART0-TX 0100: S-SPI0-MOSI 0101: S-IR-RX 0110: S-PWM0-4 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT6 1111: IO Disable
23:20	R/W	0xF	PL5_SELECT PL5 Select. 0000: Input 0001: Output 0010: S-JTAG-CK 0011: S-TWI2-SDA 0100: S-SPI0-CLK 0101: Reserved 0110: S-PWM0-3 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT5 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: PL_CFG0
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0xF	PL4_SELECT PL4 Select. 0000: Input 0001: Output 0010: S-JTAG-MS 0011: S-TWI2-SCK 0100: S-SPI0-CS0 0101: S-IR-RX 0110: S-PWM0-2 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT4 1111: IO Disable
15:12	R/W	0xF	PL3_SELECT PL3 Select. 0000: Input 0001: Output 0010: S-UART1-RX 0011: S-UART0-RX 0100: S-TWI1-SCK 0101: S-IR-RX 0110: S-PWM0-1 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT3 1111: IO Disable
11:8	R/W	0xF	PL2_SELECT PL2 Select. 0000: Input 0001: Output 0010: S-UART1-TX 0011: S-UART0-TX 0100: S-TWI1-SDA 0101: Reserved 0110: S-PWM0-0 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT2 1111: IO Disable
7:4	R/W	0xF	PL1_SELECT PL1 Select. 0000: Input 0001: Output 0010: S-TWI0-SDA 0011: S-TWI1-SDA 0100: S-TWI2-SDA 0101: S-IR-RX 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT1 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: PL_CFG0
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xF	PL0_SELECT PL0 Select. 0000: Input 0001: Output 0010: S-TWI0-SCK 0011: S-TWI1-SCK 0100: S-TWI2-SCK 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT0 1111: IO Disable

18.14.7.2 0x0004 PL Configure Register 1 (Default Value: 0x00FF_FFFF)

Offset: 0x0004			Register Name: PL_CFG1
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:20	R/W	0xF	PL13_SELECT PL13 Select. 0000: Input 0001: Output 0010: S-UART1-RX 0011: S-TWI1-SDA 0100: S-TWI2-SDA 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT13 1111: IO Disable
19:16	R/W	0xF	PL12_SELECT PL12 Select. 0000: Input 0001: Output 0010: S-UART1-TX 0011: S-TWI1-SCK 0100: S-TWI2-SCK 0101: S-IR-RX 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT12 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: PL_CFG1
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0xF	PL11_SELECT PL11 Select. 0000: Input 0001: Output 0010: S-UART0-RX 0011: S-TWI2-SDA 0100: S-UART1-RX 0101: S-IR-RX 0110: S-PWM0-9 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT11 1111: IO Disable
11:8	R/W	0xF	PL10_SELECT PL10 Select. 0000: Input 0001: Output 0010: S-UART0-TX 0011: S-TWI2-SCK 0100: S-UART1-TX 0101: Reserved 0110: S-PWM0-8 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT10 1111: IO Disable
7:4	R/W	0xF	PL9_SELECT PL9 Select. 0000: Input 0001: Output 0010: S-TWI1-SDA 0011: S-UART1-RX 0100: S-TWI0-SDA 0101: S-TWI2-SDA 0110: S-PWM0-7 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT9 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0004			Register Name: PL_CFG1
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xF	PL8_SELECT PL8 Select. 0000: Input 0001: Output 0010: S-TWI1-SCK 0011: S-UART1-TX 0100: S-TWI0-SCK 0101: S-TWI2-SCK 0110: S-PWM0-6 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT8 1111: IO Disable

18.14.7.3 0x0010 PL Data Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: PL_DAT
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0	PL_DAT PL Data. If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

18.14.7.4 0x0014 PL Multi-Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x0014			Register Name: PL_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PL7_DRV PL7 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PL6_DRV PL6 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: PL_DRV0
Bit	Read/Write	Default/Hex	Description
23:22	/	/	/
21:20	R/W	0x1	PL5_DRV PL5 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PL4_DRV PL4 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PL3_DRV PL3 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PL2_DRV PL2 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PL1_DRV PL1 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PL0_DRV PL0 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

18.14.7.5 0x0018 PL Multi-Driving Register 1 (Default Value: 0x0011_1111)

Offset: 0x0018			Register Name: PL_DRV1
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:20	R/W	0x1	PL13_DRV PL13 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0018			Register Name: PL_DRV1
Bit	Read/Write	Default/Hex	Description
17:16	R/W	0x1	PL12_DRV PL12 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PL11_DRV PL11 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PL10_DRV PL10 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PL9_DRV PL9 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PL8_DRV PL8 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

18.14.7.6 0x0024 PL Pull Register 0 (Default Value: 0x0000_0005)

Offset: 0x0024			Register Name: PL_PUL0
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:26	R/W	0x0	PL13_PULL PL13 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PL12_PULL PL12 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0024			Register Name: PL_PUL0
Bit	Read/Write	Default/Hex	Description
23:22	R/W	0x0	PL11_PULL PL11 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PL10_PULL PL10 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PL9_PULL PL9 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PL8_PULL PL8 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PL7_PULL PL7 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PL6_PULL PL6 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PL5_PULL PL5 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PL4_PULL PL4 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PL3_PULL PL3 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PL2_PULL PL2 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0024			Register Name: PL_PUL0
Bit	Read/Write	Default/Hex	Description
3:2	R/W	0x1	PL1_PULL PL1 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x1	PL0_PULL PL0 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

18.14.7.7 0x0030 PM Configure Register 0 (Default Value: 0x00FF_FFFF)

Offset: 0x0030			Register Name: PM_CFG0
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:20	R/W	0xF	PM5_SELECT PM5 Select. 0000: Input 0001: Output 0010: S-UART0-RX 0011: S-TWI2-SDA 0100: S-TWI1-SDA 0101: S-UART1-RX 0110: S-PWM0-1 0111: S-IR-RX 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PM-EINT5 1111: IO Disable
19:16	R/W	0xF	PM4_SELECT PM4 Select. 0000: Input 0001: Output 0010: S-UART0-TX 0011: S-TWI2-SCK 0100: S-TWI1-SCK 0101: S-UART1-TX 0110: S-PWM0-0 0111: S-IR-RX 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PM-EINT4 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0030			Register Name: PM_CFG0
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0xF	PM3_SELECT PM3 Select. 0000: Input 0001: Output 0010: S-JTAG-DI 0011: S-SPI0-MISO 0100: S-UART0-RX 0101: S-UART1-RX 0110: S-PWM0-5 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PM-EINT3 1111: IO Disable
11:8	R/W	0xF	PM2_SELECT PM2 Select. 0000: Input 0001: Output 0010: S-JTAG-DO 0011: S-SPI0-MOSI 0100: S-UART0-TX 0101: S-UART1-TX 0110: S-PWM0-4 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PM-EINT2 1111: IO Disable
7:4	R/W	0xF	PM1_SELECT PM1 Select. 0000: Input 0001: Output 0010: S-JTAG-CK 0011: S-SPI0-CLK 0100: S-RJTAG-CK 0101: S-TWI1-SDA 0110: S-PWM0-3 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PM-EINT1 1111: IO Disable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0030			Register Name: PM_CFG0
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xF	PM0_SELECT PM0 Select. 0000: Input 0001: Output 0010: S-JTAG-MS 0011: S-SPI0-CS0 0100: S-RJTAG-MS 0101: S-TWI1-SCK 0110: S-PWM0-2 0111: S-IR-RX 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PM-EINT0 1111: IO Disable

18.14.7.8 0x0040 PM Data Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: PM_DAT
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5:0	R/W	0	PM_DAT PM Data. If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

18.14.7.9 0x0044 PM Multi-Driving Register 0 (Default Value: 0x0011_1111)

Offset: 0x0044			Register Name: PM_DRV0
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:20	R/W	0x1	PM5_DRV PM5 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PM4_DRV PM4 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0044			Register Name: PM_DRV0
Bit	Read/Write	Default/Hex	Description
15:14	/	/	/
13:12	R/W	0x1	PM3_DRV PM3 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PM2_DRV PM2 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PM1_DRV PM1 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PM0_DRV PM0 Multi-driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

18.14.7.10 0x0054 PM Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: PM_PUL0
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:10	R/W	0x0	PM5_PULL PM5 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PM4_PULL PM4 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PM3_PULL PM3 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0054			Register Name: PM_PUL0
Bit	Read/Write	Default/Hex	Description
5:4	R/W	0x0	PM2_PULL PM2 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PM1_PULL PM1 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PM0_PULL PM0 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

18.14.7.11 0x0200 PL External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: PL_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0200			Register Name: PL_INT_CFG0
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0x0	EINT4_CFG External INT4 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.14.7.12 0x0204 PL External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0204			Register Name: PL_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:20	R/W	0x0	EINT13_CFG External INT13 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0204			Register Name: PL_INT_CFG1
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0x0	EINT9_CFG External INT9 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

18.14.7.13 0x0210 PL External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: PL_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R/W	0x0	EINT13_CTL External INT13 Enable. 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable. 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable. 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0210			Register Name: PL_INT_CTL
Bit	Read/Write	Default/Hex	Description
9	R/W	0x0	EINT9_CTL External INT9 Enable. 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable. 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable. 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable. 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable. 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable. 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable. 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable. 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable. 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.14.7.14 0x0214 PL External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0214			Register Name: PL_INT_STA
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R/W1C	0x0	EINT13_STATUS External INT13 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W1C	0x0	EINT12_STATUS External INT12 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W1C	0x0	EINT11_STATUS External INT11 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W1C	0x0	EINT10_STATUS External INT10 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W1C	0x0	EINT9_STATUS External INT9 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W1C	0x0	EINT8_STATUS External INT8 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W1C	0x0	EINT7_STATUS External INT7 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0214			Register Name: PL_INT_STA
Bit	Read/Write	Default/Hex	Description
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

18.14.7.15 0x0218 PL External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0218			Register Name: PL_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0218			Register Name: PL_INT_DEB
Bit	Read/Write	Default/Hex	Description
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n. The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select. 0: RTC_32K 1: SYS_CLK24M

18.14.7.16 0x0220 PM External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0220			Register Name: PM_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:20	R/W	0x0	EINT5_CFG External INT5 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0220			Register Name: PM_INT_CFG0
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0x0	EINT2_CFG External INT2 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

18.14.7.17 0x0230 PM External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: PM_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	EINT5_CTL External INT5 Enable. 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable. 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0230			Register Name: PM_INT_CTL
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	EINT3_CTL External INT3 Enable. 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable. 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable. 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable. 0: Disable 1: Enable

18.14.7.18 0x0234 PM External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: PM_INT_STA
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0234			Register Name: PM_INT_STA
Bit	Read/Write	Default/Hex	Description
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

18.14.7.19 0x0238 PM External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0238			Register Name: PM_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n. The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select. 0: RTC_32K 1: SYS_CLK24M

18.14.7.20 0x0340 GPIO Group Withstand Voltage Mode Select Register (Default Value: 0x0000_000A)

Offset: 0x0340			Register Name: SGPIO_POW_MOD_SEL
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0340			Register Name: SGPIO_POW_MOD_SEL
Bit	Read/Write	Default/Hex	Description
3:2	R/W	0x2	PM_PWR_MOD_SEL PM_POWER MODE SELECT. 00: 3.3V 01: auto 10: 3.3V 11: 1.8V
1:0	R/W	0x2	PL_PWR_MOD_SEL PL_POWER MODE SELECT. 00: 3.3V 01: auto 10: 3.3V 11: 1.8V

18.14.7.21 0x0348 GPIO Group Power Value Register (Default Value: 0x0000_0005)

Offset: 0x0348			Register Name: SGPIO_POW_VAL
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:2	R	0x1	PM_PWR_VAL PM_PORT POWER VALUE. 00: Invalid 01: Invalid 10: 3.3V 11: 1.8V
1:0	R	0x1	PL_PWR_VAL PL_PORT POWER VALUE. 00: Invalid 01: Invalid 10: 3.3V 11: 1.8V

18.14.7.22 0x0400 PL SECURE Configure Register (Default Value: 0x0000_0000)

Offset: 0x0400			Register Name: PL_SECURE
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PORT31_SEC_SEL Port31 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0400			Register Name: PL_SECURE
Bit	Read/Write	Default/Hex	Description
30	R/W	0x0	PORT30_SEC_SEL Port30 secure select. 0: Not secure 1: Secure
29	R/W	0x0	PORT29_SEC_SEL Port29 secure select. 0: Not secure 1: Secure
28	R/W	0x0	PORT28_SEC_SEL Port28 secure select. 0: Not secure 1: Secure
27	R/W	0x0	PORT27_SEC_SEL Port27 secure select. 0: Not secure 1: Secure
26	R/W	0x0	PORT26_SEC_SEL Port26 secure select. 0: Not secure 1: Secure
25	R/W	0x0	PORT25_SEC_SEL Port25 secure select. 0: Not secure 1: Secure
24	R/W	0x0	PORT24_SEC_SEL Port24 secure select. 0: Not secure 1: Secure
23	R/W	0x0	PORT23_SEC_SEL Port23 secure select. 0: Not secure 1: Secure
22	R/W	0x0	PORT22_SEC_SEL Port22 secure select. 0: Not secure 1: Secure
21	R/W	0x0	PORT21_SEC_SEL Port21 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0400			Register Name: PL_SECURE
Bit	Read/Write	Default/Hex	Description
20	R/W	0x0	PORT20_SEC_SEL Port20 secure select. 0: Not secure 1: Secure
19	R/W	0x0	PORT19_SEC_SEL Port19 secure select. 0: Not secure 1: Secure
18	R/W	0x0	PORT18_SEC_SEL Port18 secure select. 0: Not secure 1: Secure
17	R/W	0x0	PORT17_SEC_SEL Port17 secure select. 0: Not secure 1: Secure
16	R/W	0x0	PORT16_SEC_SEL Port16 secure select. 0: Not secure 1: Secure
15	R/W	0x0	PORT15_SEC_SEL Port15 secure select. 0: Not secure 1: Secure
14	R/W	0x0	PORT14_SEC_SEL Port14 secure select. 0: Not secure 1: Secure
13	R/W	0x0	PORT13_SEC_SEL Port13 secure select. 0: Not secure 1: Secure
12	R/W	0x0	PORT12_SEC_SEL Port12 secure select. 0: Not secure 1: Secure
11	R/W	0x0	PORT11_SEC_SEL Port11 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0400			Register Name: PL_SECURE
Bit	Read/Write	Default/Hex	Description
10	R/W	0x0	PORT10_SEC_SEL Port10 secure select. 0: Not secure 1: Secure
9	R/W	0x0	PORT9_SEC_SEL Port9 secure select. 0: Not secure 1: Secure
8	R/W	0x0	PORT8_SEC_SEL Port8 secure select. 0: Not secure 1: Secure
7	R/W	0x0	PORT7_SEC_SEL Port7 secure select. 0: Not secure 1: Secure
6	R/W	0x0	PORT6_SEC_SEL Port6 secure select. 0: Not secure 1: Secure
5	R/W	0x0	PORT5_SEC_SEL Port5 secure select. 0: Not secure 1: Secure
4	R/W	0x0	PORT4_SEC_SEL Port4 secure select. 0: Not secure 1: Secure
3	R/W	0x0	PORT3_SEC_SEL Port3 secure select. 0: Not secure 1: Secure
2	R/W	0x0	PORT2_SEC_SEL Port2 secure select. 0: Not secure 1: Secure
1	R/W	0x0	PORT1_SEC_SEL Port1 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0400			Register Name: PL_SECURE
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	PORT0_SEC_SEL Port0 secure select. 0: Not secure 1: Secure

18.14.7.23 0x0404 PM SECURE Configure Register (Default Value: 0x0000_0000)

Offset: 0x0404			Register Name: PM_SECURE
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PORT31_SEC_SEL Port31 secure select. 0: Not secure 1: Secure
30	R/W	0x0	PORT30_SEC_SEL Port30 secure select. 0: Not secure 1: Secure
29	R/W	0x0	PORT29_SEC_SEL Port29 secure select. 0: Not secure 1: Secure
28	R/W	0x0	PORT28_SEC_SEL Port28 secure select. 0: Not secure 1: Secure
27	R/W	0x0	PORT27_SEC_SEL Port27 secure select. 0: Not secure 1: Secure
26	R/W	0x0	PORT26_SEC_SEL Port26 secure select. 0: Not secure 1: Secure
25	R/W	0x0	PORT25_SEC_SEL Port25 secure select. 0: Not secure 1: Secure
24	R/W	0x0	PORT24_SEC_SEL Port24 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0404			Register Name: PM_SECURE
Bit	Read/Write	Default/Hex	Description
23	R/W	0x0	PORT23_SEC_SEL Port23 secure select. 0: Not secure 1: Secure
22	R/W	0x0	PORT22_SEC_SEL Port22 secure select. 0: Not secure 1: Secure
21	R/W	0x0	PORT21_SEC_SEL Port21 secure select. 0: Not secure 1: Secure
20	R/W	0x0	PORT20_SEC_SEL Port20 secure select. 0: Not secure 1: Secure
19	R/W	0x0	PORT19_SEC_SEL Port19 secure select. 0: Not secure 1: Secure
18	R/W	0x0	PORT18_SEC_SEL Port18 secure select. 0: Not secure 1: Secure
17	R/W	0x0	PORT17_SEC_SEL Port17 secure select. 0: Not secure 1: Secure
16	R/W	0x0	PORT16_SEC_SEL Port16 secure select. 0: Not secure 1: Secure
15	R/W	0x0	PORT15_SEC_SEL Port15 secure select. 0: Not secure 1: Secure
14	R/W	0x0	PORT14_SEC_SEL Port14 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0404			Register Name: PM_SECURE
Bit	Read/Write	Default/Hex	Description
13	R/W	0x0	PORT13_SEC_SEL Port13 secure select. 0: Not secure 1: Secure
12	R/W	0x0	PORT12_SEC_SEL Port12 secure select. 0: Not secure 1: Secure
11	R/W	0x0	PORT11_SEC_SEL Port11 secure select. 0: Not secure 1: Secure
10	R/W	0x0	PORT10_SEC_SEL Port10 secure select. 0: Not secure 1: Secure
9	R/W	0x0	PORT9_SEC_SEL Port9 secure select. 0: Not secure 1: Secure
8	R/W	0x0	PORT8_SEC_SEL Port8 secure select. 0: Not secure 1: Secure
7	R/W	0x0	PORT7_SEC_SEL Port7 secure select. 0: Not secure 1: Secure
6	R/W	0x0	PORT6_SEC_SEL Port6 secure select. 0: Not secure 1: Secure
5	R/W	0x0	PORT5_SEC_SEL Port5 secure select. 0: Not secure 1: Secure
4	R/W	0x0	PORT4_SEC_SEL Port4 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0404			Register Name: PM_SECURE
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	PORT3_SEC_SEL Port3 secure select. 0: Not secure 1: Secure
2	R/W	0x0	PORT2_SEC_SEL Port2 secure select. 0: Not secure 1: Secure
1	R/W	0x0	PORT1_SEC_SEL Port1 secure select. 0: Not secure 1: Secure
0	R/W	0x0	PORT0_SEC_SEL Port0 secure select. 0: Not secure 1: Secure

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.15 LEDC

18.15.1 Overview

The LEDC is used to control the external LED lamp.

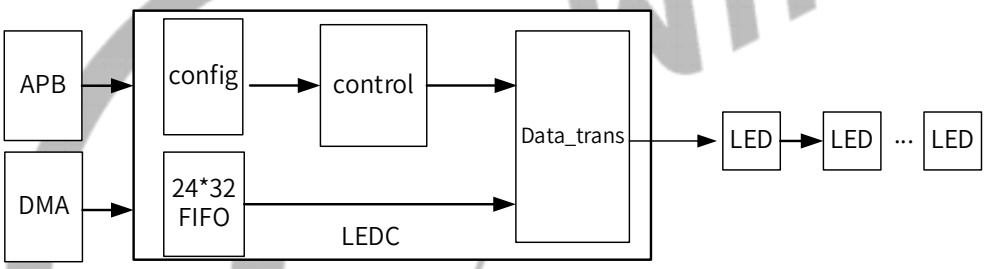
The LEDC has the following features:

- Configurable LED output high-/low-level width
- Configurable LED reset time
- LEDC data supports DMA configuration mode and CPU configuration mode
- Maximum 1024 LEDs serial connect
- LED data transfer rate up to 800 kbit/s
- Configurable RGB display mode

18.15.2 Block Diagram

The following figure shows a block diagram of the LEDC.

Figure 18-78 LEDC Block Diagram



LEDC contains the following sub-blocks:

Table 18-42 LEDC Sub-blocks

Sub-block	Description
Config	Register configuration.
Control	It controls the timing and status of LEDC.
FIFO	The size is up to 32 layer*24bit.
Data_trans	The input data is transferred to 0 and 1.

18.15.3 Clock Sources

The following table describes the clock sources of LEDC. For clock setting, configurations, and gating information, refer to the section CCU.

Module	Clock Sources	Description
LEDC	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

	PERI0_600M	Its frequency is 600 MHz by default.
	DCXO	The external high-frequency crystal oscillator. Its frequency is 26 MHz.

18.15.4 External Signals

The following table describes the external signals of the LEDC.

Table 18-43 LEDC External Signals

Signal Name	Description	Type
LEDC	Intelligent Control LED Signal Output	O

18.15.5 Functional Description

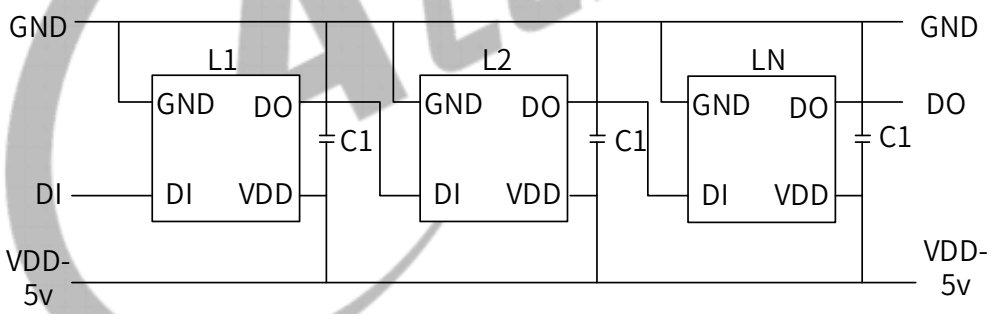
18.15.5.1 LED Data Input

The RGB mode of LEDC data is configurable. By default, the data is sent in GRB order, and the higher bit is transmitted first. The following tables and figure show LED input data structure and code, and data input time and mode.

Figure 18-79 LED Input Data Structure

G7	G6	G5	G4	G3	G2	G1	G0	R7	R6	R5	R4	R3	R2	R1	R0	B7	B6	B5	B4	B3	B2	B1	B0

Figure 18-80 LED Typical Circuit



C1 is the filter capacitor of LED lights, which is usually set as 100NF.

Figure 18-81 LED Input Data Code

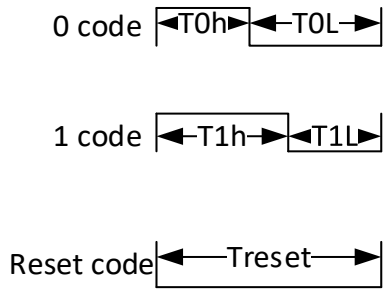


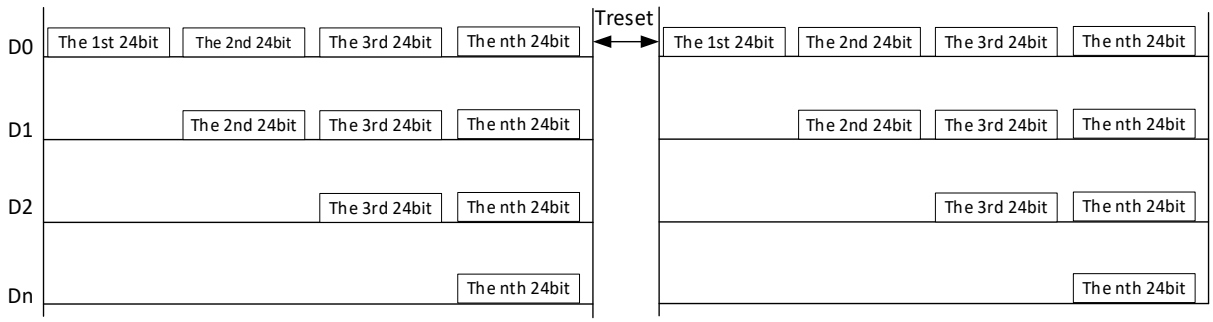
Table 18-44 LED Data Input Time

T0H	0 code, high-level time	220 ns to 380 ns

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

T0L	0 code, low-level time	580 ns to 1.6 us
T1H	1 code, high-level time	580 ns to 1.6 us
T1L	1 code, low-level time	220 ns to 420 ns
RESET	Frame unit, low-level time	> 280 us

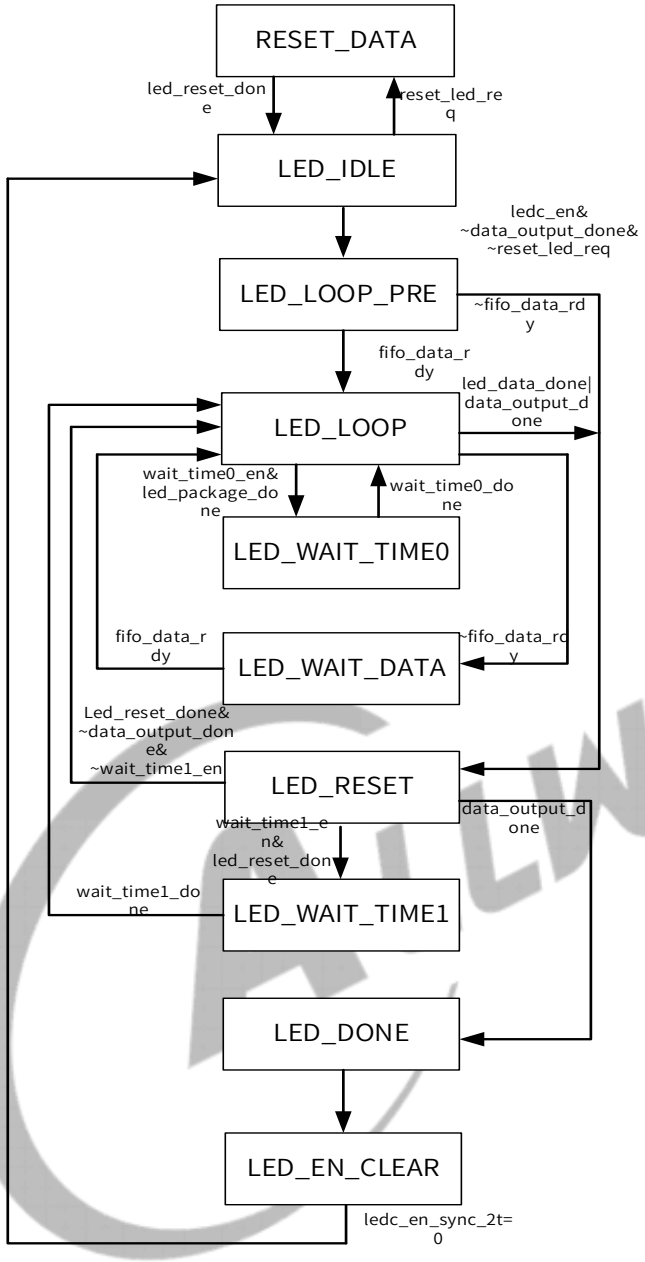
Figure 18-82 LED Data Transfer Mode



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.15.5.2 LED Control State Machine

The following figure shows the LED internal control state machine.



State Name	Description
LED_IDLE	LEDC idle state. LEDC outputs low level by default.
LED_LOOP_PRE	Intermediate state. LEDC detects whether there is data before data transfer.
RESET_DATA	LEDC send the request of data reset to LED.
LED_LOOP	LEDC cyclic output data state. It will output LED_NUM*24 data based on the connected LED number.
LED_WAIT_TIME0	The interval between two LED data. When led_wait_time0_en is enabled, automatically insert the low level waiting time by default after led_wait_time0_en is enabled.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

State Name	Description
LED_WAIT_DATA	When LEDC doesn t finish data transfer yet and the internal data FIFO is null, LEDC will enter this state.
LED_RESET	When LEDC finishes a data package transfer, a low level of reset time will be auto inserted.
LED_WAIT_TIME1	The interval between LED frame data. After led_wait_time1_en is enabled, the waiting time of low level will be auto inserted by default.
LED_DONE	Intermediate state. It indicates the data transfer has finished.
LED_EN_CLEAR	It indicates the LEDC_EN has synchronize from hclk to led_clk. At this time, the LEDC_EN has been cleared to 0.

18.15.5.3 LEDC Output Timing

The following figures show the output timing diagrams of LEDC package.

Figure 18-83 LEDC Package Output Timing Diagram

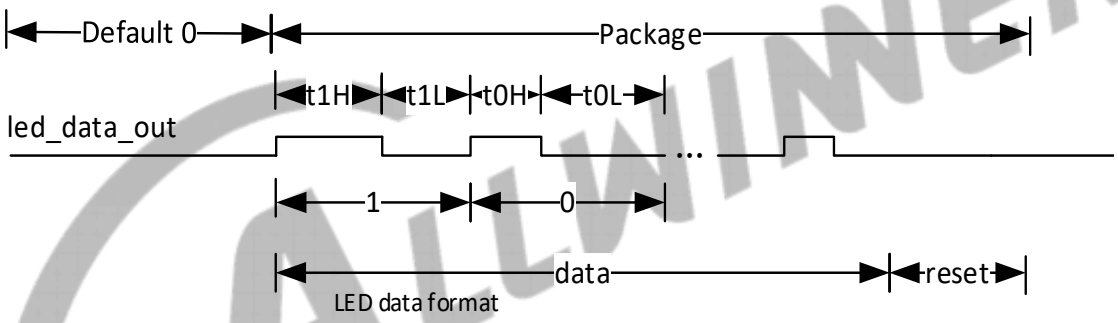
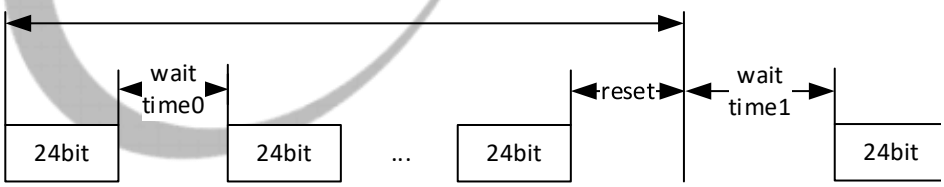


Figure 18-84 LEDC 1-frame Output Timing Diagram



18.15.5.4 LEDC Data Transfer

The LEDC supports DMA data transfer mode and CPU data transfer mode through APB bus.

- Data transfer in DMA mode

When the valid space of internal FIFO is greater than the setting FIFO space threshold, the LEDC will send the DMA_REQ to require DMA to transfer data from DRAM to LEDC. The maximum data

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

transfer size in DMA mode is 16 words. (The internal FIFO level is 32.) The DMA data transfer mode is set by LEDC_DMA_EN.

- Data transfer in CPU mode

When the valid space of internal FIFO is greater than the setting FIFO space threshold, the LEDC will send LEDC_CPUREQ_INT to require CPU to transfer data to LEDC. The transfer data size in CPU mode is controlled by software. The internal FIFO destination address is 0x06700014. The data width is 32-bit. (The lower 24-bit is valid.)

18.15.5.5 LEDC Interrupt

Interrupt Name	Description
FIFO_OVERFLOW_INT	FIFO overflow interrupt. The amount of written data exceeds the maximum storage space of LED FIFO. The LEDC is in the data loss state. At this time, the anomaly should be handled by software as follows. a) Query the LED_FIFO_DATA_REG to determine which data has been stored in the internal FIFO of LEDC. Resend the overflow data to LEDC. b) Soft_reset the LEDC to refresh all the data.
WAITDATA_TIMEOUT_INT	Wait Data Timeout Interrupt When internal FIFO of LEDC cannot get data resulting from some anomaly, the timeout interrupt will be enabled after the led_wait_data_time. At this time, the LEDC is in WAIT_DATA state, and the LEDC will output the level configured by the LED_PAUSE_LEVEL. During the wait_data, the LEDC will continue to transfer data. In this condition, if LEDC waiting time exceeds the LED reset time, it is as if the LEDC has sent a reset operation. The LED will enter refreshing state by mistake, and the data hasn t been completely sent.
FIFO_CPUREQ_INT	FIFO Request CPU Data Interrupt When FIFO data amount is less than the threshold, the interrupt will be reported to the CPU.
LEDC_TRANS_FINISH_INT	Data Transfer Finish Interrupt It indicates that the configured data of total_data_length finishes transfer.

LEDC interrupt usage scenario:

- CPU mode

The software can enable GLOBAL_INT_EN, FIFO_CPUREQ_INT_EN, WAITDATA_TIMEOUT_INT_EN, FIFO_OVERFLOW_INT_EN, and LED_TRANS_FINISH_INT_EN in the LEDC_INTERRUPT_CTRL_REG, and cooperate with LEDC_FIFO_TRIG_LEVEL in the LEDC_DMA_CTRL_REG to use. When

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

FIFO_CPUREQ_INT is set to 1, the software can configure data of LEDC_FIFO_TRIG_LEVEL to LEDC.

- DMA mode

The software can enable GLOBAL_INT_EN, WAITDATA_TIMEOUT_INT_EN, FIFO_OVERFLOW_INT_EN, and LEDC_TRANS_FINISH_INT_EN in the LEDC_INTERRUPT_CTRL_REG, and cooperate with LEDC_FIFO_TRIG_LEVEL in the LEDC_DMA_CTRL_REG to use. After receiving LEDC DMA_REQ, DMA can transfer data of LEDC_FIFO_TRIG_LEVEL to LEDC.

18.15.6 Programming Guidelines

18.15.6.1 Normal Configuration

Step 1 Configure LEDC_CLK and bus pclk as described in the section CCU.

Step 2 Configure the LEDC data to be written.

Step 3 Configure 0-code, 1-code, reset time, LEDC wait time, and the number of connected LED and the threshold of DMA transferred data by setting LED_T01_TIMING_CTRL_REG, LEDC_DATA_FINISH_CNT_REG, LED_RESET_TIMING_CTRL_REG, LEDC_WAIT_TIME0_CTRL_REG, LEDC_DMA_CTRL_REG, LEDC_INTERRUPT_CTRL_REG.

Step 4 Enable LEDC_EN through LEDC_CTRL_REG. The LEDC will start outputting data.

Step 5 When the LED_TRANS_FINISH_INT_EN in LEDC_INTERRUPT_CTRL_REG is enabled, it indicates the configured data has been transferred. Then, LED_EN will be set to 0, and the read/write point of LEDC FIFO is cleared.

Step 6 Repeat the first four steps to start a new round of configuration, and enable LEDC_EN. The LEDC will restart data transfer.

18.15.6.2 Abnormal Processing

WAITDATA_TIMEOUT

Step 1 When a WAITDATA_TIMEOUT_INT occurs, it indicates the internal FIFO data request of LEDC doesn't obtain a response. In this condition, if the default output level is low, the external LED device will mistakenly believe it is a reset operation, resulting in refreshing LED data by mistake.

Step 2 Write 1 to LEDC_SOFT_RESET in the LEDC_CTRL_REG to reset the LEDC by software. Afterwards, LEDC_EN will be automatically disabled. All the status registers will go back to the idle status. LEDC FIFO read &write point are cleared to 0. LEDC The interrupts are cleared.

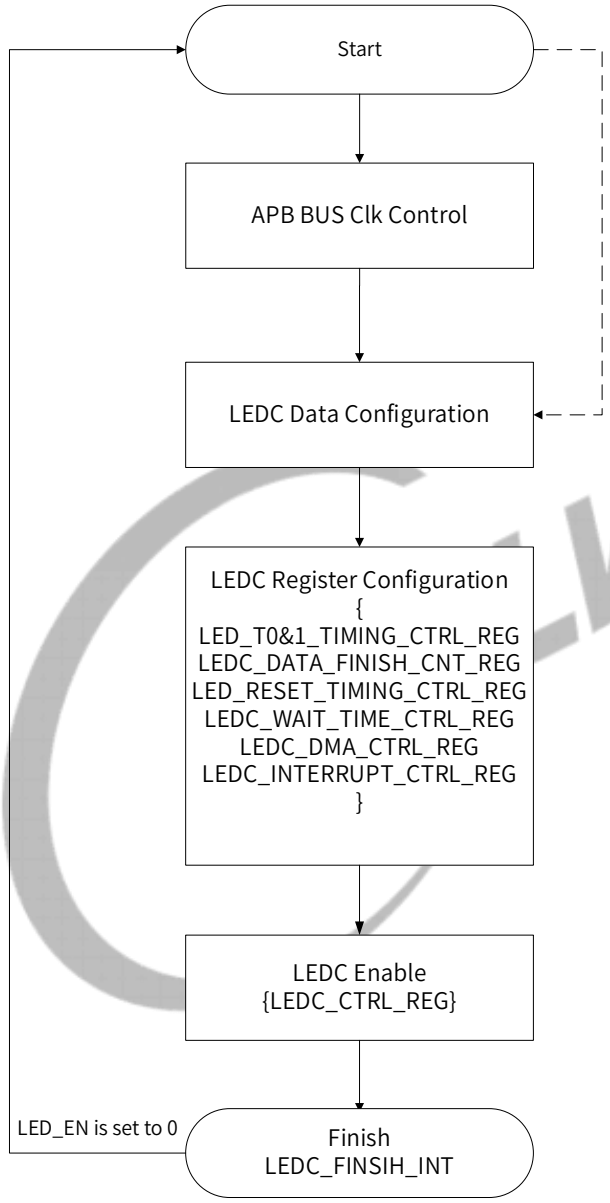
Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 3 Write 1 to RESET_LED_EN in the LEDC_CTRL_REG. The LEDC will send the reset order to ensure the external LED lights stay in the right status.

Step 4 Read the RESET_LED_EN in the LEDC_CTRL_REG. 1 indicates that LEDC hasn't sent the reset order. 0 indicates that LEDC has sent the reset order.

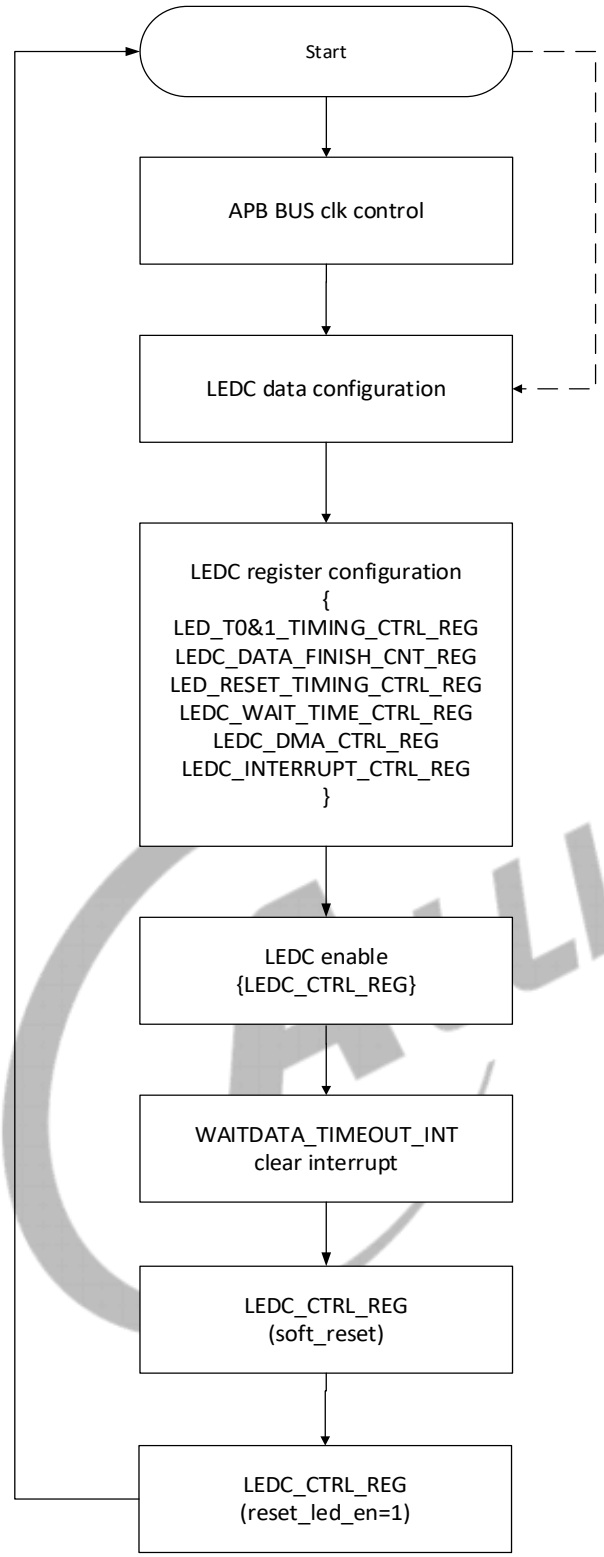
Step 5 When the LEDC reset operation finishes, the LEDC will restart the configuration of data and registers. The data transfer starts again.

Figure 18-85 LEDC Normal Configuration Flow



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 18-86 LEDC Timeout Abnormal Processing Flow



FIFO_OVERFLOW

Step 1 When FIFO_OVERFLOW_INT occurs, it indicates the data configured by software exceeds the LEDC FIFO space, at this time the redundant data will be lost.

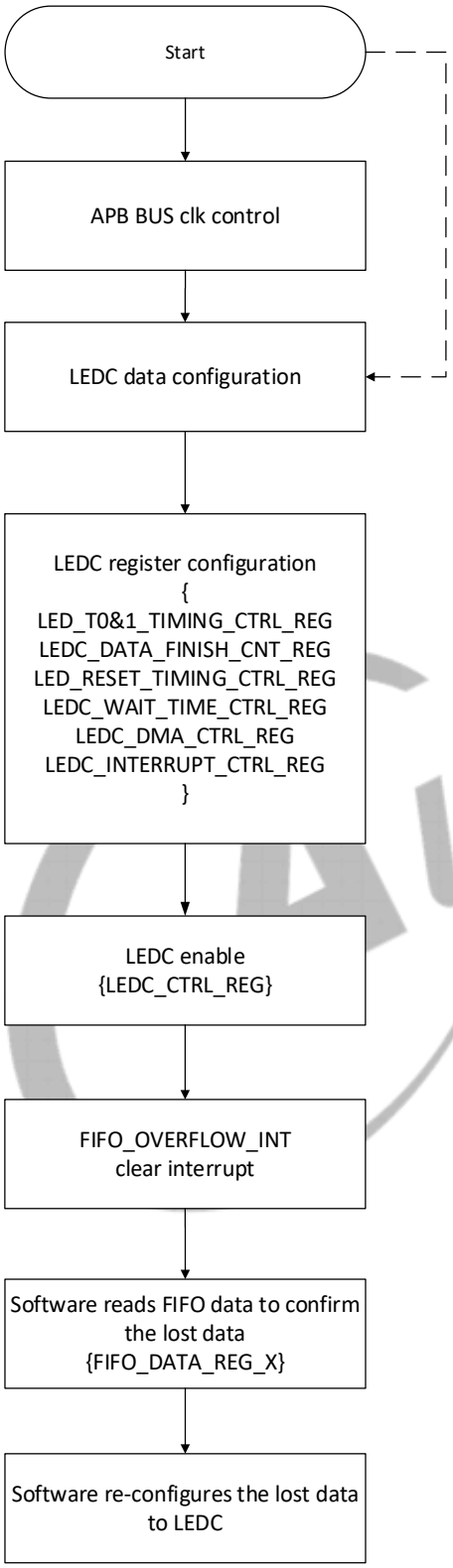
Step 2 Read the data in LEDC_FIFO_DATA_X to confirm the lost data.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step 3 Re-configure the lost data to the LEDC.

Step 4 Refer to the WAITDATA_TIMEOUT processing flow above if soft_reset is needed.

Figure 18-87 FIFO Overflow Abnormal Processing Flow



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.15.7 Register List

Module Name	Base Address
LEDC	0x02520000

Register Name	Offset	Description
LEDC_CTRL_REG	0x0000	LEDC Control Register
LED_T01_TIMING_CTRL_REG	0x0004	LED T0 & T1 Timing Control Register
LEDC_DATA_FINISH_CNT_REG	0x0008	LEDC Data Finish Counter Register
LED_RESET_TIMING_CTRL_REG	0x000C	LED Reset Timing Control Register
LEDC_WAIT_TIME0_CTRL_REG	0x0010	LEDC Wait Time0 Control Register
LEDC_DATA_REG	0x0014	LEDC Data Register
LEDC_DMA_CTRL_REG	0x0018	LEDC DMA Control Register
LEDC_INT_CTRL_REG	0x001C	LEDC Interrupt Control Register
LEDC_INT_STS_REG	0x0020	LEDC Interrupt Status Register
LEDC_WAIT_TIME1_CTRL_REG	0x0028	LEDC Wait Time1 Control Register
LEDC_FIFO_DATA_REG	0x0030+N*0x04 (N=0~31)	LEDC FIFO Data Register

18.15.8 Register Description

18.15.8.1 0x0000 LEDC Control Register (Default Value: 0x0000_003C)

Offset: 0x0000			Register Name: LEDC_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
30	R/W	0x0	LED_PAUSE_LEVEL The output level in the status of LED_WAIT_TIME0, LED_WAIT_TIME1, and LED_WAIT_DATA when LED is working. 1: High level 0: Low level
29	R/W	0x0	LED_IDLE_LEVEL The default output level when LED doesn t work. 1: High level 0: Low level

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: LEDC_CTRL_REG
Bit	Read/Write	Default/Hex	Description
28:16	R/W	0x0	TOTAL_DATA_LENGTH Total Length of Data to be transferred (range: 0 to 8K, unit: 32-bit, only low 24-bit is valid) It is recommended to be set to an integer multiple of (LED_NUM+1). If TOTAL_DATA_LENGTH is larger than (LED_NUM+1), but non-integer multiple, the last frame of data will transfer data less than (LED_NUM+1).
15:11	/	/	/
10	R/WAC	0x0	RESET_LED_EN LED Reset Enable **Write Operation:** Write 1 by software. The CPU will trigger LEDC to send a reset order to LED. Note: a) Only when LEDC is in IDLE status, the reset will be performed. After the reset finishes, the state machine returns to the IDLE status. Then, the LEDC stays in the IDLE status through SOFT_RESET. b) Read this bit to check if the reset is complete. **Read operation:** 0: LEDC has sent the LED reset order. 1: LEDC doesn t send the LED reset order.
9	/	/	/
8:6	R/W	0x0	LED_RGB_MODE 000 GRB (bypass) 001 GBR 010 RGB 011 RBG 100 BGR 101 BRG c) The data is configured and sent to LEDC by software according to GRB (MSB) mode. Then, the LEDC arrays data and outputs them to the external LED based on the LED_RGB_MODE configuration. d) The configuration in other software input modes is as follows.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: LEDC_CTRL_REG
Bit	Read/Write	Default/Hex	Description

Software Input Mode	Configuration	LEDC Output Mode
GRB	000	GRB
	001	GBR
	010	RGB
	011	RBG
	100	BGR
	101	BRG
GBR	000	GBR
	001	GRB
	010	BGR
	011	BRG
	100	RGB
	101	RBG
RGB	000	RGB
	001	RBG
	010	GRB
	011	GBR
	100	BRG
	101	BGR
RBG	000	RBG
	001	RGB
	010	BRG
	011	BGR
	100	GRB
	101	GBR
BGR	000	BGR
	001	BRG
	010	GBR
	011	GRB
	100	RBG
	101	RGB
BRG	000	BRG
	001	BGR
	010	RBG
	011	RGB
	100	GBR
	101	GRB

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: LEDC_CTRL_REG
Bit	Read/Write	Default/Hex	Description
5	R/W	0x1	LED_MSB_TOP Adjust sequence of the arrayed GRB data 0: LSB 1: MSB (by default)
4	R/W	0x1	LED_MSB_G MSB control for Green data 0: LSB 1: MSB (by default)
3	R/W	0x1	LED_MSB_R MSB control for Red data 0: LSB 1: MSB (by default)
2	R/W	0x1	LED_MSB_B MSB control for Blue data 0: LSB 1: MSB (by default)
1	R/W1C	0x0	LEDC_SOFT_RESET LEDC Soft Reset Write 1 to clear it. In this condition, the LEDC will be reset by software. Consequently, all the internal state register and state machine returns to the idle state. LEDC FIFO read &write point is cleared to 0. The interrupts of LEDC are cleared. 1. LEDC_CTRL_REG (LEDC_EN is cleared to 0). 2. PLL_T0&1_TIMING_CTRL_REG remains unchanged. 3. LEDC_DATA_FINISH_CNT_REG (LEDC_DATA_FINISH_CNT is cleared to 0). 4. LED_RESET_TIMING_CTRL_REG remains unchanged. 5. LEDC_WAIT_TIME_CTRL_REG remains unchanged. 6. LEDC_DMA_CTRL_REG remains unchanged. 7. LEDC_INTERRUPT_CTRL_REG remains unchanged. 8. LEDC_INT_STS _REG is cleared to 0. 9. LEDC_CLK_GATING_REG remains unchanged. 10. LEDC_FIFO_DATA_REG remains unchanged.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: LEDC_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	LEDC_EN LEDC Enable 0: Disable 1: Enable LEDC_EN indicates that the LEDC can start working. When LEDC finishes data transmission or LEDC_SOFT_RESET, LEDC_EN will be auto cleared to 0 by hardware.

18.15.8.2 0x0004 LED T0 & T1 Timing Control Register (Default Value: 0x0286_01D3)

Offset: 0x0004			Register Name: LED_T01_TIMING_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:21	R/W	0x14	T1H_TIME LED T1H time Unit: cycle (24 MHz), T1H_TIME=42 ns*(N+1) The default value is 882 ns, the range is 80 ns(b'2)560 ns. N: 1(b'3)F. When is 0, t1h_time = 3F
20:16	R/W	0x6	T1L_TIME LED T1L time Unit: cycle (24 MHz), t1l_time =42 ns*(N+1) The default value is 294 ns, the range is 80 ns(b'1)280 ns. N: 1(b'1)F. When is 0, t1l_time = 1F
15:11	/	/	/
10:6	R/W	0x7	T0H_TIME LED T0h time Unit: cycle (24 MHz), t0h_time =42 ns*(N+1) The default value is 336 ns, the range is 80 ns(b'1)280 ns. N: 1(b'1)F. When is 0, t0h_time = 1F
5:0	R/W	0x13	T0L_TIME LED T0l time Unit: cycle (24 MHz), t0L_time =42 ns*(N+1) The default value is 840 ns, the range is 80 ns(b'2)560 ns. N: 1(b'3)F. When is 0, t0L_time = 3F

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.15.8.3 0x0008 LEDC Data Finish Counter Register (Default Value: 0x1D4C_0000)

Offset: 0x0008			Register Name: LEDC_DATA_FINISH_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x1D4C	LED_WAIT_DATA_TIME The value is the time that internal FIFO in LEDC waits for data. When the time is out, the LEDC will send the wait_data_timeout_int. (This is an abnormal scene, LEDC needs to be soft_reset.) The value is about 300 us by default. The adjustable range is 80 ns(bit)655 us. led_wait_data_time=42ns*(N+1). N ranges from 1 to 1FFF. When the field is 0, LEDC_WAIT_DATA_TIME=1FFF
15:13	/	/	/
12:0	R	0x0	LED_DATA_FINISH_CNT The value is the total number (0(bit)8k) of LED data that have been sent.

18.15.8.4 0x000C LED Reset Timing Control Register (Default Value: 0x1D4C_0000)

Offset: 0x000C			Register Name: LED_RESET_TIMING_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x1D4C	TR_TIME Reset time control of LED light Unit: cycle (24 MHz), tr_time=42 ns*(N+1) The default value is 300 us. The adjust range is 80 ns(bit)327 us. N ranges from 1 to 1FFF If the value is 0, TR_TIME=1FFF.
15:10	/	/	/
9:0	R/W	0x0	LED_NUM The value is the number of LED lights, up to 1024. The default value is 0, indicating that 1 LED light is connected. The range is from 0 to 1023.

18.15.8.5 0x0010 LEDC Wait Time 0 Control Register (Default Value: 0x0000_00FF)

Offset: 0x0010			Register Name: LEDC_WAIT_TIME0_CTRL_REG
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0010			Register Name: LEDC_WAIT_TIME0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	WAIT_TIM0_EN WAIT_TIME0 enable When it is 1, the waiting time will be automatically inserted among LED package data. 0: Disable 1: Enable
7:0	R/W	0xFF	TOTAL_WAIT_TIME0 Waiting time between 2 LED data. The LEDC output level is controlled by the LED_PAUSE_LEVEL The adjust range is 80 ns(b)10 us. wait_time0=42 ns*(N+1) Unit: cycle (24 MHz) N: 1(b)FF

18.15.8.6 0x0014 LEDC Data Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: LEDC_DATA_REG
Bit	Read/Write	Default/Hex	Description
31:0	W	0x0	LEDC DATA LED display data (the lower 24-bit is valid)

18.15.8.7 0x0018 LEDC DMA Control Register (Default Value: 0x0000_002F)

Offset: 0x0018			Register Name: LEDC_DMA_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x1	LEDC_DMA_EN LEDC DMA Request Enable 0: Disable the request of DMA transfer data 1: Enable the request of DMA transfer data
4:0	R/W	0x0F	LEDC_FIFO_TRIG_LEVEL The remaining space of internal FIFO in LEDC The internal FIFO in LEDC is 24*32. When the remaining space of internal FIFO in LEDC is larger or equal to LEDFIFO_TRIG_LEVEL, the DMA or the CPU request will be generated. The value is 15 by default, which ranges from 1 to 31 and is recommended to be 7 or 15. If the value is 0, LEDFIFO_TRIG_LEVEL is F.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.15.8.8 0x001C LEDC Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: LEDC_INT_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	GLOBAL_INT_EN Global Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	FIFO_OVERFLOW_INT_EN FIFO Overflow Interrupt Enable When the data written by the software is larger than the internal FIFO level of LEDC, the LEDC is in the data loss state. 0: Disable 1: Enable
3	R/W	0x0	WAITDATA_TIMEOUT_INT_EN The internal FIFO in LEDC cannot get data in some abnormal scene. After led_wait_data_time, the interrupt will be enabled. 0: Disable 1: Enable
2	/	/	/
1	R/W	0x0	FIFO_CPUREQ_INT_EN FIFO request CPU Data Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	LED_TRANS_FINISH_INT_EN Data Transmission Finish Interrupt Enable 0: Disable 1: Enable

18.15.8.9 0x0020 LEDC Interrupt Status Register (Default Value: 0x0002_0000)

Offset: 0x0020			Register Name: LEDC_INT_STS_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R	0x1	FIFO_EMPTY FIFO Empty Status Flag
16	R	0x0	FIFO_FULL FIFO Full Status Flag

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0020			Register Name: LEDC_INT_STS_REG
Bit	Read/Write	Default/Hex	Description
15:10	R	0x0	FIFO_WLW FIFO Internal Valid Data Depth It indicates the space FIFO has been occupied.
9:5	/	/	/
4	R/W1C	0x0	FIFO_OVERFLOW_INT FIFO Overflow Interrupt The amount of written data exceeds the maximum storage space of LED FIFO. The LEDC is in the data loss state. At this time, the anomaly should be handled by software as follows. a) Query the LED_FIFO_DATA_REG to determine which data has been stored in the internal FIFO of LEDC. Resend the overflow data to LEDC. b) Soft_reset the LEDC to refresh all the data. 0: FIFO doesn t overflow 1: FIFO overflows Write 1 to clear the interrupts.
3	R/W1C	0x0	WAITDATA_TIMEOUT_INT When internal FIFO of LEDC cannot get data resulting from some anomaly, the timeout interrupt will be enabled after the led_wait_data_time. At this time, the LEDC is in WAIT_DATA state, and the LEDC will output the level configured by the LED_PAUSE_LEVEL. During the wait_data, the LEDC will continue to transfer data. In this condition, if LEDC waiting time exceeds the LED reset time, it is as if the LEDC has sent a reset operation. The LED will enter refreshing state by mistake, and the data hasn t been completely sent. 0: LEDC not timeout 1: LEDC timeout Write 1 to clear the interrupts.
2	/	/	/
1	R/W1C	0x0	FIFO_CPUREQ_INT FIFO Request CPU Data Interrupt When FIFO data amount is less than the threshold, the interrupt will be reported to the CPU. 0: FIFO doesn t request that CPU transfers data 1: FIFO requests that CPU transfers data Write 1 to clear the interrupts.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0020			Register Name: LEDC_INT_STS_REG
Bit	Read/Write	Default/Hex	Description
0	R/W1C	0x0	LED_TRANS_FINISH_INT Data Transfer Finish Interrupt It indicates that the configured data of total_data_length finishes transfer. 0: Data is not transferred completely 1: Data is transferred completely Write 1 to clear the interrupts.

18.15.8.10 0x0028 LEDC Wait Time1 Control Register (Default Value: 0x01FF_FFFF)

Offset: 0x0028			Register Name: LEDC_WAIT_TIME1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	WAIT_TIM1_EN WAIT_TIME1 enable When it is 1, the waiting time will be automatically inserted among the LED frame data. 0: Disable 1: Enable
30:0	R/W	0x01FFFFFF	TOTAL_WAIT_TIME1 Waiting Time between Two Frames of Data. The LEDC output is controlled by the LED_PAUSE_LEVEL. The adjust range is 80 ns(b)85 s. wait_time1=42 ns*(N+1) Unit: cycle (24 MHz) N: 0x80(b)0x7FFFFFFF If it is 0, TOTAL_WAIT_TIME1 is 0x7FFFFFFF

18.15.8.11 0x0030+N*0x04 (N=0~31) LEDC FIFO Data Register (Default Value: 0x0000_0000)

Offset: 0x0030+N*0x04 (N=0~31)			Register Name: LEDC_FIFO_DATA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	LEDC_FIFO_DATA_X Internal FIFO data of LEDC The lower 24-bit is valid.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.16 CIR Receiver (IR_RX)

18.16.1 Overview

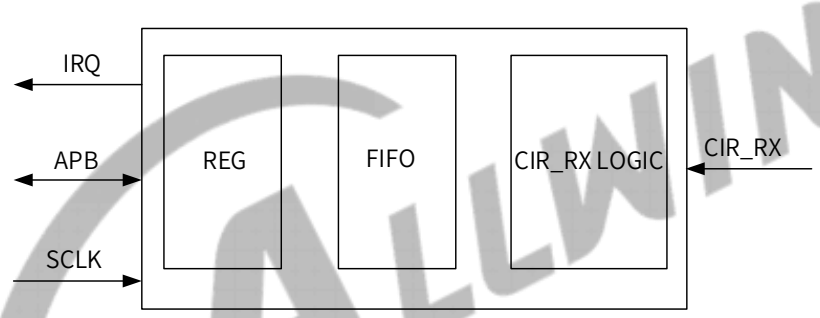
The Consumer Infrared (CIR) receiver captures pulse from the IR Receiver module and uses the Run-Length Code (RLC) to encode the pulse.

The CIR receiver has the following features:

- One IR_RX interface in CPUX domain and one IR_RX interface in CPUS domain
- Supports CIR for remote control
- 64x8 bits FIFO for data buffer
- Sample clock up to 1 MHz

18.16.2 Block Diagram

Figure 18-88 CIR Receiver Block Diagram



The CIR receiver samples the input signal on the programmable frequency and records these samples into RX FIFO when one CIR signal is found on the air. The CIR receiver uses Run-Length Code (RLC) to encode pulse width. The encoded data is buffered in 64 levels and 8-bit width RX FIFO; the MSB bit is used to record the polarity of the receiving CIR signal, the rest 7 bits are used for the length of RLC. The maximum length of the RLC is 128. If the duration of one level (high or low level) is more than 128, another byte is used.

18.16.3 Clock Sources

The following table describes the clock sources of IR_RX and S_IR_RX. For clock setting, configurations, and gating information, refer to the section CCU and PRCM.

Module	Clock Sources	Description
IR_RX	RTC_32K	Its frequency is 32.768 KHz by default.
	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.
	DXCO	The external high-frequency crystal oscillator. Its frequency is 26 MHz.
S_IR_RX	RTC_32K	Its frequency is 32.768 KHz by default.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

	DCXO	The external high-frequency crystal oscillator. Its frequency is 26 MHz.
	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.

18.16.4 External Signals

The following table describes the external signals of IR_RX.

Table 18-45 IR_RX External Signals

Signal Name	Description	Type
IR-RX	Consumer Infrared Receiver	I
S-IR-RX	Consumer infrared receiver	I

18.16.5 Functional Description

NEC mode

Figure 18-89 A typical Pulse Train of the NEC

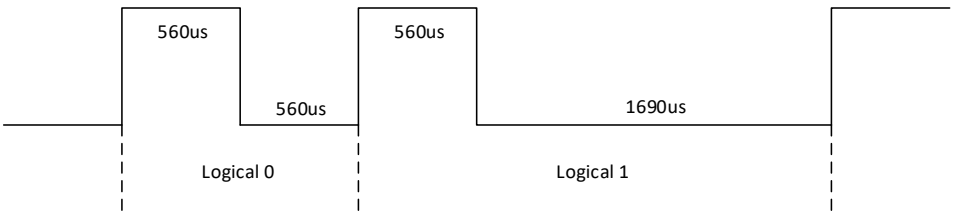
The CIR receiver module is a timer with a capture function.

When CIR_RX signals satisfy the Active Threshold (ATHR), the CIR receiver starts capturing. The signals whose pulse width less than Noise Threshold (NTHR) will be ignored. When the signals satisfy Idle Threshold (ITHR), the capture process will be stopped and the Receiver Packet End interrupt will be generated, then the Receiver Packet End Flag will be asserted.

In a capture process, every effective pulse is buffered to FIFO in bytes according to the form of the Run-Length Code. The MSB bit of a byte indicates the polarity of pulse, and the rest 7 bits indicate the pulse width by taking Sample Clock as a basic unit. This is the code form of the RLC-Byte. When the level changes or the pulse width counter overflows, the RLC-Byte is buffered to FIFO. Afterwards, the CIR_RX module receives the infrared signals transmitted by the infrared remote control, the software decodes the signals.

Sample Clock

Figure 18-90 Logical 0 and Logical 1 of NEC Protocol



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

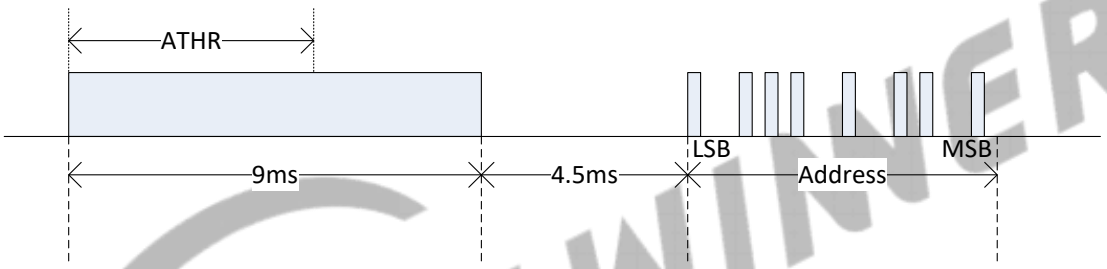
For NEC protocol, a logical "1" takes 2.25 ms (560 us+1680 us) to transmit, while a logical "0" only takes 1.12 ms (560 us+560 us) to transmit.

For example, if the sample clock frequency is 31.25 kHz, and a sample cycle is 32 us, then 18 sample cycles are 560 us. So the RLC of 560 us low level is 0x12 (b 00010010), the RLC of 560 us high level is 0x92 (b 10010010). For instance, a logical 1 will samples 0x12 (b 00010010) and 0xb5 (b 10110101), of which bit 7 indicates level, and bit 6 indicates sampling cycles. Therefore, 00010010 0x12 indicates 18 sampling cycles of low level (approximately 560 us).

Active Threshold (ATHR)

When the CIR receiver is in the idle state, if the electrical level of the IR_RX signal changes (positive jump or negative jump), and the duration reaches this threshold, then the CIR receiver takes the starting of the signal as a lead code. It turns into an active state and starts to capture IR_RX signals.

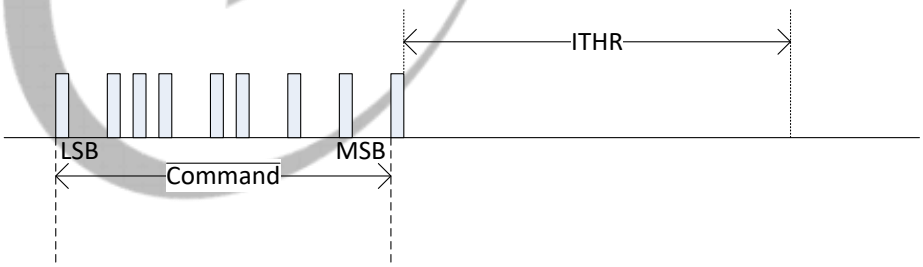
Figure 18-91 ATHR Definition



Idle Threshold (ITHR)

If the level of IR_RX signals has no change, and the duration reaches this threshold, then the CIR receiver enters into Idle state and ends this capture.

Figure 18-92 ITHR Definition

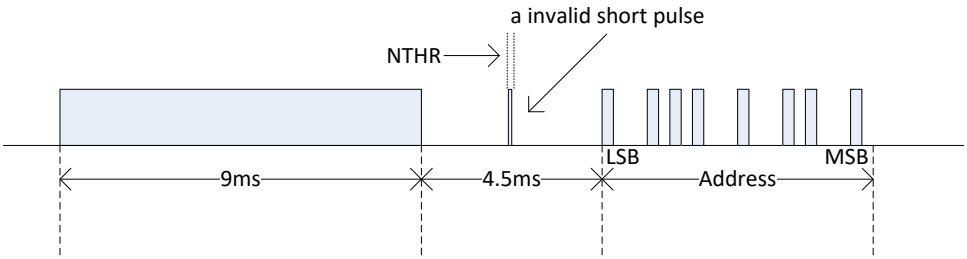


Noise Threshold (NTHR)

In the capture process, the pulse is ignored if its width is less than the Noise Threshold.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

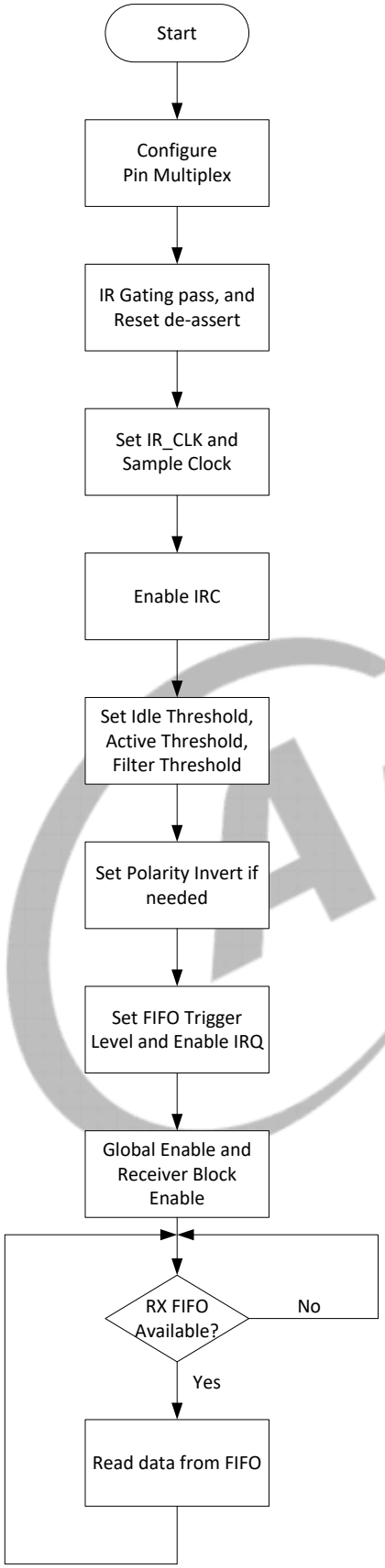
Figure 18-93 NTHR Definition



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.16.6 Operation Guidelines

Figure 18-94 CIR Receiver Process



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.16.7 Register List

Module Name	Base Address
IRRX	0x02526000
S_IRRX	0x07040000

Register Name	Offset	Description
CIR_CTL	0x0000	CIR Receiver Control Register
CIR_RXCTL	0x0010	CIR Receiver Configure Register
CIR_RXFIFO	0x0020	CIR Receiver FIFO Register
CIR_RXINT	0x002C	CIR Receiver Interrupt Control Register
CIR_RXSTA	0x0030	CIR Receiver Status Register
CIR_CONFIG	0x0034	CIR Receiver Configure Register
CIR_STORE0	0x0080	CIR Receiver Store Register0
CIR_STORE1	0x0084	CIR Receiver Store Register1
CIR_STORE2	0x0088	CIR Receiver Store Register2
CIR_STORE3	0x008C	CIR Receiver Store Register3

18.16.8 Register Description

18.16.8.1 0x0000 CIR Receiver Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CIR_CTL
Bit	Read/Write	Default/HEX	Description
31:8	/	/	/
7:6	R/W	0x0	APAM Active Pulse Accept Mode 00, 01: Both positive and negative pulses are valid as a leading code. 10: Only negative pulse is valid as a leading code. 11: Only positive pulse is valid as a leading code.
5:4	R/W	0x0	CEN CIR ENABLE 00-10: Reserved 11: CIR mode enable
3:2	/	/	/
1	R/W	0x0	RXEN Receiver Block Enable 0: Disable 1: Enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: CIR_CTL
Bit	Read/Write	Default/HEX	Description
0	R/W	0x0	GEN Global Enable A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable

18.16.8.2 0x0010 CIR Receiver Configure Register (Default Value: 0x0000_0004)

Offset: 0x0010			Register Name: CIR_RXCTL
Bit	Read/Write	Default/HEX	Description
31:3	/	/	/
2	R/W	0x1	RPPI Receiver Pulse Polarity Invert. 0: Do not invert receiver signal 1: Invert receiver signal
1:0	/	/	/

18.16.8.3 0x0020 CIR Receiver FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: CIR_RXFIFO
Bit	Read/Write	Default/HEX	Description
31:8	/	/	/
7:0	R	0x0	RBF Receiver Byte FIFO

18.16.8.4 0x002C CIR Receiver Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: CIR_RXINT
Bit	Read/Write	Default/HEX	Description
31:14	/	/	/
13:8	R/W	0x0	RAL RX FIFO Available Received Byte Level for interrupt and DMA request TRIGGER_LEVEL = RAL + 1

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x002C			Register Name: CIR_RXINT
Bit	Read/Write	Default/HEX	Description
5	R/W	0x0	DRQ_EN RX FIFO DMA Enable 0: Disable 1: Enable When set to 1 , the Receiver FIFO DRQ is asserted if reaching RAL. The DRQ is de-asserted when condition fails.
4	R/W	0x0	RAI_EN RX FIFO Available Interrupt Enable 0: Disable 1: Enable When set to 1 , the Receiver FIFO IRQ is asserted if reaching RAL. The IRQ is de-asserted when condition fails.
3:2	/	/	/
1	R/W	0x0	RPEI_EN Receiver Packet End Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	ROI_EN Receiver FIFO Overrun Interrupt Enable 0: Disable 1: Enable

18.16.8.5 0x0030 CIR Receiver Status Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: CIR_RXSTA
Bit	Read/Write	Default/HEX	Description
31:15	/	/	/
14:8	R	0x0	RAC RX FIFO Available Counter 0x0: No available data in RX FIFO 0x1: 1-byte available data in RX FIFO 0x2: 2-byte available data in RX FIFO (p) 0x40: 64 byte available data in RX FIFO
7	R	0x0	STAT Status of CIR 0x0: Idle 0x1: busy
6:5	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0030			Register Name: CIR_RXSTA
Bit	Read/Write	Default/HEX	Description
4	R/W1C	0x0	RA RX FIFO Available 0: RX FIFO not available according its level 1: RX FIFO available according its level This bit is cleared by writing a 1 .
3:2	/	/	/
1	R/W1C	0x0	RPE Receiver Packet End Flag 0: STO was not detected. In CIR mode, one CIR symbol is receiving or not detected. 1: STO field or packet abort symbol (7 b0000,000 and 8 b0000,0000 for MIR and FIR) is detected. In CIR mode, one CIR symbol is received. This bit is cleared by writing a 1 .
0	R/W1C	0x0	ROI Receiver FIFO Overrun 0: Receiver FIFO not overrun 1: Receiver FIFO overrun This bit is cleared by writing a 1 .

18.16.8.6 0x0034 CIR Receiver Configure Register (Default Value: 0x0000_1828)

Offset: 0x0034			Register Name: CIR_CONFIG
Bit	Read/Write	Default/HEX	Description
31:25	/	/	/
24	R/W	0x0	SCS2 Bit2 of Sample Clock Select for CIR This bit is defined by SCS bits below.
23	R/W	0x0	ATHC Active Threshold Control for CIR 0x0: ATHR in Unit of (Sample Clock) 0x1: ATHR in Unit of (128*Sample Clocks)
22:16	R/W	0x0	ATHR Active Threshold for CIR These bits control the duration of CIR from Idle to Active State. The duration can be calculated by ((ATHR + 1) *(ATHC? Sample Clock: 128*Sample Clock)).

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

<table>
<tr><th colspan="3">Offset: 0x0034</th><th>Register Name: CIR_CONFIG</th></tr>
<tr><th>Bit</th><th>Read/Write</th><th>Default/HEX</th><th>Description</th></tr>
<tr><td>15:8</td><td>R/W</td><td>0x18</td><td>ITHR
Idle Threshold for CIR
The Receiver uses it to decide whether the CIR command has been received. If there is no CIR signal on the air, the receiver is staying in IDLE status. One active pulse will bring the receiver from IDLE status to Receiving status. After the CIR is end, the inputting signal will keep the specified level (high or low level) for a long time. The receiver can use this idle signal duration to decide that it has received the CIR command. The corresponding flag is asserted. If the corresponding interrupt is enabled, the interrupt line is asserted to CPU.
When the duration of signal keeps one status (high or low level) for the specified duration ((ITHR + 1)*128 sample_clk), this means that the previous CIR command has been finished.</td></tr>
<tr><td>7:2</td><td>R/W</td><td>0xa</td><td>NTHR
Noise Threshold for CIR
When the duration of signal pulse (high or low level) is less than NTHR, the pulse is taken as noise and should be discarded by hardware.
0x0: all samples are recorded into RX FIFO
0x1: If the signal is only one sample duration, it is taken as noise and discarded.
0x2: If the signal is less than (<=) two sample duration, it is taken as noise and discarded.
(p)
0x3d: if the signal is less than (<=) sixty-one sample duration, it is taken as noise and discarded.</td></tr>
<tr><td>1:0</td><td>R/W</td><td>0x0</td><td>SCS
Sample Clock Select for CIR
<table>
<tr><th>SCS2</th><th>SCS[1]</th><th>SCS[0]</th><th>Sample Clock</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>IR_CLK/64</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>IR_CLK /128</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>IR_CLK /256</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>IR_CLK /512</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>IR_CLK</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
</table>

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.16.8.7 0x0080 CIR Receiver Store Register0 (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: CIR_STORE0
Bit	Read/Write	Default/HEX	Description
31:0	R/W	0x0	SV0 Receiver Store Value 0

18.16.8.8 0x0084 CIR Receiver Store Register1 (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: CIR_STORE1
Bit	Read/Write	Default/HEX	Description
31:0	R/W	0x0	SV1 Receiver Store Value 1

18.16.8.9 0x0088 CIR Receiver Store Register2 (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: CIR_STORE2
Bit	Read/Write	Default/HEX	Description
31:0	R/W	0x0	SV2 Receiver Store Value 2

18.16.8.10 0x008C CIR Receiver Store Register3 (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: CIR_STORE3
Bit	Read/Write	Default/HEX	Description
31:0	R/W	0x0	SV3 Receiver Store Value 3

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.17 CIR Transmitter (IR_TX)

18.17.1 Overview

The CIR transmitter (IR_TX) transfer arbitrary waves which can be modulated with configurable carrier waves such as 38 kHz. IR_TX only uses lower 8 bits of the 32-bit registers, and stores a 16-bit number in 2 registers, where one register contains the higher 8 bits while the other contains the lower 8 bits.

The IR_TX has the following features:

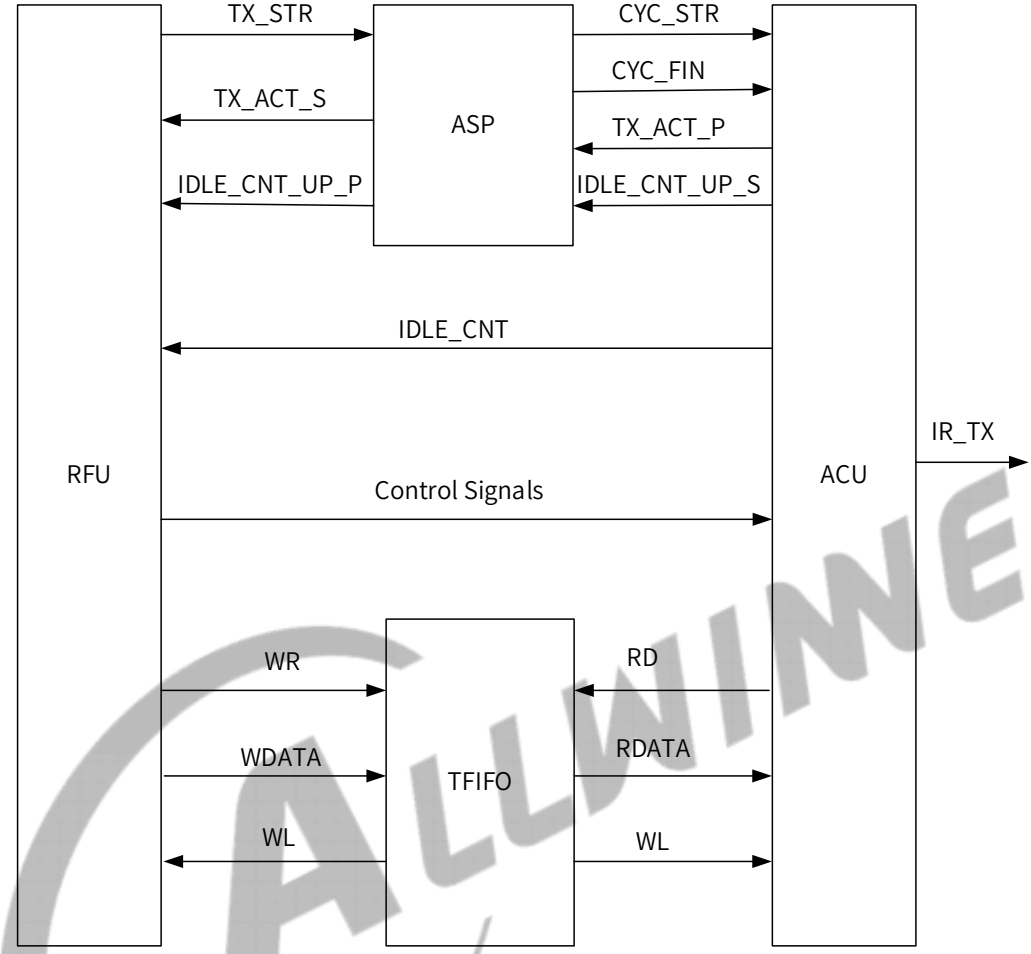
- One IR_TX interface in CPUX domain
- Supports industry-standard AMBA Peripheral Bus (APB) and it is fully compliant with the AMBA Specification, Revision 2.0
- Full physical layer implementation
- Arbitrary wave generator
- Configurable carrier frequency
- Handshake mode and waiting mode of DMA
- 128 bytes FIFO for data buffer
- Supports Interrupts and DMA

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.17.2 Block Diagram

The following figure shows a block diagram of the IR_TX.

Figure 18-95 IR_TX Block Diagram



18.17.3 Clock Sources

The following table describes the clock sources of IR_TX. For clock setting, configurations, and gating information, refer to the section Clock Controller Unit (CCU).

Module	Clock Sources	Description
IR_TX	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.
	PERI1_600M	Its frequency is 600 MHz by default.
	DCXO	The external high-frequency crystal oscillator. Its frequency is 26 MHz.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.17.4 External Signals

The following table describes the external signals of IR_TX.

Table 18-46 IR_TX External Signals

Signal Name	Description	Type
IR-TX	Consumer Infrared Transmitter	O

18.17.5 Functional Description

The IR_TX is used to generate a waveform of arbitrary length, arbitrary shape, and no high-speed requirement, and it can change the data into the high-/low-level sequence of a certain length. Every data is transmitted in bytes, the Bit[7] of a byte means whether the level of a transmitting wave is high or low, the Bit[6:0] is the length of this wave. If the current transmitting frequency-division is 1, 0x88 is a high level of 8 cycles, 0x08 is a low level of 8 cycles. If the current transmitting frequency-division is 4, 0x88 is a high level of 32 cycles, 0x08 is a low level of 32 cycles.

The IR_TX has two transmission modes: non-cycle transmission and cycle transmission.

The non-cycle transmission is to transmit all the data in TX_FIFO until the FIFO is empty.

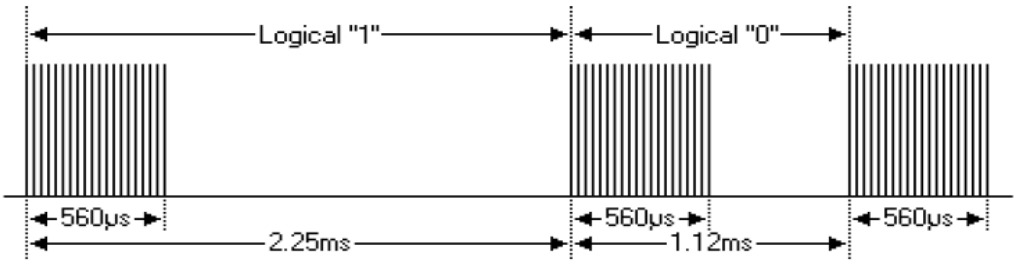
The cycle transmission is to transmit all the data in TX_FIFO; after the transmission completion, wait for a certain time to recover the data in TX_FIFO and then send it until a stop signal is detected. The data recovery in FIFO is implemented by clearing the read pointer.

Timing Diagram

The IR remote control contains many protocols designed by different manufacturers. Here take NEC protocol as an example, the IR_TX module uses a variable pulse-width modulation technique to encompass the various formats of infrared encoding for remote-control applications. A message is started by a 9 ms AGC burst, which is used to set the gain of the earlier CIR receivers. This AGC burst is then followed by a 4.5 ms space, which is then followed by the address and command.

Bit definition: the logical 1 takes 2.25 ms to transmit, while a logical 0 is only 1.12 ms.

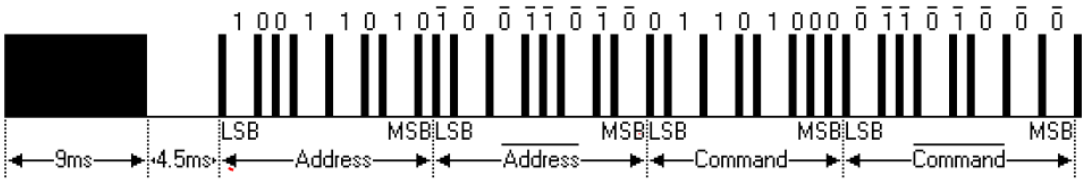
Figure 18-96 Definitions of Logical 1 and Logical 0



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Timing for a message:

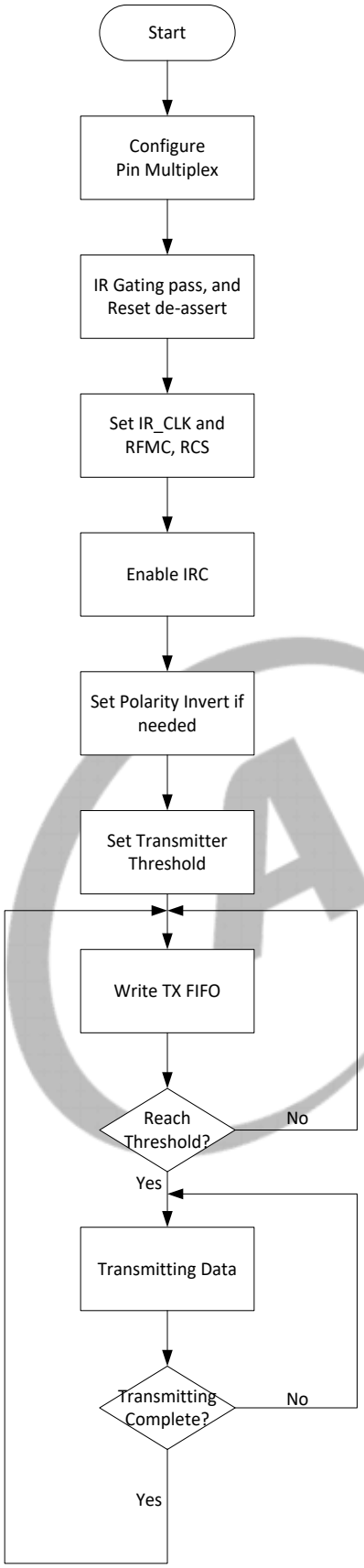
Figure 18-97 CIR Message Timing Diagram



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.17.6 Operation Guidelines

Figure 18-98 CIR Transmitter Process



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.17.7 Register List

Module Name	Base Address
IRTX	0x02525000

Register Name	Offset	Description
CIR_TGLR	0x0000	CIR Transmitter Global Register
CIR_TMCR	0x0004	CIR Transmitter Modulation Control Register
CIR_TCR	0x0008	CIR Transmitter Control Register
CIR_IDC_H	0x000C	CIR Transmitter Idle Duration Counter High Register
CIR_IDC_L	0x0010	CIR Transmitter Idle Duration Counter Low Register
CIR_TICR_H	0x0014	CIR Transmitter Idle Counter High Register
CIR_TICR_L	0x0018	CIR Transmitter Idle Counter Low Register
CIR_TEL	0x0020	CIR Transmitter FIFO Empty Level Register
CIR_TXINT	0x0024	CIR Transmitter Interrupt Control Register
CIR_TAC	0x0028	CIR Transmitter FIFO Available Counter Register
CIR_TXSTA	0x002C	CIR Transmitter Status Register
CIR_TXT	0x0030	CIR Transmitter Threshold Register
CIR_DMA	0x0034	CIR Transmitter DMA Control Register
CIR_TXFIFO	0x0080	CIR Transmitter FIFO Data Register

18.17.8 Register Description

18.17.8.1 0x0000 CIR Transmitter Global Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CIR_TGLR
Bit	Read/Write	Default	Description
31:8	/	/	/
7	R/W	0x0	IMS Internal Modulation Select 0: the transmitting signal is not modulated 1: the transmitting signal is modulated internally
6:5	R/W	0x0	DRMC Duty ratio of modulated carrier is high level /low level. 00: Low level is the one time of high level 01: Low level is the two times of high level 10: Low level is the three times of high level 11: Reserved
4:3	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0000			Register Name: CIR_TGLR
Bit	Read/Write	Default	Description
2	R/W	0x0	TPPI Transmit Pulse Polarity Invert 0: Not invert transmit pulse 1: Invert transmit pulse
1	R/W	0x0	TR Transmit Reset When this bit is set, the transmitting is reset. The FIFO will be flush, the TIC filed and CSS field will be clean during Transmit Reset. This field will automatically clean when the Transmit Reset is finished, and the CIR transmitter will state Idle .
0	R/W	0x0	TXEN Transmit Block Enable 0: Disable the CIR Transmitter 1: Enable the CIR Transmitter

18.17.8.2 0x0004 CIR Transmitter Modulation Control Register (Default Value: 0x0000_009E)

Offset: 0x0004			Register Name: CIR_TMCR
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R/W	0x9E	RFMC Reference Frequency of Modulated Carrier Reference Frequency of modulated carrier based on a division of a fixed functional clock(FCLK). The range of the modulated carrier is usually 30KHZ to 60KHz.The most consumer electronics is 38KHz. The default modulated carrier is 38KHz when FCLK is 12MHz. RFMC= FCLK/((N+1)*(DRMC+2)).

18.17.8.3 0x0008 CIR Transmitter Control Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CIR_TCR
Bit	Read/Write	Default	Description
31:8	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0008			Register Name: CIR_TCR
Bit	Read/Write	Default	Description
7	R/W	0x0	CSS Cyclical Pulse Start/Stop Control Start to transmit when set to '1', 0: Stop when cleared to '0'. From start to stop, all data in FIFO must be transmitted. 1: Start.
6:4	/	/	/
3:1	R/W	0x0	RCS Reference Clock Select for CIR Transmit 000: CIR Transmit reference clock is ir_clk 001: CIR Transmit reference clock is ir_clk/2 010: CIR Transmit reference clock is ir_clk/4 011: CIR Transmit reference clock is ir_clk/8 100: CIR Transmit reference clock is ir_clk/64 101: CIR Transmit reference clock is ir_clk/128 110: CIR Transmit reference clock is ir_clk/256 111: CIR Transmit reference clock is ir_clk/512
0	R/W	0x0	TTS Type of the transmission signal 0: The transmitting wave is single non-cyclical pulse. 1: The transmitting wave is cyclical short-pulse.

18.17.8.4 0x000C CIR Transmitter Idle Duration Counter High Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: CIR_IDC_H
Bit	Read/Write	Default	Description
31:8	/	/	/
3:0	R/W	0x0	IDC_H Idle Duration Counter threshold (High 4 bit) Idle Duration = 128*IDC*Ts (IDC = 0-4095)

18.17.8.5 0x0010 CIR Transmitter Idle Duration Counter Low Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CIR_IDC_L
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R/W	0x0	IDC_L Idle Duration Counter threshold (Low 8 bit) Idle Duration = 128*IDC*Ts (IDC = 0-4095)

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

18.17.8.6 0x0014 CIR Transmitter Idle Counter High Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: CIR_TICR_H
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R	0x0	TIC_H Transmit Idle Counter_H (High 8 bit) Count in 128*Ts (Sample Duration, 1/Fs) when transmitter is idle, and it should be reset when the transmitter active. When this counter reaches the maximum value (0xFFFF), it will stop automatically, and should not be cleared to zero.

18.17.8.7 0x0018 CIR Transmitter Idle Counter Low Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: CIR_TICR_L
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R	0x0	TIC_L Transmit Idle Counter_L (Low 8 bit) Count in 128*Ts (Sample Duration, 1/Fs) when transmitter is idle, and it should be reset when the transmitter active. When this counter reaches the maximum value (0xFFFF), it will stop automatically, and should not be cleared to zero.

18.17.8.8 0x0020 CIR Transmitter FIFO Empty Level Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: CIR_TEL
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R/W	0x0	TEL TX FIFO empty Level for DRQ and IRQ. TRIGGER_LEVEL = TEL + 1

18.17.8.9 0x0024 CIR Transmitter Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: CIR_TXINT
Bit	Read/Write	Default	Description
31:3	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0024			Register Name: CIR_TXINT
Bit	Read/Write	Default	Description
2	R/W	0x0	DRQ_EN TX FIFO DMA Enable 0: Disable 1: Enable When set to 1 , the TX FIFO DRQ is asserted if the number of the transmitting data in the FIFO is less than the RAL. The DRQ is de-asserted when condition fails.
1	R/W	0x0	TAI_EN TX FIFO Available Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	TPEI_EN Transmit Packet End Interrupt Enable for Cyclical Pulse 0: Disable 1: Enable TUI_EN Transmitter FIFO under run Interrupt Enable for Non-Cyclical Pulse 0: Disable 1: Enable

18.17.8.10 0x0028 CIR Transmitter FIFO Available Counter Register (Default Value: 0x0000_0080)

Offset: 0x0028			Register Name: CIR_TAC
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R	0x80	TAC TX FIFO Available Space Counter 0x00: No available space in TX FIFO 0x01: 1-byte available space in TX FIFO 0x02: 2-byte available space in TX FIFO (p) 0x80: 128 byte available space in TX FIFO

18.17.8.11 0x002C CIR Transmitter Status Register (Default Value: 0x0000_0002)

Offset: 0x002C	Register Name: CIR_TXSTA

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default	Description
31:4	/	/	/
3	R	0x0	STCT Status of CIR Transmitter 0: Idle 1: Active This bit will automatically set when the controller begins transmit the data in the FIFO. The 1 will last when the data in the FIFO. It will automatically be cleaned to 0 when all data in the FIFO is transmitted. The bit is for debug. Output Level of Idle state determined by level of the last data output.
2	R	0x0	DRQ DMA Request Flag When set to 1 , the TX FIFO DRQ is asserted if the number of the transmitting data in the FIFO is less than the RAL. The DRQ is de-asserted when condition fails. This bit is for debug.
1	R/W	0x1	TAI TX FIFO Available Interrupt Flag 0: TX FIFO not available by its level 1: TX FIFO available by its level This bit can be cleared by software writing 1 .
0	R/W	0x0	TPE Transmitter Packet End Flag for Cyclical Pulse 0: Transmissions of address, control and data fields not completed 1: Transmissions of address, control and data fields completed TUR Transmitter FIFO Under Run Flag for Non-Cyclical Pulse 0: No transmitter FIFO under run 1: Transmitter FIFO under run This bit is cleared by writing a 1 .

18.17.8.12 0x0030 CIR Transmitter Threshold Register (Default Value: 0x0000_0000)

Offset: 0x0030	Register Name: CIR_TXT

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R/W	0x0	NCTT Non-cyclical Pulse Transmit Threshold The controller will trigger transmitting the data in the FIFO when the data byte number has reaches the Transmit Threshold set in this field.

18.17.8.13 0x0034 CIR Transmitter DMA Control Register (Default Value: 0x0000_00A5)

Offset: 0x0034			Register Name: CIR_DMA_CTL
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R/W	0xA5	DMA Handshake configuration 0xA5: DMA wait cycle mode 0xEA: DMA handshake mode

18.17.8.14 0x0080 CIR Transmitter FIFO Data Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: CIR_TXFIFO
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	W	0x0	Transmit Byte FIFO When the transmitting is trigger, the data in the FIFO will be transmitted until the data number has been transmitted finished. Note: The data should not be zero.

19 Security

19.1 Crypto Engine (CE)

19.1.1 Overview

The Crypto Engine (CE) module is one encryption/decryption algorithms accelerator. It supports kinds of symmetric, asymmetric, HASH, and RBG algorithms. There are two software interfaces for secure and non-secure world each. Algorithm control information is written in memory by task descriptor, then CE automatically reads it when executing request. It supports parallel requests from 4 channels each world and 4 different types of algorithms simultaneously. This

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

module also has an internal DMA controller to transfer data between CE and memory. It supports parallel running for symmetric, HASH, asymmetric algorithms.

The CE has the following features:

- Symmetrical algorithm:
  - AES symmetrical algorithm
    - Key size: 128/192/256 bits (not XTS), 256/512 bits (XTS)
    - CFB mode includes: CFB1, CFB8, CFB64, and CFB128
    - CTR mode includes: CTR16, CTR32, CTR64, and CTR128
    - Supports ECB, CBC, CTS, OFB, CBC-MAC, GCM, and XTS modes
  - DES symmetrical algorithm
    - CTR mode, includes: CTR16, CTR32, and CTR64
    - Supports ECB, CBC, and CBC-MAC mode
  - Supports 3DES
  - SM4 symmetrical algorithm supports ECB and CBC mode
  - Supports RC4
- Hash algorithms
  - Supports MD5, SHA1, SHA224, SHA256, SHA384, SHA512, and SM3
  - Supports HMAC-SHA1, HMAC-SHA256
  - Supports multi-package[1] mode for these ones
  - Supports hardware padding
- Random bit generator algorithms
  - Supports PRNG, 175 bits seed width, and output with multiple of 5 words
  - Supports TRNG, post-process by hardware with SHA256, output with multiple of 8 words
  - Supports TRNG single/double entropy source mode
  - Supports TRNG healthy test
  - Supports Instantiate/Reseed/Generate/Uninstantiate 4 process
  - Supports prediction resistance requests
  - Supports 8 separate suits of Internal State
  - Maxim 2^32 BYTE length of Entropy input, Nonce, Personalization, Additional input. And length is multiple of word

[1] If it is not the last package, input should be aligned with computation block in the size of 512bits or 1024bit.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- Public key algorithms
  - Supports RSA public key algorithms: 512/1024/2048/3072/4096-bit width
  - Supports ECC public key algorithms: 160/224/256/384/521-bit width
  - Supports SM2 algorithms
- Security Strategy and System Feature
  - Symmetric, asymmetric, HASH/RBG ctrl logics are separate, can handle task simultaneously. Symmetric logic can select instantiate 2 suits at implementation time.
  - Supports task chain mode for each request. Task or task chain are executed at request order.
  - multi- scatter group(sg) are supported for both input and output data
  - Supports secure and non-secure interfaces respectively, each world issues task request through its own interface, don t know each other s existence.
  - Each world has 4 channels for software request, each channel has an interrupt control and status bit, and channels are independent with each other.
  - Supports byte-aligned address for all configurations
- keyladder
  - kl0 supports 1 suit KL5
  - kl1 supports 1 suit KL3 or KL5

NOTE

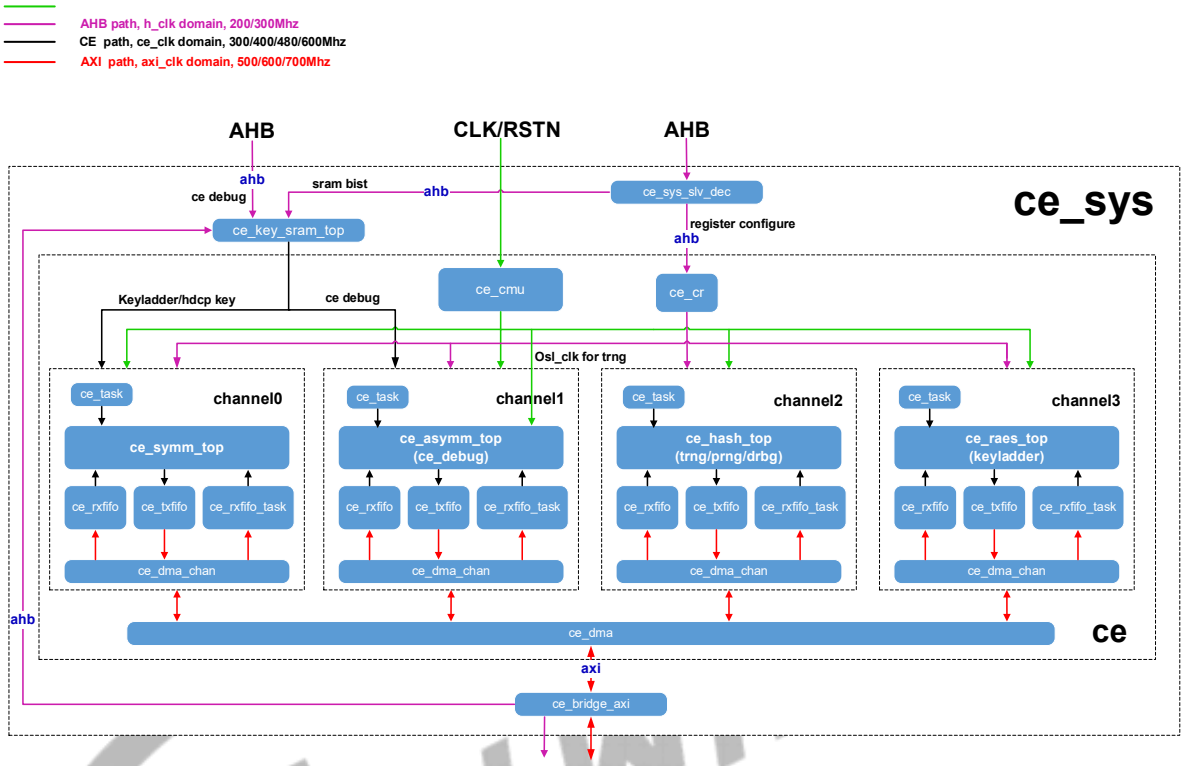
In the hash algorithms, if not last package, input should be aligned with computation block, namely 512 bits or 1024 bits.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

19.1.2 Block Diagram

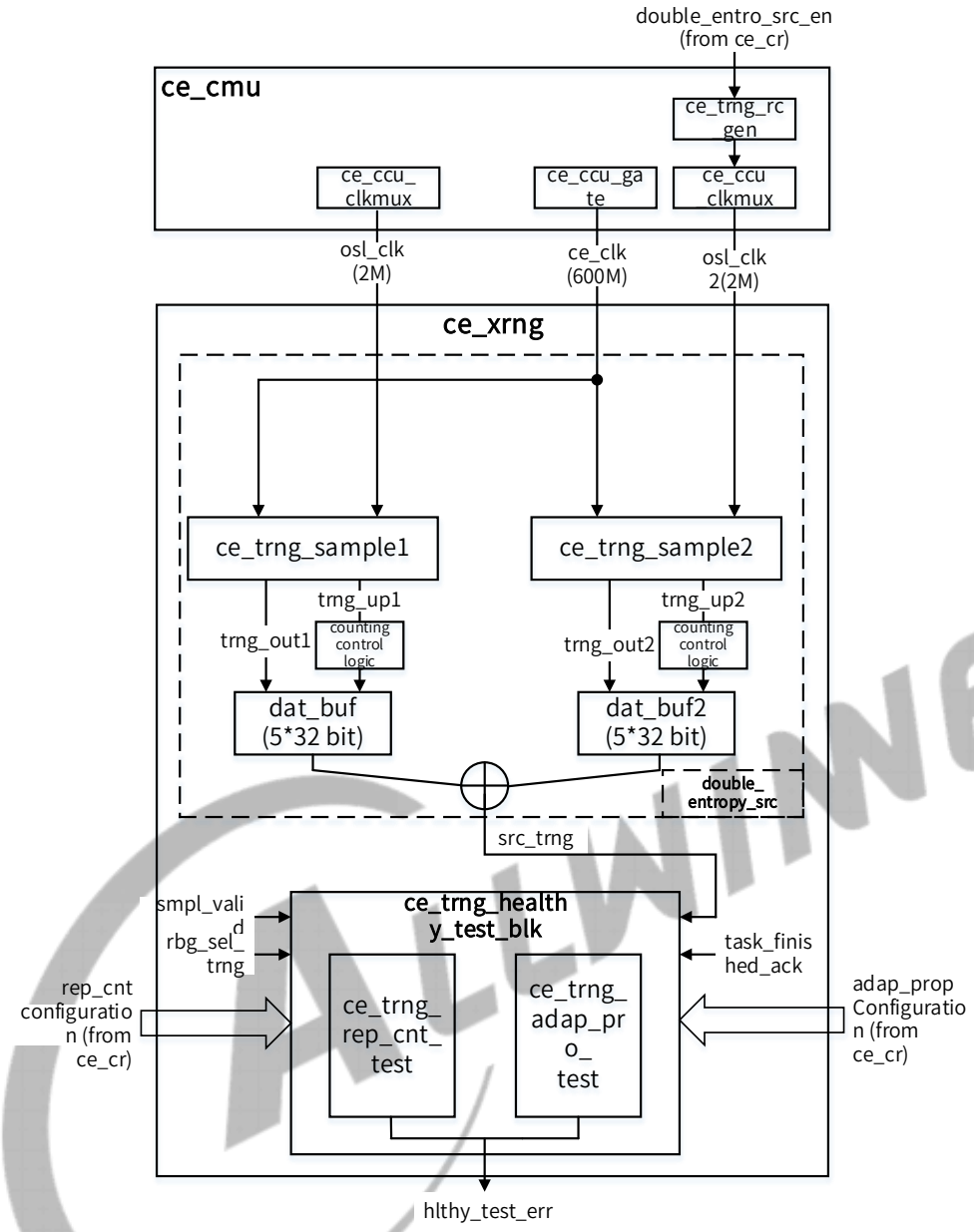
The following figures show the block diagrams of CE and CE XRNG Modify.

Figure 19-1 CE Block Diagram



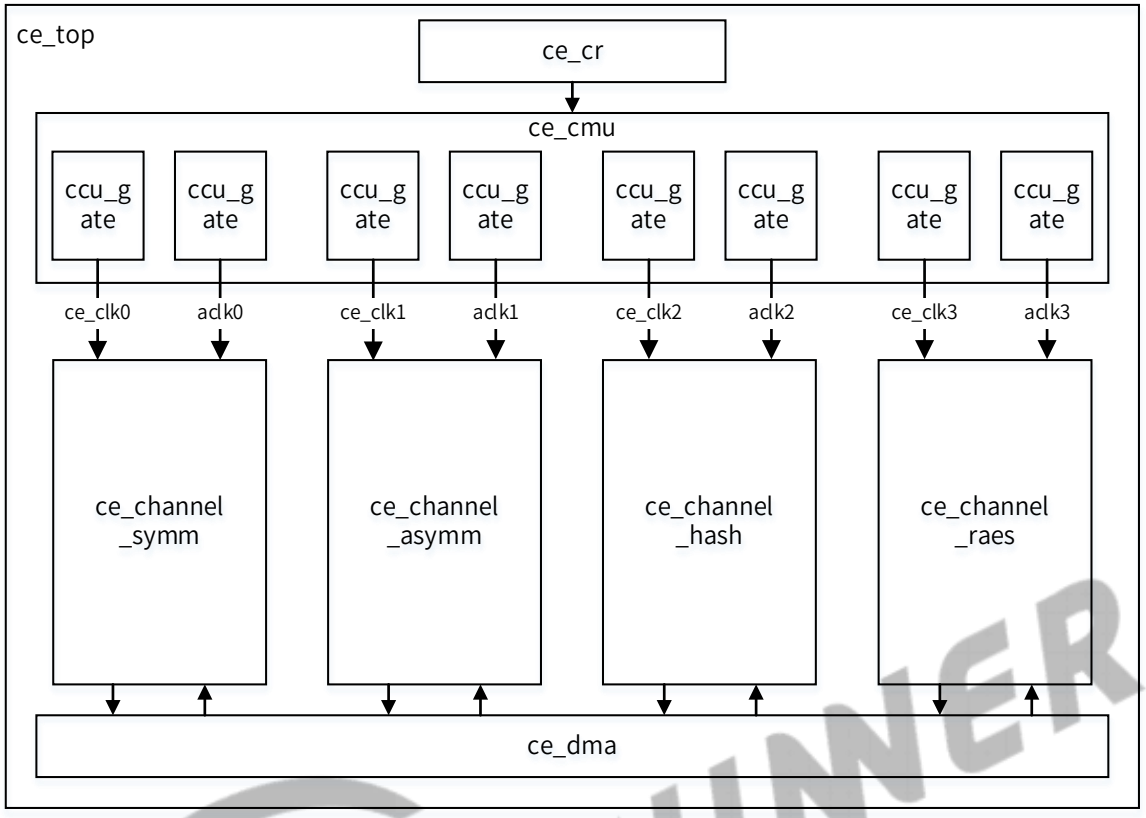
Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 19-2 CE XRNG Modify Block Diagram (ce_hash_top)



Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 19-3 CE Low Power Diagram (ce_top)



19.1.3 Clock Sources

The following table describes the clock sources of CE. For clock setting, configurations, and gating information, refer to the section Clock Controller Unit (CCU).

Module	Clock Sources	Description
CE	SYS_CLK24M	It is generated by the multiplexer between DCXO and PLL_REF. Its frequency is fixed at 24 MHz.
	PERI0_400M	Its frequency is 400 MHz by default.
	PERI0_600M	Its frequency is 600 MHz by default.

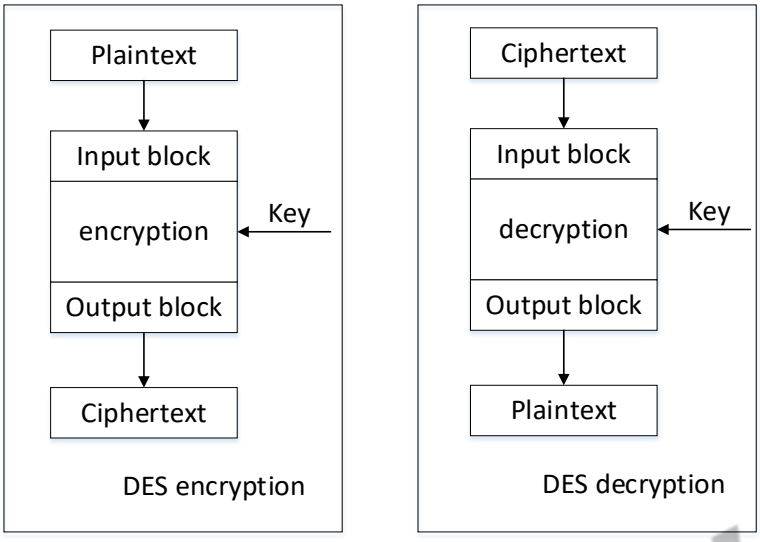
Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

19.1.4 Functional Description

19.1.4.1 DES Algorithm

The following figure shows the DES encryption and decryption operation.

Figure 19-4 DES Encryption and Decryption

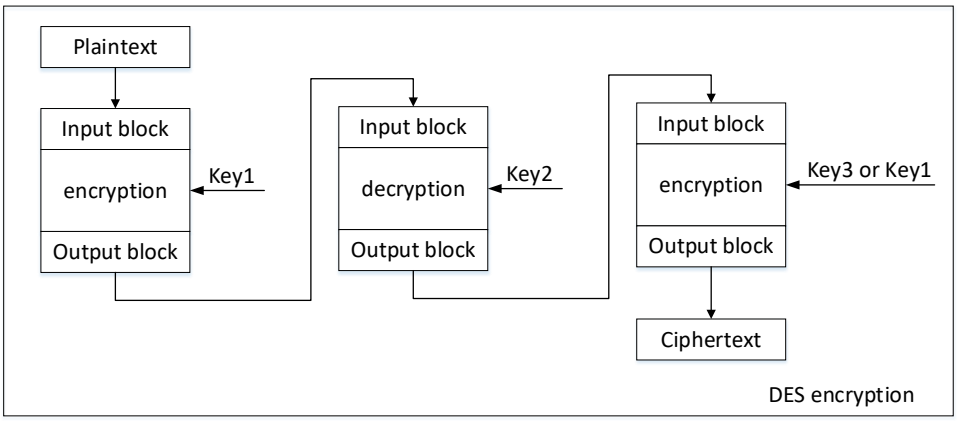


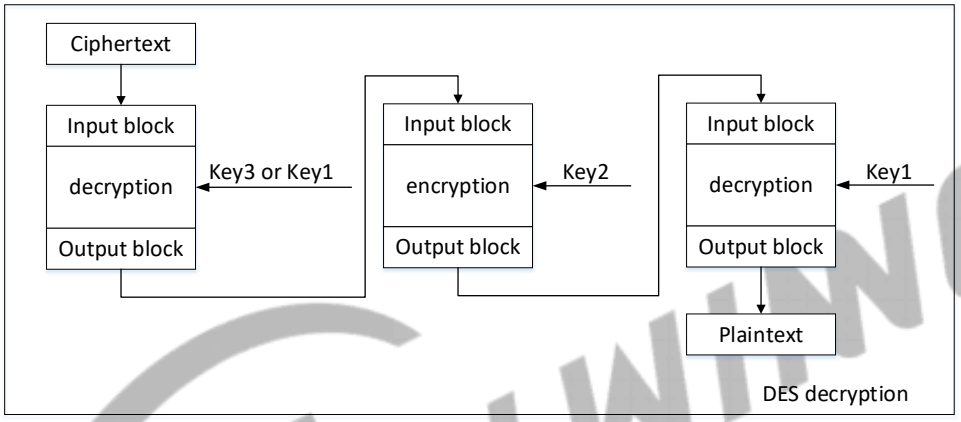
19.1.4.2 3DES Algorithm

The 3DES algorithm supports both 3-key and 2-key operations. A 2-key operation can be regarded as a simplified 3-key operation. To be specific, key 3 is represented by key 1 in a 2-key operation. The following figure shows the 3DES encryption and decryption operation of a 3-key operation and a 2-key operation.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 19-5 3DES Encryption and Decryption of a 3-key Operation and a 2-key Operation





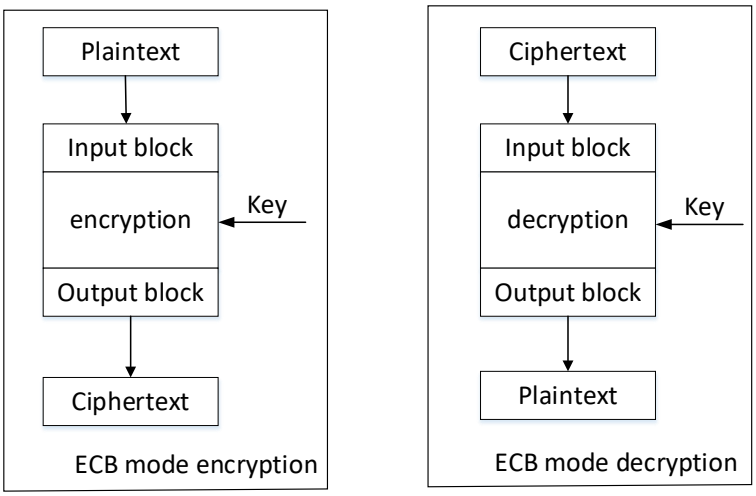
19.1.4.3 ECB Mode

The ECB mode is a confidentiality mode that features, for a given key, the assignment of a fixed ciphertext block to each plaintext block, analogous to the assignment of code words in a codebook.

In ECB mode, encryption and decryption algorithms are directly applied to the block data. The operation of each block is independent, so the plaintext encryption and ciphertext decryption can be performed concurrently.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

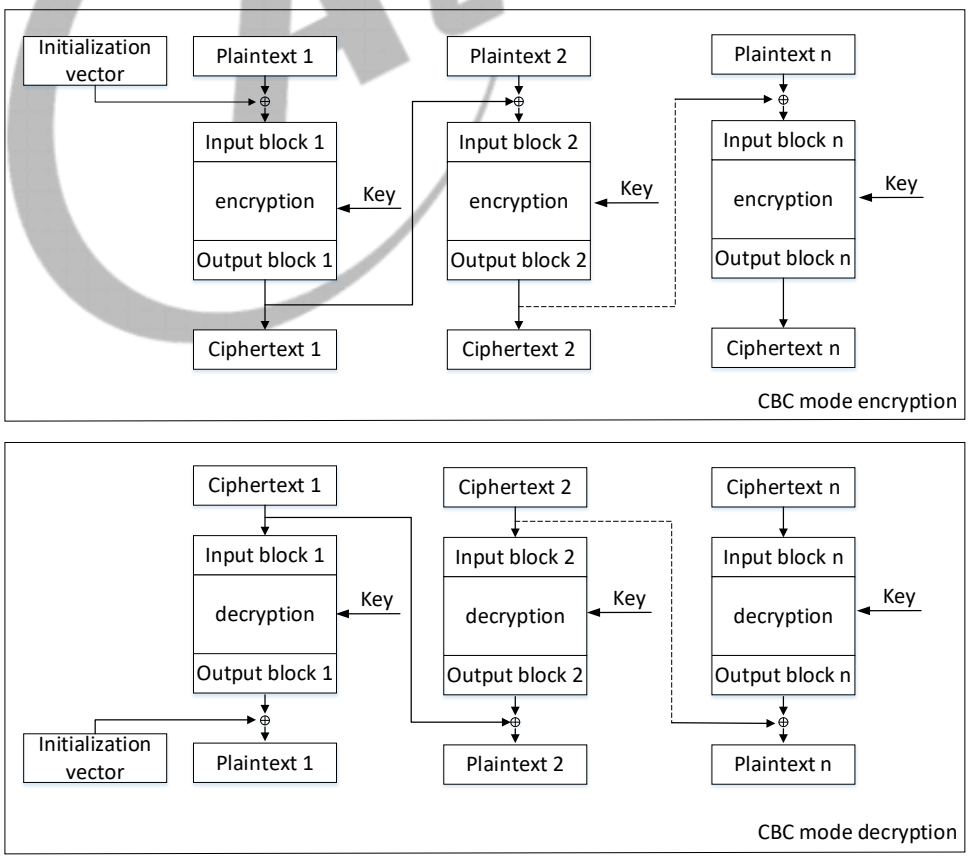
Figure 19-6 ECB Mode Encryption and Decryption



19.1.4.4 CBC Mode

The CBC mode is a confidentiality mode whose encryption process features the combining of the plaintext blocks with the previous ciphertext blocks. The CBC mode requires an initialization vector (IV) to combine with the first plaintext block. The encryption process of each plaintext block is related to the block processing result of the previous ciphertext blocks, so encryption operations cannot be concurrently performed in CBC mode. The decryption operation is independent of output plain text of the previous block, so decryption operations can be performed concurrently.

Figure 19-7 CBC Mode Encryption and Decryption

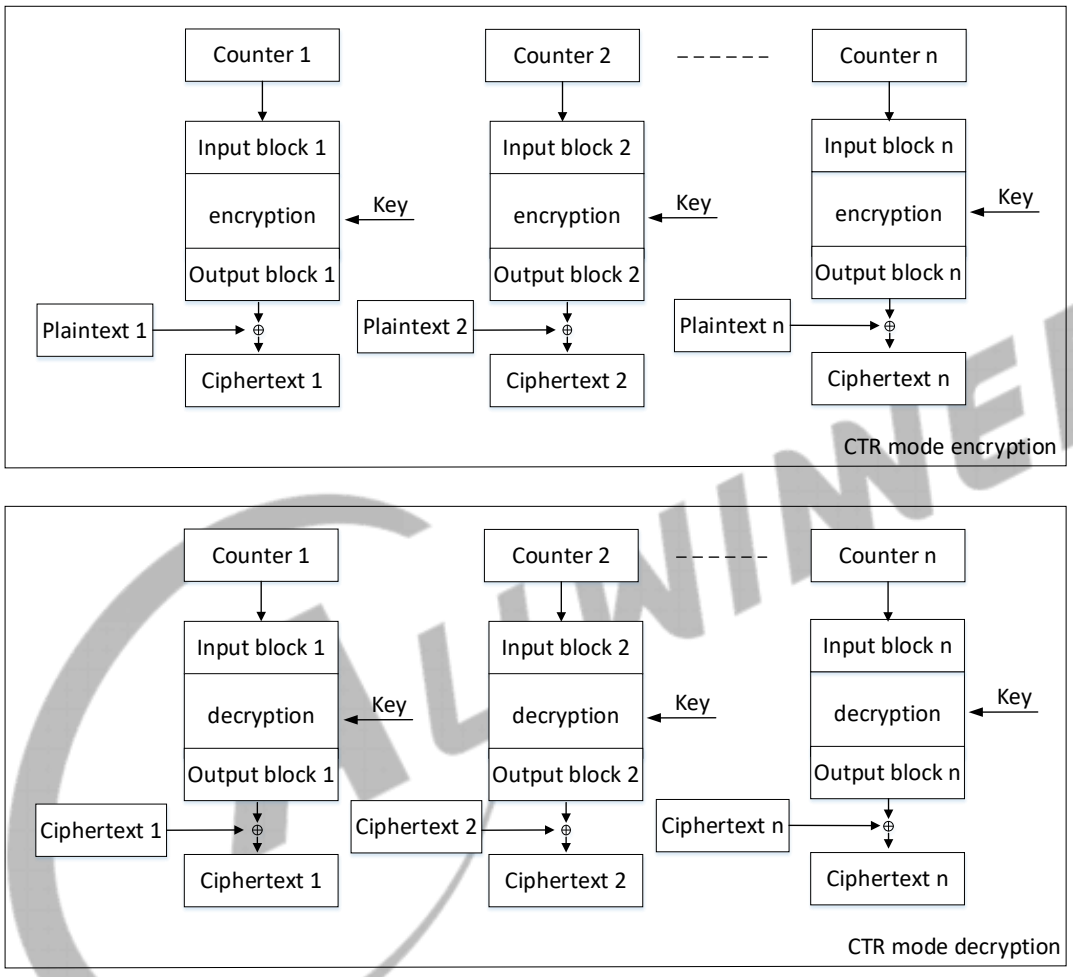


Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

19.1.4.5 CTR Mode

The CTR mode is a confidentiality mode that features the application of the forward cipher to a set of input blocks, called counters, to produce a sequence of output blocks that are exclusive-ORed with the plaintext to produce the ciphertext, and vice versa. All of the counters must be distinct.

Figure 19-8 CTR Mode Encryption and Decryption



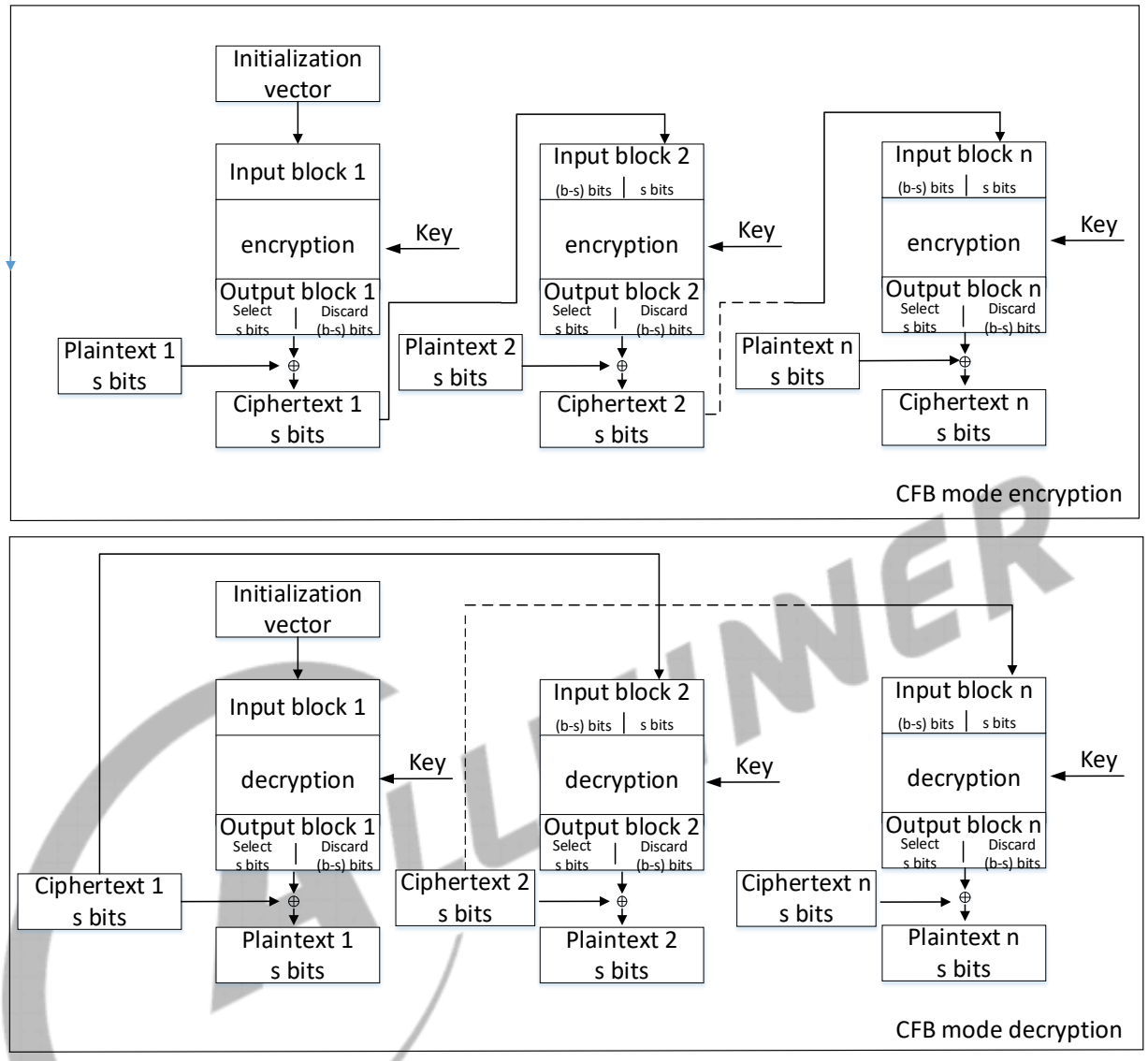
19.1.4.6 CFB Mode

The CFB mode is a confidentiality mode that features the feedback of successive ciphertext segments into the input blocks of the forward cipher to generate output blocks that are exclusive-ORed with the plaintext to produce the ciphertext, and vice versa. The CFB mode requires an IV as the initial input block, and the forward cipher operation is applied to the IV to produce the first output block. The first ciphertext segment is produced by exclusive-ORing the first plaintext segment with the s most significant bits of the first output block. The value of s is 1 bit, 8 bits, 64 bits, or 128 bits.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

The following figure shows the s-bit CFB mode of the AES algorithms.

Figure 19-9 CFB Mode Encryption and Decryption

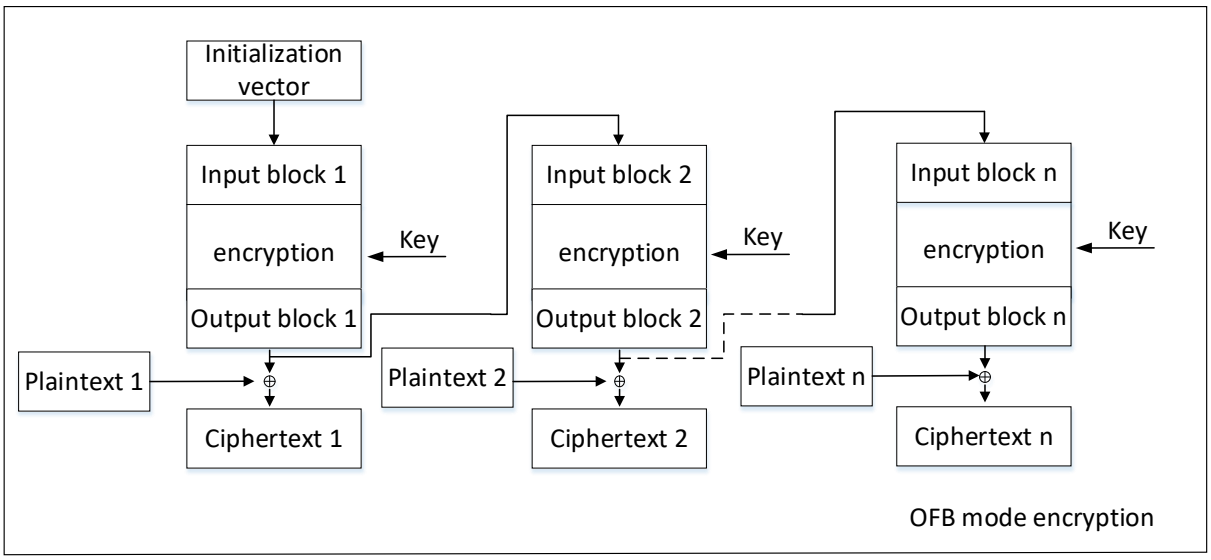


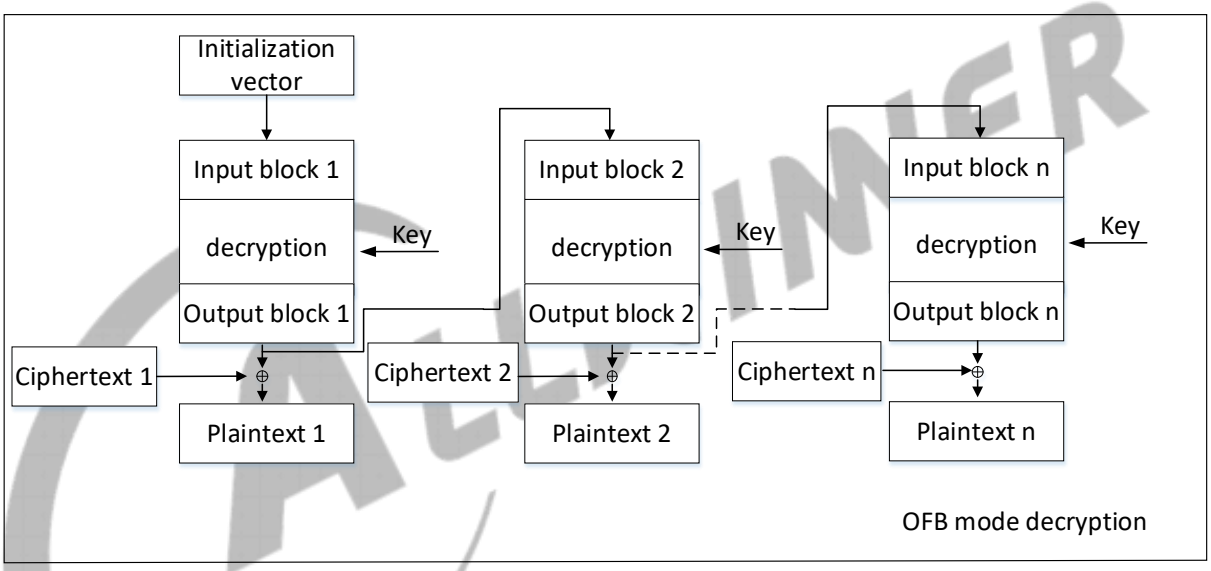
19.1.4.7 OFB Mode

The OFB mode is a confidentiality mode that features the iteration of the forward cipher on an IV to generate a sequence of output blocks that are exclusive-ORed with the plaintext to produce the ciphertext, and vice versa. If a same key is used, different IVs must be used to ensure operation security.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 19-10 OFB Mode Encryption and Decryption



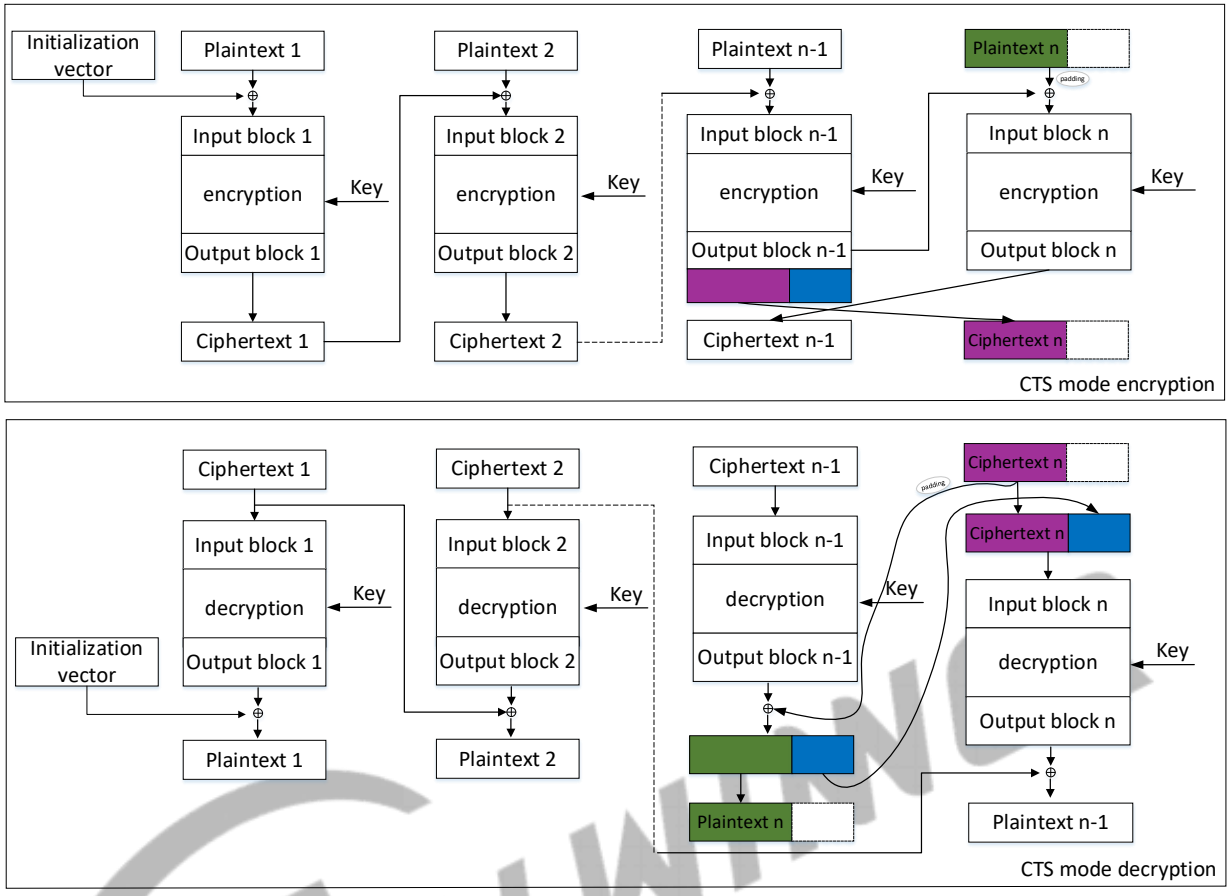


19.1.4.8 CTS Mode

The CTS mode is a confidentiality mode that accepts any plaintext input whose bit length is greater than or equal to the block size but not necessarily a multiple of the block size. Below are the diagrams for CTS encryption and decryption.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 19-11 CTS Mode Encryption and Decryption



19.1.4.9 HASH Algorithm

The hash algorithms support MD5, SHA1, SHA224, SHA256, SHA384, SHA512, HMAC-SHA1, and HMAC-SHA256. All algorithms are iterative, one-way hash functions that can process a message to produce a condensed representation called a message digest. When a message is received, the message digest can be used to verify whether the data has changed, that is, to verify its integrity.

The hash algorithm of the CE supports block-aligned total length of the input data (padded by software), that is, a multiple of 64 bytes. The message length after padding by software is used as the configured data length for the hash algorithm.

19.1.4.10 RSA Algorithm

The RSA is a public key encryption/decryption algorithm implemented through the modular exponentiation operation.

The ciphertext is obtained as follows: C = ME mod N. The plaintext is obtained as follows: M = CD mod N.

M indicates the plaintext, C indicates the ciphertext, (N, E) indicates the public key, and (N, D) indicates the private key.

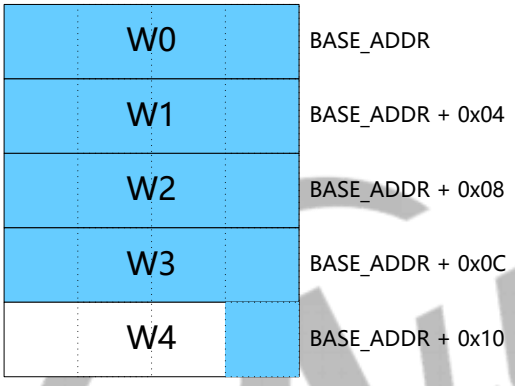
Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

19.1.4.11 Storing Message

In the application, a message may not be stored contiguously in the memory, but divided into multiple segments. Or a piece of continuously stored messages can be artificially split into multiple pieces as needs. Then each segment corresponds to a set of the source address and source length in the descriptor. Multiple segments correspond to groups 0-7 source address/source length in sequence.

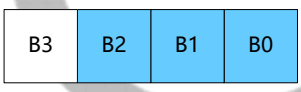
Each task supports up to 8 message segments, and the data volume of each message segment supports up to 4 GWord (AES-CTS is 1 GByte). The total amount of all segments in a task (that is a package) supports up to 4 GWord (AES-CTS is 1 GByte). If a message is divided into multiple packages, all others are required to be whole words; when the last package of AES-CTS is less than one word, 0 needs to be padded, and those less than one word are counted as one word. The following figure shows the address order structure.

Figure 19-12 Word Address of Message



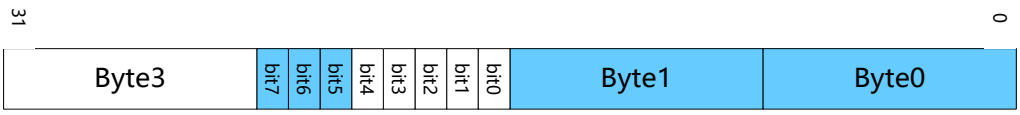
Byte order: low byte first, high byte last. When the data is less than one word, the low byte is filled first. The following figure shows the byte order structure (blue means it is filled by the message).

Figure 19-13 Byte Order



Bit order: high bit first, low bit last. When the data is less than one Byte, the high bit is filled first. The following figure shows the bit order structure.

Figure 19-14 Bit Order



19.1.4.12 Storing Key

The length of KEY must be an integer multiple of word.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

19.1.4.13 Storing IV

For different algorithms, the length of IV is different. But they are integer multiples of word. To keep the byte order of IV and HASH digest output consistent, the byte order of IV is different from that of the message. For the multi-packet operation, the first address of the digest output result of the previous HASH can be directly configured to the first address of the next IV, and the software does not need to do any processing on the digest.

The following figure shows the storage method of 32-bit IV value.

Figure 19-15 The Storage Method of 32-bit IV

IV0[31:0]	BASE_ADDR
IV1[31:0]	BASE_ADDR + 0x04
……	……
IV7[31:0]	BASE_ADDR + 0x1C

The following figure shows the storage method of 64-bit IV value.

Figure 19-16 The Storage Method of 64-bit IV

IV0[63:32]	BASE_ADDR
IV0[31:00]	BASE_ADDR + 0x04
IV1[63:32]	BASE_ADDR + 0x08
IV1[31:00]	BASE_ADDR + 0x0C
……	……
IV7[63:32]	BASE_ADDR
IV7[31:00]	BASE_ADDR + 0x3C

19.1.4.14 Task Descriptor of Hash Algorithms and RBG Algorithms

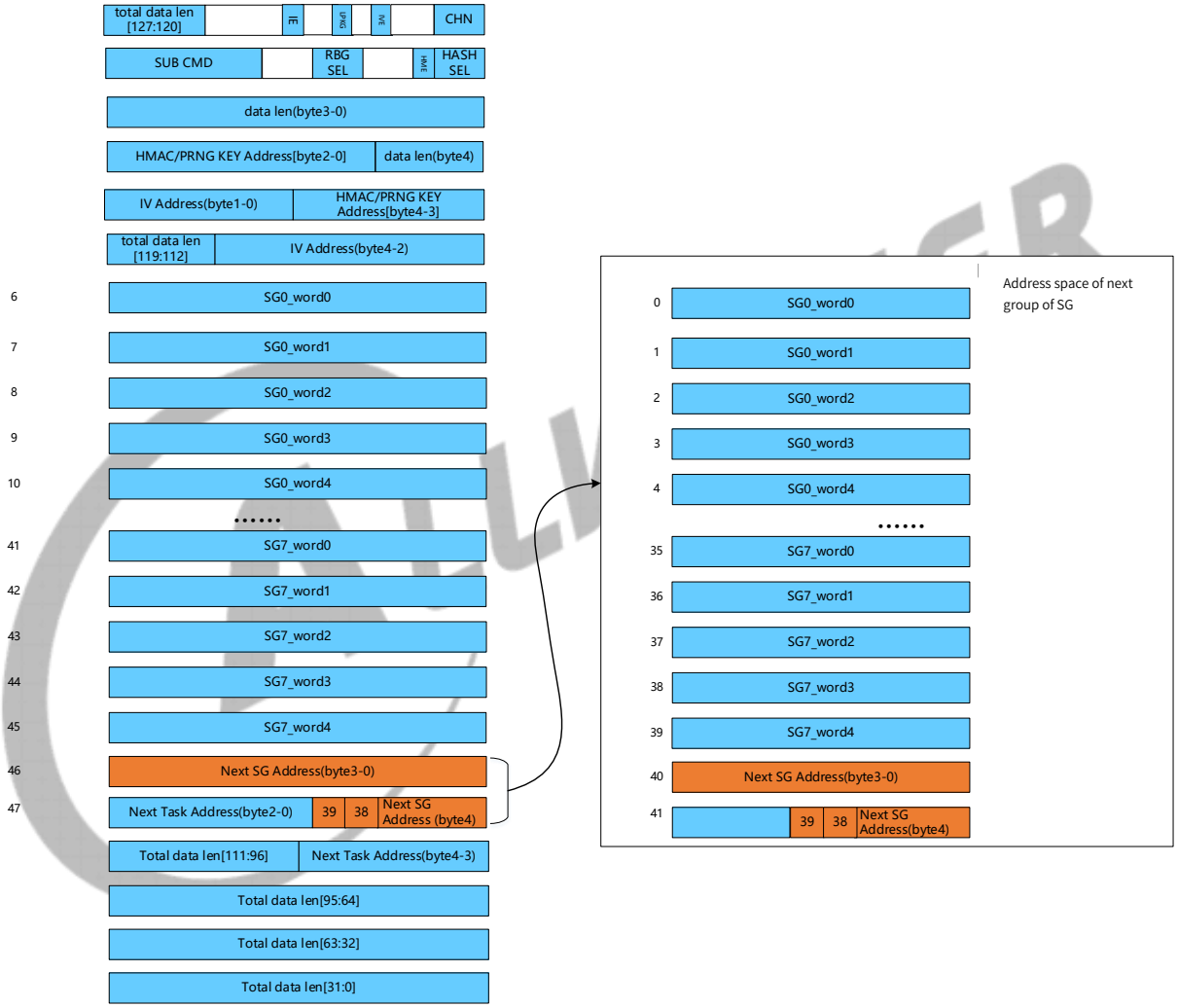
The task descriptor is data written by software to a continuous space in memory. The data describes the various properties of a task, such as algorithm type, mode, subcommand, key address, data source address, the data size read from data source, abstract destination address, the written destination data size, and the information of other tasks. First, configure the task descriptor by software; then operate the registers of CE to start this task. After the task starts, CE will read task descriptor based on the address of the task descriptor configured in register, and perform the task one time based on the described properties.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

In applications, the NEXT SG ADDR field can be configured as the starting address of the next SG descriptor to concatenate multi SG descriptors into a SG chain, thereby realizing multiple SG functions. In addition, the NEXT TASK ADDR field can be configured as the starting address of the next task descriptor to concatenate multi task descriptors into a SG chain, thereby realizing multiple task functions. Multiple SGs and tasks can be randomly configured. After the first take is initiated, CE will sequentially execute each SG among the tasks until NEXT SG ADDR" and "NEXT TASK ADDR" field is invalid.

The HASH/RBG algorithms and Symmetrical/Asymmetrical algorithms use different descriptor structures, as shown below.

Figure 19-17 Task Chaining of Hash Algorithms and Random Bit Generator Algorithms



The detail structures are as follows.

No.	Descriptor	Name	Width	Description
0	CTRL	CHN	[1:0]	Channel ID
		IVE	[8]	IV mode Enable, Active High
		LPKG	[12]	Last Package flag, , Active High
		IE	[16]	Interrupt Enable for current task, Active High

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

No.	Descriptor	Name	Width	Description
		Total data len	[31:24]	Total data len[127:120]
1	CMD	HASH SEL	[3:0]	Hash algorithms select: 0: MD5 1: SHA1 2: SHA224 3: SHA256 4: SHA384 5: SHA512 6: SM3 Other: Reserved
		HME	[4]	HMAC mode Enable, Active High
		RGB SEL	[11:8]	RGB algorithms select: 0: No RGB use 1: PRNG 2: TRNG Other: Reserved
		SUB CMD	[31:16]	Sub-command in a specific algorithm When using PRNG, sub_cmd[15] indicates PRNG seed reload and sub_cmd[14:0] indicates PRNG liner shift seed.
2	DLA	DLA	[31:0]	data length in current task, data len[31:0]
3	DLA	DLA	[7:0]	data length in current task, data len[39:32]
	KA	KA	[31:8]	KEY Address: The byte address bit[23:0], where HMAC KEY or PRNG KEY is saved.
4	KA	KA	[15:0]	KEY Address: The byte address bit[39:24], where HMAC KEY or PRNG KEY is saved.
	IVA	IVA	[31:16]	IV Address: The byte address bit[15:0], where IV is saved.
5	IVA	IVA	[23:0]	IV Address: The byte address bit[39:16], where IV is saved.
	Total calculate data length	Total data len	[31:24]	Total data len[119:112]
6+5*x	SGx_W0	SGx_WORD0	[31:0]	Source Data Address x: The byte address bit[31:0], where Source Datax is saved.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

No.	Descriptor	Name	Width	Description
7+5*x	SGx_W1	SGx_WORD1	[7:0]	Source Data Address x: The byte address bit[39:32] where Source Datax is saved.
			[31:8]	Output Data Address x: The byte address bit[23:0]where Output Datax to be saved.
8+5*x	SGx_W2	SGx_WORD2	[15:0]	Output Data Address x: The byte address bit[39:24]where Output Datax to be saved.
	Reversed	Reversed	[31:16]	/
9+5*x	SGx_W3	SGx_WORD3	[31:0]	Source Data length x: The Length (by bytes) of Source Datax.
10+5*x	SGx_W4	SGx_WORD4	[31:0]	Output Data length x: The Length (by bytes) of output Datax.
46	NSA	NSA	[31:0]	Next SG Address: The byte address bit[31:0].where the descriptor of the next 8 sg in a task is saved. If this is the only one group sg or the last group of a task, NSA must be 32 h0.
47	NSA	NSA	[7:0]	Next SG Address: The byte address bit[39:32].where the descriptor of the next 8 sg in a task is saved. If this is the only one group sg or the last group of a task, NSA must be 8 h0. The [38] indicate whether the next set of source sg exists.[39] bit indicate whether the next set of output dst sg exists.
	NTA	NTA	[31:8]	Next task Address: The byte address bit[23:0] where the descriptor of the next task in a task-chain is saved. If this is the only task or the last task of a task-chain, NTA must be 24 h0.
48	NTA	NTA	[7:0]	Next task Address: The byte address bit[39:24] where the descriptor of the next task in a task-chain is saved. If this is the only task or the last task of a task-chain, NTA must be 16 h0.
	Total calculate data length	Total data len	[31:16]	Total data len[111:96]
49			[31:0]	Total data len[95:64]
50			[31:0]	Total data len[63:32]
51			[31:0]	Total data len[31:0]

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

19.1.4.15 Task Descriptor of Other Algorithms

Software make request through task descriptor, providing algorithm type, mode, key address, source/destination sg address and size, etc. The task descriptor is as follows.

Figure 19-18 Task Chaining of Other Algorithms

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Channel id supports 0-3 for each world.

- Common ctrl

Bit	Read/Write	Default	Description
31	R/W	0	interrupt enable for current task 0: Disable interrupt 1: Enable interrupt
30:25	/	/	/
24:17	R/W	0	cbc_mac_len the outcome bit length of CBC-MAC when in CBC-MAC mode. The part also be used as gcm/ocb mode tag_len.
16:9	/	/	/
8	R/W	0	OP DIR Algorithm Operation Direction 0: Encryption 1: Decryption
7	/	/	/
6:0	R/W	0	Algorithm type 0x0: AES 0x1: DES 0x2: Triple DES (3DES) 0x3: SM4 others: Reserved 0x20: RSA 0x21: ECC 0x22: SM2 others: Reserved 0x30: RAES 0x31: RC4 Others: reserved

- Symmetric ctrl

Bit	Read/Write	Default	Description
31:30	/	/	/
29:28	R/W	0	SCK_SEL 0: use sck0/maskkey0 1: use sck1/maskkey1 2: use sck2/maskkey2 3: reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default	Description
27	R/W	0	ESCK_EN 0: the process ESCK to SCK not need 1: the process ESCK to SCK need *Anyway, when firstly starting the keyladder as after reset, it will be the process ESCK to SCK whether the bit is 1 or not. When once again ,the process ESCK to SCK will see the bit.
26	R/W	0	no_modk 0: have module key derivation function 1: no module key derivation function
25:24	R/W	0	Key ladder stage 0: no key ladder 1: 3-stage key ladder 2: 5-stage key ladder 3: reserved
23:20	R/W	0	KEY Select key select for AES/SM4/TDES TDES only configured as 0/8-15 HUK/SSK0/SSK1 only access by AES/SM4 0: Select input CE_KEYx (Normal Mode) 1: Select {SSK} 2: Select {HUK} 3: Select {RSSK} 4-7: Reserved 8-15: Select internal Key n (n from 0 to 7)
19:18	R/W	0	cfb_width or AES-CFB width 0: CFB1 1: CFB8 2: CFB64 3: CFB128
17	/	/	/
16	R/W	0	AES CTS last package flag When set to '1', it means this is the last package for AES-CTS mode (the size of the last package >128bit). The part also be used as gcm/ocb mode gcm_last/ocb_last .
15:14	/	/	/
13	R/W	0	xts_last 0: Not last block for XTS 1: last block for XTS
12	R/W	0	xts_first 0: Not first block for XTS 1: first block for XTS

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default	Description
11:8	R/W	0	AES/DES/3DES/RAES modes. DES/3DES only supports ECB/CBC/CTR. RAES only supports ECB/CBC/XTS. RAES only supports ECB/CBC/XTS. operation mode for symmetric 0x0: Electronic Code Book (ECB) mode 0x1: Cipher Block Chaining (CBC) mode 0x2: Counter (CTR) mode 0x3: CipherText Stealing (CTS) mode 0x4: Output feedback (OFB)mode 0x5: Cipher feedback (CFB)mode 0x6: CBC-MAC mode 0x7: OCB mode 0x8: GCM mode 0x9: XTS mode 0xa: RC4 mode Other: reserved
7:6	/	/	/
5:4	R/W	0	gcm_iv_mode[1:0] gcm_iv_mode[0]:value 1 show the last req for iv calculate gcm_iv_mode[1]: 0: no GHASH calculate mode 1: GHASH calculate mode gcm_iv_mode[1:0]: 00: IDLE state, this calculate do not have the process from iv to J0. 01: by iv padding generating J0. On the mode, iv padding is 96 bits, so iv_length will be 96bits. 10: by GHASH calculate for iv generating J0, and this is not the last req for iv calculate. 11: by GHASH calculate for iv generating J0, and this is the last req for iv calculate
3:2	R/W	0	CTR Width Counter Width for CTR Mode 0: 16-bits Counter 1: 32-bits Counter, gcm mode always use this setting without software 2: 64-bits Counter 3: 128-bits Counter
1:0	R/W	0	AES Key Size 0: 128-bits 1: 192-bits 2: 256-bits 3: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

- Asymmetric ctrl

Bit	Read/Write	Default	Description
31:21	/	/	/
20:16	R/W	0	PKC algorithm mode. For modular computation: 00000: modular exponent(RSA) 00001: modular add 00010: modular minus 00011: modular multiplication others: Reserved For ECC: 00000: point add 00001: point double 00010: point multiplication 00011: point verification 00100: encryption 00101: decryption 00110: sign 00111: sign verify others: Reserved For SM2: 00000: encryption 00001: decryption 00010: sign 00011: sign verify 00100: key exchange
15:8	/	/	/
7:0	R/W	0	Asymmetric algorithms operation width field. It indicates how much width this request apply, as words.

key addr field is address for each algorithm s key, also for extension feature micro codes address. (By byte)

ctr addr is address for next block s IV. (By byte)

src/dst sgX addr field indicate 40bits address for source and destination data. (By byte)

src/dst sgX size field indicates size for each sg respectively (by byte)

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

For SG, the detail as flow:

byte3	byte2	byte1	byte0	
SRC_ADDR0[B3]	SRC_ADDR0[B2]	SRC_ADDR0[B1]	SRC_ADDR0[B0]	SG_WORD0
DST_ADDR0[B2]	DST_ADDR0[B1]	DST_ADDR0[B0]	SRC_ADDR0[B4]	SG_WORD1
		DST_ADDR0[B4]	DST_ADDR0[B3]	SG_WORD2
SRC_SIZE0 [B3]	SRC_SIZE0 [B2]	SRC_SIZE0 [B1]	SRC_SIZE0 [B0]	SG_WORD3
DST_SIZE0 [B3]	DST_SIZE0 [B2]	DST_SIZE0 [B1]	DST_SIZE0 [B0]	SG_WORD4

1 group SG has 8 sg, each sg has 5 words, the ADDR is 40 bits and byte-addr; the SIZE is 32bits and byte-unit. We will support unlimited SG number, but the 1860 just use for test. This has many group SG in a task, using the next_sg_addr to create the new SG information in the task.

Next sg field should be set to 0 when no next group sg, else set to next sg's descriptor.

next task field should be set to 0 when no next task, else set to next task's descriptor.

19.1.4.16 PKC Microcode

PKC module supports RSA, ECC, SM2 algorithms in the form of microcode. It implements basic modular add, minus, multiplication, point add, point double, and logic computing, etc. Complete RSA/ECC/SM2 encryption, decryption, sign, verify are implemented with these microcodes.

Asymmetric algorithms RSA/ECC/SM2 are implemented as microcode in PKC module. The encryption, decryption, sign, verify operations of asymmetric algorithms are composed with certain fixed microcodes with hardware.

19.1.4.17 PKC Configuration

Before starting PKC, task description must be configured. Parameters to PKC are assigned to source sg, outcome is put to destination sg.

For RSA, parameters should be at the order of key, modulus, plaintext.

For ECC point add P2 = P0 + P1, parameters should be at the order of p, P0x, P0y, P1x, P1y. Output is at the order of P2x, P2y.

For ECC point double P2 = 2*P0, parameters should be at the order of p, a, P0x, P0y. Output is at the order of P2x, P2y.

For ECC point multiplication P2 = k*P0, parameters should be at the order of p, k, a, P0x, P0y. Output is at the order of P2x, P2y.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

For ECC point verification, parameters should be at the order of p, a, P0x, P0y, b. Output is 1 or 0.

For ECC encryption, parameters should be at the order of random k, p, a, Gx, Gy, Qx, Qy, m. Output is at the order of Rx, Ry, c.

For ECC decryption, parameters should be at the order of random k, p, a, Rx, Ry, c. Output is m.

For ECC signature, parameters should be at the order of random k, p, a, Gx, Gy, n, d, e. Output is at the order of r, s.

For ECC signature verification, parameters should be at the order of n, s, e, r, p, a, Gx, Gy, Qx, Qy, n, r. Output is 1 or 0.

19.1.4.18 Error Check

After CE reads the task descriptor, CE can monitor error during algorithm operation. When the error is monitored, CE will do the following operations:

The task will pause immediately

Generates interrupt

The corresponding channel of the task status register is Fail

The corresponding channel bit of error status register can be read error number

The error number has the following types.

Code	Name	Description	Algorithms Type
0x01	algorithm not support	The algorithm type is not supported.	All
0x11	KEYSRAM access error	In AES decryption task, RSSK is used as plaintext, the DST address is not in KEYSRAM space.	AES decryption
0x21	key ladder configuration error	/	KL
0x31	data length error	Input size or output size configuration size error.	All

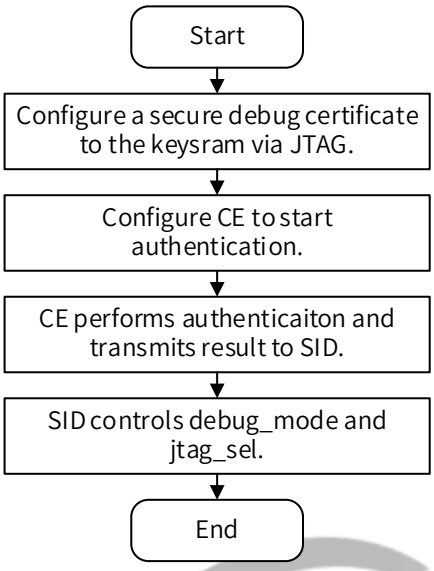
Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

19.1.5 Programming Guidelines

19.1.5.1 Processing Secure Debug

The following figure shows the secure debug process.

Figure 19-19 Secure Debug Process



In secure debug process, CE mainly performs the following operations:

- Signature authentication
- Comparison of hash values of public key and chip_id
- Transmission of debug mode and transmission of authentification result

19.1.6 Register List

There are three groups of registers in

Module Name	Base Address	Comments
CE_NS	0x04603000	Non-Security CE
CE_S	0x04603800	Security CE
SECURE_DEBUG_CFG	0x04605000	Secure Debug Configuration

19.1.6.1 CE_NS Register List

Register Name	Offset	Description
CE_TDA0_NS	0x0000	Non-Security CE Task Descriptor Address0 Register
CE_TDA1_NS	0x0004	Non-Security CE Task Descriptor Address1 Register
CE_ICR_NS	0x0008	Non-Security CE Interrupt Control Register
CE_ISR_NS	0x000C	Non-Security CE Interrupt Status Register
CE_TLR_NS	0x0010	Non-Security CE Task Load Register
CE_TSR_NS	0x0014	Non-Security CE Task Status Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
CE_ESR_NS	0x0018	Non-Security CE Error Status Register
CE_LPC_NS	0x00D0	Non-Security CE Low Power Configuration Register

19.1.6.2 CE_S Register List

Register Name	Offset	Description
CE_TDA0_S	0x0000	Security CE Task Descriptor Address0 Register
CE_TDA1_S	0x0004	Security CE Task Descriptor Address1 Register
CE_ICR_S	0x0008	Security CE Interrupt Control Register
CE_ISR_S	0x000C	Security CE Interrupt Status Register
CE_TLR_S	0x0010	Security CE Task Load Register
CE_TSR_S	0x0014	Security CE Task Status Register
CE_ESR_S	0x0018	Security CE Error Status Register
CE_SCSA0_S	0x0020	Security CE Symmetric algorithm DMA Current Source Address0 Register
CE_SCSA1_S	0x0024	Security CE Symmetric algorithm DMA Current Source Address1 Register
CE_SCDA0_S	0x0028	Security CE Symmetric algorithm DMA Current Destination Address0 Register
CE_SCDA1_S	0x002C	Security CE Symmetric algorithm DMA Current Destination Address1 Register
CE_ACSA0_S	0x0030	Security CE Asymmetric algorithm DMA Current Source Address0 Register
CE_ACSA1_S	0x0034	Security CE Asymmetric algorithm DMA Current Source Address1 Register
CE_ACDA0_S	0x0038	Security CE Asymmetric algorithm DMA Current Destination Address0 Register
CE_ACDA1_S	0x003C	Security CE Asymmetric algorithm DMA Current Destination Address1 Register
CE_HCSA0_S	0x0040	Security CE HASH algorithm DMA Current Source Address0 Register
CE_HCSA1_S	0x0044	Security CE HASH algorithm DMA Current Source Address1 Register
CE_HCDA0_S	0x0048	Security CE HASH algorithm DMA Current Destination Address0 Register
CE_HCDA1_S	0x004C	Security CE HASH algorithm DMA Current Destination Address1 Register
CE_XCSA0_S	0x0050	Security CE XTS algorithm DMA Current Source Address0 Register
CE_XCSA1_S	0x0054	Security CE XTS algorithm DMA Current Source Address1 Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
CE_XCDA0_S	0x0058	Security CE XTS algorithm DMA Current Destination Address0 Register
CE_XCDA1_S	0x005C	Security CE XTS algorithm DMA Current Destination Address1 Register
CE_KL_CFG_REG0_S	0x0060	Security CE Key Ladder Config0
CE_VEN_ID_A0_S	0x0064	Security CE Vendor ID Address0
CE_MOD_ID_A0_S	0x0068	Security CE Module ID Address0
CE_K4_SD_A0_S	0x006c	Security CE Ek5 (K4) Address0
CE_K3_SD_A0_S	0x0070	Security CE Ek4 (K3) Address0
CE_K2_SD_A0_S	0x0074	Security CE Ek3 (K2) Address0
CE_K1_SD_A0_S	0x0078	Security CE Ek2 (K1) Address0
CE_CW_SD_A0_S	0x007c	Security CE Ek1 (CW) Address0
CE_Nonce_A0_S	0x0080	Security CE Nonce Address0
CE_DA_A0_S	0x0084	Security CE DA Address0
CE_RCTC_S	0x0090	Security CE Repetition Count Test C Register
CE_APTC_S	0x0094	Security CE Adaptive Proportion Test C Register
CE_APTWP_S	0x0098	Security CE Adaptive Proportion Test W Period Register
CE_HTCR_S	0x009c	Security CE Healthy Test Control Register
CE_KL_CFG_REG1_S	0x00b0	Security CE Key Ladder Config1
CE_VEN_ID_A1_S	0x00b4	Security CE Vendor ID Address1
CE_MOD_ID_A1_S	0x00b8	Security CE Module ID Address1
CE_K4_SD_A1_S	0x00bc	Security CE Ek5 (K4) Address1
CE_K3_SD_A1_S	0x00c0	Security CE Ek4 (K3) Address1
CE_K2_SD_A1_S	0x00c4	Security CE Ek3 (K2) Address1
CE_K1_SD_A1_S	0x00c8	Security CE Ek2 (K1) Address1
CE_CW_SD_A1_S	0x00cc	Security CE Ek1 (CW) Address1
CE_Nonce_A1_S	0x00d0	Security CE Nonce Address1
CE_DA_A1_S	0x00d4	Security CE DA Address1
CE_KL0_WA1_S	0x0140	Security CE KL0 Widen Address1 Register
CE_KL0_WA2_S	0x0144	Security CE KL0 Widen Address2 Register
CE_KL0_WA3_S	0x0148	Security CE KL0 Widen Address3 Register
CE_KL1_WA1_S	0x014c	Security CE KL1 Widen Address1 Register
CE_KL1_WA2_S	0x0150	Security CE KL1 Widen Address2 Register
CE_KL1_WA3_S	0x0154	Security CE KL1 Widen Address3 Register

19.1.6.3 SECURE_DEBUG_CFG Register List

Register Name	Offset	Description
DEBUG_CTRL_AUTH	0x0000	Debug Authentication control Register

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

19.1.7 CE_NS Register Description

19.1.7.1 0x0000 Non-Security CE Task Descriptor Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CE_TDA0_NS
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TASK_DES_Address0 Task Descriptor Address0 is bit[31:0] (byte addr)

19.1.7.2 0x0004 Non-Security CE Task Descriptor Address1 Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: CE_TDA1_NS
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	TASK_DES_Address1 Task Descriptor Address is bit[39:32] (byte addr)

19.1.7.3 0x0008 Non-Security CE Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CE_ICR_NS
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	TASK_CHAN3_INT_EN Channel 3 Task Interrupt Enable 0: interrupt disable 1: interrupt enable
2	R/W	0x0	TASK_CHAN2_INT_EN Channel 2 Task Interrupt Enable 0: interrupt disable 1: interrupt enable
1	R/W	0x0	TASK_CHAN1_INT_EN Channel 1 Task Interrupt Enable 0: interrupt disable 1: interrupt enable
0	R/W	0x0	TASK_CHAN0_INT_EN Channel 0 Task Interrupt Enable 0: interrupt disable 1: interrupt enable

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

19.1.7.4 0x000C Non-Security CE Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: CE_ISR_NS
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:6	R/W1C	0x0	TASK_CHAN3_STA Channel 3 task Status: Read 0x1: Task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
5:4	R/W1C	0x0	TASK_CHAN2_STA Channel 2 task Status: Read 0x1: Task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
3:2	R/W1C	0x0	TASK_CHAN1_STA Channel 1 task Status: Read 0x1: Task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
1:0	R/W1C	0x0	TASK_CHAN0_STA Channel 0 task Status: Read 0x1: Task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.

Note: As the four channels supports parallel computing, their interrupts may be pulled high simultaneously.

19.1.7.5 0x0010 Non-Security CE Task Load Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CE_TLR_NS
Bit	Read/Write	Default	Description
31:16	/	/	/
15	R/W	0x0	TASK_LOAD_RAES When set, channel 3 can load the descriptor. 1: Load ares task 0: No effect
14:11	/	/	/
10	R/W	0x0	TASK_LOAD_HASH When set, channel 2 can load the descriptor of task. 1: Load hash task 0: No effect
9:6	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0010			Register Name: CE_TLR_NS
Bit	Read/Write	Default	Description
5	R/W	0x0	TASK_LOAD_ASYMM When set, channel 1 can load the descriptor of task. 1: Load asymm task 0: No effect
4:1	/	/	/
0	R/W	0x0	TASK_LOAD_SYMM When set, channel 0 can load the descriptor of task. 1: Load symm task 0: No effect

19.1.7.6 0x0014 Non-Security CE Task Status Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: CE_TSR_NS
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:24	R	0x0	TASK_CHAN_XTS indicate which channel in run for XTS. 00: Task channel0 01: Task channel1 10: Task channel2 11: Task channel3
23:19	/	/	/
18:16	R	0x0	TASK_CHAN_ASYMM indicate which channel in run for asymmetric. 00: Task channel0 01: Task channel1 10: Task channel2 11: Task channel3
15:11	/	/	/
10:8	R	0x0	TASK_CHAN_DIG indicate which channel in run for digest. 00: Task channel0 01: Task channel1 10: Task channel2 11: Task channel3
7:3	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: CE_TSR_NS
Bit	Read/Write	Default/Hex	Description
2:0	R	0x0	TASK_CHAN_SYMM indicate which channel in run for symmetric. 00: Task channel0 01: Task channel1 10: Task channel2 11: Task channel3

19.1.7.7 0x0018 Non-Security CE Error Status Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: CE_ESR_NS
Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	CHAN3_ERR_STATE Error code for task channel 3 0x00: No error 0x01: Algorithm not support 0x11: KEYSRAM access error 0x21: Key ladder configuration error 0x31: Data length error Others: Reserved
23:16	R	0x0	CHAN2_ERR_STATE Error code for task channel 2 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x21: key ladder configuration error 0x31: data length error Others: Reserved
15:8	R	0x0	CHAN1_ERR_STATE Error code for task channel 1 0x00: No error 0x01: Algorithm not support 0x11: KEYSRAM access error 0x21: Key ladder configuration error 0x31: Data length error Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0018			Register Name: CE_ESR_NS
Bit	Read/Write	Default/Hex	Description
7:0	R	0x0	CHAN0_ERR_STATE Error code for task channel 0 0x00: No error 0x01: Algorithm not support 0x11: KEYSRAM access error 0x21: Key ladder configuration error 0x31: Data length error Others: Reserved

19.1.7.8 0x00D0 Non-Security CE Low Power Configuration Register (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: CE_LPC_NS
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	DBL_ENT_SRC_EN Double Entropy Source Enable 1: double entropy source enable 0: single entropy source enable (double entropy source disable
0	R/W	0x0	LOW_POWER_EN ce low power enable 1: low power function enable 0: low power function disable

19.1.8 CE_S Register Description

19.1.8.1 0x0000 Security CE Task Descriptor Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CE_TDA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TASK_DES_ADDR0 Task Descriptor Address is bit[31:0] (byte addr)

19.1.8.2 0x0004 Security CE Task Descriptor Address1 Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: CE_TDA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	TASK_DES_ADDR1 Task Descriptor Address is bit[39:32] (byte addr)

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

19.1.8.3 0x0008 Security CE Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CE_ICR_S
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	TASK_CHAN3_INT_EN Channel 3 Task Interrupt Enable 0: interrupt disable 1: interrupt enable
2	R/W	0x0	TASK_CHAN2_INT_EN Channel 2 Task Interrupt Enable 0: interrupt disable 1: interrupt enable
1	R/W	0x0	TASK_CHAN1_INT_EN Channel 1 Task Interrupt Enable 0: interrupt disable 1: interrupt enable
0	R/W	0x0	TASK_CHAN0_INT_EN Channel 0 Task Interrupt Enable 0: interrupt disable 1: interrupt enable

19.1.8.4 0x000C Security CE Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: CE_ISR_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:6	R/W1C	0x0	TASK_CHAN3_STA Channel 3 task Status: Read 0x1: Task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
5:4	R/W1C	0x0	TASK_CHAN2_STA Channel 2 task Status: Read 0x1: Task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
3:2	R/W1C	0x0	TASK_CHAN1_STA Channel 1 task Status: Read 0x1: Task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x000C			Register Name: CE_ISR_S
Bit	Read/Write	Default/Hex	Description
1:0	R/W1C	0x0	TASK_CHAN0_STA Channel 0 task Status: Read 0x1: Task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.

Note: As the four channels supports parallel computing, their interrupts may be pulled high simultaneously.

19.1.8.5 0x0010 Security CE Task Load Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CE_TLR_S
Bit	Read/Write	Default	Description
15	R/W	0x0	TASK_LOAD_RAES When set, channel 3 can load the descriptor. 1: Load ares task 0: No effect
14:11	/	/	/
10	R/W	0x0	TASK_LOAD_HASH When set, channel 2 can load the descriptor of task. 1: Load hash task 0: No effect
9:6	/	/	/
5	R/W	0x0	TASK_LOAD_ASYMM When set, channel 1 can load the descriptor of task. 1: Load asymm task 0: No effect
4:1	/	/	/
0	R/W	0x0	TASK_LOAD_SYMM When set, channel 0 can load the descriptor of task. 1: Load symm task 0: No effect

19.1.8.6 0x0014 Security CE Task Status Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: CE_TSR_S
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0014			Register Name: CE_TSR_S
Bit	Read/Write	Default/Hex	Description
26:24	R	0x0	TASK_CHAN_XTS indicate which channel in run for XTS. 000: Task channel0 001: Task channel1 010: Task channel2 011: Task channel3
23:19	/	/	/
18:16	R	0x0	TASK_CHAN_ASYMM indicate which channel in run for asymmetric. 000: Task channel0 001: Task channel1 010: Task channel2 011: Task channel3
15:12	/	/	/
10:8	R	0x0	TASK_CHAN_DIG indicate which channel in run for digest. 000: Task channel0 001: Task channel1 010: Task channel2 011: Task channel3
7:3	/	/	/
2:0	R	0x0	TASK_CHAN_SYMM indicate which channel in run for symmetric. 000: Task channel0 001: Task channel1 010: Task channel2 011: Task channel3

19.1.8.7 0x0018 Security CE Error Status Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: CE_ESR_S
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0018			Register Name: CE_ESR_S
Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	CHAN3_ERR_STATE Error code for task channel 3 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x21: key ladder configuration error 0x31: data length error 0x43: TRNG rep_cnt(repetition count) test error 0x4c: TRNG adap_pro(adaptive proportion) test error 0x4f: TRNG rep_cnt and adap_pro tests occur both errors Others: Reserved
23:16	R	0x0	CHAN2_ERR_STATE Error code for task channel 2 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x21: key ladder configuration error 0x31: data length error 0x43: TRNG rep_cnt(repetition count) test error 0x4c: TRNG adap_pro(adaptive proportion) test error 0x4f: TRNG rep_cnt and adap_pro tests occur both errors Others: Reserved
15:8	R	0x0	CHAN1_ERR_STATE Error code for task channel 1 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x21: key ladder configuration error 0x31: data length error 0x43: TRNG rep_cnt(repetition count) test error 0x4c: TRNG adap_pro(adaptive proportion) test error 0x4f: TRNG rep_cnt and adap_pro tests occur both errors Others: Reserved

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0018			Register Name: CE_ESR_S
Bit	Read/Write	Default/Hex	Description
7:0	R	0x0	CHAN0_ERR_STATE Error code for task channel 0 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x21: key ladder configuration error 0x31: data length error 0x43: TRNG rep_cnt(repetition count) test error 0x4c: TRNG adap_pro(adaptive proportion) test error 0x4f: TRNG rep_cnt and adap_pro tests occur both errors others: Reserved

19.1.8.8 0x0020 Security CE Symmetric algorithm DMA Current Source Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: CE_SCSA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	SYMM_CUR_SRC_ADDR0 Symmetric algorithm current source address DMA reads. Bit[31:0], byte addr.

19.1.8.9 0x0024 Security CE Symmetric algorithm DMA Current Source Address1 Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: CE_SCSA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	SYMM_CUR_SRC_ADDR1 Symmetric algorithm current source address DMA reads. Bit[39:32], byte addr.

19.1.8.10 0x0028 Security CE Symmetric algorithm DMA Current Destination Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: CE_SCDA0_S
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0028			Register Name: CE_SCDA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	SYMM_CUR_DST_ADDR0 Symmetric algorithm current destination address DMA writes. Bit[31:0], byte addr.

19.1.8.11 0x002C Security CE Symmetric algorithm DMA Current Destination Address1 Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: CE_SCDA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	SYMM_CUR_DST_ADDR1 Symmetric algorithm current destination address DMA writes. Bit[39:32], byte addr.

19.1.8.12 0x0030 Security CE Asymmetric algorithm DMA Current Source Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: CE_ACSA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	ASYMM_CUR_SRC_ADDR0 Asymmetric algorithm current source address DMA reads. Bit[31:0], byte addr.

19.1.8.13 0x0034 Security CE Asymmetric algorithm DMA Current Source Address1 Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: CE_ACSA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	ASYMM_CUR_SRC_ADDR1 Asymmetric algorithm current source address DMA reads. Bit[39:32], byte addr.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

19.1.8.14 0x0038 Security CE Asymmetric algorithm DMA Current Destination Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: CE_ACDA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	ASYMM_CUR_DST_ADDR0 Asymmetric algorithm current destination address DMA writes. Bit[31:0], byte addr.

19.1.8.15 0x003C Security CE Asymmetric algorithm DMA Current Destination Address1 Register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: CE_ACDA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	ASYMM_CUR_DST_ADDR1 Asymmetric algorithm current destination address DMA writes. Bit[39:32], byte addr.

19.1.8.16 0x0040 Security CE HASH algorithm DMA Current Source Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: CE_HCSA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	HASH_CUR_SRC_ADDR0 HASH algorithm current source address DMA reads. Bit[31:0], byte addr.

19.1.8.17 0x0044 Security CE HASH algorithm DMA Current Source Address1 Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: CE_HCSA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	HASH_CUR_SRC_ADDR1 HASH algorithm current source address DMA reads. Bit[39:32], byte addr.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

19.1.8.18 0x0048 Security CE HASH algorithm DMA Current Destination Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: CE_HCDA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	HASH_CUR_DST_ADDR0 HASH algorithm current destination address DMA writes. Bit[31:0], byte addr.

19.1.8.19 0x004C Security CE HASH algorithm DMA Current Destination Address1 Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: CE_HCDA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	HASH_CUR_DST_ADDR1 HASH algorithm current destination address DMA writes. Bit[39:32], byte addr.

19.1.8.20 0x0050 Security CE XTS algorithm DMA Current Source Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: CE_XCSA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	XTS_CUR_CUR_ADDR0 XTS algorithm current source address DMA reads.

19.1.8.21 0x0054 Security CE XTS algorithm DMA Current Source Address1 Register (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: CE_XCSA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	XTS_CUR_CUR_ADDR1 XTS algorithm current source address DMA reads.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

19.1.8.22 0x0058 Security CE XTS algorithm DMA Current Destination Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: CE_XCDA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	XTS_CUR_DST_ADDR0 XTS algorithm current destination address DMA writes. Bit[31:0], byte addr.

19.1.8.23 0x005C Security CE XTS algorithm DMA Current Destination Address1 Register (Default Value: 0x0000_0000)

Offset: 0x005C			Register Name: CE_XCDA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	XTS_CUR_DST_ADDR1 XTS algorithm current destination address DMA writes. Bit[39:32], byte addr.

19.1.8.24 0x0060 Security CE Key Ladder Config0 (Default Value: 0x0000_0002)

Offset: 0x0060			Register Name: CE_KL_CFG_REG0_S
Bit	Read/Write	Default/Hex	Description
31:22	R/W	0x0	Reserved
21	R/W	0x0	interrupt enable for current task 0: Disable interrupt 1: Enable interrupt
20	R/W	0x0	Algorithm type 0x0: AES 0x1: Triple DES (3DES)
19:18	/	/	/
17:16	R/W	0x0	SCK_SEL 0: use sck0/maskkey0 others: Reserved
15	R/W	0x0	ESCK_EN 0: the process ESCK to SCK not need 1: the process ESCK to SCK need *Anyway, when firstly starting the keyladder as after reset, it will be the process ESCK to SCK.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0060			Register Name: CE_KL_CFG_REG0_S
Bit	Read/Write	Default/Hex	Description
14	R/W	0x0	no_modk Root Key Derivation Switch 0: have module key derivation function 1: no module key derivation function
13:12	R/W	0x0	KL_STAGE 00: Reserved 01: Reserved 10: 5-stage key ladder 11: Reserved
11:2	/	/	/
1	R	0x1	KL_DONE key_ladder done 0: keyladder hasn t finish computing. New requests cannot be configured. 1: Configure new key ladder request. When keyladder module computing finishes, write 1 to this bit. When new keyladder request is sent, the bit will be cleared to 0.
0	R/W	0x0	KL_EN 1: keyladder start enable 0: keyladder start not enable When Kl_DONE is 1, clear KL_EN.

19.1.8.25 0x0064 Security CE Vendor ID Address0 (Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: CE_VEN_ID_A0_S
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VENDOR_ID_ADDR

19.1.8.26 0x0068 Security CE Module ID Address0 (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: CE_MOD_ID_A0_S
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	MOUDLE_ID_ADDR

19.1.8.27 0x006c Security CE Ek5 (K4) Address0 (Default Value: 0x0000_0000)

Offset: 0x006c			Register Name: CE_K4_SD_A0_S
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x006c			Register Name: CE_K4_SD_A0_S
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	EK5_K4 The source data address of decryption result K4.

19.1.8.28 0x0070 Security CE Ek4 (K3) Address0 (Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: CE_K3_SD_A0_S
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	EK4_K3 The source data address of decryption result K3.

19.1.8.29 0x0074 Security CE Ek3 (K2) Address0 (Default Value: 0x0000_0000)

Offset: 0x0074			Register Name: CE_K2_SD_A0_S
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	EK3_K2 The source data address of decryption result K2.

19.1.8.30 0x0078 Security CE Ek2 (K1) Address0 (Default Value: 0x0000_0000)

Offset: 0x0078			Register Name: CE_K1_SD_A0_S
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	EK2_K1 The source data address of decryption result K1.

19.1.8.31 0x007c Security CE Ek1 (CW) Address0 (Default Value: 0x0000_0000)

Offset: 0x007c			Register Name: CE_CW_SD_A0_S
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	EK1_CW The source data address of decryption result CW.

19.1.8.32 0x0080 Security CE Nonce Address0 (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: CE_Nonce_A0_S
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	NONCE_SRC_ADDR The source data address of Nonce.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

19.1.8.33 0x0084 Security CE DA Address0 (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: CE_DA_A0_S
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	DA_DST_ADDR The destination address of DA data.

19.1.8.34 0x0090 Security CE Repetition Count Test C Register (Default Value：0x0000_0000)

Offset: 0x0090			Register Name: CE_RCTC_S
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	REP_CNT_TEST_C Channel2 Repetition Count Test, C value is bit[31:0] (by binary)

NOTE

In the repetition count test, the formula of C is shown as below

$$C = 1 + \left\lceil \frac{-\log_2 \alpha}{H} \right\rceil.$$

α can be valued as 10^{-20} from 10^{-20} to 10^{-40}; H can be valued as 160, indicating the sampling value is 169 bits.

19.1.8.35 0x0094 Security CE Adaptive Proportion Test C Register (Default Value：0x0000_0000)

Offset: 0x0094			Register Name: CE_APTC_S
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	ADAP_PRO_TEST_C Channel2 Adaptive Proportion Test, C value is bit[31:0] (by binary)

NOTE

In the adaptive proportion test, the formula of C is shown as below

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

$$1+CRITBINOM(W, power(2,(-H)),1-\alpha).$$

α can be valued as 10^{-20} from 10^{-20} to 10^{-40}; W can be valued as 160, indicating the sampling value is 169 bits.

19.1.8.36 0x0098 Security CE Adaptive Proportion Test W Period Register (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: CE_APTWP_S
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	ADAP_PRO_TEST_W_Period Channel2 Adaptive Proportion Test, window W period between two tests is bit[31:0] (by binary) 0: no wait, start next test directly >0: wait window W period time, start next test.

19.1.8.37 0x009c Security CE Healthy Test Control Register (Default Value: 0x0000_0000)

Offset: 0x009c			Register Name: CE_HTCR_S
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	ADAP_PRO_TEST_EN Channel2 Adaptive Proportion Test Enable 1: adap_pro healthy test enable 0: adap_pro healthy test disable
16	R/W	0x0	REP_CNT_TEST_EN Channel2 Repetition Count Test Enable 1: rep_cnt healthy test enable 0: rep_cnt healthy test disable
15:11	/	/	/
10:0	R/W	0x0	ADAP_PRO_TEST_W Channel2 Adaptive Proportion Test, window size W value is bit[10:0] 1024: noise source is binary 512: noise source is not binary

19.1.8.38 0x00b0 Security CE Key Ladder Config1 (Default Value: 0x0000_0002)

Offset: 0x00b0			Register Name: CE_KL_CFG_REG1_S
Bit	Read/Write	Default/Hex	Description

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x00b0			Register Name: CE_KL_CFG_REG1_S
Bit	Read/Write	Default/Hex	Description
31:22	R/W	0x0	Reserved
21	R/W	0x0	interrupt enable for current task 0: Disable interrupt 1: Enable interrupt
20	R/W	0x0	Algorithm type 0x0: AES 0x1: Triple DES (3DES)
19:18	/	/	/
17:16	R/W	0x0	SCK_SEL 0: use sck0/maskkey0 Others: reserved
15	R/W	0x0	ESCK_EN 0: the process ESCK to SCK not need 1: the process ESCK to SCK need Note: when firstly starting the keyladder after reset, it will be the process ESCK to SCK.
14	R/W	0x0	no_modk (Root Key Derivation Switch) 0: have module key derivation function 1: no module key derivation function
13:12	R/W	0x0	KL_STAGE 00: no key ladder 01: 3-stage key ladder 10: 5-stage key ladder 11: Reserved
11:2	/	/	/
1	R	0x1	KL_DONE key_ladder end
0	R/W	0x0	KL_EN 1: Keyladder start enable 0: Keyladder start not enable

19.1.8.39 0x00b4 Security CE Vendor ID Address1 (Default Value: 0x0000_0000)

Offset: 0x00b4			Register Name: CE_VEN_ID_A1_S
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VENDOR_ID_ADDR

19.1.8.40 0x00b8 Security CE Module ID Address1 (Default Value: 0x0000_0000)

Offset: 0x00b8	Register Name: CE_MOD_ID_A1_S

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	MOUDLE_ID_ADDR

19.1.8.41 0x00bc Security CE Ek5 (K4) Address1 (Default Value: 0x0000_0000)

Offset: 0x00bc			Register Name: CE_K4_SD_A1_S
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	EK5_K4 The source data address of decryption result K4.

19.1.8.42 0x00c0 Security CE Ek4 (K3) Address1 (Default Value: 0x0000_0000)

Offset: 0x00c0			Register Name: CE_K3_SD_A1_S
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	EK4_K3 The source data address of decryption result K3.

19.1.8.43 0x00c4 Security CE Ek3 (K2) Address1 (Default Value: 0x0000_0000)

Offset: 0x00c4			Register Name: CE_K2_SD_A1_S
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	EK3_K2 The source data address of decryption result K2.

19.1.8.44 0x00c8 Security CE Ek2 (K1) Address1 (Default Value: 0x0000_0000)

Offset: 0x00c8			Register Name: CE_K1_SD_A1_S
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	EK2_K1 The source data address of decryption result K1.

19.1.8.45 0x00cc Security CE Ek1 (CW) Address1 (Default Value: 0x0000_0000)

Offset: 0x00cc			Register Name: CE_CW_SD_A1_S
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	EK1_CW The source data address of decryption result CW.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

19.1.8.46 0x00d0 Security CE Nonce Address1 (Default Value: 0x0000_0000)

Offset: 0x00d0			Register Name: CE_Nonce_A1_S
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	NONCE_SRC_ADDR The source data address of Nonce.

19.1.8.47 0x00d4 Security CE DA Address1 (Default Value: 0x0000_0000)

Offset: 0x00d4			Register Name: CE_DA_A1_S
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	DA_DST_ADDR The destination address of DA data.

19.1.8.48 0x0140 Security CE KL0 Widen Address1 Register (Default Value: 0x0000_0000)

Offset: 0x0140			Register Name:CE_KL0_WA1_S
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	KL0_EK4_K3 The source data address [39:32] of decryption result K3.
23:16	R/W	0x0	KL0_EK5_K4 The source data address [39:32] of decryption result K4.
15:8	R/W	0x0	KL0_MODULE_ID_ADDR Module ID addr[39:32]
7:0	R/W	0x0	KL0_VENDOR_ID_ADDR Vendor ID addr[39:32]

19.1.8.49 0x0144 Security CE KL0 Widen Address2 Register (Default Value: 0x0000_0000)

Offset: 0x0144			Register Name:CE_KL0_WA2_S
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	KL0_NONCE_SRC_ADDR The source data address [39:32] of Nonce.
23:16	R/W	0x0	KL0_EK1_CW The source data address [39:32] of decryption result CW.
15:8	R/W	0x0	KL0_EK2_K1 The source data address [39:32] of decryption result K1.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0144			Register Name:CE_KL0_WA2_S
Bit	Read/Write	Default/Hex	Description
7:0	R/W	0x0	KL0_EK3_K2 The source data address [39:32] of decryption result K2.

19.1.8.50 0x0148 Security CE KL0 Widen Address3 Register (Default Value: 0x0000_0000)

Offset: 0x0148			Register Name:CE_KL0_WA3_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	KL0_DA_DST_ADDR The destination address [39:32] of DA data.

19.1.8.51 0x014C Security CE KL1 Widen Address1 Register (Default Value: 0x0000_0000)

Offset: 0x014C			Register Name:CE_KL1_WA1_S
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	KL1_EK4_K3 The source data address [39:32] of decryption result K3.
23:16	R/W	0x0	KL1_EK5_K4 The source data address [39:32] of decryption result K4.
15:8	R/W	0x0	KL1_MOUDLE_ID_ADDR Module ID addr[39:32]
7:0	R/W	0x0	KL1_VENDOR_ID_ADDR Vendor ID addr[39:32]

19.1.8.52 0x0150 Security CE KL1 Widen Address2 Register (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name:CE_KL1_WA2_S
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	KL1_NONCE_SRC_ADDR The source data address [39:32] of Nonce.
23:16	R/W	0x0	KL1_EK1_CW The source data address [39:32] of CW.
15:8	R/W	0x0	KL1_EK2_K1 The source data address [39:32] of decryption result K1.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Offset: 0x0150			Register Name:CE_KL1_WA2_S
Bit	Read/Write	Default/Hex	Description
7:0	R/W	0x0	KL1_EK3_K2 The source data address [39:32] of decryption result K2.

19.1.8.53 0x0154 Security CE KL1 Widen Address3 Register (Default Value: 0x0000_0000)

Offset: 0x0154			Register Name:CE_KL1_WA3_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	KL1_DA_DST_ADDR The destination address [39:32] of DA data.

19.1.9 SECURE_DEBUG_CFG register Description

19.1.9.1 0x0000 Debug Authentication Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: SEC_DBG_CFG
Bit	Read/Write	Default	Description
31:1	/	/	/
0	R/WAC	0x0	AUTH_EN Authentication enable Write 1 to enable authentication. When authentication completes, clear it by sec_dbg_en.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

Copyright©2025 Allwinner Technology Co.,Ltd. All Rights Reserved.

This documentation is the original work and copyrighted property of Allwinner Technology Co.,Ltd (Allwinner). No part of this document may be reproduced, modify, publish or transmitted in any form or by any means without prior written consent of Allwinner.

Trademarks and Permissions

Allwinner and the Allwinner logo (incomplete enumeration) are trademarks of Allwinner Technology Co.,Ltd. All other trademarks, trade names, product or service names mentioned in this document are the property of their respective owners.

Important Notice and Disclaimer

The purchased products, services and features are stipulated by the contract made between Allwinner Technology Co.,Ltd (Allwinner) and the customer. All or part of the products, services and features described in this document may not be within the purchase scope or the usage scope. Please read the terms and conditions of the contract and relevant instructions carefully before using, and follow the instructions in this documentation strictly. Allwinner assumes no responsibility for the consequences of improper use (including but not limited to overvoltage, overclock, or excessive temperature).

The information in this document is provided just as a reference or typical applications, and is subject to change without notice. Every effort has been made in the preparation of this document to ensure accuracy of the contents. Allwinner is not responsible for any damage (including but not limited to indirect, incidental or special loss) or any infringement of third party rights arising from the use of this document. All statements, information, and recommendations in this document do not constitute a warranty or commitment of any kind, express or implied.

No license is granted by Allwinner herein express or implied or otherwise to any patent or intellectual property of Allwinner. Third party licences may be required to implement the solution/product. Customers shall be solely responsible to obtain all appropriately required third party licences. Allwinner shall not be liable for any licence fee or royalty due in respect of any required third party licence. Allwinner shall have no warranty, indemnity or other obligations with respect to third party licences.

Copyright © 2025 Allwinner Technology Co., Ltd. All Rights Reserved.

Allwinner Technology Co., Ltd.
No.9 Technology Road 2, High-Tech Zone,
Zhuhai, Guangdong Province, China

Contact US:
Service@allwinnertech.com
www.allwinnertech.com